ADSP-BF518F EZ-Board®
Evaluation System Manual

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Analog Devices, Inc.
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The ADSP-BF518F EZ-Board is designed to be used solely in a laboratory environment. The board is not intended for use as a consumer end product or as a portion of a consumer end product. The board is an open system design which does not include a shielded enclosure and therefore may cause interference to other electrical devices in close proximity. This board should not be used in or near any medical equipment or RF devices.

The ADSP-BF518F EZ-Board has been certified to comply with the essential requirements of the European EMC directive 2004/108/EC and therefore carries the "**CE**" mark.

The ADSP-BF518F EZ-Board has been appended to Analog Devices, Inc. EMC Technical File (EMC TF) referenced **DSPTOOLS1**, issue 2 dated June 4, 2008 and was declared CE compliant by an appointed Notified Body (No.0673) as listed below.

Notified Body Statement of Compliance: Z600ANA2.032, dated March, 2009.

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The EZ-Board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store the unused EZ-Board in the protective shipping package.

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PREFACE

Thank you for purchasing the ADSP-BF518F EZ-Board®, Analog Devices, Inc. evaluation system for Blackfin® processors.

Blackfin processors embody a type of embedded processor designed specifically to meet the computational demands and power constraints of today's embedded audio, video, and communications applications. They deliver breakthrough signal-processing performance and power efficiency within a reduced instruction set computing (RISC) programming model.

Blackfin processors support a media instruction set computing (MISC) architecture. This architecture is the natural merging of RISC, media functions, and digital signal processing (DSP) characteristics. Blackfin processors deliver signal-processing performance in a microprocessor-like environment.

Based on the Micro Signal Architecture (MSA), Blackfin processors combine a 32-bit RISC instruction set, dual 16-bit multiply accumulate (MAC) DSP functionality, and eight-bit video processing performance that had previously been the exclusive domain of very-long instruction word (VLIW) media processors.

The evaluation board is designed to be used in conjunction with the CrossCore® Embedded Studio (CCES) and VisualDSP++® development environments to test the capabilities of the ADSP-BF512/BF512F, ADSP-BF514/BF514F, ADSP-BF516/BF516F, and ADSP-BF518/BF518F Blackfin processors. The development environment aids advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and assembly
- Load, run, step, halt, and set breakpoints in application programs
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the processor from a personal computer (PC) is achieved through a USB port or an external JTAG emulator. The USB interface of the standalone debug agent gives unrestricted access to the processor and evaluation board's peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. To learn more about Analog Devices emulators and processor development tools, go to `http://www.analog.com/dsp/tools`.

The ADSP-BF518F EZ-Board provides example programs to demonstrate the capabilities of the product.

Product Overview

The board features:

- Analog Devices ADSP-BF518F Blackfin processor
    - Core performance up to 400 MHz
    - External bus performance up to 80 MHz
    - 176-pin LQFP package
    - 25 MHz crystal
- Programmable VDDINT core power
    - Analog Devices AD5258 TWI digital potentiometer
    - Analog Devices ADP1715 low dropout linear regulator
- Synchronous dynamic random access memory (SDRAM)
    - Micron MT48LC32M16A2TG – 64 MB (32M x 16-bits)
- Parallel flash memory
    - Numonyx M29W320EB – 4 MB (2M x 16-bits)
- eMMC flash memory
    - Micron MTFC8GKQDI – 8 GB
- SPI flash memory
    - Numonyx M25P16 – 16 Mb

- Analog audio interface
    - Analog Devices SSM2603 low-power audio codec
    - One stereo `LINE OUT` jack
    - One headphone `LINE IN`
    - One input `MIC` jack
    - One input stereo `LINE IN` jack
- Ethernet interface
    - National Semiconductor DP83848 PHY device
    - 10-BaseT and 100-BaseTX
    - Auto-MDIX
- ADC interface
    - Analog Devices AD7266 2 MSPS, 12-bit, 3-channel SAR analog-to-digital converter
- Thumbwheel
    - Panasonic EVQ-WKA001 rotary encoder
- Universal asynchronous receiver/transmitter (UART)
    - ADM3202 RS-232 line driver/receiver
    - DB9 female connector

- LEDs
    - Five LEDs: one board reset (red), three general-purpose (amber), one configurable ethernet LEDs (amber) and one power (green)
- Push buttons
    - Three push buttons: one reset, two programmable flags with debounce logic
- Expansion interface II
    - Next generation of the expansion interface design, provides access to most of the ADSP-BF518F processor signals
- Land grid array
    - Easy probing of all port pins and most EBIU signals
- Other features
    - JTAG ICE 14-pin header
    - Blackfin power measurement jumpers

For information about the hardware components of the EZ-Board, refer to Chapter 2, "ADSP-BF518F EZ-Board Hardware Reference".

Purpose of This Manual

The *ADSP-BF518F EZ-Board Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes operation and configuration of the board components and provides guidelines for running your own code on the ADSP-BF518F EZ-Board. Finally, a schematic and a bill of materials are provided for reference.

Intended Audience

The primary audience for this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set.

Programmers who are unfamiliar with Analog Devices processors can use this manual, but should supplement it with other texts that describe your target architecture. For the locations of these documents, see "Related Documents".

Programmers who are unfamiliar with CCES or VisualDSP++ should refer to the online help and user's manuals.

Manual Contents

The manual consists of:

- Chapter 1, "Using the ADSP-BF518F EZ-Board" on page 1-1
  Describes EZ-Board functionality from a programmer's perspective and provides an easy-to-access memory map.
- Chapter 2, "ADSP-BF518F EZ-Board Hardware Reference" on page 2-1
  Provides information on the EZ-Board hardware components.
- Appendix A, "ADSP-BF518F EZ-Board Bill Of Materials" on page A-1
  Provides a list of components used to manufacture the EZ-Board.
- Appendix B, "ADSP-BF518F EZ-Board Schematic" on page B-1
  Provides the resources to allow board-level debugging or to use as a reference guide. Appendix B is part of the online help.

What's New in This Manual

This is revision 1.3 of the *ADSP-BF518F EZ-Board Evaluation System Manual*. The manual has been updated to include CCES information. Additional changes include the following.

- Updated System Architecture graphic, Figure 2-1.
- Updated Configuration Jumper Locations graphic, Figure 2-3.
- Updated Connector Locations graphic, Figure 2-5.
- Updated Ethernet connectors.
- Updated Bill of Materials, Appendix A, "ADSP-BF518F EZ-Board Bill Of Materials".
- Modifications and corrections based on errata reports against the previous manual revision have been made.

For the latest version of this manual, please refer to the Analog Devices Web site.

Technical Support

You can reach Analog Devices processors and DSP technical support in the following ways:

- Post your questions in the processors and DSP support community at EngineerZone®:
  `http://ez.analog.com/community/dsp`
- Submit your questions to technical support directly at:
  `http://www.analog.com/support`

- E-mail your questions about processors, DSPs, and tools development software from **CrossCore Embedded Studio** or **VisualDSP++**:

  Choose **Help > Email Support**. This creates an e-mail to `processor.tools.support@analog.com` and automatically attaches your **CrossCore Embedded Studio** or **VisualDSP++** version information and `license.dat` file.

- E-mail your questions about processors and processor applications to:
  `processor.support@analog.com` or
  `processor.china@analog.com` (Greater China support)

- In the **USA only**, call **1-800-ANALOGD** (1-800-262-5643)

- Contact your Analog Devices sales office or authorized distributor. Locate one at:
  `www.analog.com/adi-sales`

- Send questions by mail to:
  Processors and DSP Technical Support
  Analog Devices, Inc.
  Three Technology Way
  P.O. Box 9106
  Norwood, MA 02062-9106
  USA

Supported Processors

This evaluation system supports Analog Devices ADSP-BF512/BF512F, ADSP-BF514/BF514F, ADSP-BF516/BF516F, and ADSP-BF518/BF518F Blackfin embedded processors.

Product Information

Product information can be obtained from the Analog Devices Web site and the online help system.

Analog Devices Web Site

The Analog Devices Web site, www.analog.com, provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and digital signal processors.

To access a complete technical library for each processor family, go to http://www.analog.com/processors/technical_library. The manuals selection opens a list of current manuals related to the product as well as a link to the previous revisions of the manuals. When locating your manual title, note a possible errata check mark next to the title that leads to the current correction report against the manual.

Also note, myAnalog is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information about products you are interested in. You can choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests, including documentation errata against all manuals. myAnalog provides access to books, application notes, data sheets, code examples, and more.

Visit myAnalog to sign up. If you are a registered user, just log on. Your user name is your e-mail address.

EngineerZone

EngineerZone is a technical support forum from Analog Devices. It allows you direct access to ADI technical support engineers. You can search FAQs and technical information to get quick answers to your embedded processing and DSP design questions.

Use EngineerZone to connect with other DSP developers who face similar design challenges. You can also use this open forum to share knowledge and collaborate with the ADI support team and your peers. Visit http://ez.analog.com to sign up.

Related Documents

For additional information about the product, refer to the following publications.

Table 1. Related Processor Publications

Title	Description
ADSP-BF512/ADSP-BF514/ADSP-BF516/ ADSP-BF518(F) Blackfin Embedded Processor Data Sheet	General functional description, pinout, and timing of the processor
ADSP-BF51x Blackfin Processor Hardware Reference	Description of internal processor architecture and all register functions
Blackfin Processor Programming Reference	Description of all allowed processor assembly instructions

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (**File** menu)	Titles in reference sections indicate the location of an item within the development environment's menu system (for example, the **Close** command appears on the **File** menu).
`{this | that}`	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as `this` or `that`. One or the other is required.
`[this | that]`	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional `this` or `that`.
`[this,…]`	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipse; read the example as an optional comma-separated list of `this`.
`.SECTION`	Commands, directives, keywords, and feature names are in text with `letter gothic` font.
`filename`	Non-keyword placeholders appear in text with italic style format.
	Note: For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word **Note** appears instead of this symbol.
	Caution: Incorrect device operation may result if ... **Caution:** Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word **Caution** appears instead of this symbol.
	Warning: Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word **Warning** appears instead of this symbol.

1 USING THE ADSP-BF518F EZ-BOARD

This chapter provides information to assist you with development of programs for the ADSP-BF518F EZ-Board evaluation system.

The following topics are covered.

- "Package Contents" on page 1-3
- "Default Configuration" on page 1-3
- "CCES Install and Session Startup" on page 1-5
- "VisualDSP++ Install and Session Startup" on page 1-9
- "CCES Evaluation License" on page 1-11
- "VisualDSP++ Evaluation License" on page 1-12
- "Lockbox Key Security Features" on page 1-13
- "Memory Map" on page 1-13
- "SDRAM Interface" on page 1-15
- "Parallel Flash Memory Interface" on page 1-16
- "eMMC Interface" on page 1-16
- "SPI Interface" on page 1-17
- "Parallel Peripheral Interface (PPI)" on page 1-19
- "Rotary Encoder Interface" on page 1-19

- "Ethernet Interface" on page 1-20
- "Audio Interface" on page 1-21
- "ADC Interface" on page 1-22
- "UART Interface" on page 1-23
- "RTC Interface" on page 1-24
- "LEDs and Push Buttons" on page 1-24
- "JTAG Interface" on page 1-25
- "Land Grid Array" on page 1-26
- "Expansion Interface II" on page 1-26
- "Power Measurements" on page 1-27
- "Power-On-Self Test" on page 1-28
- "Example Programs" on page 1-28
- "Board Design Database" on page 1-28

For information about the graphical user interface, including the boot loading, target options, and other facilities of the EZ-Board system, refer to the online help.

For more information about the ADSP-BF518F Blackfin processor, see documents referred to at "Related Documents".

Package Contents

Your ADSP-BF518F EZ-Board evaluation system package contains the following items.

- ADSP-BF518F EZ-Board
- Universal 5.0V DC power supply
- Secure digital (SD) memory card
- 7-foot Ethernet patch cable
- Two 6-foot 3.5 mm male-to-male audio cables
- 3.5 mm stereo earbuds

If any item is missing, contact the vendor where you purchased your EZ-Board or contact Analog Devices, Inc.

Default Configuration

The EZ-Board evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store the unused EZ-Board in the protective shipping package.

The ADSP-BF518F EZ-Board board is designed to run outside your personal computer as a standalone unit. You do not have to open your computer case.

When removing the EZ-Board from the package, handle the board carefully to avoid the discharge of static electricity, which can damage some components. Figure 1-1 shows the default jumper and switch settings,

connector locations, and LEDs used in installation. Confirm that your board is in the default configuration before using the board.

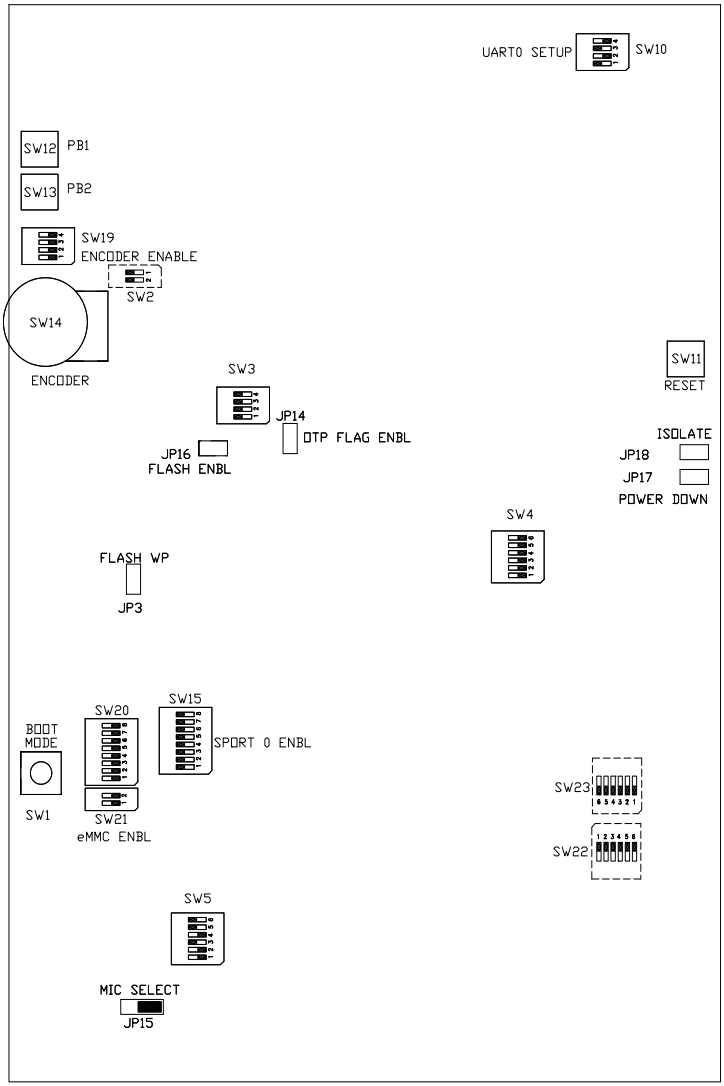

Figure 1-1. Default EZ-Board Hardware Setup

CCES Install and Session Startup

For information about CCES and to download the software, go to www.analog.com/CCES. A link for the ADSP-BF518F EZ-KIT Lite Board Support Package (BSP) for CCES can be found at http://www.analog.com/Blackfin/EZKits.

Follow these instructions to ensure correct operation of the product software and hardware.

Step 1: Connect the EZ-KIT Lite board to a personal computer (PC) running CCES using one of two options: an Analog Devices emulator or via the debug agent.

Using an Emulator:

1. Plug one side of the USB cable into the USB connector of the emulator. Plug the other side into a USB port of the PC running CCES.
2. Attach the emulator to the header connector P1 (labeled JTAG) on the EZ-Board.

Using the standalone Debug Agent:

1. Attach the standalone debug agent to connectors P1 (labeled JTAG) and ZP1 of the EZ-Board.
2. Plug one side of the USB cable into the USB connector of the debug agent P4. Plug the other side of the cable into a USB port of the PC running CCES.

Step 2: Attach the provided cord and appropriate plug to the 5V power adaptor.

1. Plug the jack-end of the power adaptor into the power connector `J3` (labeled `5V`) on the EZ-Board.
2. Plug the other side of the power adaptor into a power outlet. The power LED (labeled `LED13`) is lit green when power is applied to the board.
3. Power the emulator (if used). Plug the jack-end of the assembled power adaptor into the emulator and plug the other side of the power adaptor into a power outlet. The enable/power is lit green when power is applied.

Step 3 (if connected through the debug agent): Verify that the yellow USB monitor LED (labeled `LED2`) and the green power LED (labeled `LED1`) on the debug agent are both on. This signifies that the board is communicating properly with the host PC and ready to run CCES.

Session Startup

It is assumed that the CrossCore Embedded Studio software is installed and running on your PC.

Note: If you connect the board or emulator first (before installing CCES) to the PC, the Windows driver wizard may not find the board drivers.

1. Navigate to the CCES environment via the **Start** menu.

   Note that CCES is not connected to the target board.

2. Use the system configuration utility to connect to the EZ-Board.

   If a debug configuration exists already, select the appropriate configuration and click **Apply and Debug** or **Debug**. Go to step 8.

   To create a debug configuration, do one of the following:

   - Click the down arrow next to the little bug icon, select **Debug Configurations**
   - Choose **Run** > **Debug Configurations**.

   The **Debug Configuration** dialog box appears.

3. Select **CrossCore Embedded Studio Application** and click (**New launch configuration**).

   The **Select Processor** page of the **Session Wizard** appears.

4. Ensure **Blackfin** is selected in **Processor family**. In **Processor type**, select **ADSP-BF518F**. Click **Next**.

   The **Select Connection Type** page of the **Session Wizard** appears.

5. Select one of the following:

   - For standalone debug agent connections, **EZ-Board** and click **Next**.
   - For emulator connections, **Emulator** and click **Next**.

   The **Select Platform** page of the **Session Wizard** appears.

6. Do one of the following:
   - For standalone debug agent connections, ensure that the selected platform is **ADSP-BF518F EZ-Board** via Debug Agent.
   - For emulator connections, choose the type of emulator that is connected to the board.
7. Click **Finish** to close the wizard.

   The new debug configuration is created and added to the program(s) to load list.
8. In the **Program(s) to load** section, choose the program to load when connecting to the board. If not loading any program upon connection to the target, do not make any changes.

   Note that while connected to the target, there is no way to choose a program to download. To load a program once connected, terminate the session.

To delete a configuration, go to the **Debug Configurations** dialog box and select the configuration to delete. Click ✖ and choose **Yes** when asked if you wish to delete the selected launch configuration. Then **Close** the dialog box.

To disconnect from the target board, click the terminate button (red box) or choose **Run** > **Terminate**.

To delete a session, choose **Target** > **Session** > **Session List**. Select the session name from the list and click **Delete**. Click **OK**.

VisualDSP++ Install and Session Startup

For information about VisualDSP++ and to download the software, go to www.analog.com/VisualDSP.

There are two options to connect the EZ-Board hardware to a personal computer (PC) running VisualDSP++: via an Analog Devices emulator or via a standalone debug agent module. The standalone debug agent allows a debug agent to interface to the ADSP-BF518F EZ-Board. The standalone debug agent is shipped with the kit.

To connect the EZ-Board to a PC via an emulator:

1. Plug the 5V adaptor into connector J3 (labeled 5V).
2. Attach the emulator header to connector P1 (labeled JTAG) on the back side of the EZ-Board.

To connect the EZ-Board to a PC via a standalone debug agent:

The debug agent can be used only when power is supplied from the wall adaptor.

1. Attach the standalone debug agent to connectors P1 (labeled JTAG) and ZP1 on the backside of the EZ-Board, watching for the keying pin of P1 to connect correctly. Plug the 5V adaptor into connector J3 (labeled 5V).
2. Plug one side of the provided USB cable into the USB connector of the standalone debug agent. Plug the other side of the cable into a USB port of the PC running VisualDSP++.
3. Verify that the yellow USB monitor LED on the standalone debug agent (LED2, located on the back side of the board) is lit. This signifies that the board is communicating properly with the host PC and ready to run VisualDSP++.

Session Startup

1. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start > Programs** menu. The main window appears. Note that VisualDSP++ is not connected to any session. Skip the rest of this step to step 2.

   If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 3.

2. To connect to a new EZ-Board session, start **Session Wizard** by selecting one of the following.

   - From the **Session** menu, **New Session**.
   - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
   - From the **Session** menu, **Connect to Target**.

3. The **Select Processor** page of the wizard appears on the screen. Ensure **Blackfin** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-BF518F**. Click **Next**.

4. The **Select Connection Type** page of the wizard appears on the screen. For standalone debug agent connections, select **EZ-Board** and click **Next**. For emulator connections, select **Emulator** and click **Next**.

5. The **Select Platform** page of the wizard appears on the screen. For standalone debug agent connections, ensure that the selected platform is **ADSP-BF518F EZ-Board via Debug Agent**. For emulator connections, choose the type of emulator that is connected.

Specify your own **Session name** for the session or accept the default name.

The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and open a new session.

Click **Next**.

6. The **Finish** page of the wizard appears on the screen. The page displays your selections. Check the selections. If you are not satisfied, click **Back** to make changes; otherwise, click **Finish**. VisualDSP++ creates the new session and connects to the EZ-Board. Once connected, the main window's title is changed to include the session name set in step 5.

To disconnect from a session, click the disconnect button or select **Session > Disconnect from Target**.

To delete a session, select **Session > Session List**. Select the session name from the list and click **Delete**. Click **OK**.

CCES Evaluation License

The ADSP-BF518F EZ-Board software is part of the Board Support Package (BSP) for the Blackfin ADSP-BF51x family. The EZ-Board is a licensed product that offers an unrestricted evaluation license for 90 days after activation. Once the evaluation period ends, the evaluation license becomes permanently disabled. If the evaluation license is installed but

not activated, it allows 10 days of unrestricted use and then becomes disabled. The license can be re-enabled by activation.

An evaluation license can be upgraded to a full license. Licenses can be purchased from:

- Analog Devices directly. Call (800) 262-5645 or 781-937-2384 or go to:
  http://www.analog.com/buyonline.
- Analog Devices, Inc. local sales office or authorized distributor. To locate one, go to:
  http://www.analog.com/salesdir/continent.asp.

The EZ-Board hardware must be connected and powered up to use CCES with a valid evaluation or full license.

VisualDSP++ Evaluation License

The ADSP-BF518F EZ-Board installation is part of the VisualDSP++ installation. The EZ-Board is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ restricts a connection to the ADSP-BF518F EZ-Board via the USB port of the standalone debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user program to 12 KB of memory for code space with no restrictions for data space.

To avoid errors when opening VisualDSP++, the EZ-Board hardware must be connected and powered up. This is true for using VisualDSP++ with a valid evaluation or full license.

Lockbox Key Security Features

Blackfin processors feature Lockbox® secure technology: hardware-enabled code security and content protection for one-time programmable (OTP) memory. Customers purchasing Blackfin processors can program their own customer public key in OTP.

The ADSP-BF518F EZ-Boards are evaluation boards with the Lockbox key pre-programmed and publicly documented—the burden of key generation and OTP programming of public keys is removed from the customer. Customers can still program other areas of OTP memory on the ADSP-BF518F EZ-Board. Analog Devices publicly document the EZ-Board's public and private key pair for customer evaluation and support of the Lockbox feature, all while avoiding any keys information exchange. As a result, there is no confidentiality associated with the Lockbox key on EZ-Boards.

To demonstrate Lockbox features using an EZ-Board, you must use the keys that are provided pre-programmed on your EZ-Board.

Use the EZ-Board key pair to generate a demo and then provide the keys to the demo users. Note that the EZ-Board cannot be used to secure any confidential information. If you wish to create a demo with confidential keys, you must build your own Blackfin board and personalize it with your own keys.

Memory Map

The ADSP-BF518F processor has internal static random access memory (SRAM) used for instructions and data storage. See Table 1-1. The internal memory details can be found in the *ADSP-BF51x Blackfin Processor Hardware Reference.*

The ADSP-BF518F EZ-Board includes four types of external memory: synchronous dynamic random access memory (SDRAM), serial peripheral

interconnect (SPI) flash, parallel flash, and eMMC. See Table 1-2. For more information about a specific memory type, go to the respective section in this chapter.

Table 1-1. EZ-Board Internal Memory Map

Start Address	Content
0xEF00 0000	BOOT ROM (32K BYTE)
0xEF00 8000	Reserved
0xFF80 0000	DATA BANKA SRAM (16K BYTE)
0xFF80 4000	DATA BANKA SRAM/CACHE (16K BYTE)
0xFF80 8000	Reserved
0xFF90 0000	DATA BANKB SRAM (16K BYTE)
0xFF90 4000	DATA BANKB SRAM/CACHE (16K BYTE)
0xFF90 8000	Reserved
0xFFA0 0000	INSTRUCTION BANK A SRAM (16K BYTE)
0xFFA0 4000	INSTRUCTION BANK B SRAM (16K BYTES)
0xFFA0 8000	Reserved
0xFFA1 0000	INSTRUCTION BANK C SRAM/CACHE (16K BYTE)
0xFFA1 4000	Reserved
0xFFB0 0000	SCRATCHPAD SRAM (4K BYTE)
0xFFB0 1000	Reserved
0xFFC0 0000	SYSTEM MMR REGISTERS
0xFFE0 0000	CORE MMR REGISTERS

Table 1-2. EZ-Board External Memory Map

Start Address	End Address	Content
0x0000 0000	0x03FF FFFF	SDRAM (SDRAM)
0x0800 0000	0x1FFF FFFF	Reserved
0x2000 0000	0x200F FFFF	ASYNC memory bank 0 (flash)

Table 1-2. EZ-Board External Memory Map (Cont'd)

Start Address	End Address	Content
0x2010 0000	0x201F FFFF	ASYNC memory bank 1 (flash)
0x2020 0000	0x202F FFFF	ASYNC memory bank 2 (flash)
0x2030 0000	0x203F FFFF	ASYNC memory bank 3 (flash)
0x2040 0000	0xEEFF FFFF	Reserved

SDRAM Interface

The ADSP-BF518F processor connects to a 64 MB Micron MT48LC32M16A2TG-75 chip through the external bus interface unit (EBIU). The SDRAM chip can operate at a maximum clock frequency of 80 MHz, which is the ADSP-BF518F processor limitation.

With a CCES or VisualDSP++ session running and connected to the EZ-Board via the USB standalone debug agent, the SDRAM registers are configured automatically each time the processor is reset. The values are used whenever SDRAM is accessed through the debugger (for example, when viewing memory windows or loading a program).

To disable the automatic setting of the SDRAM registers, do one of the following:

- CCES users, choose **Target > Settings > Target Options** and clear the **Use XML reset values** check box.
- VisualDSP++ users, choose **Settings > Target Options** and clear the **Use XML reset values** check box.

For more information on changing the reset values, refer to the online help.

An example program is included in the EZ-Board installation directory to demonstrate how to setup and access the SDRAM interface. For more

information on how to initialize the registers after a reset, search the online help for “reset values”.

Parallel Flash Memory Interface

The parallel flash memory interface of the ADSP-BF518F EZ-Board contains a 4 MB (2M x 16 bits) Numonyx M29W320EB chip. Flash memory connects to the 16-bit data bus and address lines 1 through 19. Chip enable is decoded by the $\overline{\text{AMS0–3}}$ select lines through NAND and AND gates. The address range for flash memory is 0x2000 0000 to 0x203F FFFF.

Flash memory is pre-loaded with boot code for the power-on-self test (POST) program. For more information, refer to “Power-On-Self Test” on page 1-28. Flash memory also is preloaded with configuration flash information, which contains board revision, BOM revision, and other data.

By default, the EZ-Board boots from the 16-bit parallel flash memory. The processor boots from flash memory if the boot mode select switch (SW1) is set to position 1 (see “Boot Mode Select Switch (SW1)” on page 2-8).

Flash memory code can be modified. For instructions, refer to the online help and example program included in the EZ-Board installation directory.

For more information about the parallel flash device, refer to the Numonyx Web site: http://www.numonyx.com.

eMMC Interface

The ADSP-BF518F processor is equipped with a removable storage interface (RSI), which allows the 8 GB Micron eMMC flash memory device to be attached gluelessly to the processor. The eMMC interface is attached

via the processor's specific RSI control and data lines. The eMMC interface shares pins with the secure digital (SD) interface, push buttons, analog-to-digital converter (ADC) and expansion interface II.

The RSI signals can be disconnected from the eMMC interface by turning switches SW20 and SW21 all OFF. See "eMMC Enable Switch (SW20–21)" on page 2-13 for more information.

For more information about the eMMC device, refer to the Micron Web site: http://www.micron.com.

An example program is included in the EZ-Board installation directory to demonstrate how to setup and access the eMMC interface.

SD Interface

The ADSP-BF518F processor has a secure digital interface. The SD interface consists of a clock pin, a command pin, a card detect pin, and a four-bit data bus. The SD interface of the processor connects gluelessly to the on-board SD connector. The SD interface is attached via the processor's specific RSI control and data lines. The interface shares pins with the eMMC interface, codec, and expansion interface II. The memory can be written to in one-bit and four-bit modes. For more information, refer to "SD Connector (J13)" on page 2-22. An example program is included in the EZ-Board installation directory to demonstrate how to setup and access the SD interface.

SPI Interface

The ADSP-BF518F processor has two serial peripheral interface (SPI) ports with multiple chip select lines. The SPI0 port connects directly to serial flash memory and expansion interface II.

External serial flash memory is a 16 Mb ST M25P16 device, selected using the SPISEL2 line of the processor. By default, SPI flash is not connected to the processor; see "SPI FLASH CS Enable Jumper (JP16)" on page 2-16 for more information. Internal serial flash memory is a 4 Mb device, selected using an internal SPISSEL line of the processor.

External SPI flash memory is factory programmed with Das U-Boot—the universal boot loader. Das U-Boot (*U-Boot* for short) is open source firmware for embedded processors, including the ADSP-BF518F Blackfin processors. U-Boot can load files from a variety of peripherals, such as a serial connection, an Ethernet network connection, or flash memories. U-Boot is executed at system reset, which automatically loads up another application (such as the Linux kernel or a stand alone application). U-Boot can parse many types of files on many types of storage devices.

U-Boot is controlled via a serial connection. The default setting is 56700 baud, 8 data bits, No parity, 1 stop bit. See "RS-232 Connector (J2)" on page 2-21 for information on the serial connector.

For more information about U-Boot, refer to the online documentation at:

http://docs.blackfin.uclinux.org/doku.php?id=bootloaders:u-boot.

For U-Boot support on the Blackfin processors, refer to the online help forums at:

http://blackfin.uclinux.org/gf/project/u-boot/forum/?action=ForumBrowse&forum_id=51.

SPI flash can be modified. For instructions, refer to the online help, example program included in the EZ-Board installation directory, and U-Boot documentation. U-Boot includes an SPI flash driver and can be used to download a new file over Ethernet or serial connection, and write the file to SPI flash.

By default, the EZ-Board boots from the 16-bit flash parallel memory. Internal or external SPI flash can be selected as the boot source by setting the boot mode select switch (SW1) to position 3. See "Boot Mode Select Switch (SW1)" on page 2-8.

Parallel Peripheral Interface (PPI)

The ADSP-BF518F processor provides a parallel peripheral interface (PPI), supporting data widths up to 16 bits. The PPI interface provides three multiplexed frame syncs, a multiplexed clock, and 16 multiplexed data lines. The full PPI port is accessible on the expansion interface II connector (P3). See "Expansion Interface II Connector (P3)" on page 2-24.

The PPI signals connect to multi-functional pins. The PPI is shared with the on-board codec, eMMC interface, SD interface, and Ethernet IC. To use the PPI on the expansion interface, disable the codec by turning switch SW15 to all OFF (see "SPORT0 ENBL Switch (SW15)" on page 2-12). The eMMC interface is disabled by turning switches SW20 and SW21 to all OFF, and the SPI flash is disabled by removing the jumper from JP16. See "eMMC Enable Switch (SW20–21)" on page 2-13 and "SPI FLASH CS Enable Jumper (JP16)" on page 2-16 for more information.

The PPI is not used on the EZ-Board, the PPI is intended for use on the expansion interface II.

Rotary Encoder Interface

The ADSP-BF518F processor has a built-in, up-down counter with support for a rotary encoder. The three-wire rotary encoder interface connects to the thumbwheel rotary switch (SW19) and expansion interface II. The rotary encoder can be turned clockwise for the up function, counter

clockwise for the down function, or can be pushed towards the center of the board to clear the counter.

The rotary switch is a two-bit quadrature (gray code) counter with a detent, meaning that both the down signal (CDG) and up signal (CUD) toggle when the count register increases on a rotation to the right. Upon rotating to the left, CDG and CUD toggle, and the overall count decreases.

If the processor pins are needed for the expansion interface II, disconnect the rotary encoder switch via the three-position rotary enable switch (SW19). For more information, see "Encoder Enable Switch (SW19)" on page 2-13.

An example program is included in the EZ-Board installation directory to demonstrate how to set up and access the rotary encoder interface.

Ethernet Interface

The ADSP-BF518F processor has an integrated Ethernet MAC with a media independent interface (MII), which connects to an external PHY device. The EZ-Board provides a National Semiconductor DP83848C Ethernet PHY with auto-MDIX, fully compliant with IEEE 802.3u standards. The DP83848C chip supports 10BASE-T and 100BASE-TX operations. The part is attached gluelessly to the processor.

The Ethernet signals are shared with the PPI signals, connected to the expansion interface II, and two MII connectors that can be used to interface with other PHY evaluation boards.

The PHY can be put into a power-down mode by installing JP17. The power-down mode should be used whenever the PHY is not used, and the expansion interface signals are used. See "Ethernet Power Down Jumper (JP17)" on page 2-16 for more information. The PHY can be put into isolate mode by installing JP18. The isolate mode should be used whenever the PHY is not used, and another PHY is connected to one of the MII

connectors. See "Ethernet Isolate Jumper (JP18)" on page 2-16 for more information.

The Ethernet chip is pre-loaded with a MAC address. The MAC address for the EZ-Board is stored in the configuration flash section of the parallel flash memory and can be found on a sticker on the bottom side of the board.

The PHY device connects to a PulseJack with integrated magnetics and a standard RJ-45 connector (J14). For more information, see "Ethernet Connector (J14)" on page 2-22.

Example programs are included in the EZ-Board installation directory to demonstrate how to use the Ethernet interface.

Audio Interface

The audio interface of the EZ-Board consists of a low-power stereo codec, SSM2603, with an integrated headphone driver and associated passive components. There are two inputs, a stereo line in, and a mono microphone, as well as two outputs, a headphone, and a stereo line out. The codec has integrated stereo ADCs, digital-to-analog converters (DACs), and requires minimal external circuitry.

The codec connects to the ADSP-BF518F processor via the processor's serial port 0. The SPORT0 is disconnected from the codec by turning switch SW15 OFF, which enables SPORT0 for the SD/eMMC interfaces or the expansion interface II. See "SPORT0 ENBL Switch (SW15)" on page 2-12 for more information.

The control interface of the codec is via a 2-wire interface (TWI).

Mic gain values of 14 dB, 0 dB, or –6 dB are selectable through switch SW5. For more information, see "MIC Gain/Loopback Switch (SW5)" on page 2-10.

Microphone bias is provided through a low-noise reference voltage. A jumper on positions 2&3 of JP15 connects the MICBIAS signal to the audio jack. Placing a jumper on positions 1&2 of JP15 connects the bias directly to the mic signal. For more information, see "MIC Select Jumper (JP15)" on page 2-16.

J4 and J5 are 3.5 mm connectors for the audio portion of the board. J5 connects the mic on the top portion and line-in on the bottom. J4 connects the headphone on the top portion and line-out on the bottom. If there is no 3.5 mm cable plugged into the bottom of either J4 or J5, the signals are looped back inside the connector. For more information, see "Dual Audio Connectors (J4–5)" on page 2-22.

For testing, SW15 position 4 connects the MICIN signal to the right headphone. SW5 positions 5 and 6 loop the output of the codec to the input when no cables are connected to J4 and J5. For more information, see "SPORT0 ENBL Switch (SW15)" on page 2-12.

The EZ-Board is shipped with two 3.5 mm cables, which allow you to run the example programs provided in the EZ-Board installation directory and learn about the audio interface.

ADC Interface

The ADC interface of the EZ-Board consists of a dual, 12-bit, high-speed, low-power, successive approximation analog-to-digital converter. The device contains two converters, each preceded by a 3-channel multiplexer, a low-noise, wide-bandwidth track, and holds an amplifier that can handle input frequencies in excess of 30 MHz. The inputs to the ADC are configurable as either six differential or twelve single-ended inputs. The inputs are accessed via a .1" spaced IDC connector.

The ADC connects to the ADSP-BF518F processor via the processor's serial port 1. SPORT1 is disconnected from the ADC by turning switch SW4 OFF, which enables SPORT1 for the expansion interface II or for the

multi-function pins. In the latter case, the port's signals can be used for the RSI or as push buttons. See "SPORT1 Enable Switch (SW4)" on page 2-10 for more information.

The ADC range is controlled by switch SW4 position 5. The switch selects between the 2.5V and 5V input ranges. The max voltage range for a signal connected to the ADC inputs is 0–5V. Any voltage outside of the range can damage the EZ-Board. For more information, see "SPORT1 Enable Switch (SW4)" on page 2-10.

For testing, switches SW22-23 connect an audio output signal of the codec to the input channels of the ADC. Do not connect the ADC input connectors and have switches SW22-23 ON at the same time. For more information, see "ADC Loopback Switches (SW22–23)" on page 2-13.

UART Interface

The ADSP-BF518F processor has two built-in universal asynchronous receiver transmitters (UARTs). UART0–1 share the processor's pins with other peripherals on the EZ-Board.

UART0 has full RS-232 functionality via the Analog Devices 3.3V ADM3202 line driver and receiver (U21). When using UART0, do not set switch SW10 position 4 to ON. This setting enables UART loopback and should be installed only when running the POST program.

UART0 and UART1 are connected to the expansion interface II connectors. For more information, see "Expansion Interface II Connectors (P2 and P4)" on page 2-24.

Example programs are included in the EZ-Board installation directory to demonstrate UART and RS-232 operations.

For more information on the UART interface, refer to the *ADSP-BF51x Blackfin Processor Hardware Reference*.

RTC Interface

The ADSP-BF518F processor has a real-time clock (RTC) and a watchdog timer. Typically, the RTC interface is used to implement a real-time watchdog or a life counter of the time elapsed since the last system reset. The EZ-Board is equipped with a Panasonic CR1632 lithium coin and 3V battery supplying 125 mAh. The 3V battery and 3.3V supply of the board connect to the `RTC` power pin of the processor. When the EZ-Board is powered, the RTC circuit uses the board power to supply voltage to the `RTC` pin. When the EZ-Board is not powered, the RTC circuit uses the lithium battery to maintain power to the `RTC` pin. After removing the mylar, the battery lasts for about one year with the EZ-Board unpowered.

Example programs are included in the EZ-Board installation directory to demonstrate the RTC features.

The EZ-Board is shipped with a protective Mylar sheet placed between the coin battery and positive pin of the battery holder. Remove the Mylar sheet before using the RTC in the processor.

For more information on the RTC and watchdog timer, refer to the *ADSP-BF51x Blackfin Processor Hardware Reference*.

LEDs and Push Buttons

The EZ-Board provides two push buttons and three LEDs for general-purpose I/O, as well as two additional push buttons intended for power down and wake functionality, which also can be used as GPIO flag pins.

The three LEDs, labeled `LED1` through `LED3`, are accessed via the `PH3`, `PH5`, and `PH6` pins of the processor (respectively). For information on how to program the flag pins, refer to the *ADSP-BF51x Blackfin Processor Hardware Reference*.

LED1 is shared with the ADC_A0, MMC_D7, and OTP_EN signals. LED2 is shared with the CDG and ADC_A1 signals. LED3 is shared with the CZM and ADC_A2 signals.

The LED1–3 signals also connect to the expansion interface II connectors. See "Expansion Interface II Connector (J1)" on page 2-21 and "Expansion Interface II Connectors (P2 and P4)" on page 2-24 for more information.

The two general-purpose push buttons are labeled PB1 and PB2. The status of each individual button can be read through programmable flag inputs PH0 and PH1. The flag reads '1' when a corresponding switch is being pressed. When the switch is released, the flag reads '0'. A connection between the push buttons and processor inputs is established through positions 1&2 of the DIP switch, SW2.

Push buttons 1 and 2 of SW2 are used as GPIO signals on the expansion interface II connectors (J1, P2, P4). To use the PH0 and PH1 port pins as GPIO signals on the expansion interface II, turn SW2 to all OFF.

PB1 is shared with the DR1PRI and MMC_D4 signals. PB2 is shared with the RFS1 and MMC_D5signals.

An example program is included in the ADSP-BF518F installation directory to demonstrate functionality of the LEDs and push buttons.

JTAG Interface

The JTAG connector (P1) allows the standalone debug agent to connect a debug session to the ADSP-BF518F processor. The debug agent operates only when the external 5V wall adaptor is used (J3). When operating the EZ-Board from a battery or USB bus power, the debug agent is not powered.

The standalone debug agent can be removed, and an external emulator can be attached to the EZ-Board. Be careful not to damage the connectors when removing the debug agent. The emulator connects to P1 on the back

side of the board. See "CCES Install and Session Startup" on page 1-5 or "VisualDSP++ Install and Session Startup" on page 1-9 for more information.

For more information about emulators, contact Analog Devices or go to:

http://www.analog.com/processors/tools/blackfin.

Land Grid Array

The ADSP-BF518F EZ-Board has provisions for probing every port pin and the EBIU interface of the processor on connectors P5–7. The connector locations are intended for use with a Tektronix DMAX logic analyzer connector, but can be probed with any oscilloscope or logic analyzer. For pinout information, refer to"ADSP-BF518F EZ-Board Schematic" on page B-1.

For more information on the Tektronix DMAX logic analyzer interface, go to the Tektronix Web site.

Expansion Interface II

The expansion interface II allows an Analog Devices EZ-Extender® or a custom-design daughter board to be tested across various hardware platforms that have the same expansion interface.

The expansion interface II implemented on the ADSP-BF518F EZ-Board consists of four connectors, three of which are 0.1 in. shrouded headers (P2–4), and the last of which is a Samtec QMS series header (J1). The connectors contain a majority of the ADSP-BF518F processor's signals. For pinout information, go to "ADSP-BF518F EZ-Board Schematic" on page B-1. The mechanical dimensions of the expansion connectors can be obtained by contacting Technical Support.

For more information about daughter boards, visit the Analog Devices Web site at:

http://www.analog.com/processors/tools/blackfin.

Limits to current and interface speed must be taken into consideration when using the expansion interface II. Current for the expansion interface II is sourced from the EZ-Board; therefore, the current should be limited to 1A for 5V and 500 mA for the 3.3V planes. If more current is required, then a separate power connector and a regulator must be designed on a daughter card. Additional circuitry can add extra loading to signals, decreasing their maximum effective speed.

Analog Devices does not support and is not responsible for the effects of additional circuitry.

Power Measurements

Several locations are provided for measuring the current draw from various power planes. Precision 0.1 ohm shunt resistors are available on the VDDINT, VDDEXT, VDDMEM, and VDDFLASH voltage domains. For current draw measuments, the associated jumper (P8–11) must be removed. Once the jumper is removed, voltage across the resistor can be measured using an oscilloscope. Once voltage is measured, current can be calculated by dividing the voltage by 0.1. For the highest accuracy, a differential probe should be used for measuring voltage across the resistor.

For more information, see "VDDINT Power Jumper (P8)" on page 2-16, "VDDEXT Power Jumper (P9)" on page 2-17, "VDDMEM Power Jumper (P10)" on page 2-17, and "VDDFLASH Power Jumper (P11)" on page 2-17.

Power-On-Self Test

The power-on-self-test program (POST) tests all EZ-Board peripherals and validates functionality as well as connectivity to the processor. Once assembled, each EZ-Board is fully tested for an extended period of time with a POST. All EZ-Boards are shipped with the POST preloaded into one of their on-board flash memories. The POST is executed by resetting the board and pressing the proper push button(s). The POST also can be used for reference for a custom software design or hardware troubleshooting. Note that the source code for the POST program is included in the installation directory along with the readme file, which describes how the board is configured to run a POST.

The POST program is only available when using VisualDSP++.

Example Programs

Example programs are provided with the ADSP-BF518F EZ-KIT Lite to demonstrate various capabilities of the product. The programs are included in the product installation kit and can be found in the `Examples` folder of the installation. Refer to a readme file provided with each example for more information.

CCES users are encouraged to use the example browser to find examples included with the EZ-KIT Lite Board Support Package.

Board Design Database

A `.zip` file containing all of the electronic information required for the design, layout, fabrication and assembly of the product is available for download from the Analog Devices board design database at: http://www.analog.com/board-design-database.

2 ADSP-BF518F EZ-BOARD HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-BF518F EZ-Board board.

The following topics are covered.

- "System Architecture" on page 2-2
  Describes the ADSP-BF518F EZ-Board configuration and explains how the board components interface with the processor.
- "Programmable Flags" on page 2-3
  Shows the locations and describes the programming flags (PFs).
- "Push Button and Switch Settings" on page 2-7
  Shows the locations and describes the push buttons and switches.
- "Jumpers" on page 2-14
  Shows the locations and describes the configuration jumpers.
- "LEDs" on page 2-18
  Shows the locations and describes the LEDs.
- "Connectors" on page 2-20
  Shows the locations and provides part numbers for the on-board connectors. In addition, the manufacturer and part number information is provided for the mating parts.

System Architecture

This section describes the processor's configuration on the EZ-Board (Figure 2-1).

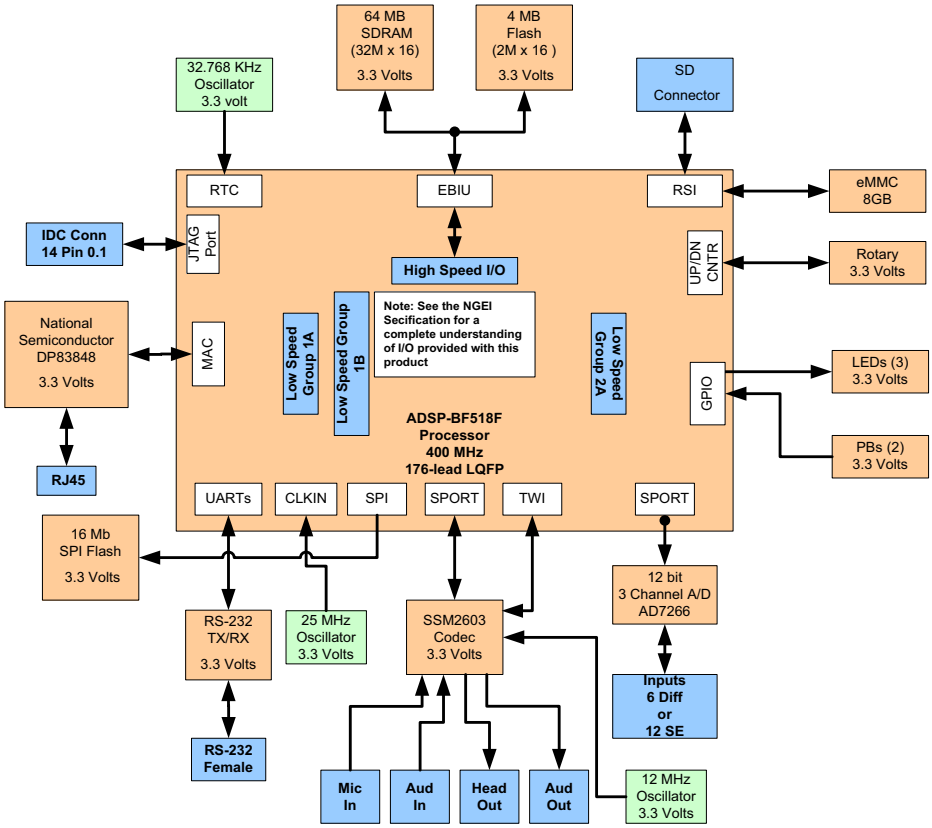

Figure 2-1. System Architecture

This EZ-Board is designed to demonstrate the ADSP-BF518F Blackfin processor capabilities. The processor has an I/O voltage of 3.3V. The core voltage of the processor is controlled by an Analog Devices ADP1715 low dropout regulator (LDO) and an Analog Devices AD5258 digipot, which

is configurable over the 2-wire interface (TWI) signals. Refer to the power-on-self test (POST) example in the ADSP-BF518F installation directory for information on how to set up the TWI interface.

The core voltage and clock rate can be set on the fly by the processor. The input clock is 25 MHz. A 32.768 kHz crystal supplies the real-time clock (RTC) inputs of the processor. The default boot mode for the processor is external parallel flash boot. See "Boot Mode Select Switch (SW1)" on page 2-8 for information on how to change the default boot mode.

Programmable Flags

The processor has 40 general-purpose input/output (GPIO) signals spread across three ports (PF, PG, and PH). The pins are multi-functional and depend on the ADSP-BF518F processor setup. The following tables show how the programmable flag pins are used on the EZ-Board.

- PF programmable flag pins – Table 2-1
- PG programmable flag pins – Table 2-2
- PH programmable flag pins – Table 2-3

Table 2-1. PF Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-Board Function
PF0	ETxD2/PPID0/SPI1_SSEL2/TACLK6	Default: ETXD2 Land grid array, expansion interface II
PF1	ERxD2/PPID1/PWM_AH/TACLK7	Default: ERXD2 Land grid array, expansion interface II
PF2	ETxD3/PPID2/PWM_AL	Default: ETXD3 Land grid array, expansion interface II
PF3	ERxD3/PPID3/PWM_BH/TACLK0	Default: ERXD3 Land grid array, expansion interface II

Table 2-1. PF Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-Board Function
PF4	ERxCLK/PPID4/PWM_BL/TACLK1	Default: ERXCLK Land grid array, expansion interface II
PF5	ERxDV/PPID5/PWM_CH/TACI0	Default: ERXDV Land grid array, expansion interface II
PF6	COL/PPID6/PWM_CL/TACI1	Default: COL Land grid array, expansion interface II
PF7	SPI0_SSEL1/PPID7/PWM_SYNC	Default: not used Land grid array, expansion interface II
PF8	MDC/PPID8/SPI1_SSEL4	Default: MDC Land grid array, expansion interface II
PF9	RMIIMDIO/PPID9/TMR2	Default: MDIO Land grid array, expansion interface II
PF10	ETxD0/PPID10/TMR3	Default: ETXD0 Land grid array, expansion interface II
PF11	ERxD0/PPID11/PWM_AH/TACI3	Default: ERXD0 Land grid array, expansion interface II
PF12	ETxD1/PPID12/PWM_AL	Default: ETXD1 Land grid array, expansion interface II
PF13	ERxD1/PPID13/PWM_BH	Default: ERXD1 Land grid array, expansion interface II
PF14	ETxEN/PPID14/PWM_BL	Default: ETXEN Land grid array, expansion interface II
PF15	RMII_PHYINT/PPID15/PWM_SYNC	Default: RMII_PHYINT Land grid array, expansion interface II

Table 2-2. PG Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-Board Function
PG0	MIICRS/RMI-ICRS/HWAIT/SPI1_SSEL3	Default: MIICRS HWAIT, land grid array, expansion interface II
PG1	ERxER/DMAR1/PWM_CH	Default: ERXER Land grid array, expansion interface II
PG2	MIITxCLK/RMIIREF_CLK/DMAR0/PWM_CL	Default: MIITXCLK Land grid array, expansion interface II
PG3	DR0PRI/RSI_DATA0/SPI0_SSEL5/TACLK3	Default: DR0PRI SD_D0, land grid array, expansion interface II
PG4	RSCLK0/RSI_DATA1/TMR5/TACI5	Default: RSCLK0 SD_D1, land grid array, expansion interface II
PG5	RFS0/RSI_DATA2/PPICLK_1/TMRCLK	Default: RFS0 SD_D2, land grid array, expansion interface II
PG6	TFS0/RSI_DATA3/TMR0/PPIFS1_1	Default: TFS0 SD_D3, land grid array, expansion interface II
PG7	DT0PRI/RSI_CMD/TMR1/PPIFS2_1	Default: DT0PRI SD_CMD, land grid array, expansion interface II
PG8	TSCLK0/RSI_CLK/TMR6/TACI6	Default: TSCLK0 SD_CLK, land grid array, expansion interface II
PG9	DT0SEC/UART0_TX/TMR4	Default: UART0_TX Land grid array, expansion interface II
PG10	DR0SEC/UART0_RX/TACI4	Default: UART0_RX Land grid array, expansion interface II
PG11	SPI0_SS/AMS[2]/SPI1_SSEL5/TACLK2	Default: AMS2 Land grid array, expansion interface II
PG12	SPI0_SCK/PPICLK_2/TMRCLK	Default: SPI0_SCK Land grid array, expansion interface II
PG13	SPI0_MISO/TMR0/PPIFS1_2	Default: SPI0_MISO Land grid array, expansion interface II

Table 2-2. PG Port Programmable Flag Connections (Cont'd)

Processor Pin	Other Processor Function	EZ-Board Function
PG14	SPI0_MOSI/TMR1/PPIFS2_2/ PWM_TRIPB	Default: SPI0_MOSI Land grid array, expansion interface II
PG15	SPI0_SSEL2/PPIFS3/AMS[3]	Default: AMS3 SPI0_SEL2, land grid array, expansion interface II

Table 2-3. PH Port Programmable Flag Connections

Processor Pin	Other Processor Function	EZ-Board Function
PH0	DR1PRI/SPI1_SS/RSI_DATA4	Default: PB1 DR1PRI, MMC_D4, land grid array, expansion interface II
PH1	RFS1/SPI1_MISO/RSI_DATA5	Default: PB2 RFS1, MMC_D5, land grid array, expansion interface II
PH2	RSCLK1/SPI1_SCK/RSI_DATA6	Default: not used RSCLK1, MMC_D6, land grid array, expansion interface II
PH3	DT1PRI/SPI1_MOSI/RSI_DATA7	Default: LED1 ADC_A0, MMC_D7, OTP_EN, land grid array, expansion interface II
PH4	TFS1/AOE/SPI0_SSEL3/CUD	Default: CUD SD card detect, land grid array, expansion interface II
PH5	TSCLK1/ARDY/ECLK/CDG	Default: LED2 CDG, ADC_A1, land grid array, expansion interface II
PH6	DT1SEC/UART1_TX/ SPI1_SSEL1/CZM	Default: LED3 CZM, ADC_A2, land grid array, expansion interface II
PH7	DR1SEC/UART1_RX/TMR7/TACI2	Default: not used DR1SEC, land grid array, expansion interface II

Push Button and Switch Settings

This section describes operation of the push buttons and switches. The push button and switch locations are shown in Figure 2-2.

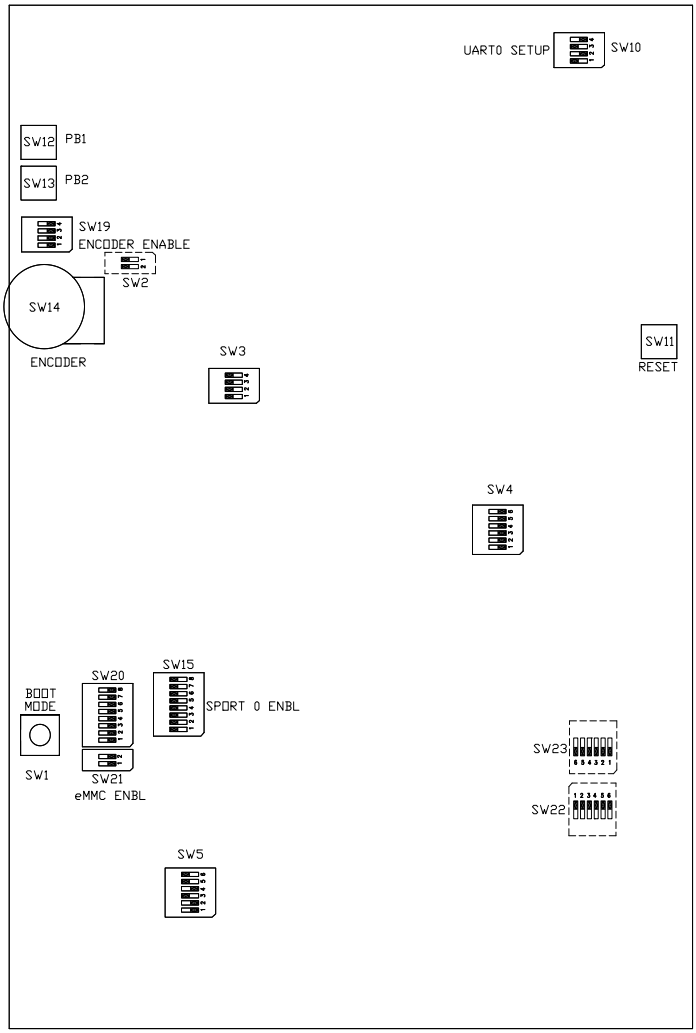

Figure 2-2. Push Button and Switch Locations

Boot Mode Select Switch (SW1)

The boot mode select switch (SW1) determines the boot mode of the processor. Table 2-4 shows the available boot mode settings. By default, the ADSP-BF518F processor boots from the on-board parallel flash memory.

The selected position of SW1 is marked by the notch down the entire rotating portion of the switch, not the small arrow.

Table 2-4. Boot Mode Select Switch (SW1)

SW1 Position	Processor Boot Mode
0	Idle – No Boot
1	**Boot from 8- or 16-bit external flash memory (default)**
2	Boot from internal SPI memory
3	Boot from external SPI memory (EEPROM or flash)
4	Boot from SPI0 host
5	Boot from OTP memory
6	Boot from SDRAM
7	Boot from UART0 host

PB Enable Switch (SW2)

The PB enable switch (SW2) disconnects the associated push buttons from the GPIO pins of the processor and allows the signals to be used for other purposes (see Table 2-5).

Table 2-5. Push Button Enable Switch (SW2)

SW2 Position (Default)	From	To	Function
1 (ON)	Push button 1 (SW12)	Processor (U12, PH0)	ON (PB1) OFF (ADC DR1PRI, eMMC, expansion interface II)
2 (ON)	Push button 2 (SW13)	Processor (U12, PH1)	ON (PB2) OFF (ADC RFS1, eMMC, expansion interface II)

Flash Enable Switch (SW3)

The flash enable switch (SW3) disconnects the $\overline{\text{AMSx}}$ signals from parallel flash memory (U5) and allows other devices to utilize the signals via the expansion interface II. For each switch listed in Table 2-6 that is turned OFF, the size of available flash memory is reduced by 1 MB. $\overline{\text{AMS3}}$ is shared with $\overline{\text{SPIO_SEL2}}$ of the external SPI flash. When using the external SPI flash, the available size for parallel flash is 3 MB.

Table 2-6. Flash Enable Switch (SW3)

SW3 Switch Position (Default)	Processor Signal
1 (ON)	$\overline{\text{AMS0}}$
2 (ON)	$\overline{\text{AMS1}}$
3 (ON)	$\overline{\text{AMS2}}$
4 (ON)	$\overline{\text{AMS3}}$

SPORT1 Enable Switch (SW4)

The SPORT1 enable switch (SW4) connects the SPORT1 interface of the processor to the ADC7266 (U2) device. SW4 position 5 is used to set the input range of the ADC to either 2.5V (ON) or 5V (OFF). SW4 position 6 is used to configure the inputs for single-ended mode (OFF) or differential mode (ON). When the SPORT1 interface is used on the expansion interface II, set SW4 to all OFF. SW4 is set to all OFF by default.

The SPORT1 interface is shared with other on-board components, such as the eMMC device and push buttons.

MIC Gain/Loopback Switch (SW5)

The microphone gain switch (SW5) sets the gain of the MIC signal, which is connected to the top 3.5 mm jack (J5). The gain can be set to 14 dB, 0 dB, or –6 dB by turning position 1, 2, or 3 of SW5 ON (see Table 2-7). When the corresponding position for the desired gain is ON, the remaining positions must be OFF. SW5 position 4 is used to connect the MICIN signal to the right headphone output for loopback testing during a POST. SW5 positions 5 and 6 are used to connect line-out to line-in for loopback testing in a POST, when no cables are connected to J4 and J5. Refer to "Audio Interface" on page 1-21 for more information about the audio codec.

Table 2-7. MIC Gain Switch (SW5)

Gain	SW5 Switch Settings
5 (14 dB)	ON, OFF, OFF, OFF
1 (0 dB)	OFF, ON, OFF, OFF
0.5 (–6 dB)	**OFF, OFF, ON, OFF (default)**
Unused	OFF, OFF, OFF, OFF

UART Setup Switch (SW10)

The UART setup switch (SW10) configures the UART0 signals from the GPIO pins of the processor. Position 4 is used to place the UART0 port of the processor in a loopback condition. The jumper connects the UART0_TX line of the processor to the UART0_RX signal of the processor. This is required when a POST program is run to test the serial port interface. By default, SW10 is ON, OFF, ON, OFF.

Reset Push Button (SW11)

The reset push button (SW11) resets the following ICs.

- Processor (U12), parallel flash (U5), and Ethernet IC (U4)

The reset push button does not reset the following ICs.

- SDRAM (U14), eMMC (U16)
- Audio codec (U1), UART0 (U21), schmitt trigger hex inverter (U6)
- Digipot (U7), power (VR1–5)

The reset push button does not reset the standalone debug agent once the debug agent is connected to a personal computer (PC). After communication between the debug agent and PC is initialized, pushing a reset button does not reset the USB chip on the debug agent. The only way to reset the USB chip on the debug agent is to power down the EZ-Board.

Programmable Flag Push Buttons (SW12–13)

Two momentary push buttons (SW12 and SW13) are provided for general-purpose user input. The buttons connect to the PH0 and PH1 GPIO pins of the processor. The push buttons are active high and, when pressed, send a high (1) to the processor. The GPIO enable switch (SW2) disconnects the push buttons from the corresponding push button signals. Refer to "PB Enable Switch (SW2)" on page 2-9 for more information.

Rotary Encoder with Momentary Switch (SW14)

The rotary encoder (SW14) can be turned clockwise for an up count or counter-clockwise for a down count. The encoder also features a momentary switch, activated by pushing the switch towards the processor, which resets the counter to zero. The rotary encoder is a two-bit quadrature (gray code) encoder. Refer to the Rotary Counter section of the *ADSP-BF51x Blackfin Processor Hardware Reference* for more information.

The rotary encoder is disconnected from the processor by setting SW19 positions 1, 2, and 3 to OFF. See "Encoder Enable Switch (SW19)" on page 2-13 for more information.

SPORT0 ENBL Switch (SW15)

The SPORT0 enable switch (SW15) connects the SPORT0 interface of the processor to the audio codec, SSM2603 (U1). SW15 positions 7 and 8 are used to disconnect the TWI bus from the codec. When the SPORT0 interface is used on the expansion interface II, set SW15 all OFF. By default, SW15 is set to all ON.

Encoder Enable Switch (SW19)

The encoder enable switch (SW19) disconnects the rotary encoder signals from the GPIO pins of the processor. SW19 position 4 is used to enable or disable the SD card detect signals: pin PF14 determines whether a card is inserted into the SD connector. When SW19 is OFF, its associated GPIO signals can be used on the expansion interface II (see Table 2-8).

Table 2-8. Encoder Enable Switch (SW19)

SW19 Position (Default)	From	To
1 (OFF)	Encoder (SW14)	Processor (U1, PH4)
2 (OFF)	Encoder (SW14)	Processor (U1, PH5)
3 (OFF)	Encoder (SW14)	Processor (U1, PH6)
4 (OFF)	SD connector (J13)	Processor (U1, PF13)

eMMC Enable Switch (SW20–21)

The eMMC enable switches (SW20 and SW21) connect the RSI signals to the on-board eMMC memory device. The eMMC and SD interfaces share the same signals; therefore, no card should be inserted into the SD connector when the eMMC device is used. The default for the switches is all OFF so that the SD connector can be used.

ADC Loopback Switches (SW22–23)

The ADC loopback switches (SW22 and SW23) are used for testing only. The switches are used to send an analog signal generated from the codec to the ADC circuit for evaluation.

Jumpers

This section describes functionality of the configuration jumpers. Figure 2-3 shows the jumper locations.

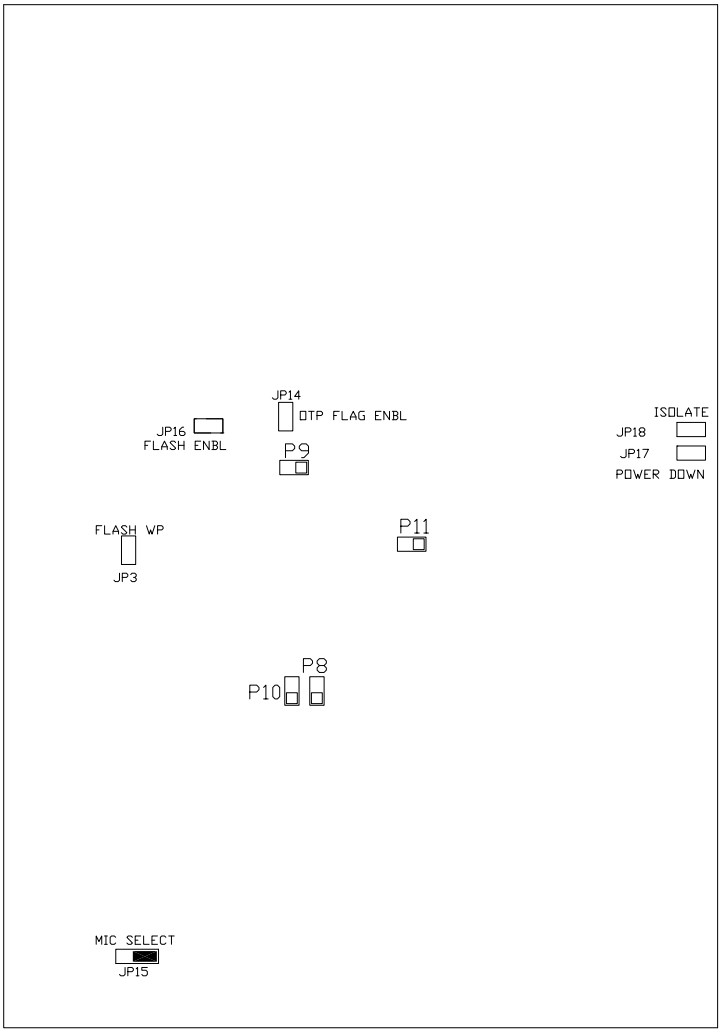

Figure 2-3. Configuration Jumper Locations

Flash WP Jumper (JP3)

The flash WP jumper (JP3) is used to write-protect block 70 of the parallel flash chip. Block 70 contains 64 KB of configuration data at address range 0x203 F0000–0x203 FFFFF. When the jumper is installed on JP3, and the parallel flash driver from Analog Devices is used, block 70 is read-only. By default, JP3 is installed.

OTP Flag Enable Jumper (JP14)

The OTP flag enable jumper (JP14) controls the precise 7V OTP voltage regulator. By default, JP14 is not installed; when installed, the jumper allows OTP writes.

JP14 must be installed for OTP writes to be successful. The nominal 2.5V for OTP is temporarily raised to 7V when PH3 is set high. Care must be taken when using the OTP_FLAG signal in order to avoid driving 7V for an extended amount of time.

There is a limited amount of time 7V can be applied to the processor's OTP interface. Violating the specifications listed in the *ADSP-BF512/ADSP-BF514/ADSP-BF516/ADSP-BF518(F) Blackfin Embedded Processor* data sheet can damage the processor.

Configured properly, JP14 connects the processor's PH3 flag pin to the shut-down pin of the ADP1611 switching converter. Refer to the *ADSP-BF51x Blackfin Processor Hardware Reference Manual* and the *ADSP-BF512/ADSP-BF514/ADSP-BF516/ADSP-BF518(F) Blackfin Embedded Processor* data sheet for more information about OTP writes.

MIC Select Jumper (JP15)

The microphone select jumper (JP15) connects the MICBIAS signal to the MICIN signal (JP15 on positions 1&2) or connects the MICBIAS signal to the 3.5 mm connector J5 (JP15 on positions 2&3). By default, JP15 is installed on positions 2&3.

SPI FLASH CS Enable Jumper (JP16)

The SPI flash CS enable jumper (JP16) connects the SPI0_SSEL2 signal to the SPI flash memory. When installing JP16, position 3 of SW3 needs to be turned OFF since the SPI0_SSEL2 signal is shared with the $\overline{\text{AMS3}}$ signal connected to parallel flash. When using SPI flash, the available memory that is accessible on parallel flash is reduced from 4 MB to 3 MB. By default, JP16 is not installed, and SPI flash is not connected.

Ethernet Power Down Jumper (JP17)

The Ethernet power down jumper (JP17) is used to put the PHY device in power-down mode, where the entire chip is powered down.

Ethernet Isolate Jumper (JP18)

The Ethernet isolate jumper (JP18) is used to put the PHY device in isolate mode. When in isolate mode, the PHY port is isolated from the media independent interface (MII) of the ADSP-BF518F processor.

VDDINT Power Jumper (P8)

The VDDINT power jumper (P8) is used to measure voltage and current supplied to the processor core. By default, P8 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper on P8 and measure voltage across the 0.1 ohm resistor. Once voltage is

measured, power can be calculated. For more information, refer to "Power Measurements" on page 1-27.

VDDEXT Power Jumper (P9)

The VDDEXT power jumper (P9) is used to measure the processor's I/O voltage and current. By default, P9 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper on P9 and measure voltage across the 0.1 ohm resistor. Once voltage is measured, power can be calculated. For more information, refer to "Power Measurements" on page 1-27.

VDDMEM Power Jumper (P10)

The VDDMEM power jumper (P10) is used to measure voltage and current supplied to the memory interface of the processor. By default, P10 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper on P10 and measure voltage across the 0.1 ohm resistor. Once voltage is measured, power can be calculated. For more information, refer to "Power Measurements" on page 1-27.

VDDFLASH Power Jumper (P11)

The VDDFLASH power jumper (P11) is used to measure flash voltage and current supplied to the processor core. By default, P11 is ON, and the power flows through the two-pin IDC header. To measure power, remove the jumper on P11 and measure voltage across the 0.1 ohm resistor. Once voltage is measured, power can be calculated. For more information, refer to "Power Measurements" on page 1-27.

LEDs

This section describes the on-board LEDs. Figure 2-4 shows the LED locations.

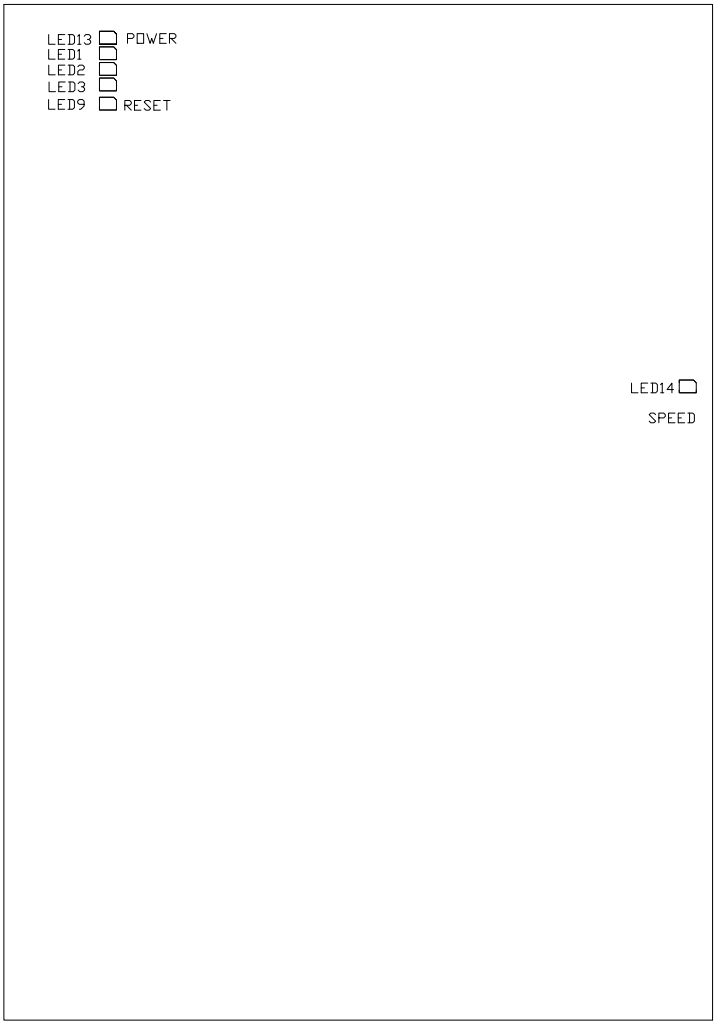

Figure 2-4. LED Locations

GPIO LEDs (LED1–3)

Three LEDs connect to three general-purpose I/O pins of the processor (see Table 2-9). The LEDs are active high and lit by writing a '1' to the correct programmable flag signal.

Table 2-9. GPIO LEDs

LED Reference Designator	Processor Programmable Flag Pin
LED1	PH3
LED2	PH5
LED3	PH6

Reset LED (LED9)

When LED9 is lit, it indicates that the master reset of all major ICs is active. The reset LED is controlled by the Analog Devices ADM708 supervisory reset circuit. You can assert the reset push button (SW11) to assert a master reset and activate LED9. For more information, see "Reset Push Button (SW11)" on page 2-11.

Power LED (LED13)

When LED13 is lit solid, it indicates that the board is powered.

Speed LED (LED14)

When LED14 is lit, the Ethernet PHY device operates at 100 Mbs. When the LED is OFF, the PHY device operates at 10 Mbs.

Connectors

This section describes connector functionality and provides information about mating connectors. See connector locations in Figure 2-5.

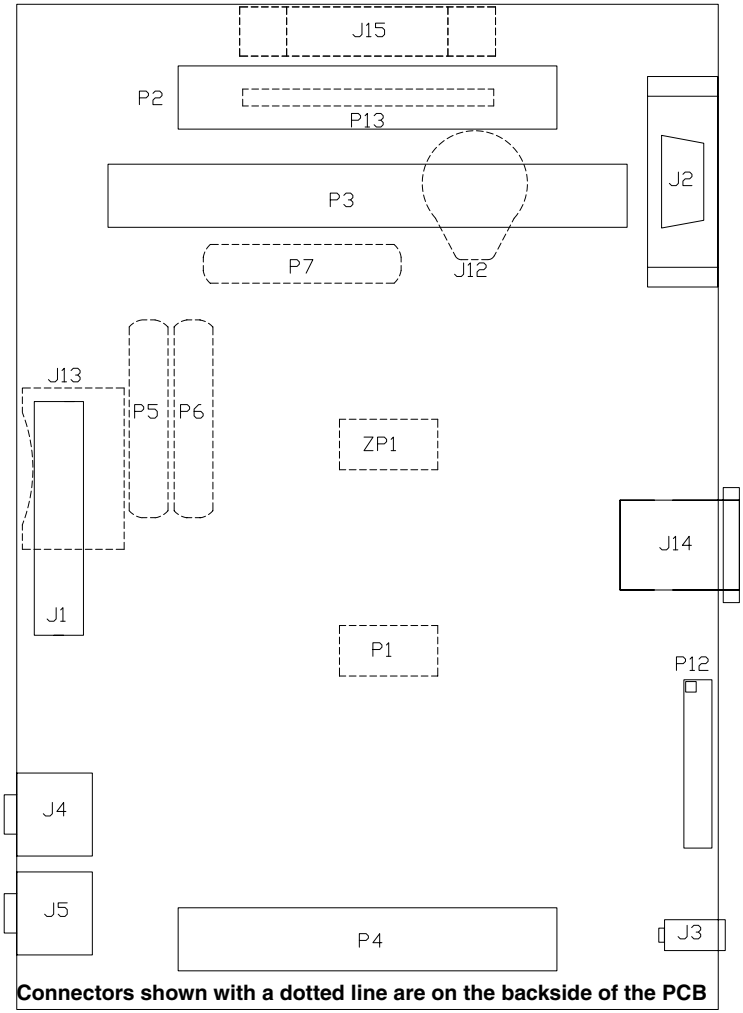

Figure 2-5. Connector Locations

Expansion Interface II Connector (J1)

J1 is a board-to-board connector providing signals from the external bus interface unit (EBIU) of the processor. The connector is located on the left edge of the board. For more information, see "Expansion Interface II" on page 1-26. For availability and pricing of the connector, contact Samtec.

Part Description	Manufacturer	Part Number
104-position 0.025", SMT header	SAMTEC	QMS-052-11-L-D-A
Mating Connector		
104-position 0.025", SMT socket	SAMTEC	QFS-052-01-L-D-A

RS-232 Connector (J2)

Part Description	Manufacturer	Part Number
DB9, female, vertical mount	NORCOMP	191-009-213-L-571
Mating Cable		
2m female-to-female cable	DIGI-KEY	AE1020-ND

Power Connector (J3)

The power connector (J3) provides all of the power necessary to operate the EZ-Board.

Part Description	Manufacturer	Part Number
0.65 mm power jack	CUI	045-0883R
Mating Power Supply (shipped with the EZ-Board)		
5.0VDC@2.5A power supply	CUI STACK	DMS050260-P12P-SZ

Dual Audio Connectors (J4–5)

Part Description	Manufacturer	Part Number
3.5 mm dual stereo jack	SWITCHCRAFT	35RAPC7JS
Mating Cable (shipped with the EZ-Board)		
3.5 mm male/male 6' cable	RANDOM	10A3-01106

Battery Holder (J12)

Part Description	Manufacturer	Part Number
16 mm battery holder	MEMORY PROTECTION	BH600
Mating Battery (shipped with the EZ-Board)		
3V 125MAH 16 mm LI-COIN	PANASONIC	CR1632

SD Connector (J13)

Part Description	Manufacturer	Part Number
SD 9-pin connector	ITT CANON	CCM05-5777LFT T50
Mating Memory Card (shipped with the EZ-Board)		
256 MB	SANDISK STACK	SDSDB-256-A10

Ethernet Connector (J14)

Part Description	Manufacturer	Part Number
RJ-45 Ethernet jack	STEWART	SS-6488-NF
Mating Cable (shipped with the EZ-Board)		
Cat 5E patch cable	RANDOM	PC10/100T-007

MII Connector (J15)

This connector is not populated on the board; it needs to be soldered on to be used. This connector allows for mating with Ethernet evaluation boards.

Part Description	Manufacturer	Part Number
40-position 0.50" TH receptacle	TE Connectivity	5787170-4F

JTAG Connector (P1)

The JTAG header is the connecting point for the JTAG interface to the ADSP-BF518F processor. The standalone debug agent requires both connectors `P1` and `ZP1`.

Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug.

When using an emulator with the EZ-Board, the standalone debug agent must be removed. Follow the installation instructions provided in "CCES Install and Session Startup" on page 1-5 or "VisualDSP++ Install and Session Startup" on page 1-9, using `P1` as the JTAG connection point.

Expansion Interface II Connectors (P2 and P4)

P2 and P4 are board-to-board connectors providing signals for the SPI, TWI, UART, SPORT interfaces and GPIO signals of the processor. The connectors are located on the upper and lower edges of the board. For more information, see "Expansion Interface II" on page 1-26. For availability and pricing of the connectors, contact Samtec.

Part Description	Manufacturer	Part Number
50-position 0.1", SMT header	SAMTEC	TSSH-125-01-L-DV-A
Mating Connector		
50-position 0.1", SMT socket	SAMTEC	SSW-125-22-F-D-VS

Expansion Interface II Connector (P3)

P3 is a board-to-board connector providing signals for the PPI, TWI, and GPIO signals of the processor. The connector is located on the upper edge of the board. For more information, see "Expansion Interface II" on page 1-26. For availability and pricing of the connector, contact Samtec.

Part Description	Manufacturer	Part Number
70-position 0.1", SMT header	SAMTEC	TSSH-135-01-L-DV-A
Mating Connector		
70-position 0.1", SMT socket	SAMTEC	SSW-135-22-F-D-VS

DMAX Land Grid Array Connectors (P5–7)

The land grid array areas (P5–7) are intended for the probing of the processor signals. The pads are exposed and designed to attach a Tektronix logic analyzer to the connectors listed in the following table. For more information about the land grid array, consult the Tektronix Web site.

Part Description	Manufacturer	Part Number
Primary retention	TEKTRONIX	020290800
Alternate retention	TEKTRONIX	020291000

Standalone Debug Agent Connector (ZP1)

ZP1 connects the standalone debug agent to the EZ-Board. The standalone debug agent requires both the ZP1 and P1 connectors. For more information, see "CCES Install and Session Startup" on page 1-5 or "VisualDSP++ Install and Session Startup" on page 1-9.

A ADSP-BF518F EZ-BOARD BILL OF MATERIALS

The bill of materials corresponds to "ADSP-BF518F EZ-Board Schematic" on page B-1.

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
1	1	74LVC14A SOIC14	U6	TI	74LVC14AD
2	1	IDT74FCT3244 APY SSOP20	U10	IDT	IDT74FCT3244APYG
3	1	32.768KHZ OSC008	U3	EPSON	MC-156 32.7680KA-A0:ROHS
4	1	25MHZ OSC003	U19	EPSON	SG-8002CA MP
5	4	SN74LVC1G08 SOT23-5	U23-U26	TI	SN74LVC1G08DBVR
6	1	MT48LC32M16 A2TG-75 TSOP54	U14	MICRON	MT48LC32M16A2P-75
7	1	SI4411DY SO-8	U8	VISHAY	Si4411DY-T1-E3
8	1	12MHZ OSC003	U20	EPSON	SG-8002CA-MP
9	1	SN74AUC1G00 SOT23-5	U13	TI	SN74AUC1G00DBVR

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
10	1	DP83848 LQFP48	U35	NATIONAL SEMI	DP83848CVV/NOPB
11	1	BF518 M25P16 “U9”	U9	NUMONYX	M25P16-VMW6G
12	1	BF518 M29W320EB "U5"	U5	NUMONYX	M29W320EB70ZE6E
13	1	MTFC8GKQDI	U16	MICRON	MTFC2GDKDM-WT
14	1	ADM708SARZ SOIC8	U22	ANALOG DEVICES	ADM708SARZ
15	1	ADM3202ARNZ SOIC16	U21	ANALOG DEVICES	ADM3202ARNZ
16	1	ADSP-BF518F LQFP176	U12	ANALOG DEVICES	ADSP-BF518BSWZ-4F4
17	1	ADP1864AUJZ SOT23-6	VR1	ANALOG DEVICES	ADP1864AUJZ-R7
18	1	ADP1611 MSOP8	VR6	ANALOG DEVICES	ADP1611ARMZ-R7
19	1	ADP1715 MSOP8	VR5	ANALOG DEVICES	ADP1715ARMZ-R7
20	1	ADP1710 TSOT5	VR3	ANALOG DEVICES	ADP1710AUJZ-R7
21	1	ADR550B SOT23-3	U11	ANALOG DEVICES	ADR550BRTZ-REEL7
22	1	AD5258 MSOP10	U7	ANALOG DEVICES	AD5258BRMZ10

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
23	1	ADP1715 MSOP8	VR4	ANALOG DEVICES	ADP1715ARMZ-1.8-R7
24	6	AD8022 MSOP8	U29-U34	ANALOG DEVICES	AD8022ARMZ
25	1	AD7266BCPZ LFCSP32	U2	ANALOG DEVICES	AD7266BCPZ
26	1	ADP1610 MSOP8	VR2	ANALOG DEVICES	ADP1610ARMZ-R7
27	1	SSM2603 ICS009	U1	ANALOG DEVICES	SSM2603CPZ-R2
28	2	DIP8 SWT016	SW15,SW20	C&K	TDA08H0SB1
29	4	DIP6 SWT017	SW4-SW5, SW22-SW23	CTS	218-6LPST
30	3	DIP4 SWT018	SW3,SW10, SW19	ITT	TDA04HOSB1
31	1	DB9 9PIN CON038	J2	NORCOMP	191-009-213-L-571
32	2	DIP2 SWT020	SW2,SW21	C&K	CKN9064-ND
33	8	IDC 2X1 IDC2X1	JP3,JP14, JP17-JP18, P8-P11	FCI	90726-402HLF
34	1	IDC 3X1 IDC3X1	JP15	FCI	90726-403HLF
35	1	IDC 12X2 IDC12X2	P12	SAMTEC	SSW-112-01-T-D

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
36	1	3A RESETABLE FUS004	F1	TYCO	SMD300F-2
37	10	IDC 2PIN_JUMPER_ SHORT	SJ1,SJ3-SJ11	DIGI-KEY	S9001-ND
38	1	PWR .65MM CON045	J3	DIG	CP1-023-ND
39	2	3.5MM DUAL_STEREO CON050	J4-J5	SWITCHCRAFT	35RAPC7JS
40	1	SD_CONN 9PIN CON051	J13	DIGI-KEY	401-1954-ND
41	3	MOMENTARY SWT024	SW11-SW13	PANASONIC	EVQ-Q2K03W
42	1	ROTARY_ENC_ EDGE SWT025	SW14	PANASONIC	EVQ-WKA001
43	1	QMS 52x2 QMS52x2_SMT	J1	SAMTEC	QMS-052-06.75-L-D-A
44	2	IDC 25x2 IDC25x2_SMTA	P2,P4	SAMTEC	TSSH-125-01-L-DV-A
45	1	IDC 35x2 IDC35x2_SMTA	P3	SAMTEC	TSSH-135-01-L-DV-A
46	1	IDC 7x2 IDC7x2_SMTA	P1	SAMTEC	TSM-107-01-T-DV-A
47	1	BATT_HOLDER 16MM BATT_COIN16 MM	J12	MEMORY PROTECTI	BH600

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
48	1	IDC 2X1 IDC2X1_SMT	JP16	SAMTEC	TSM-102-01-T-SV
49	1	ROTARY SWT027	SW1	COPAL	S-8110
50	1	RJ45 W/LEDS CON065	J14	PULSE ENG.	J0011D21BNL
51	1	IDC 18X2 IDC18X2_M_SMT	P13	SAMTEC	TSM-118-01-T-DV
52	3	YELLOW LED001	LED1-LED3	DIGI-KEY	P512TR-ND
53	2	100 1/10W 5% 0805	R165,R167	VISHAY	CRCW0805100RJNEA
54	8	600 100MHZ 200MA 0603	FER2-FER9	DIGI-KEY	490-1014-2-ND
55	2	600 100MHZ 500MA 1206	FER15-FER16	STEWARD	HZ1206B601R-10
56	2	10UF 16V 20% CAP002	CT1-CT2	PANASONIC	EEE1CA100SR
57	1	0 1/8W 5% 0805	R69	VISHAY	CRCW08050000Z0EA
58	1	190 100MHZ 5A FER002	FER17	MURATA	DLW5BSN191SQ2
59	2	0.47UF 16V 10% 0805	C59-C60	AVX	0805YC474KAT2A
60	2	1UF 10V 10% 0805	C123-C124	AVX	0805ZC105KAT2A

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
61	13	10UF 6.3V 10% 0805	C7,C10, C15-C16,C37, C41,C61,C64, C66,C71,C75, C88,C90	AVX	08056D106KAT2A
62	1	4.7UF 6.3V 10% 0805	C145	AVX	08056D475KAT2A
63	48	0.1UF 10V 10% 0402	C4-C6,C9, C11-C14,C25, C39,C42-C45, C47-C48, C62-C63,C65, C72,C76, C86-C87,C89, C115-C118, C140,C152, C188-C194, C211-C220, C222	AVX	0402ZD104KAT2A
64	52	0.01UF 16V 10% 0402	C1,C8,C17-C24, C26-C36,C38, C46,C49-C58, C73,C119-C122, C139,C154, C179-C187, C223-C225	AVX	0402YC103KAT2A
65	1	10K 1/16W 5% 0402	R246	VISHAY	CRCW040210K0FKED

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
66	42	10K 1/16W 5% 0402	R1,R11, R18-R21,R26, R59,R143-R145, R152, R154-R156, R161-R164, R168,R173, R203,R245, R268,R270, R356-R370, R382,R390	VISHAY	CRCW040210K0FKED
67	9	4.7K 1/16W 5% 0402	R6-R8,R13-R17, R269	VISHAY	CRCW04024K70JNED
68	27	0 1/16W 5% 0402	R9,R202, R205-R206, R209-R212, R214-R215, R217-R218, R221-R222, R224-R225, R227-R228, R230-R233, R235-R236, R238-R239,R267	PANASONIC	ERJ-2GE0R00X
69	10	22 1/10W 5% 0402	R146-R151, R241-R244	DIGI-KEY	P22JTR-ND
70	9	33 1/16W 5% 0402	R3,R12,R60, R66-R67,R199, R313-R314,R325	VISHAY	CRCW040233R0JNEA
71	2	18PF 50V 5% 0805	C2-C3	AVX	08055A180JAT2A
72	2	2.2UF 10V 10% 0805	C150-C151	AVX	0805ZD225KAT2A

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
73	3	1A SK12 DO-214AA	D16-D18	DIODES INC	B120B-13-F
74	24	10PF 50V 5% 0805	C155-C178	AVX	08055A100JAT2A
75	2	107.0 1/10W 1% 0805	R379-R380	DIGI-KEY	311-107CRTR-ND
76	2	0.1UF 16V 10% 0603	C40,C136	AVX	0603YC104KAT2A
77	5	1UF 16V 10% 0603	C79-C81,C199, C208	DIG01	399-5090-2-ND
78	3	1UF 16V 10% 0603	C133, C209-C210	DIG01	399-5090-2-ND
79	1	68PF 50V 5% 0603	C144	AVX	06035A680JAT2A
80	3	4.7UF 6.3V 20% 0603	C137-C138, C141	AVX	06036D475MAT2A
81	1	470PF 50V 5% 0603	C143	AVX	06033A471JAT2A
82	3	220UF 6.3V 20% D2E	CT3-CT4,CT6	SANYO	10TPE220ML
83	1	10M 1/10W 5% 0603	R10	VISHAY	CRCW060310M0FNEA
84	5	330 1/10W 5% 0603	R153,R157-R160	DIG01	541-330GTR-ND
85	4	0.0 1/10W 1% 0603	R52-R53,R195, R346	PHYCOMP	232270296001L

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
86	2	0.0 1/10W 1% 0603	R345,R351	PHYCOMP	232270296001L
87	18	49.9 1/16W 1% 0603	R68,R71-R77, R79-R84, R371-R374	VISHAY	CRCW060349R9FNEA
88	15	10 1/10W 5% 0603	R166,R169, R207-R208, R213,R216, R219-R220, R223,R226, R229,R234, R237,R240,R349	VISHAY	CRCW060310R0JNEA
89	1	10.0K 1/10W 1% 0603	R183	DIGI-KEY	311-10.0KHRTR-ND
90	8	100PF 50V 5% 0603	C67-C70, C82-C85	AVX	06035A101JAT2A
91	1	1000PF 50V 5% 0603	C207	PANASONIC	ECJ-1VC1H102J
92	8	2.21K 1/10W 1% 0603	R377-R378, R381,R383-R387	DIGI-KEY	311-2.21KHRTR-ND
93	1	2200PF 50V 5% 0603	C130	KEMET	C0603C222J5RACTU
94	2	100 1/16W 5% 0402	R49,R54	DIGI-KEY	311-100JRTR-ND
95	1	4.99K 1/16W 1% 0603	R347	VISHAY	CRCW06034K99FKEA
96	1	24.9K 1/10W 1% 0603	R192	DIGI-KEY	311-24.9KHTR-ND

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
97	3	511.0 1/16W 1% 0402	R140-R142	DIGI-KEY	311-511LCT-ND
98	1	10UF 10V 10% 0805	C142	PANASONIC	ECJ-2FB1A106K
99	1	10UF 10V 10% 0805	C221	PANASONIC	ECJ-2FB1A106K
100	1	2.0K 1/16W 1% 0603	R182	PANASONIC	ERJ-3EKF2001V
101	6	0.05 1/2W 1% 1206	R190-R191, R194,R196, R198,R204	SEI	CSF 1/2 0.05 1%R
102	11	10UF 16V 10% 1210	C125-C127, C135,C146, C149, C200-C203, C205	AVX	1210YD106KAT2A
103	2	GREEN LED001	LED13-LED14	PANASONIC	LN1361CTR
104	1	RED LED001	LED9	PANASONIC	LN1261CTR
105	2	1000PF 50V 5% 1206	C147-C148	AVX	12065A102JAT2A
106	1	255.0K 1/10W 1% 0603	R197	VISHAY	CRCW06032553FK
107	1	80.6K 1/10W 1% 0603	R193	VISHAY	CRCW060380K6FKEA
108	2	22000PF 25V 10% 0402	C131,C197	DIGI-KEY	490-3252-1-ND

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
109	2	5A MBRS540T3G SMC	D7-D8	ON SEMI	MBRS540T3G
110	1	20MA MA3X717E DIO005	D1	DIODES INC	BAS70-05-7-F
111	1	2.5UH 30% IND013	L3	COILCRAFT	MSS1038-252NL_
112	1	33.0K 1/16W 1% 0402	R201	ROHM	MCR01MZPF3302
113	5	47.0K 1/16W 1% 0402	R46,R48, R50-R51,R55	ROHM	MCR01MZPF4702
114	1	5.6K 1/16W 5% 0402	R247	PANASONIC	ERJ-2GEJ562X
115	1	1.0K 1/16W 1% 0402	R189	PANASONIC	ERJ-2RKF1001X
116	1	1.50K 1/16W 1% 0402	R355	PANASONIC	ERJ-2RKF1501X
117	3	220PF 50V 10% 0402	C153, C195-C196	DIGI-KEY	311-1035-2-ND
118	2	220PF 50V 10% 0402	C74,C91	DIGI-KEY	311-1035-2-ND
119	4	5.6K 1/16W 0.5% 0402	R40,R43-R45	SUSUMU	RR0510P-562-D
120	1	680 1/16W 1% 0402	R42	BC COMPONENTS	2312 275 16801

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
121	1	90.9K 1/16W 5% 0402	R41	DIGI-KEY	541-90.9KLCT-ND
122	1	40.2K 1/16W 5% 0402	R47	DIGI-KEY	541-40.2KLCT-ND
123	3	100K 1/16W 5% 0402	R200,R350,R391	DIGI-KEY	541-100KJTR-ND
124	4	2.2UF 25V 10% 0805	C129,C132, C204,C206	DIGI-KEY	445-6860-2-ND
125	1	21.5K 1/10W 1% 0603	R179	DIGI-KEY	311-21.5KHRCT-ND
126	1	21.5K 1/10W 1% 0603	R352	DIGI-KEY	311-21.5KHRCT-ND
127	6	1A MBR130LSFT1G SOD-123FL	D2-D5,D9-D10	ON SEMI	MBR130LSFT1G
128	1	22UH 20% IND018	L1	COILCRAFT	MSS4020-223MLB
129	3	1UH 20% IND019	L2,L6-L7	COILCRAFT	ME3220-102MLB
130	13	33 1/32W 5% RNS005	RN4-RN13, RN17-RN19	PANASONIC	EXB-28V330JX
131	3	1.2K 1/16W 1% 0402	R4-R5,R186	VISHAY	CRCW04021K20FKED
132	2	4.3 1/4W 5% 1206	R185,R188	PANASONIC	ERJ-8GEYJ4R3V

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
133	1	2.67K 1/16W 1% 0402	R187	PANASONIC	ERJ-2RKF2671X
134	3	1.0M 1/16W 1% 0402	R248-R250	VISHAY	CRCW04021M00FKED
135	2	22UH 20% IND024	L8-L9	COILCRAFT	MSD7342-223MLC
136	4	330 100MHZ 1.5A 0805	FER1, FER19-FER21	MURATA	BLM21PG331SN1D
137	8	22 1/32W 5% RNS005	RN1-RN3, RN14-RN16, RN20-RN21	PANASONIC	EXB-28V220JX
138	1	3300PF 50V 5% 0603	C198	PANASONIC	ECJ-1VB1H332K
139	1	24.0K 1/10W 1% 0603	R176	PANASONIC	ERJ-3EKF2402V
140	1	140.0K 1/10W 1% 0603	R181	PANASONIC	ERJ-3EKF1403V
141	1	44.2K 1/10W 1% 0603	R348	PANASONIC	ERJ-3EKF4422V
142	1	1.91K 1/10W .1% 0603	R180	SUSUMU	RG1608P-1911-B-T5
143	1	3.01K 1/10W .1% 0603	R184	SUSUMU	RG1608P-3011-B-T1
144	1	20.0K 1/16W 1% 0402	R344	VISHAY	CRCW040220K0FKED

Ref.	Qty	Description	Reference Designator	Manufacturer	Part Number
145	1	30A GSOT05 SOT23-3	D14	VISHAY	GSOT05-GS08
146	1	30A GSOT03 SOT23-3	D15	VISHAY	GSOT03-GS08
147	2	40A ESD5Z2.5T1 SOD-523	D11-D12	ON SEMI	ESD5Z2.5T1G
148	1	7A VESD01-02V-GS 08 SOD-523	D13	VISHAY	VESD01-02V-GS08
149	2	165.0 1/10W 1% 0603	R375-R376	DIGI-KEY	P165HTR-ND
150	1	220.0 1/10W 1% 0603	R389	DIGI-KEY	P220HTR-ND
151	1	4.87K 1/10W 1% 0402	R388	DIGI-KEY	541-4.87KHCT-ND

ADSP-BF518F EZ-BOARD SCHEMATIC

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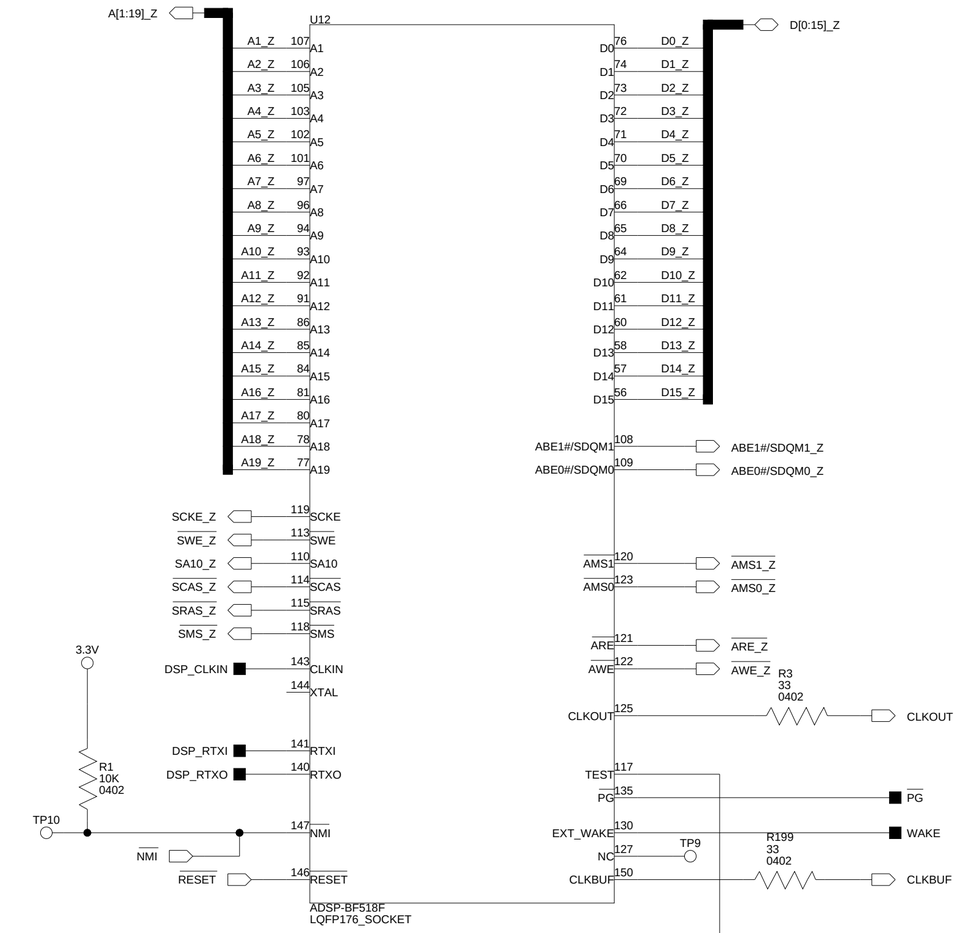
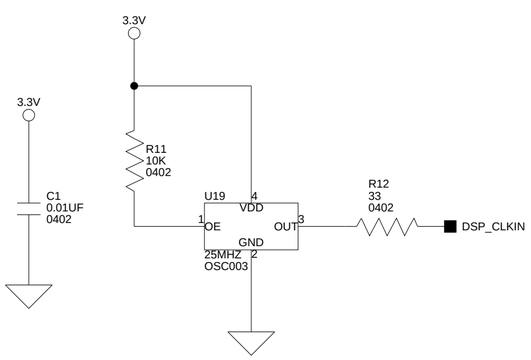
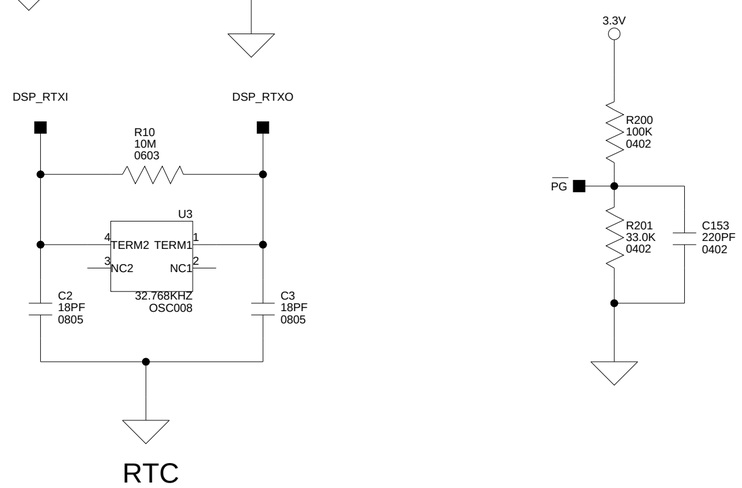
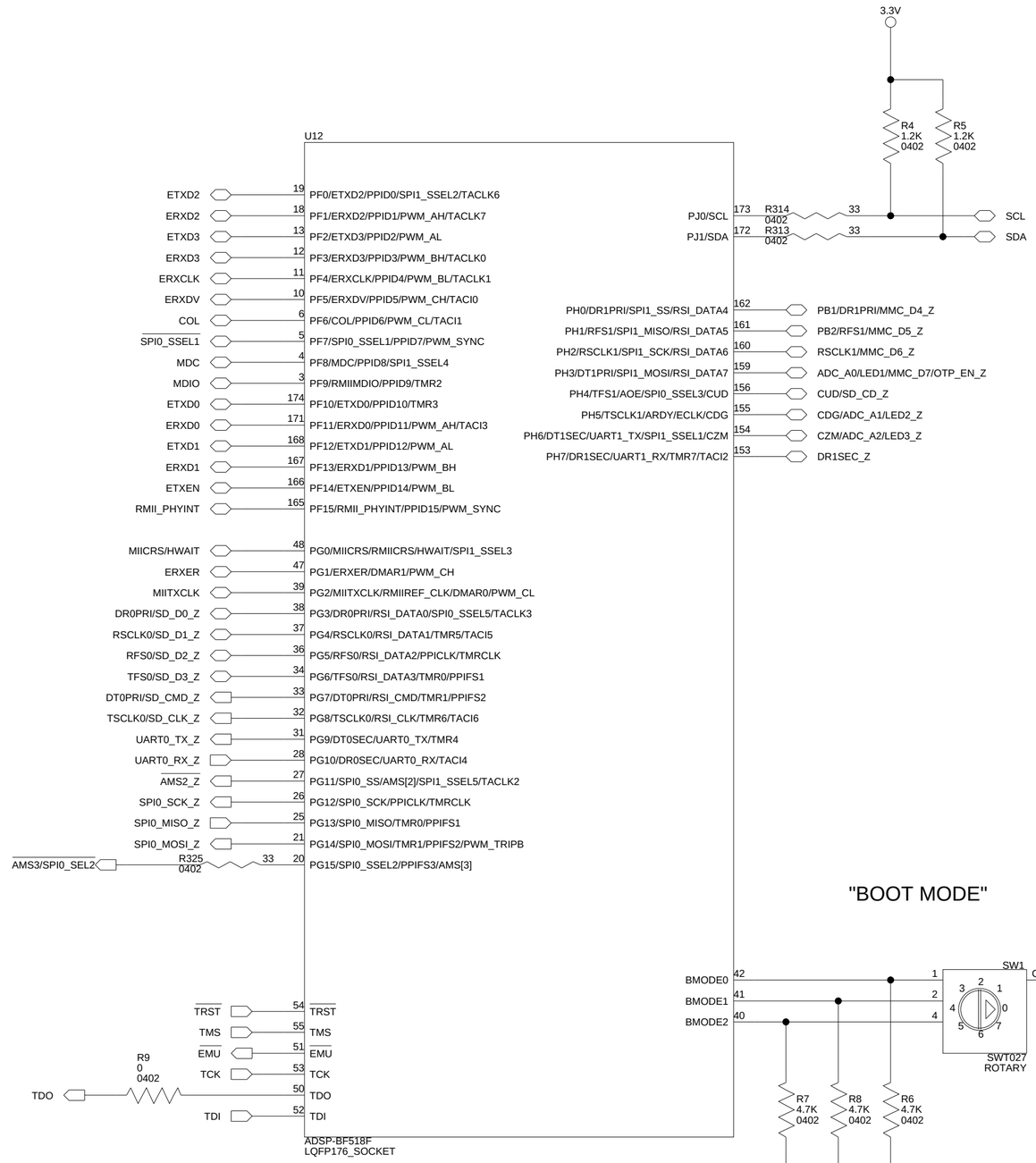
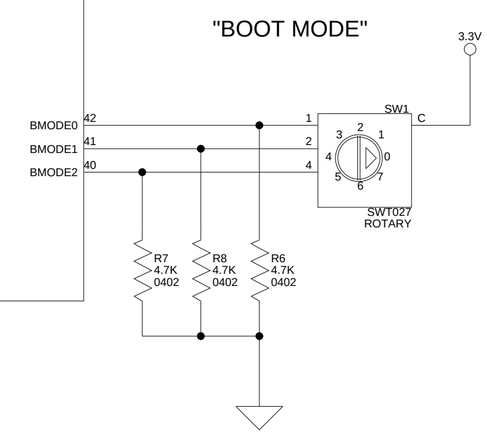
Title	ADSP-BF518F EZ-BOARD TITLE		
Size C	Board No. A0217-2008		Rev 1.0
Date	5-11-2009_10:44	Sheet 1 of 16	











SW1: Boot Mode Select Switch

	POSITION	BOOT MODE
Default	0	Idle-No Boot
	1	Boot from 8 or 16-bit external flash memory
	2	Boot from internal SPI memory
	3	Boot from external SPI memory
	4	Boot from SPI0 host
	5	Boot from OTP memory
	6	Boot from SDRAM
	7	Boot from UART0 host

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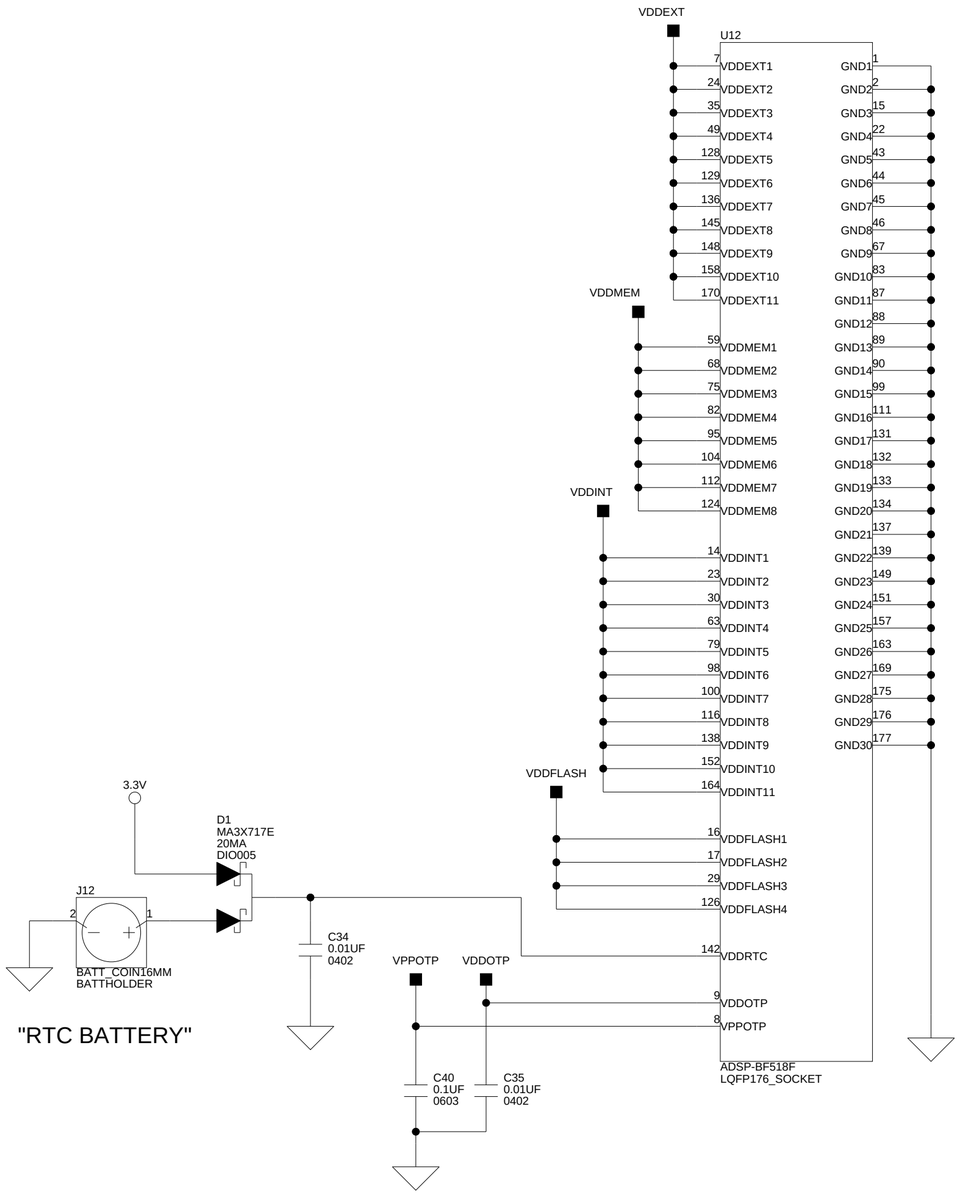
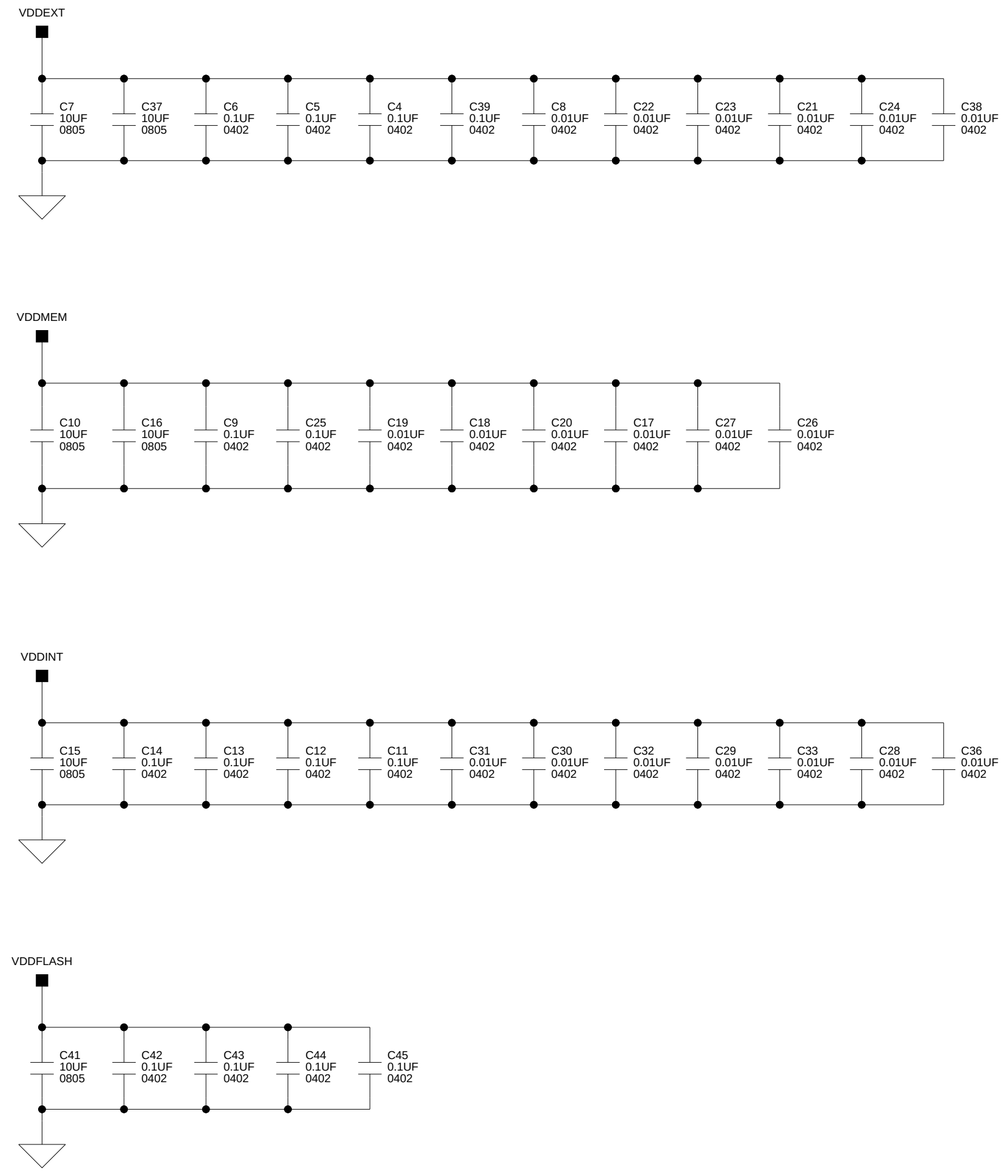
Title	ADSP-BF518F EZ-BOARD DSP EBIU + CONTROL		
Size C	Board No. A0217-2008		Rev 1.0
Date 5-11-2009_10:44		Sheet 2 of 16	





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Title	ADSP-BF518F EZ-BOARD DSP POWER, BYPASS CAPS		
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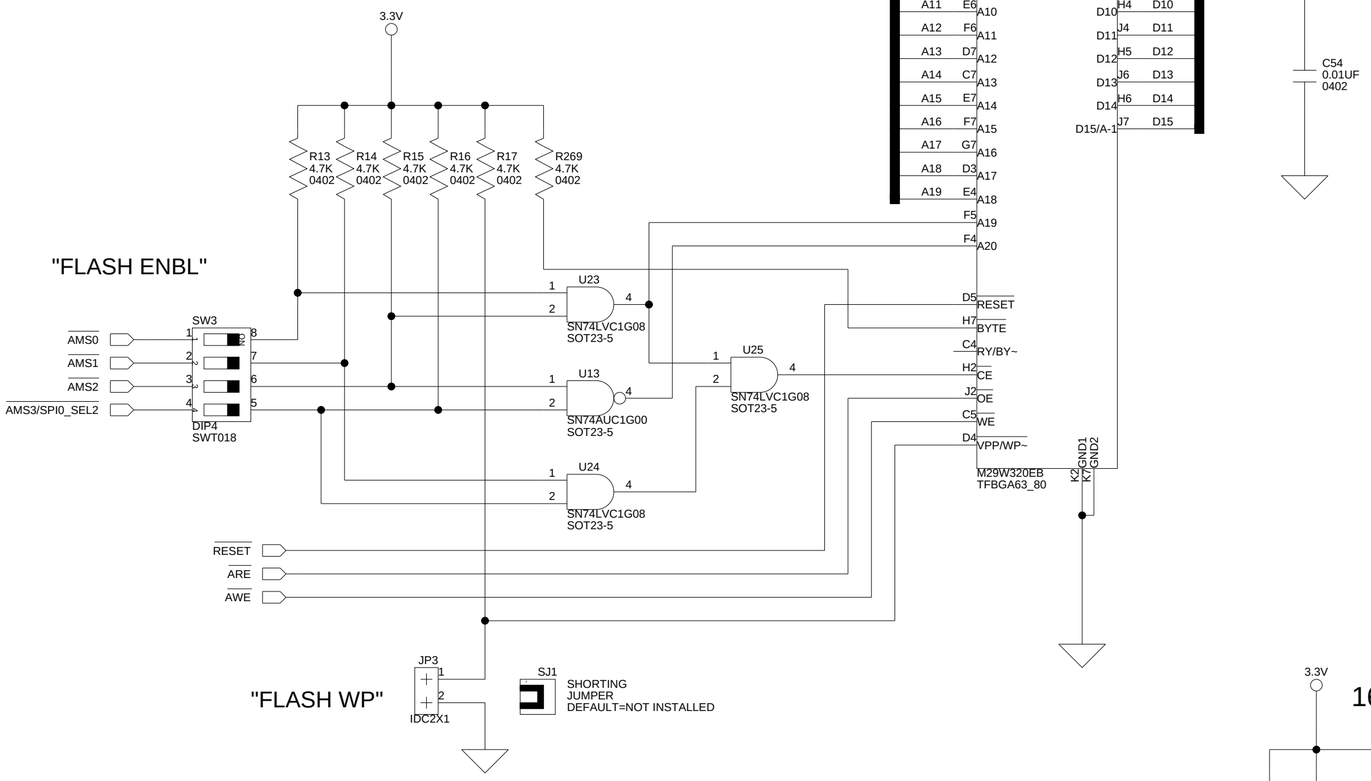
4 MB FLASH

(2M x 16)

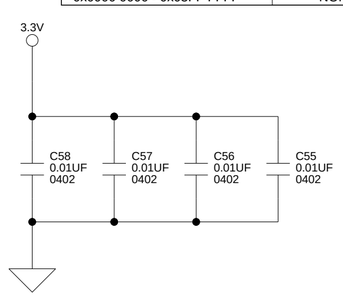
SW3: FLASH ENABLE

POS.	FROM	TO	DEFAULT	ALTERNATE FUNCTION / OFF MODE
1	DSP (U12)	FLASH (U5)	ON	Expansion Interface
2	DSP (U12)	FLASH (U5)	ON	Expansion Interface
3	DSP (U12)	FLASH (U5)	ON	Expansion Interface
4	DSP (U12)	FLASH (U5)	ON	Expansion Interface, SPI FLASH CS

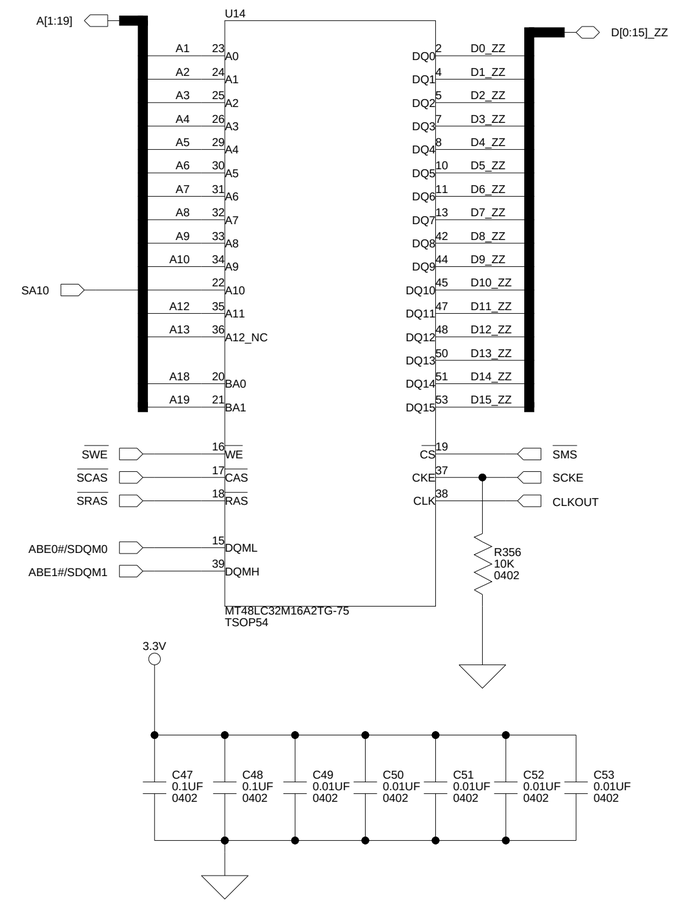


MEMORY MAP

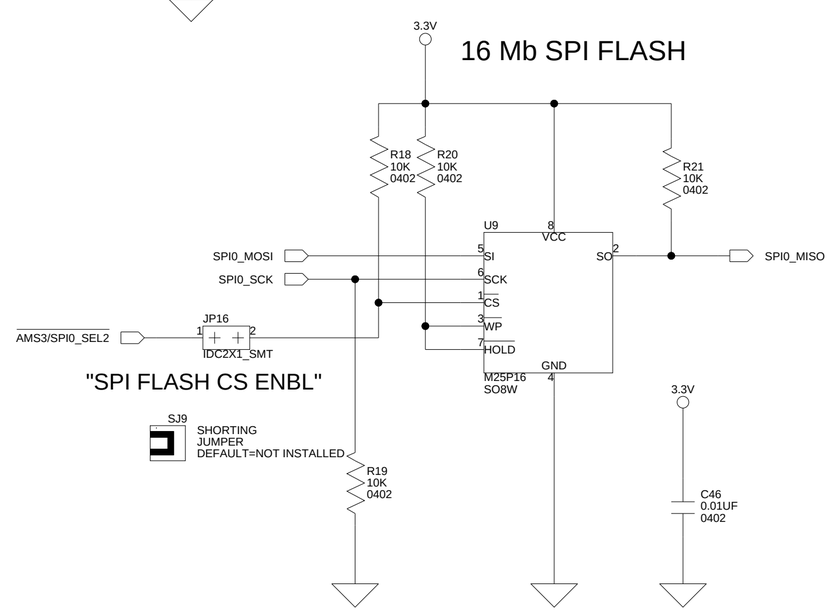
ADDRESS RANGE	SELECT LINE	TYPE
0x2030 0000 - 0x203F FFFF	ASYNC BANK 3	FLASH
0x2020 0000 - 0x202F FFFF	ASYNC BANK 2	FLASH
0x2010 0000 - 0x201F FFFF	ASYNC BANK 1	FLASH
0x2000 0000 - 0x200F FFFF	ASYNC BANK 0	FLASH
0x0000 0000 - 0x03FF FFFF	NONE	SDRAM



64MB SDRAM (32M x 16)



16 Mb SPI FLASH



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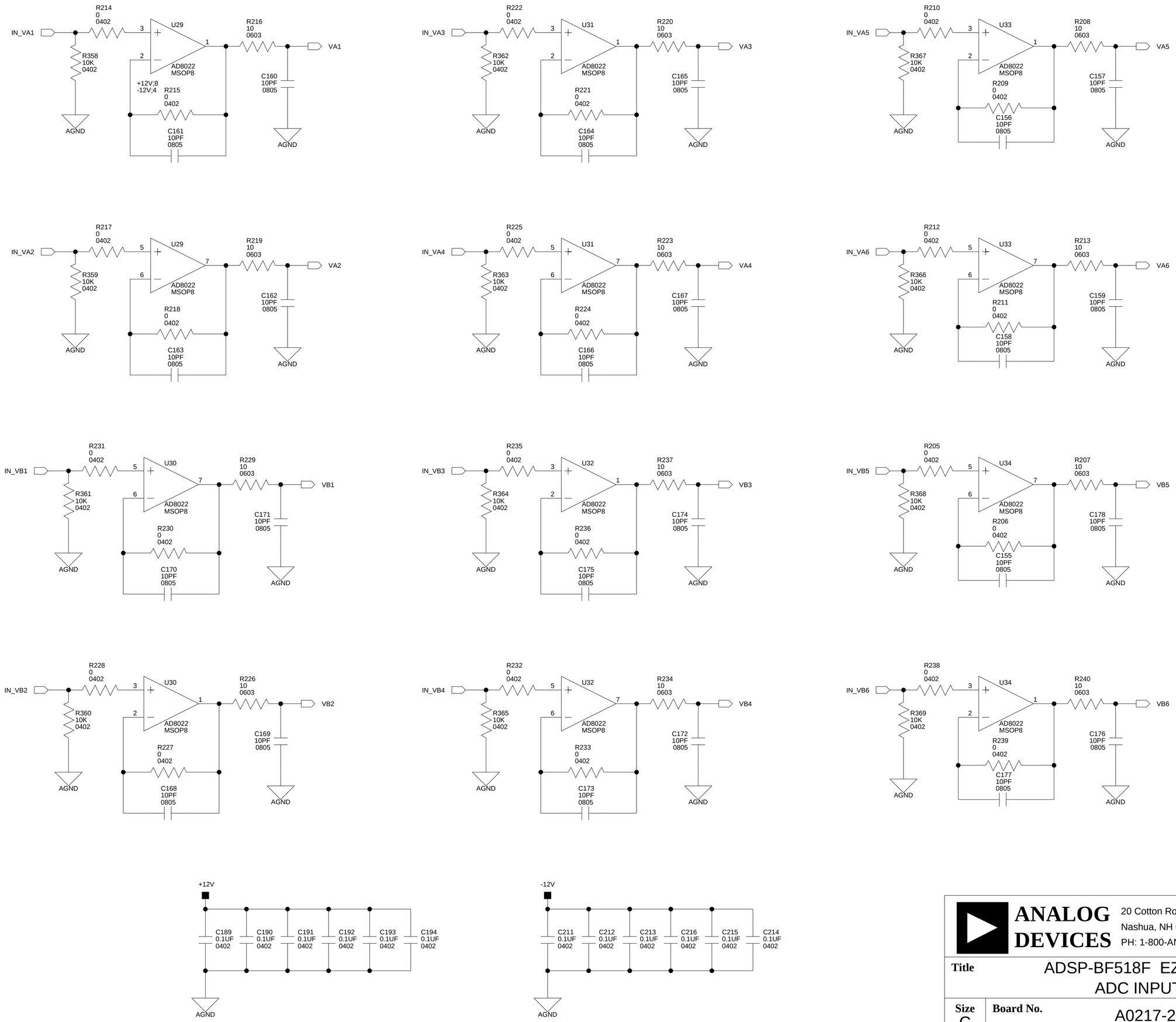
Title	ADSP-BF518F EZ-BOARD EXTERNAL MEMORY		
Size C	Board No. A0217-2008		Rev 1.0
Date 5-11-2009_10:44		Sheet 4 of 16	



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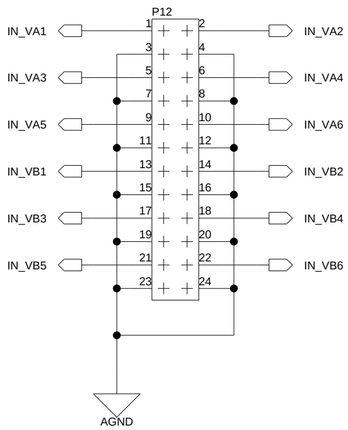
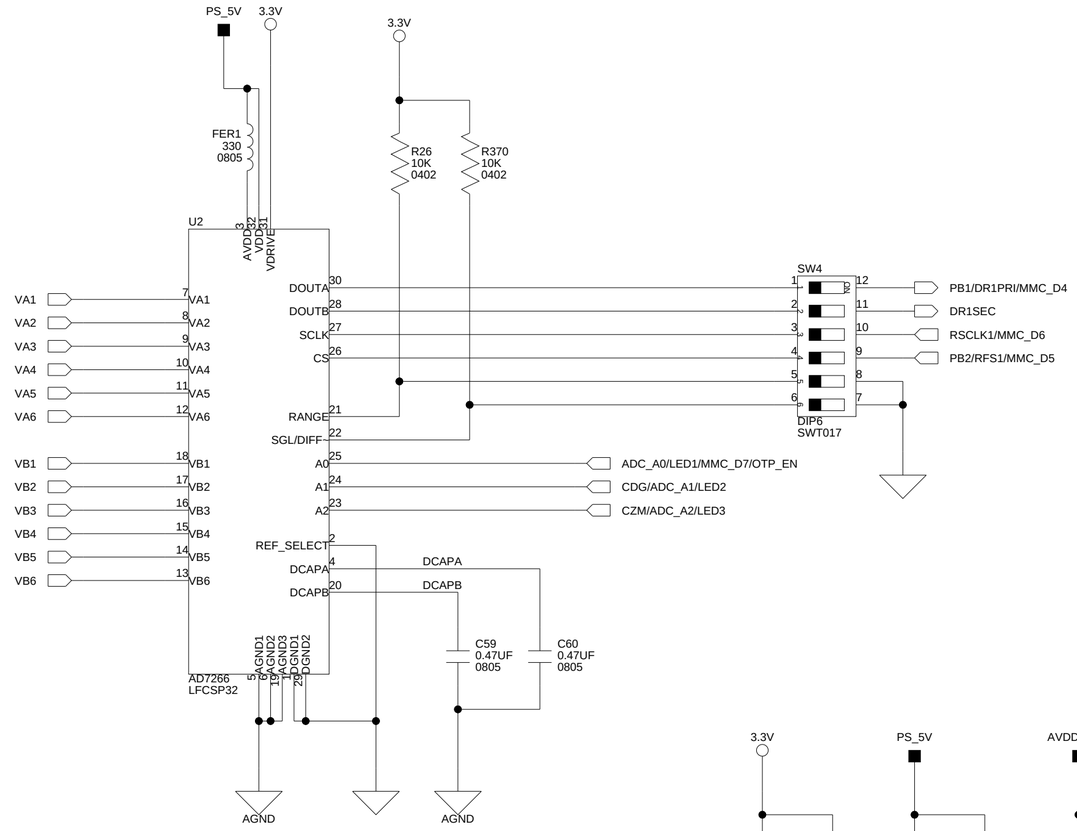
Title	ADSP-BF518F EZ-BOARD ADC INPUTS		
Size C	Board No. A0217-2008		Rev 1.0
Date 5-11-2009_10:44		Sheet 5 of 16	

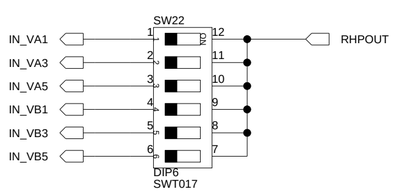
"ADC INPUTS"

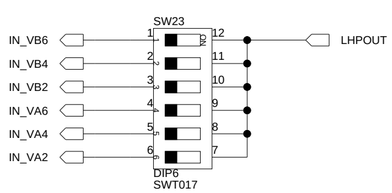




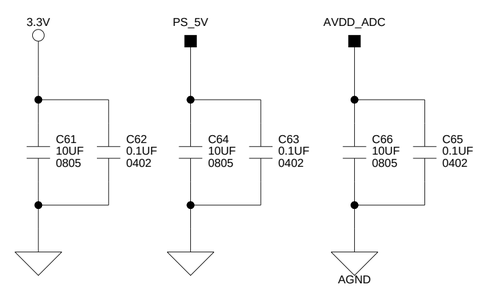
SW4 disconnects DSP from ADC

"SPORT1 ENBL"

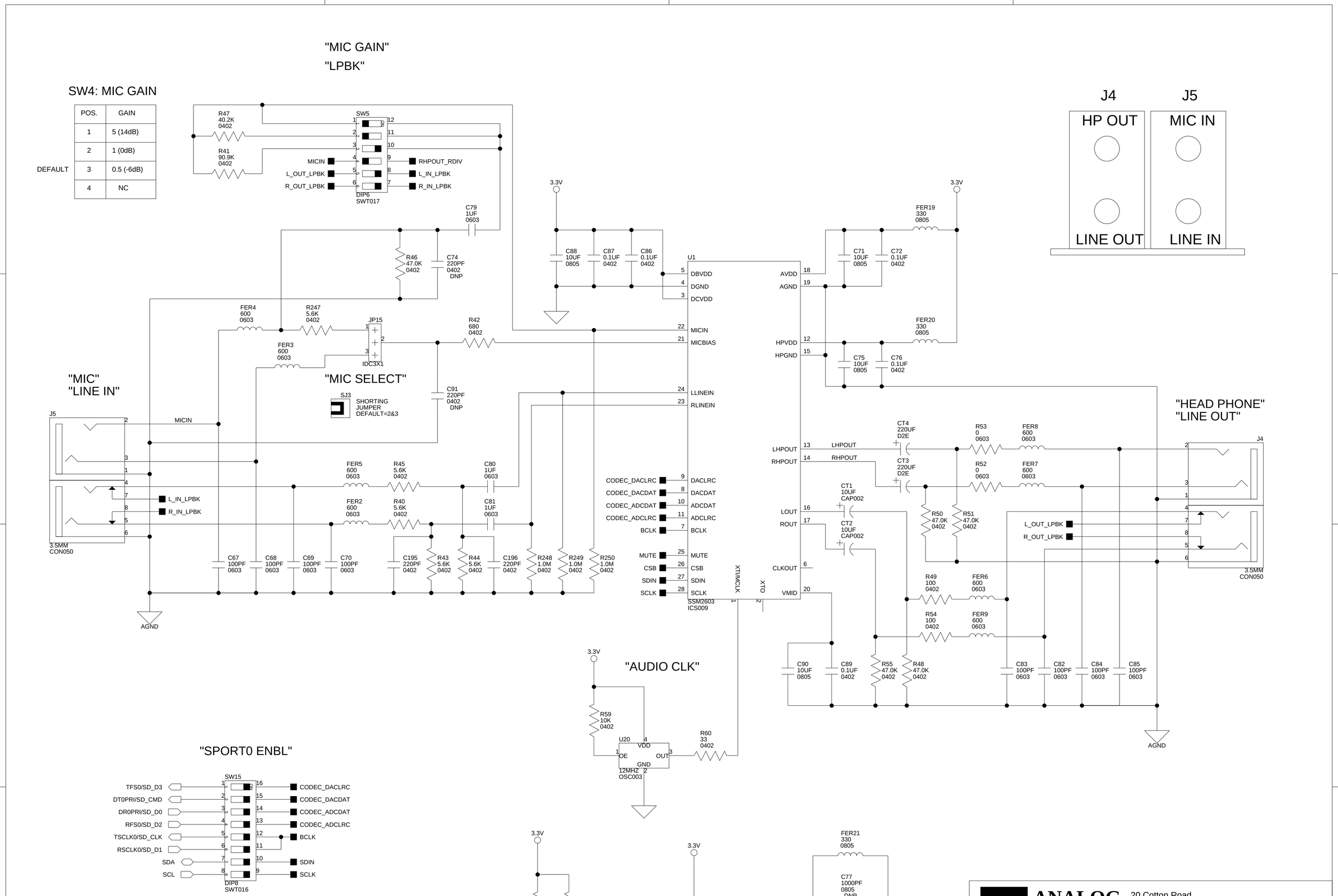




SW22 & 23 are only used for POST



ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD		
Title	ADSP-BF518F EZ-BOARD ADC		
Size C	Board No. A0217-2008		Rev 1.0
Date	5-11-2009_10:44	Sheet 6 of 15	



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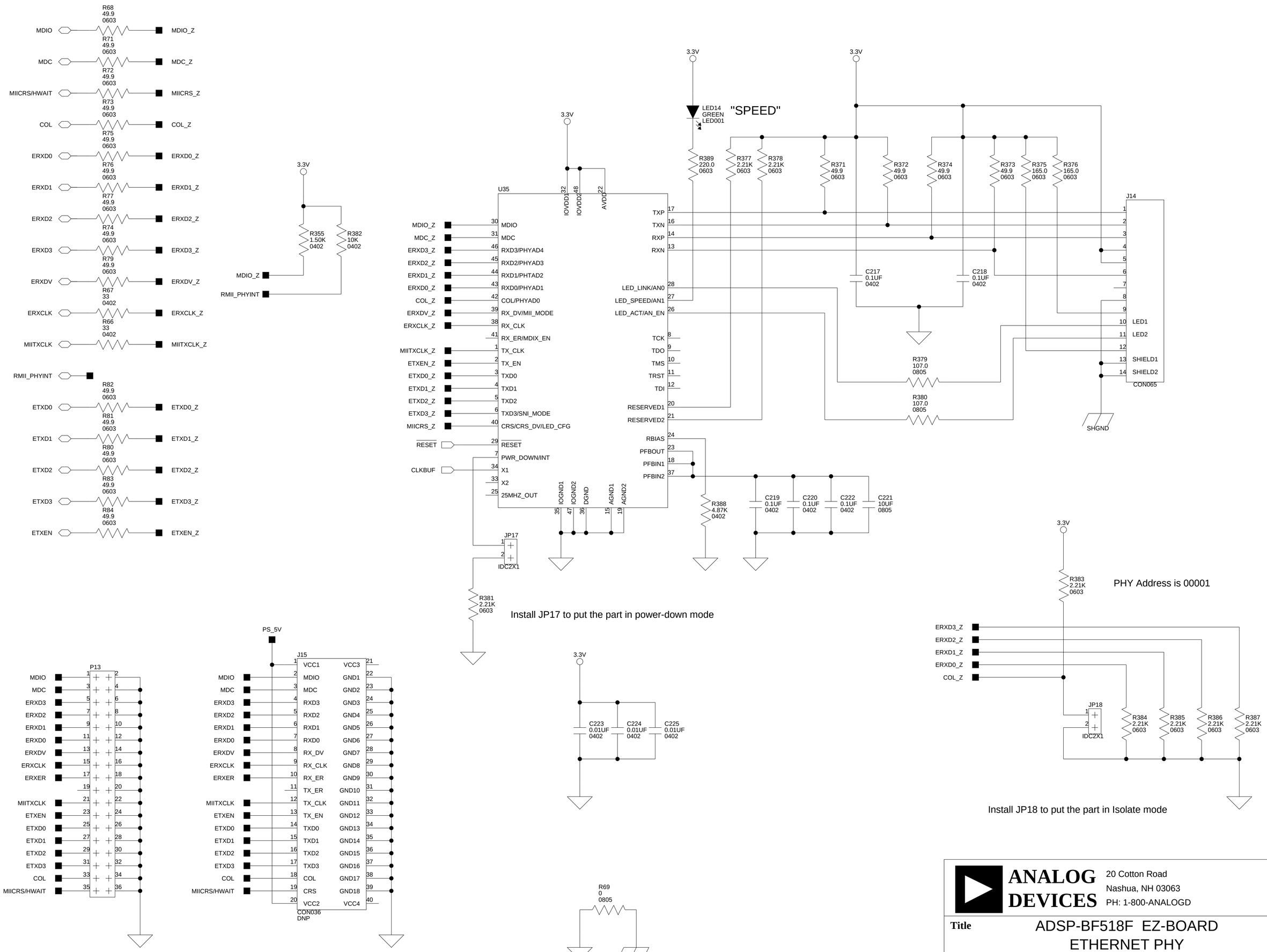
Title	ADSP-BF518F EZ-BOARD AUDIO CODEC		
Size C	Board No. A0217-2008		Rev 1.0
Date 5-11-2009_10:44		Sheet 7 of 16	



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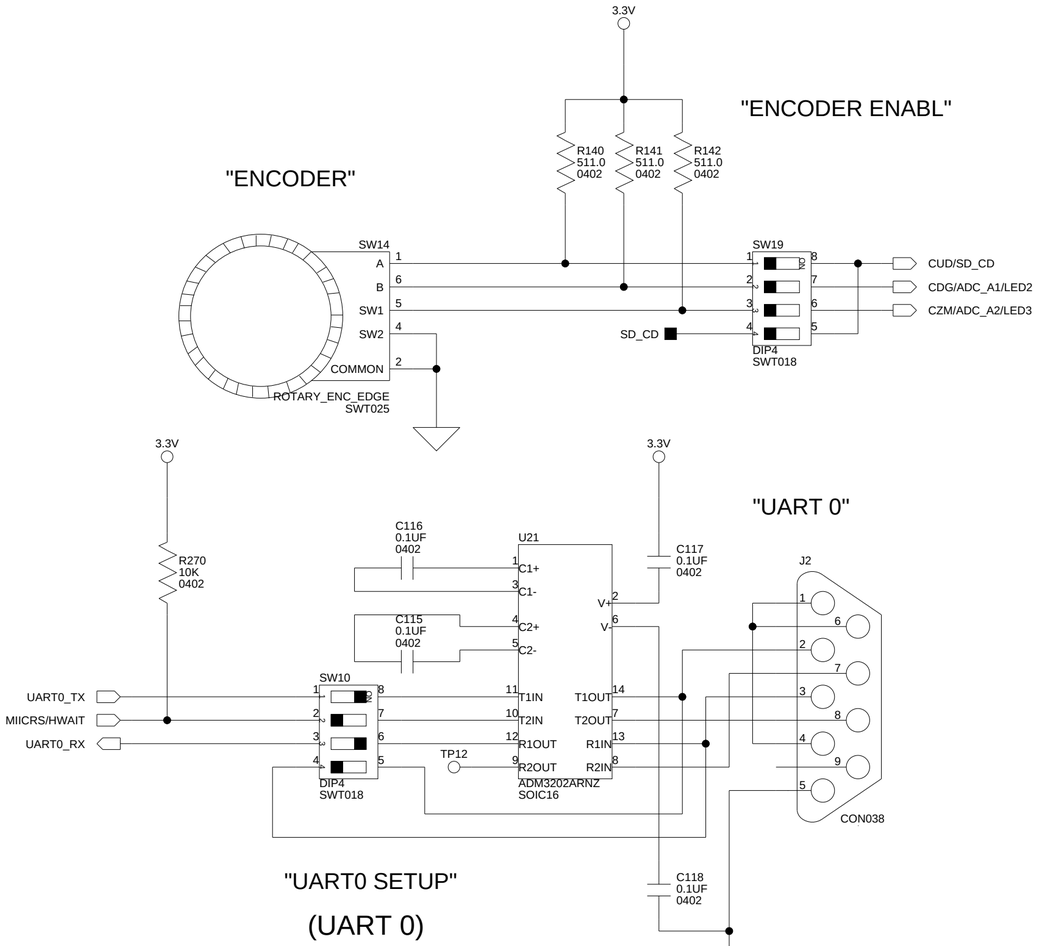
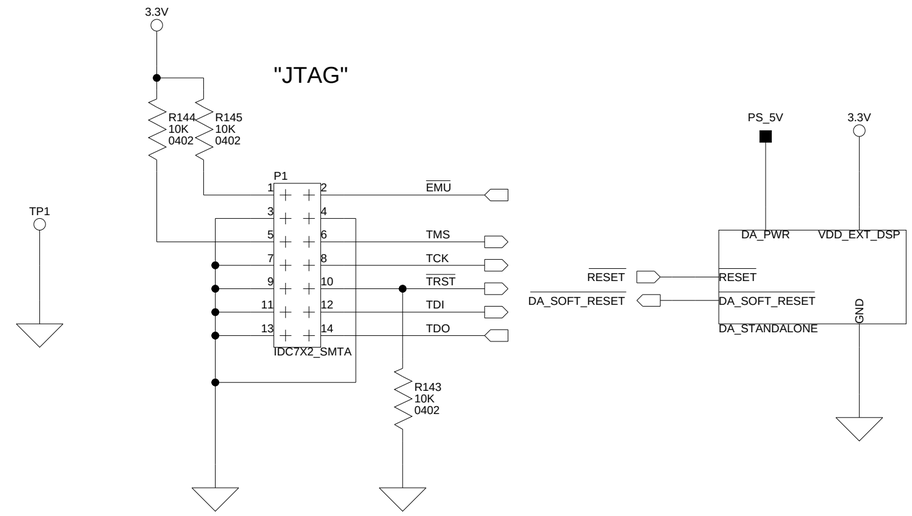
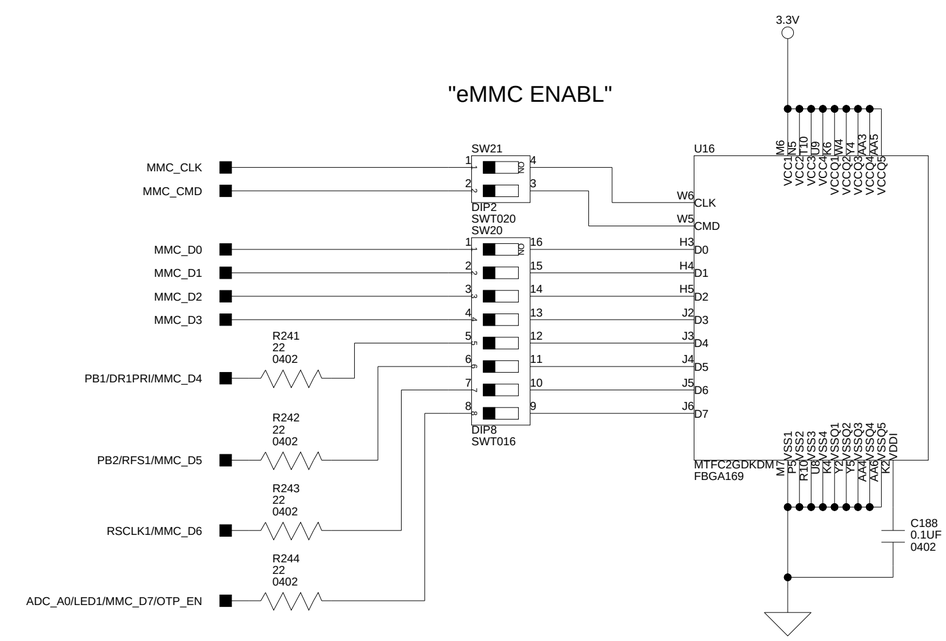
Title	ADSP-BF518F EZ-BOARD ETHERNET PHY		
Size C	Board No. A0217-2008		Rev 1.0
Date 5-13-2009_15:06		Sheet 8 of 15	

All USB interface circuitry is considered proprietary and has been omitted from this schematic.

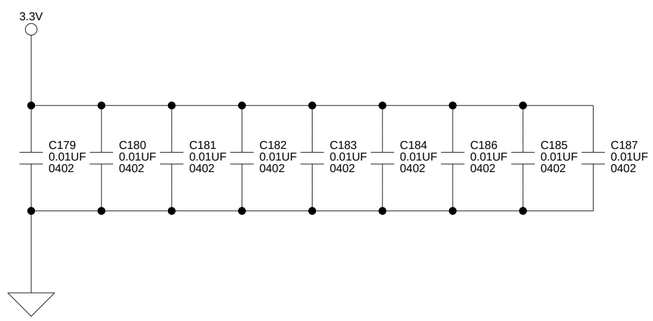
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at http://www.analog.com

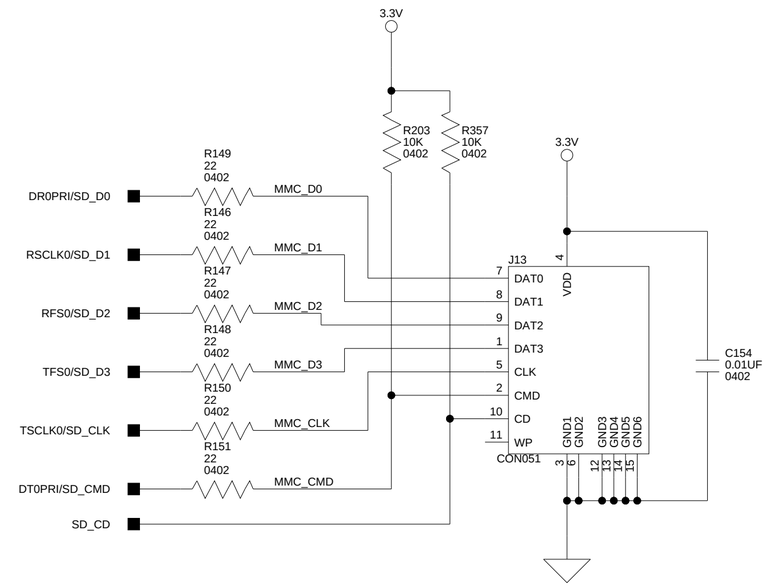






2GB eMMC





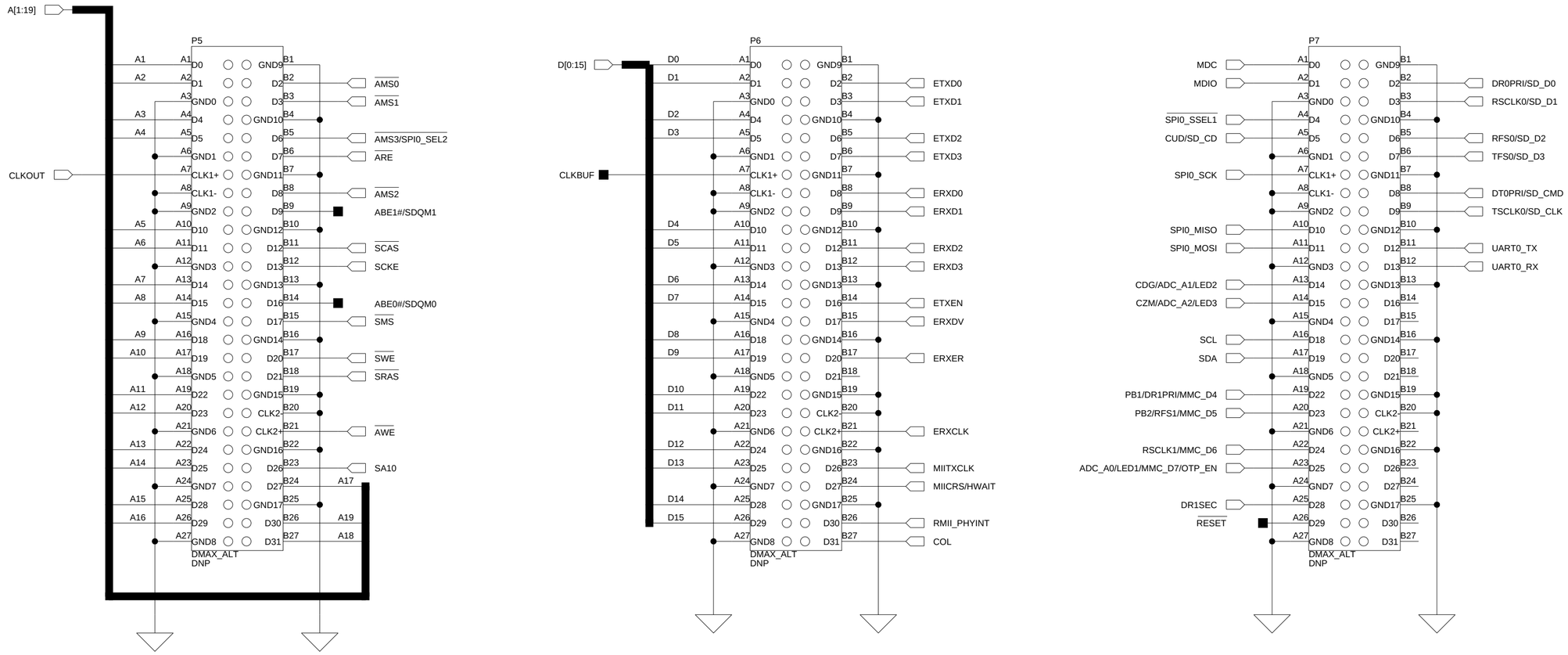
"SD CARD"

ANALOG DEVICES

20 Cotton Road
Nashua, NH 03063
PH: 1-800-ANALOGD

Title	ADSP-BF518F EZ-BOARD ROTARY ENCODER, JTAG, RS232, EMMC, SD		
Size C	**Board No.** A0217-2008		**Rev** 1.0
Date 5-13-2009_16:18		**Sheet** 9 **of** 16	

LOGIC ANALYZER COMPRESSION LAND GRID ARRAY



ANALOG DEVICES

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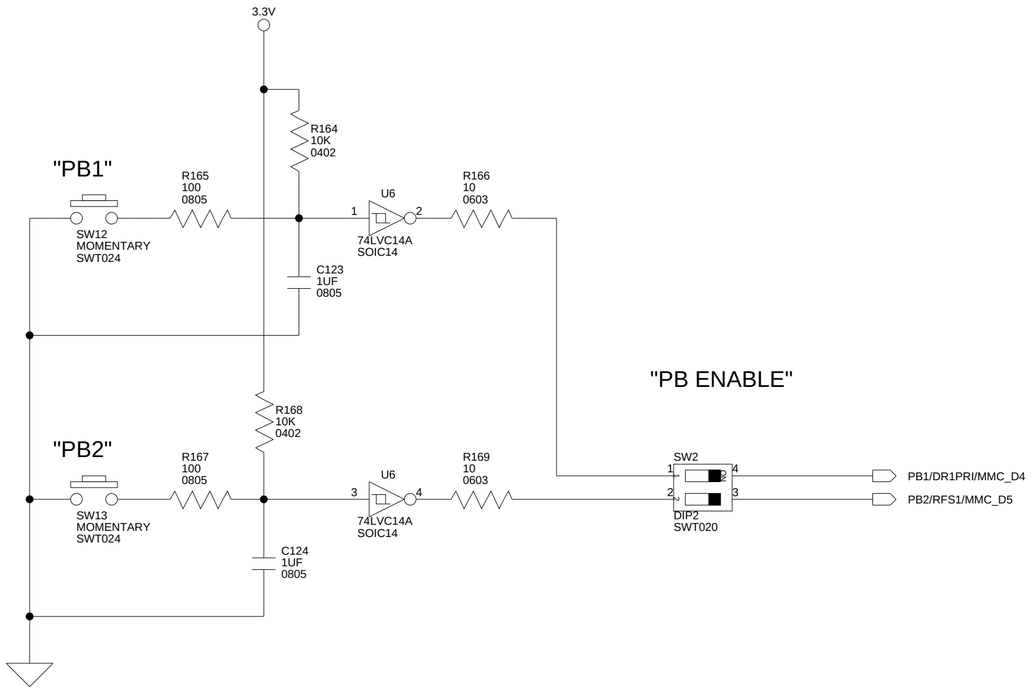
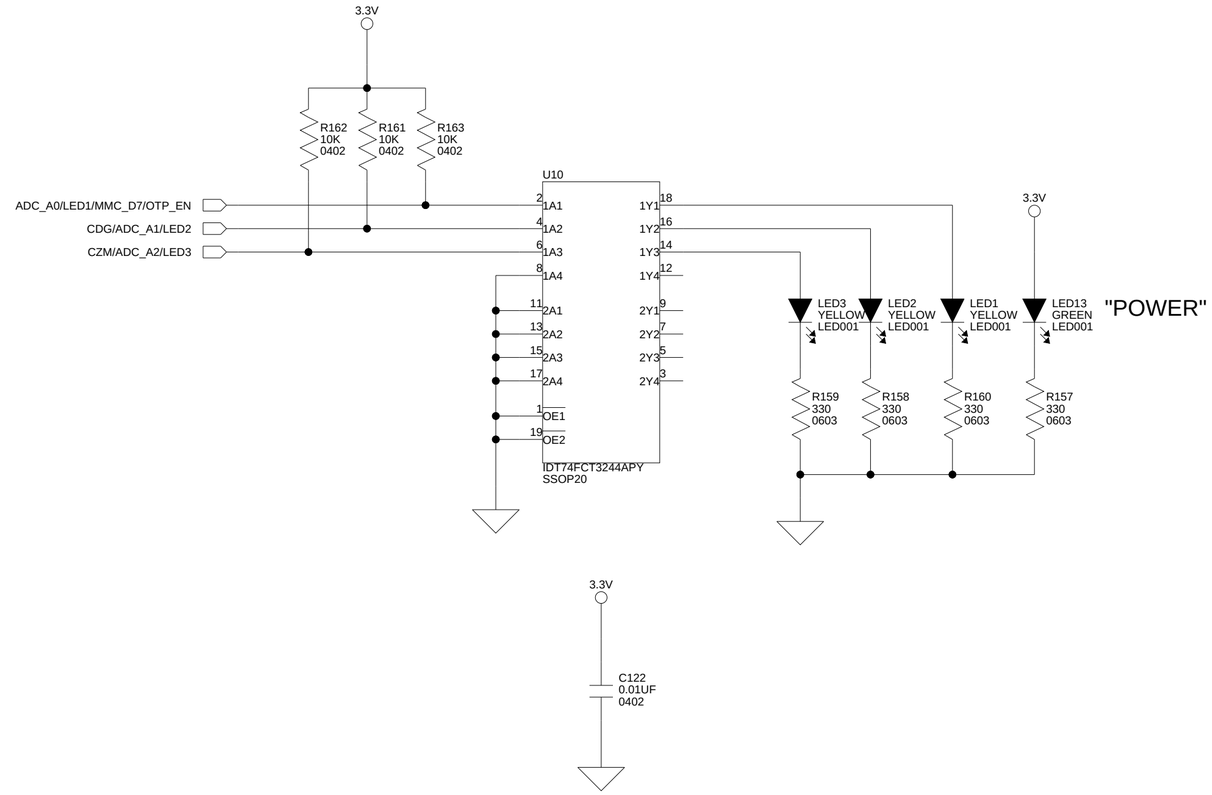
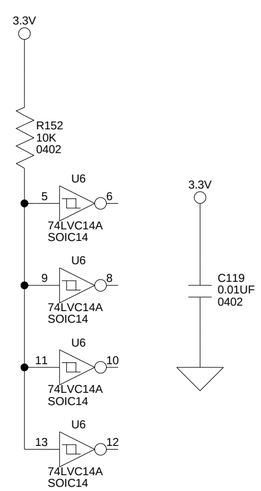
Title	ADSP-BF518F EZ-BOARD LOGIC ANALYZER CONN		
Size C	**Board No.** A0217-2008		**Rev** 1.0
Date 5-11-2009_10:44		**Sheet** 10 **of** 16	

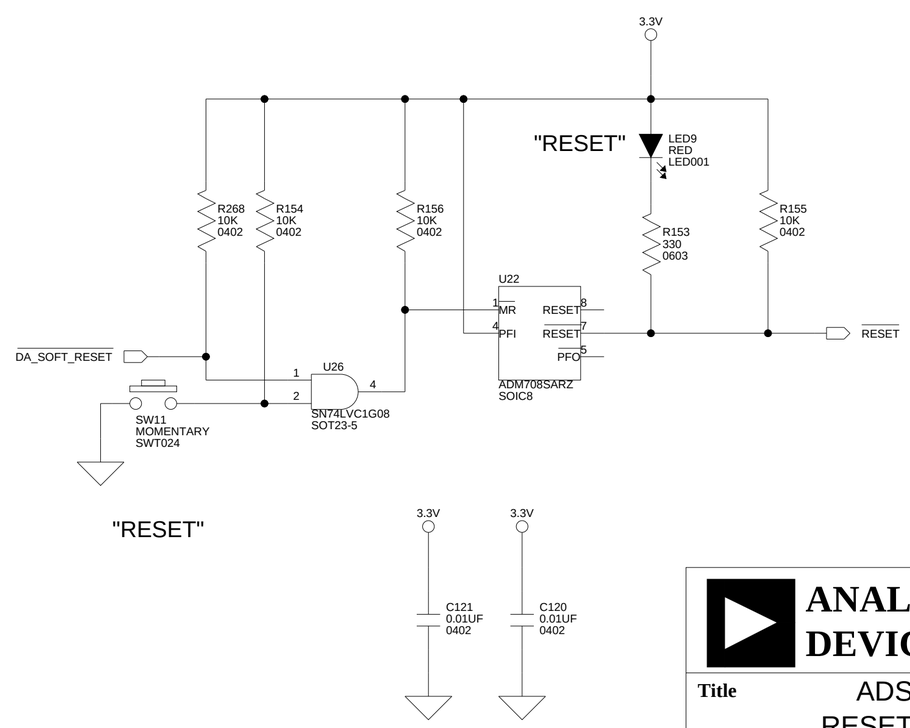




SW2: GPIO enable

POS.	FROM	TO	DEFAULT	FUNCTIONS
1	push button 1	DSP (U12, PH0)	ON	ON (PB1), OFF eMMC, ADC, Expansion Interface)
2	push button 2	DSP (U12, PH1)	ON	ON (PB2), OFF eMMC, ADC, Expansion Interface)





ANALOG DEVICES
20 Cotton Road
Nashua, NH 03063
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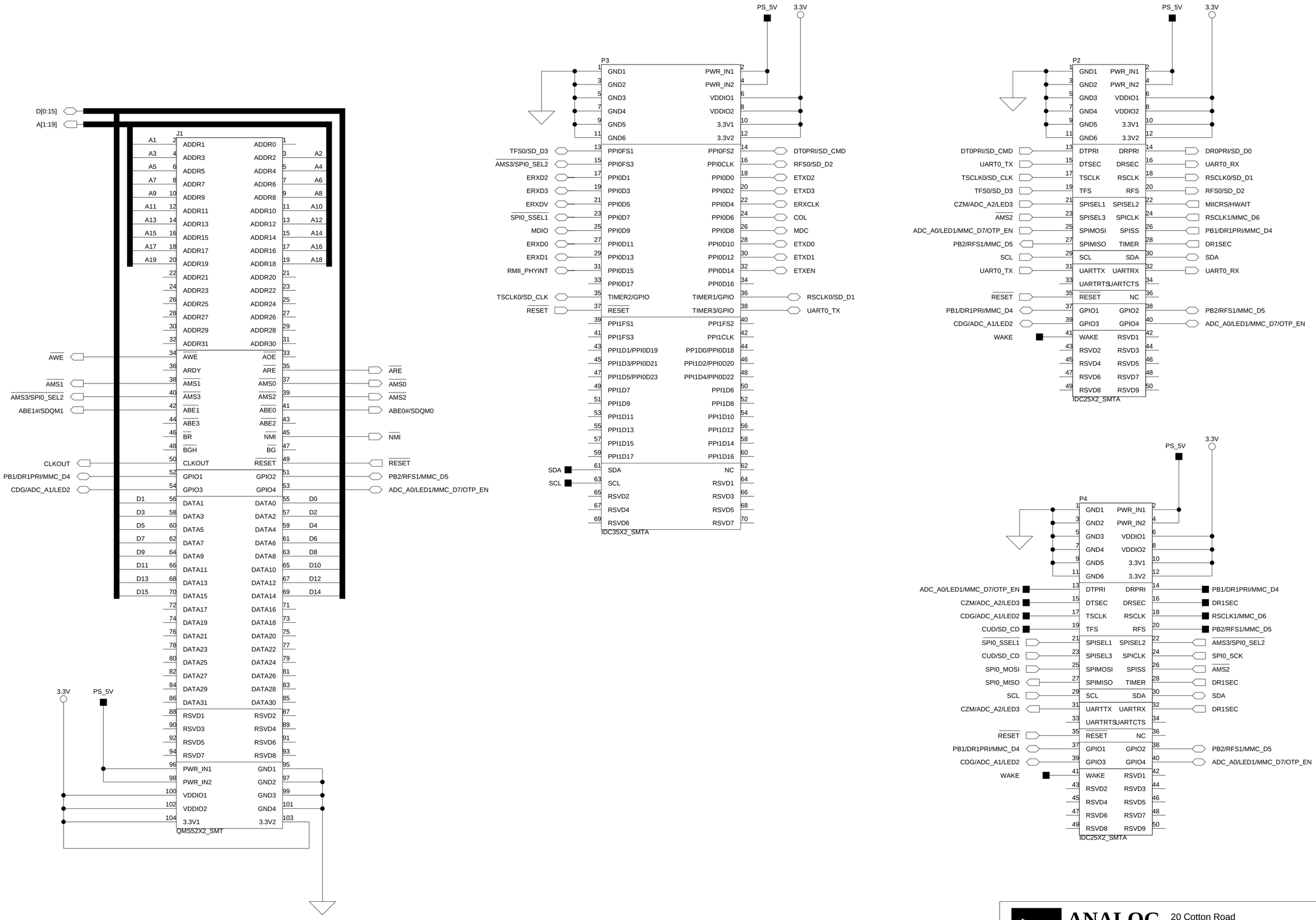
Title ADSP-BF518F EZ-BOARD
RESET, LEDS, PUSH BUTTONS

Size C | **Board No.** A0217-2008 | **Rev** 1.0

Date 5-13-2009_16:18 | **Sheet** 11 **of** 16



ANALOG DEVICES

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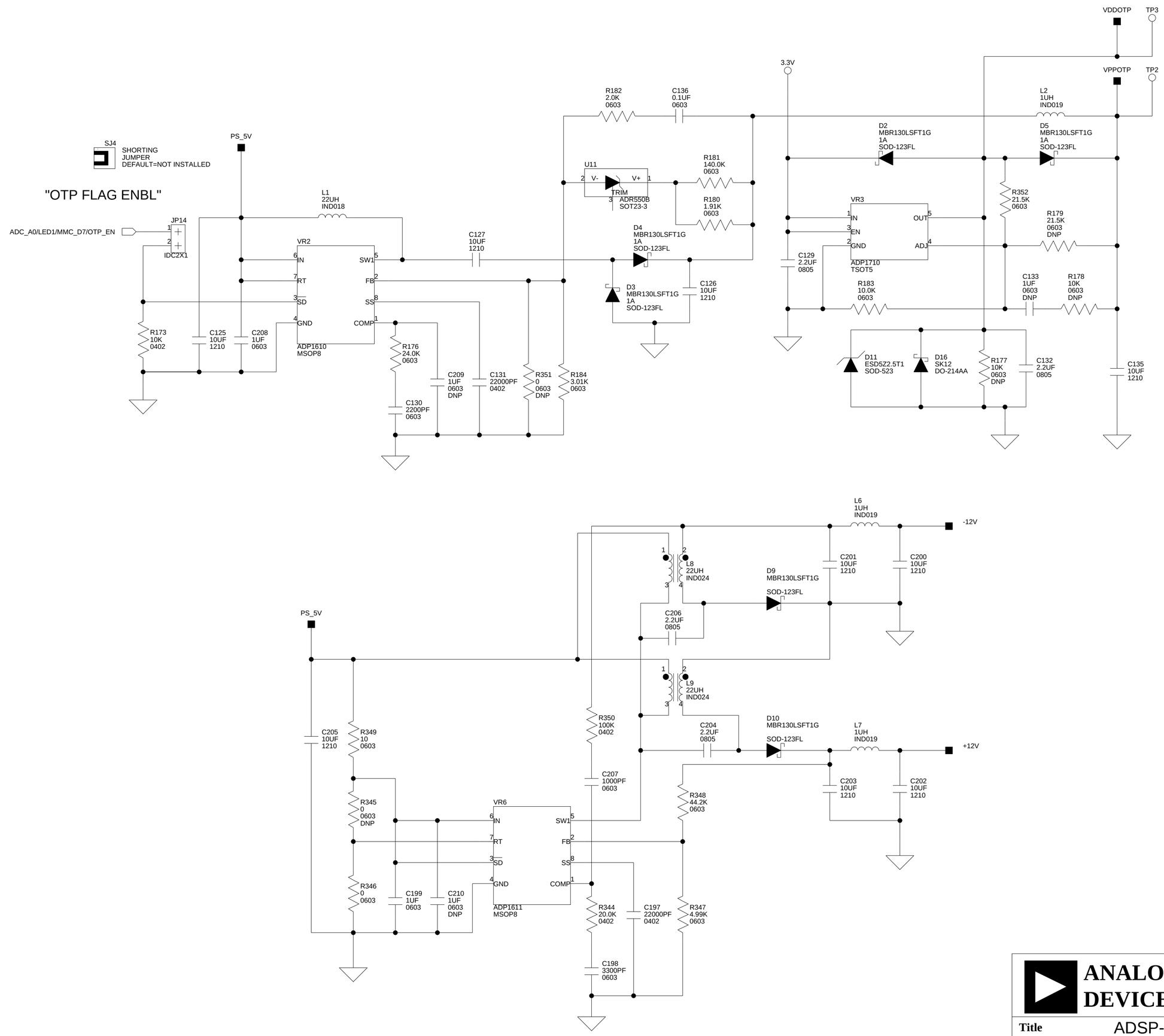
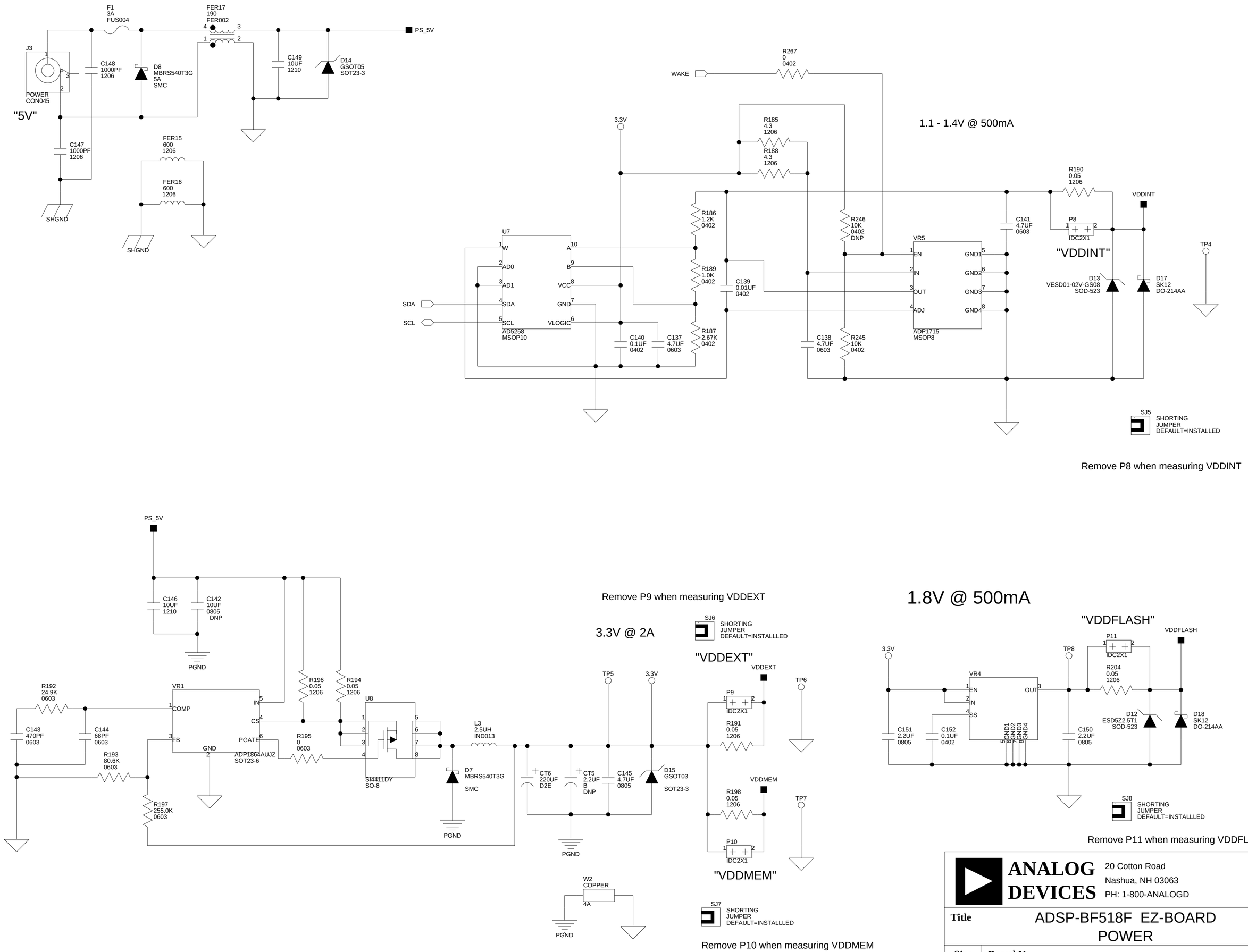
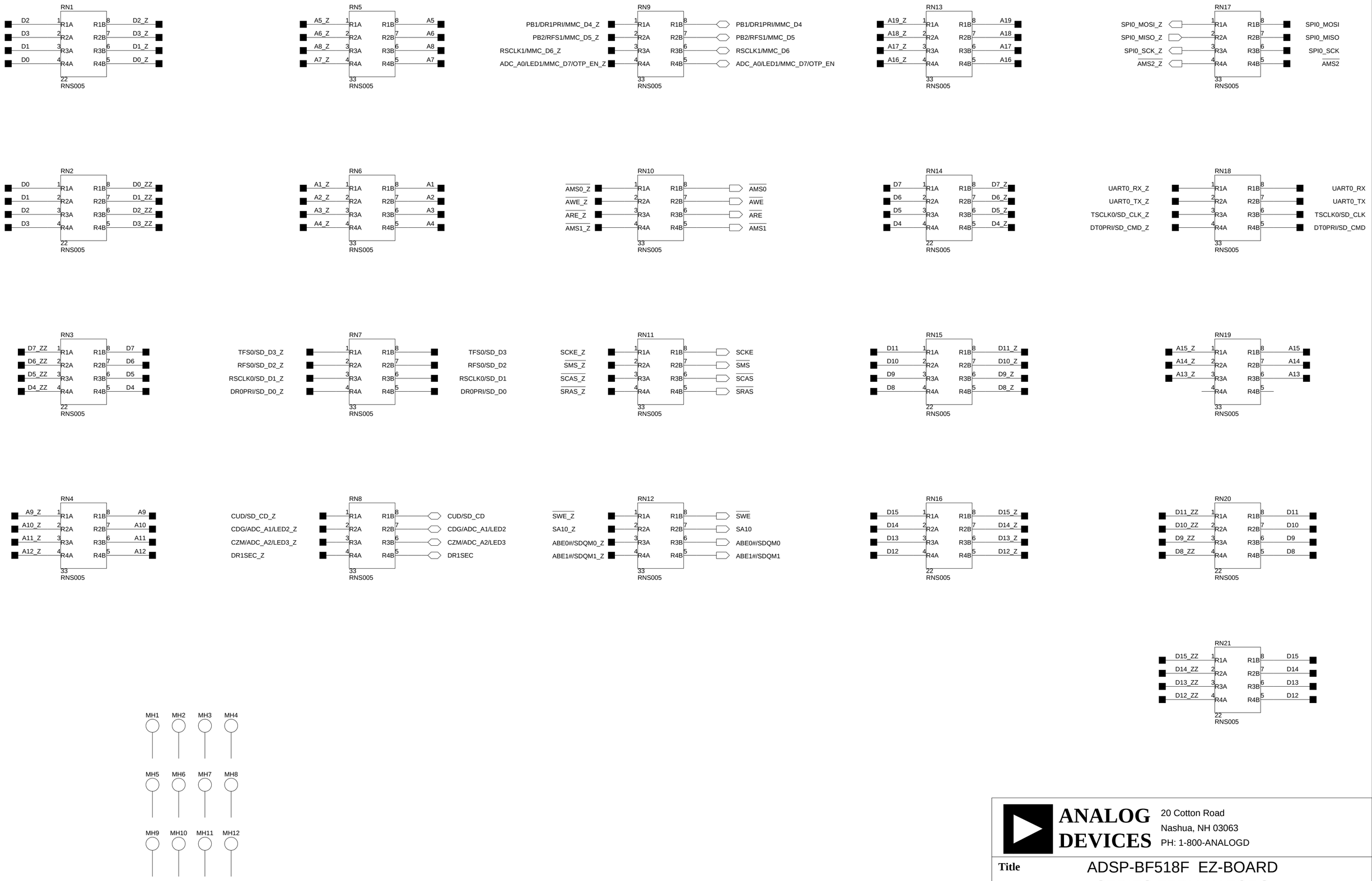
Title	ADSP-BF518F EZ-BOARD EXPANSION INTERFACE		
Size C	**Board No.** A0217-2008		**Rev** 1.0
Date 5-11-2009_10:44		**Sheet** 12 **of** 16	



ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-BF518F EZ-BOARD OTP AND DUAL POWER	
Size C	Board No. A0217-2008	Rev 1.0
Date 5-11-2009_10:44	Sheet 13 of 16	



ANALOG DEVICES	20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
Title	ADSP-BF518F EZ-BOARD POWER	
Size C	**Board No.** A0217-2008	**Rev** 1.0
Date 5-13-2009_16:19	**Sheet** 14 **of** 15	



ANALOG DEVICES

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Title	ADSP-BF518F EZ-BOARD SERIES TERMINATORS		
Size C	Board No. A0217-2008		Rev 1.0
Date 5-11-2009_10:44		Sheet 15 of 15	

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