



Complementary N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
N-Channel	20	0.396 at V _{GS} = 4.5 V	0.5	0.75 nC
		0.456 at V _{GS} = 2.5 V	0.2	
		0.546 at V _{GS} = 1.8 V	0.2	
		0.760 at V _{GS} = 1.5 V	0.05	
P-Channel	- 20	0.756 at V _{GS} = - 4.5 V	- 0.35	1 nC
		1.038 at V _{GS} = - 2.5 V	- 0.35	
		1.440 at V _{GS} = - 1.8 V	- 0.1	
		2.4 at V _{GS} = - 1.5 V	- 0.05	

FEATURES

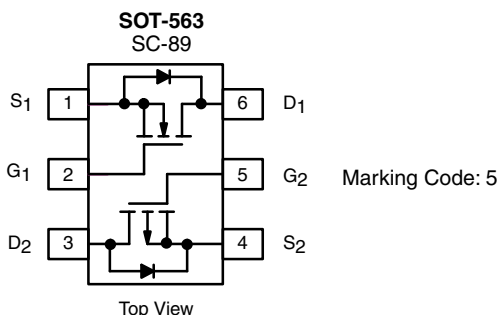
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- High-Side Switching
- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Typical ESD Protection: N-Channel 1500 V
P-Channel 1000 V (HBM)
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



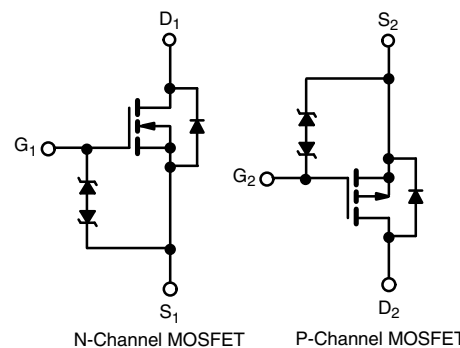
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch, Small Signal Switches and Level-Shift Switches
- Battery Operated Systems
- Portable



Ordering Information: Si1016CX-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	- 20	V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	0.6 ^{a, b}	- 0.6 ^{a, b}	A
	T _A = 70 °C		0.49 ^{a, b}	- 0.49 ^{a, b}	
Pulsed Drain Current (t = 300 μs)		I _{DM}	2	- 1.5	
Source Drain Current Diode Current	T _A = 25 °C	I _S	0.18 ^{a, b}	- 0.18 ^{a, b}	W
Maximum Power Dissipation	T _A = 25 °C	P _D	0.22 ^{a, b}	0.22 ^{a, b}	
	T _A = 70 °C		0.14 ^{a, b}	0.14 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	470	565	470	565	°C/W
		560	675	560	675	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
b. t = 5 s.
c. Maximum under steady state conditions is 675 °C/W.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	20			V
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 20			
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		17		mV/°C
		I _D = - 250 μA	P-Ch		- 12		
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 1.8		
		I _D = - 250 μA	P-Ch		1.8		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.4		1	V
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 0.4		- 1	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 4.5 V	N-Ch			± 1	μA
			P-Ch			± 1	
		V _{DS} = 0 V, V _{GS} = ± 8 V	N-Ch			± 30	
			P-Ch			± 30	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			1	
		V _{DS} = - 20 V, V _{GS} = 0 V	P-Ch			- 1	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			10	
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			- 10	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	2			A
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 1.5			
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 0.5 A	N-Ch		0.330	0.396	Ω
		V _{GS} = - 4.5 V, I _D = - 0.35 A	P-Ch		0.630	0.756	
		V _{GS} = 2.5 V, I _D = 0.2 A	N-Ch		0.380	0.456	
		V _{GS} = - 2.5 V, I _D = - 0.35 A	P-Ch		0.865	1.038	
		V _{GS} = 1.8 V, I _D = 0.2 A	N-Ch		0.420	0.546	
		V _{GS} = - 1.8 V, I _D = - 0.1 A	P-Ch		1.2	1.44	
		V _{GS} = 1.5 V, I _D = 0.05 A	N-Ch		0.505	0.760	
		V _{GS} = - 1.5 V, I _D = - 0.05 A	P-Ch		1.6	2.4	
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 0.5 A	N-Ch		2		S
		V _{DS} = - 10 V, I _D = - 3.6 A	P-Ch		1		
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		43		pF
	P-Ch			45			
Output Capacitance	C _{oss}		N-Ch		14		
	P-Ch			15			
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		8		
			P-Ch		10		
Dynamic ^a							
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 0.6 A	N-Ch		1.3	2	nC
		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 0.4 A	P-Ch		1.65	2.50	
		N-Channel V _{DS} = 10 V, V _{GS} = 2.5 V, I _D = 0.6 A	N-Ch		0.75	1.2	
			P-Ch		1	2	
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = - 10 V, V _{GS} = - 2.5 V, I _D = - 0.4 A	N-Ch		0.15		
	P-Ch			0.2			
Gate-Drain Charge	Q _{gd}		N-Ch		0.13		
	P-Ch			0.26			
Gate Resistance	R _g	f = 1 MHz	N-Ch	2.4	12.2	24.4	Ω
			P-Ch	2.4	12	24	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.



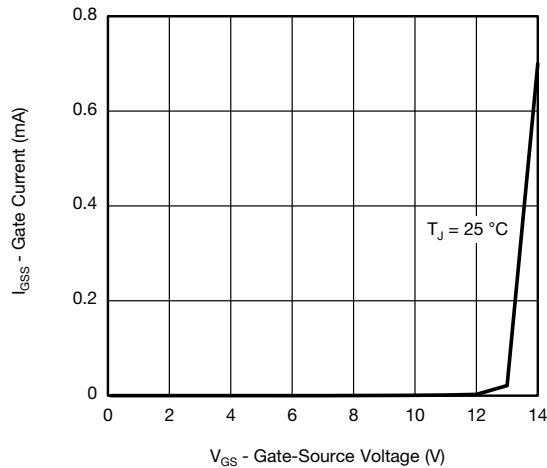
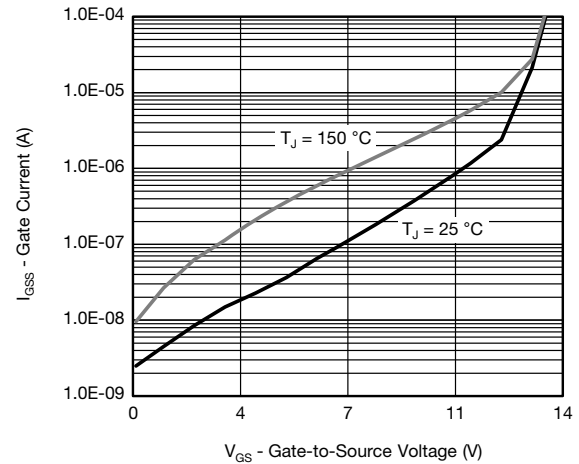
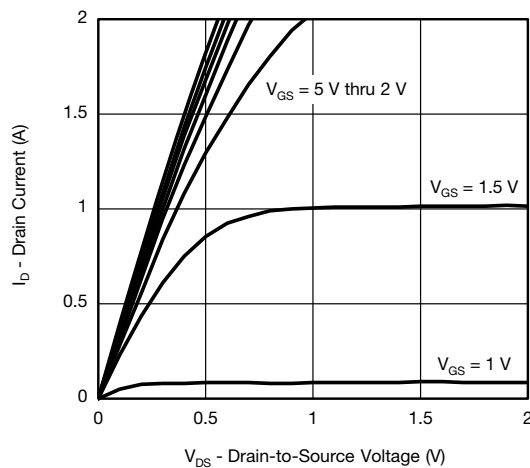
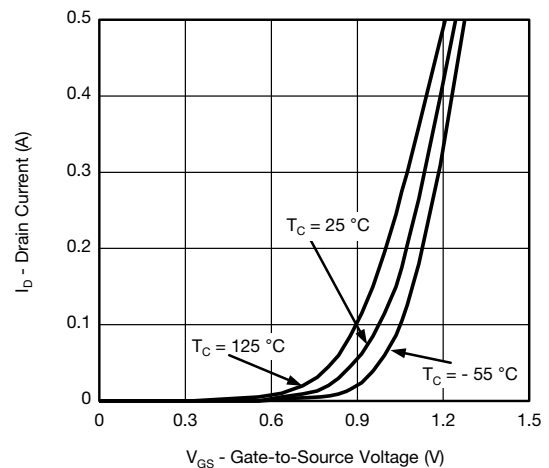
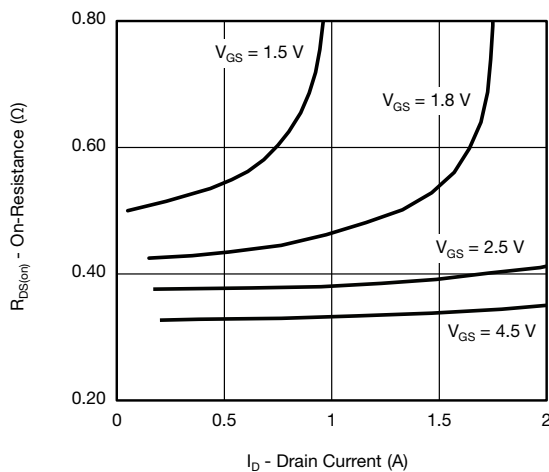
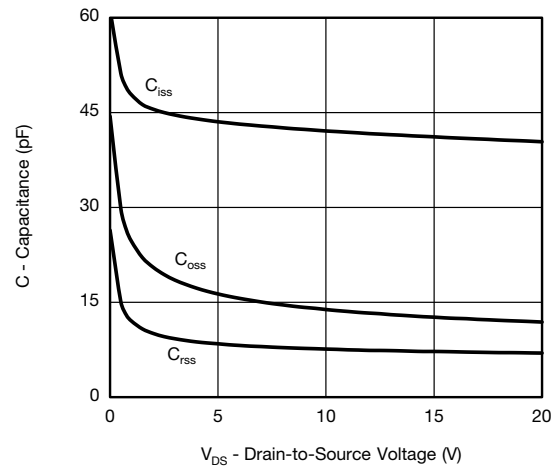
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 20 Ω I _D ≅ 0.5 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch		11	20	ns
			P-Ch		9	18	
Rise Time	t _r		N-Ch		16	24	
			P-Ch		10	20	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 10 V, R _L = 33.3 Ω I _D ≅ - 0.3 A, V _{GEN} = - 4.5 V, R _g = 1 Ω	N-Ch		26	39	
			P-Ch		10	20	
Fall Time	t _f		N-Ch		11	20	
			P-Ch		8	16	
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 20 Ω I _D ≅ 0.5 A, V _{GEN} = 8 V, R _g = 1 Ω	N-Ch		2	4	
			P-Ch		1	2	
Rise Time	t _r		N-Ch		13	20	
			P-Ch		8	16	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = - 10 V, R _L = 33.3 Ω I _D ≅ - 0.3 A, V _{GEN} = - 8 V, R _g = 1 Ω	N-Ch		7	14	
			P-Ch		9	18	
Fall Time	t _f		N-Ch		5	10	
			P-Ch		5	10	
Drain-Source Body Diode Characteristics							
Pulse Diode Forward Current ^a	I _{SM}		N-Ch			2	A
			P-Ch			- 1.5	
Body Diode Voltage	V _{SD}	I _S = 0.5 A, V _{GS} = 0 V	N-Ch		0.85	1.2	V
		I _S = - 0.3 A, V _{GS} = 0 V	P-Ch		- 0.87	- 1.2	
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 0.5 A, dI/dt = 100 A/μs, T _J = 25 °C	N-Ch		10	20	ns
			P-Ch		16	24	
Body Diode Reverse Recovery Charge	Q _{rr}		N-Ch		2	4	nC
			P-Ch		8	20	
Reverse Recovery Fall Time	t _a	P-Channel I _F = - 0.3 A, dI/dt = - 100 A/μs, T _J = 25 °C	N-Ch		5		ns
			P-Ch		11		
Reverse Recovery Rise Time	t _b		N-Ch		5		
			P-Ch		5		

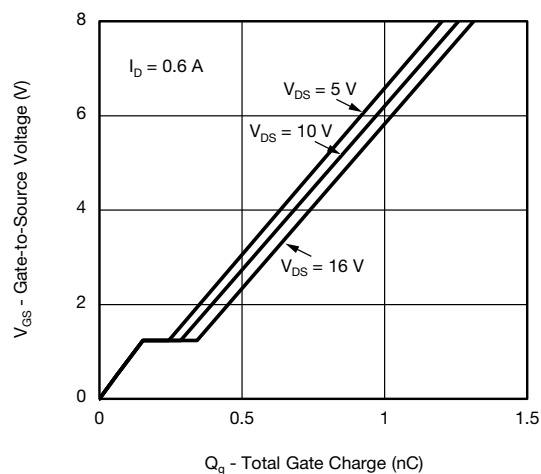
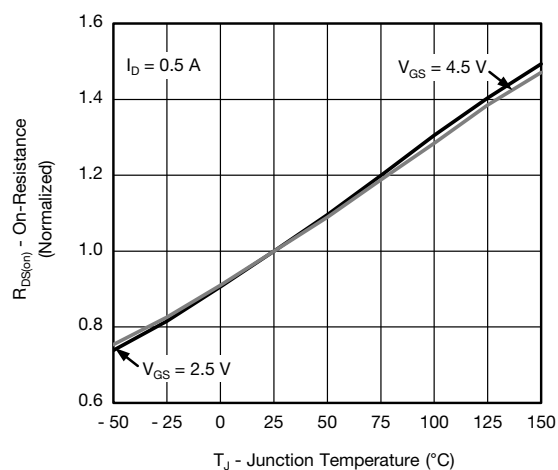
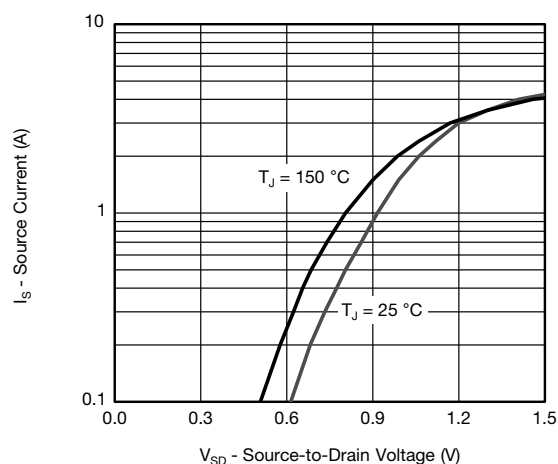
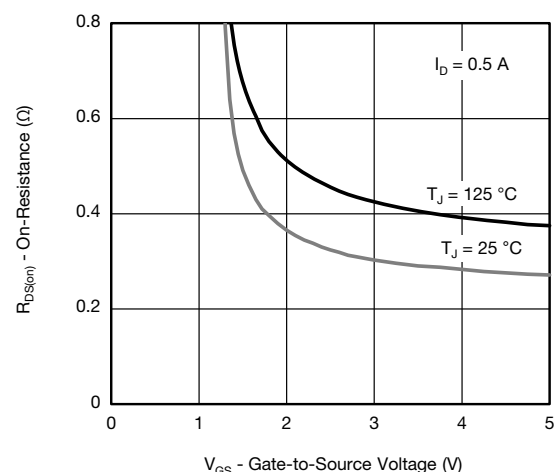
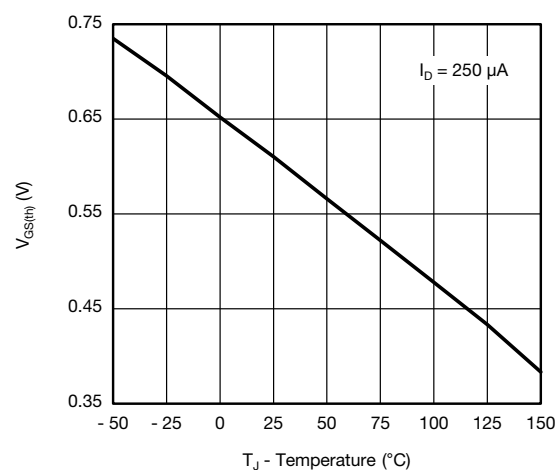
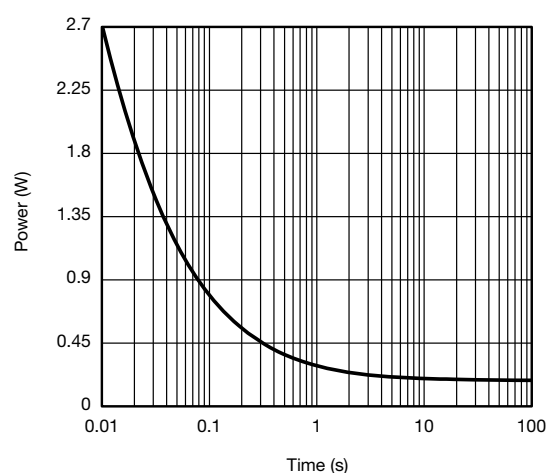
Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

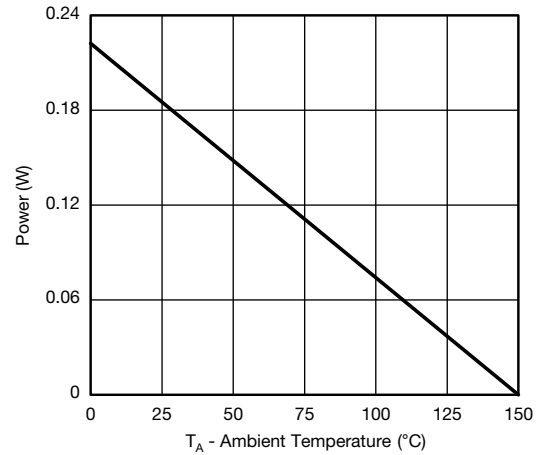
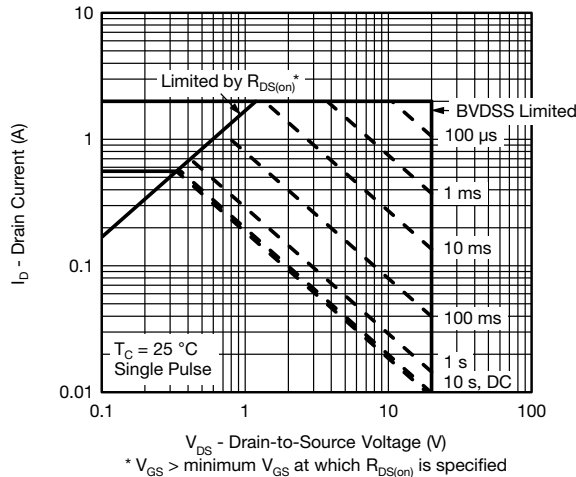
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Gate Current vs. Gate-Source Voltage****Gate Current vs. Gate-Source Voltage****Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance**

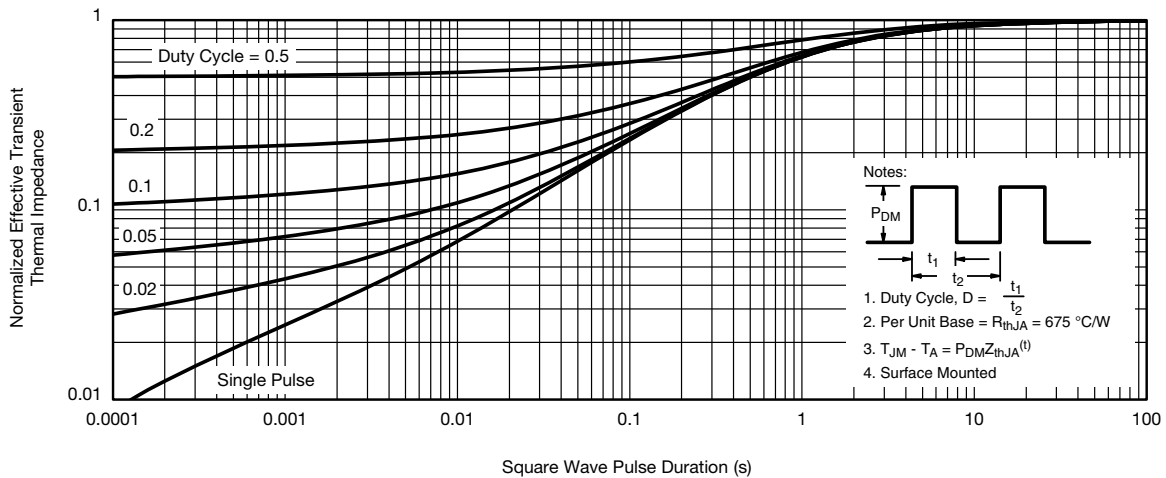

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power, Junction-to-Ambient

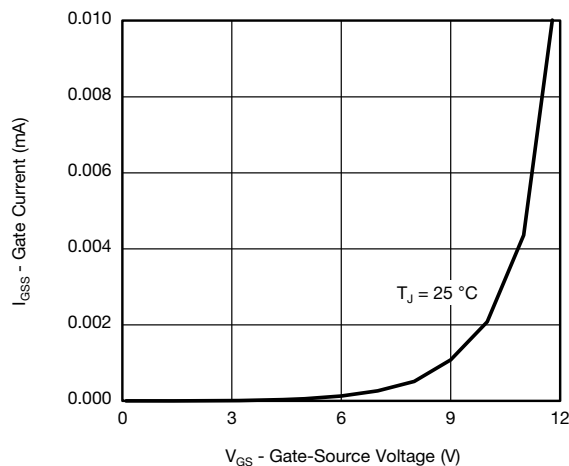
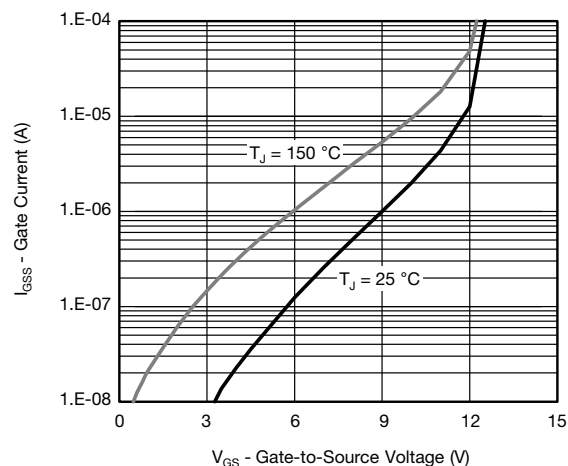
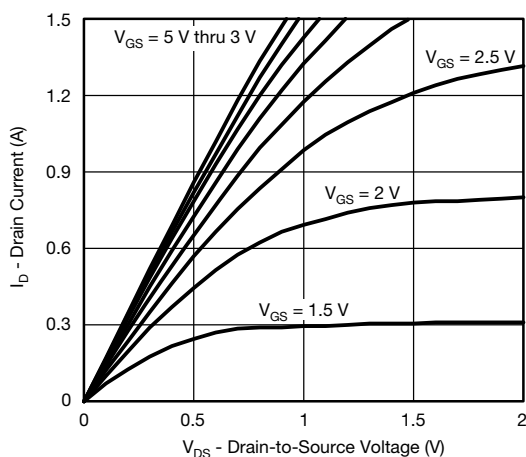
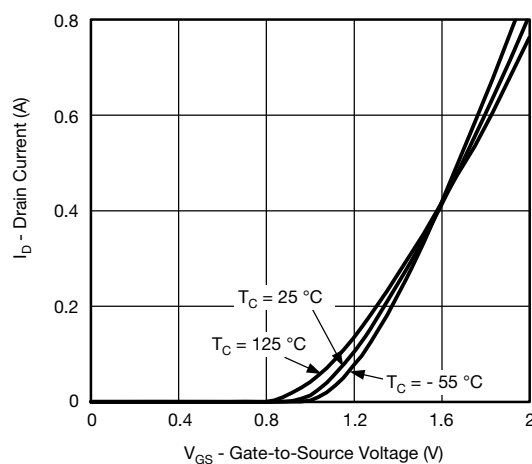
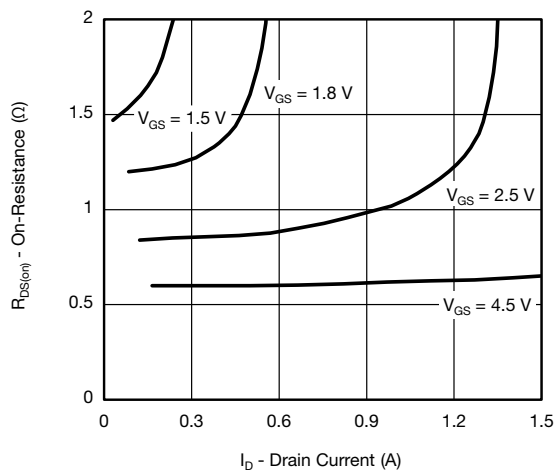
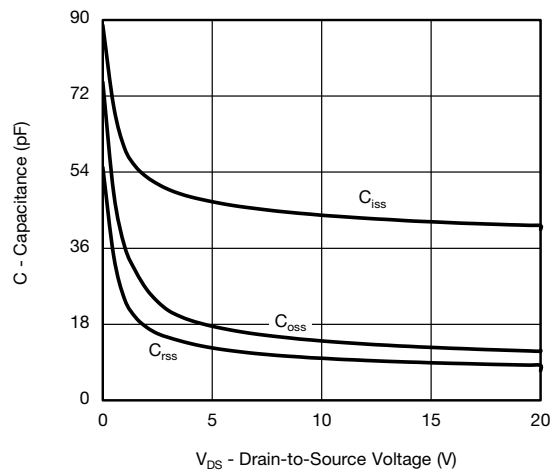
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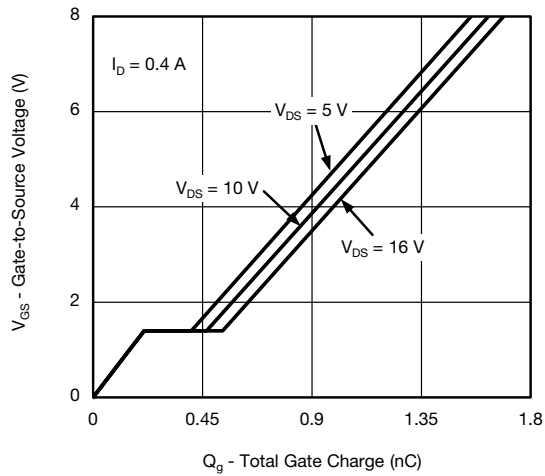
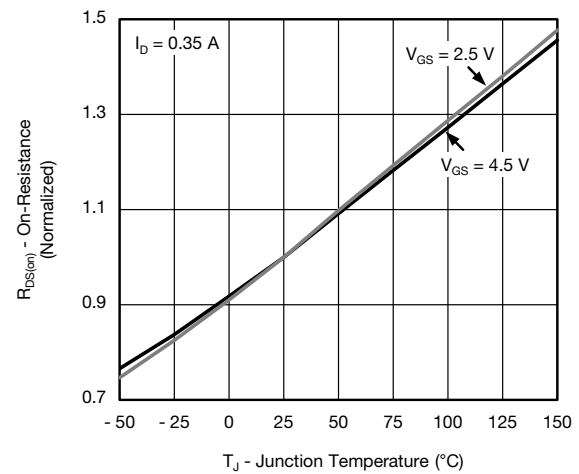
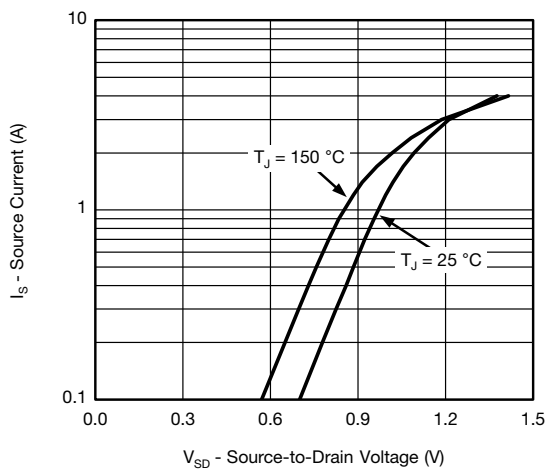
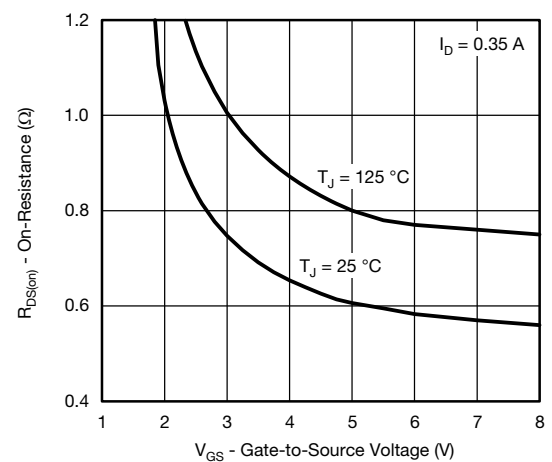
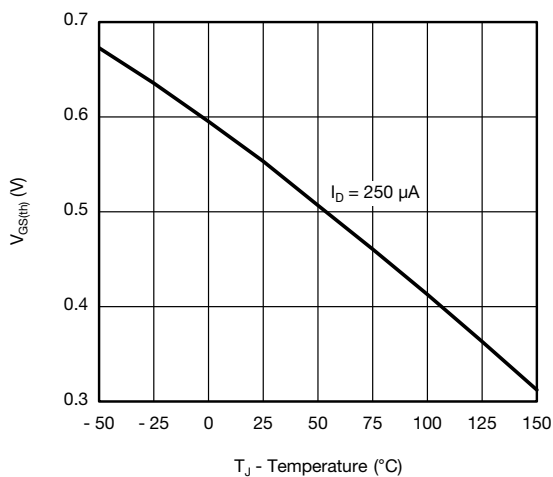
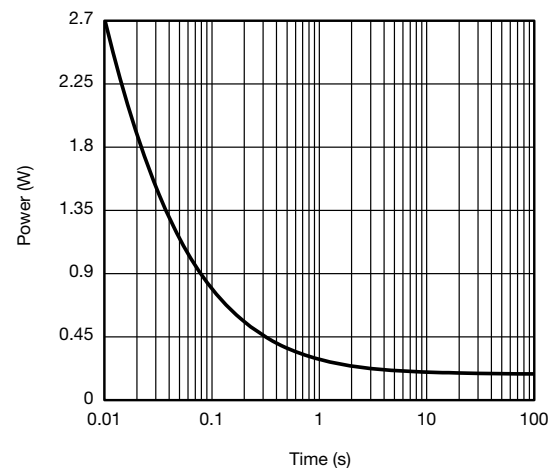
Vishay Siliconix

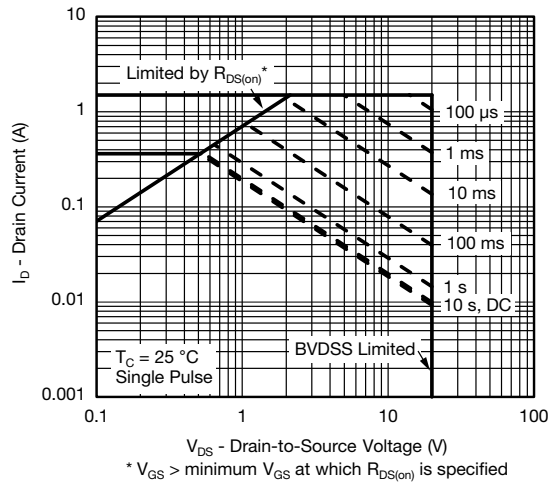
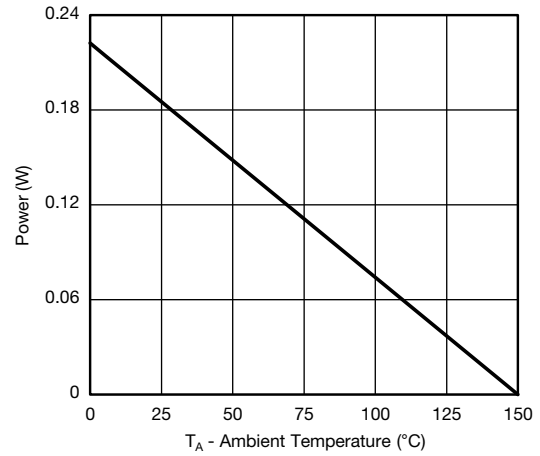
**N-CHANNEL TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

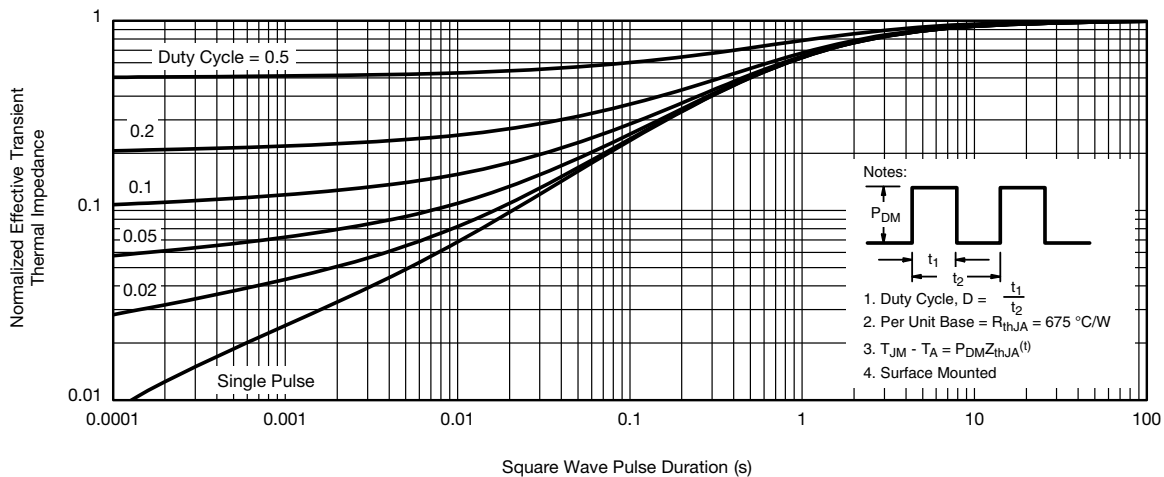



P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Gate Charge****On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient**

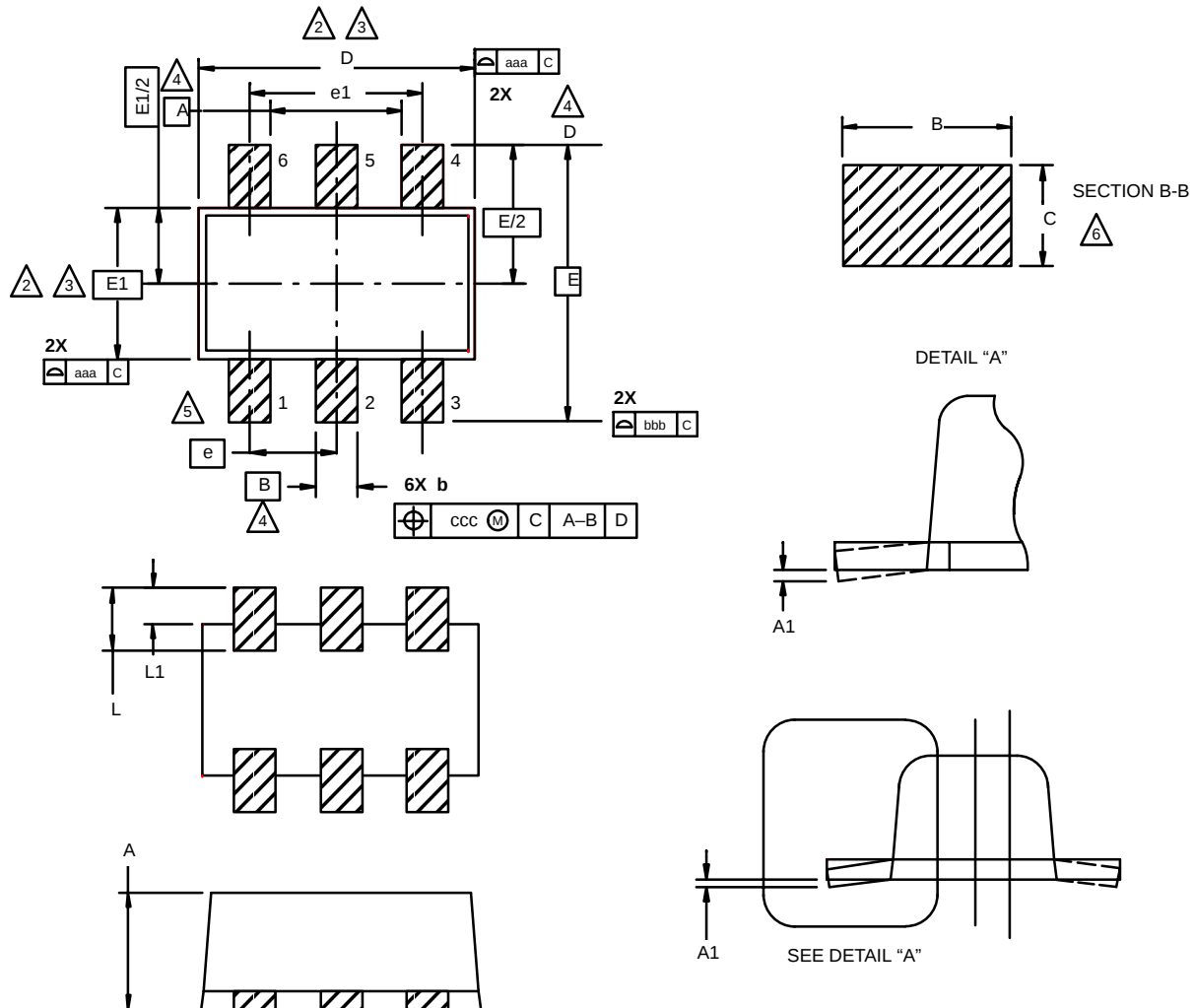

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Safe Operating Area, Junction-to-Ambient

Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67535.

SC89: 6- LEADS (SOT-563F)



NOTES:

1. Dimensions in millimeters.

△2 Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

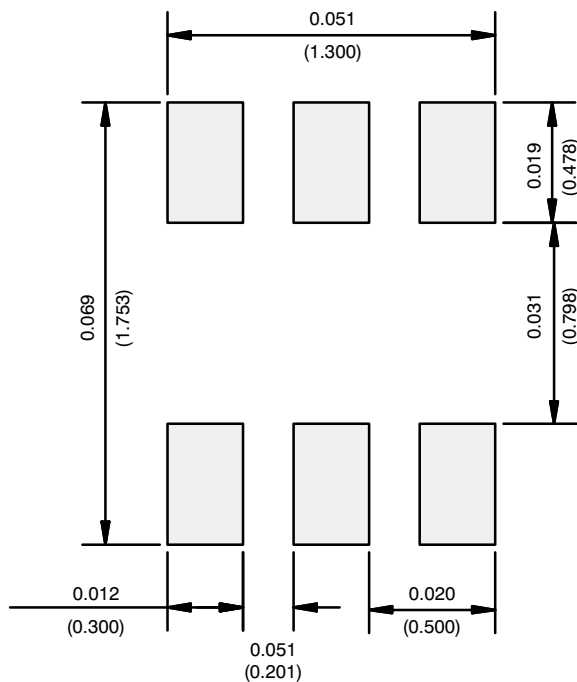
△3 Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

△4 Datums A, B and D to be determined 0.10 mm from the lead tip.

△5 Terminal numbers are shown for reference only.

△6 These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.