

## MKE02P64M20SF0

### KE02 Sub-Family

Supports the following:

MKE02Z16VLC2(R),  
MKE02Z32VLC2(R),  
MKE02Z64VLC2(R),  
MKE02Z16VLD2(R),  
MKE02Z32VLD2(R),  
MKE02Z64VLD2(R),  
MKE02Z32VLH2(R),  
MKE02Z64VLH2(R),  
MKE02Z32VQH2(R), and  
MKE02Z64VQH2(R)


#### Key features

- Operating characteristics
  - Voltage range: 2.7 to 5.5 V
  - Flash write voltage range: 2.7 to 5.5 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 20 MHz ARM® Cortex-M0+ core
  - Single cycle 32-bit x 32-bit multiplier
  - Single cycle I/O access port
- Memories and memory interfaces
  - Up to 64 KB flash
  - Up to 256 B EEPROM
  - Up to 4 KB RAM
- Clocks
  - Oscillator (OSC) - loop-controlled Pierce oscillator, crystal or ceramic resonator range of 31.25 kHz to 39.0625 kHz or 4 MHz to 20 MHz
  - Internal clock source (ICS) - internal FLL with internal or external reference, precision trimming of internal reference allowing 1% deviation across temperature range of 0 °C to 70 °C and 1.5% deviation across temperature range of -40 °C to 105 °C, up to 20 MHz
  - Internal 1 kHz low-power oscillator (LPO)



- System peripherals
  - Power management module (PMC) with three power modes: Run, Wait, Stop
  - Low-voltage detection (LVD) with reset or interrupt, selectable trip points
  - Watchdog with independent clock source (WDOG)
  - Programmable cyclic redundancy check module (CRC)
  - Serial wire debug interface (SWD)
  - Bit manipulation engine (BME)
- Security and integrity modules
  - 64-bit unique identification (ID) number per chip
- Human-machine interface
  - Up to 57 general-purpose input/output (GPIO)
  - Two 8-bit keyboard interrupt modules (KBI)
  - Interrupt (IRQ)
- Analog modules
  - One 16-channel 12-bit SAR ADC, operation in Stop mode, optional hardware trigger (ADC)
  - Two analog comparators containing a 6-bit DAC and programmable reference input (ACMP)
- Timers
  - One 6-channel FlexTimer/PWM (FTM)
  - Two 2-channel FlexTimer/PWM (FTM)
  - One 2-channel periodic interrupt timer (PIT)
  - One real-time clock (RTC)

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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- Communication interfaces
    - Two SPI modules (SPI)
    - Three UART modules (UART)
    - One I2C module (I2C)
  - Package options
    - 64-pin QFP/LQFP
    - 44-pin LQFP
    - 32-pin LQFP

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# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: KE02Z.

## 2 Part identification

### 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 2.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

### 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
KE##	Kinetis family	<ul style="list-style-type: none"> <li>KE02</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>Z = M0+ core</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>16 = 16 KB</li> <li>32 = 32 KB</li> <li>64 = 64 KB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>

*Table continues on the next page...*

Field	Description	Values
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>LC = 32 LQFP (7 mm x 7 mm)</li> <li>LD = 44 LQFP (10 mm x 10 mm)</li> <li>QH = 64 QFP (14 mm x 14 mm)</li> <li>LH = 64 LQFP (10 mm x 10 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>2 = 20 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>R = Tape and reel</li> <li>(Blank) = Trays</li> </ul>

## 2.4 Example

This is an example part number:

MKE02Z64VQH2

## 3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

**Table 1. Parameter classifications**

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

## 4 Ratings

### 4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-6000	+6000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

### 4.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either  $V_{SS}$  or  $V_{DD}$ ) or the programmable pullup resistor associated with the pin is enabled.

**Table 2. Voltage and current operating ratings**

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Supply voltage	-0.3	6.0	V
$I_{DD}$	Maximum current into $V_{DD}$	—	120	mA
$V_{DIO}$	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	$V_{DD} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup> , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Analog pins are defined as pins that do not have an associated general-purpose I/O port function.

## 5 General

### 5.1 Nonswitching electrical specifications

#### 5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

**Table 3. DC characteristics**

Symbol	C	Descriptions		Min	Typical <sup>1</sup>	Max	Unit
—	—	Operating voltage		2.7	—	5.5	V
$V_{OH}$	P	Output high voltage	All I/O pins, standard-drive strength	5 V, $I_{load} = -5$ mA	$V_{DD} - 0.8$	—	V
	C			3 V, $I_{load} = -2.5$ mA	$V_{DD} - 0.8$	—	V
	P	High current drive pins, high-drive strength	5 V, $I_{load} = -20$ mA	$V_{DD} - 0.8$	—	V	
	C		3 V, $I_{load} = -10$ mA	$V_{DD} - 0.8$	—	V	

Table continues on the next page...

**Table 3. DC characteristics (continued)**

Symbol	C	Descriptions		Min	Typical <sup>1</sup>	Max	Unit	
I <sub>OHT</sub>	D	Output high current	Max total I <sub>OH</sub> for all ports	5 V	—	—	-100	mA
				3 V	—	—	-60	
V <sub>OL</sub>	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I <sub>load</sub> = 5 mA	—	—	0.8	V
	C			3 V, I <sub>load</sub> = 2.5 mA	—	—	0.8	V
	P	High current drive pins, high-drive strength <sup>2</sup>	5 V, I <sub>load</sub> = 20 mA	—	—	0.8	V	
	C		3 V, I <sub>load</sub> = 10 mA	—	—	0.8	V	
I <sub>OLT</sub>	D	Output low current	Max total I <sub>OL</sub> for all ports	5 V	—	—	100	mA
				3 V	—	—	60	
V <sub>IH</sub>	P	Input high voltage	All digital inputs	V <sub>DD</sub> > 4.5 V	0.70 × V <sub>DD</sub>	—	—	V
				V <sub>DD</sub> > 2.7 V	0.75 × V <sub>DD</sub>	—	—	
V <sub>IL</sub>	P	Input low voltage	All digital inputs	V <sub>DD</sub> > 4.5 V	—	—	0.30 × V <sub>DD</sub>	V
				V <sub>DD</sub> > 2.7 V	—	—	0.35 × V <sub>DD</sub>	
V <sub>hys</sub>	C	Input hysteresis	All digital inputs	—	0.06 × V <sub>DD</sub>	—	—	mV
I <sub>In</sub>	P	Input leakage current	All input only pins (per pin)	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	0.1	1	μA
I <sub>OZ</sub>	C	Hi-Z (off-state) leakage current	All input/output (per pin)	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	0.1	1	μA
I <sub>OZTOT</sub>	C	Total leakage combined for all inputs and Hi-Z pins	All input only and I/O	V <sub>IN</sub> = V <sub>DD</sub> or V <sub>SS</sub>	—	—	2	μA
R <sub>PU</sub>	P	Pullup resistors	All digital inputs, when enabled	—	30.0	—	50.0	kΩ
I <sub>IC</sub>	D	DC injection current <sup>3, 4, 5</sup>	Single pin limit	V <sub>IN</sub> < V <sub>SS</sub> , V <sub>IN</sub> > V <sub>DD</sub>	-0.2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C <sub>In</sub>	C	Input capacitance, all pins		—	—	—	7	pF
V <sub>RAM</sub>	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support ultra high current output.
3. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V<sub>SS</sub> and V<sub>DD</sub>.
4. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the large value.
5. Power supply must maintain regulation within operating V<sub>DD</sub> range during instantaneous and operating maximum current conditions. If the positive injection current (V<sub>in</sub> > V<sub>DD</sub>) is higher than I<sub>DD</sub>, the injection current may flow out of V<sub>DD</sub> and could result in external power supply going out of regulation. Ensure that external V<sub>DD</sub> load will shunt current higher than maximum injection current when the MCU is not consuming power, such as no system clock is present, or clock rate is very low (which would reduce overall power consumption).



**Table 4. LVD and POR specification**

Symbol	C	Description	Min	Typ	Max	Unit	
V <sub>POR</sub>	D	POR re-arm voltage <sup>1</sup>	1.5	1.75	2.0	V	
V <sub>LVDH</sub>	C	Falling low-voltage detect threshold—high range (LVDV = 1) <sup>2</sup>	4.2	4.3	4.4	V	
V <sub>LWV1H</sub>	C	Falling low-voltage warning threshold—high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V <sub>LWV2H</sub>	C		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V <sub>LWV3H</sub>	C		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V <sub>LWV4H</sub>	C		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V <sub>HYSH</sub>	C	High range low-voltage detect/warning hysteresis	—	100	—	mV	
V <sub>LVDL</sub>	C	Falling low-voltage detect threshold—low range (LVDV = 0)	2.56	2.61	2.66	V	
V <sub>LWV1L</sub>	C	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V <sub>LWV2L</sub>	C		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V <sub>LWV3L</sub>	C		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V <sub>LWV4L</sub>	C		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V <sub>HYSDL</sub>	C	Low range low-voltage detect hysteresis	—	40	—	mV	
V <sub>HYSWL</sub>	C	Low range low-voltage warning hysteresis	—	80	—	mV	
V <sub>BG</sub>	P	Buffered bandgap output <sup>3</sup>	1.14	1.16	1.18	V	

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V<sub>DD</sub> = 5.0 V, Temp = 25 °C

Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (standard drive strength) ( $V_{DD} = 5\text{ V}$ )

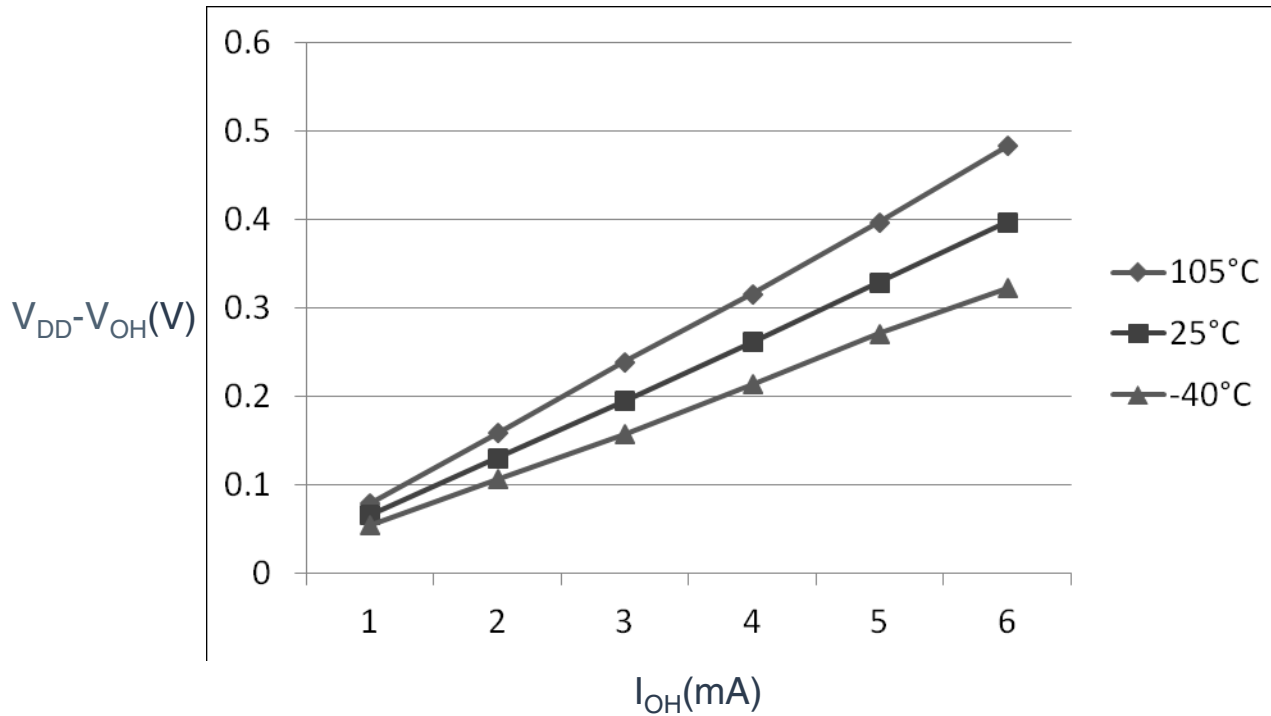


Figure 1. Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (standard drive strength) ( $V_{DD} = 5\text{ V}$ )

Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

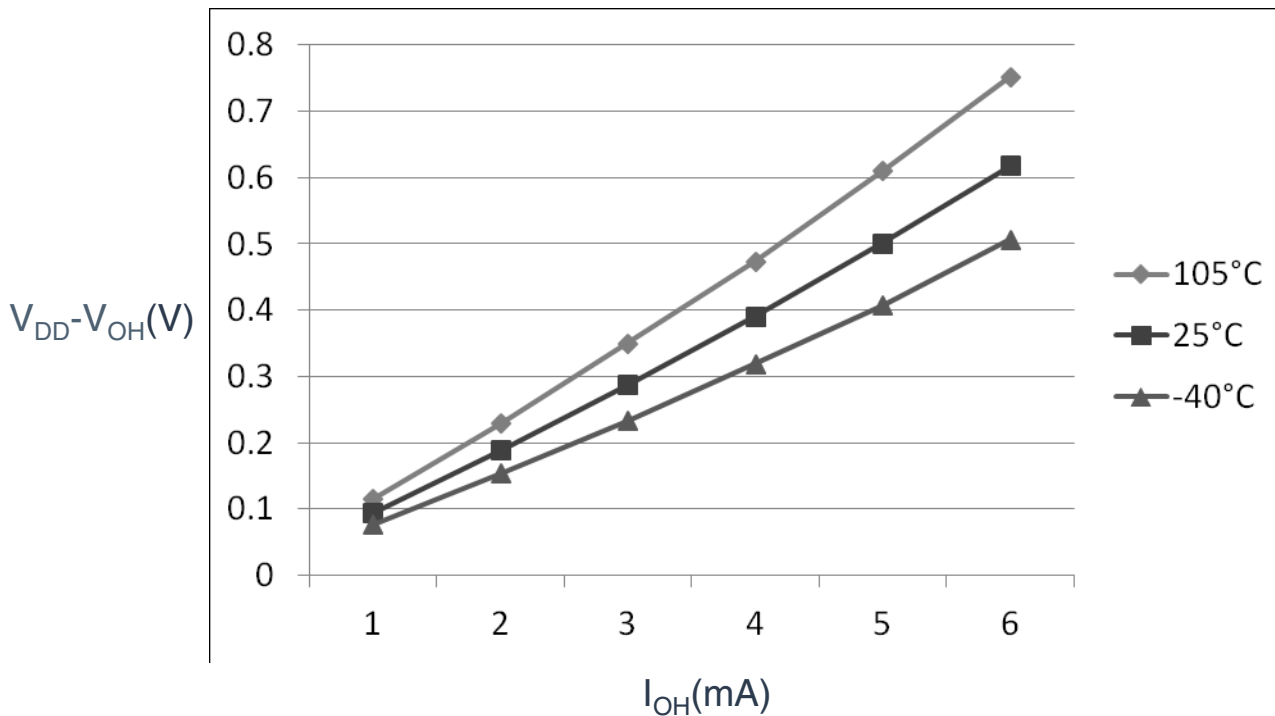


Figure 2. Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

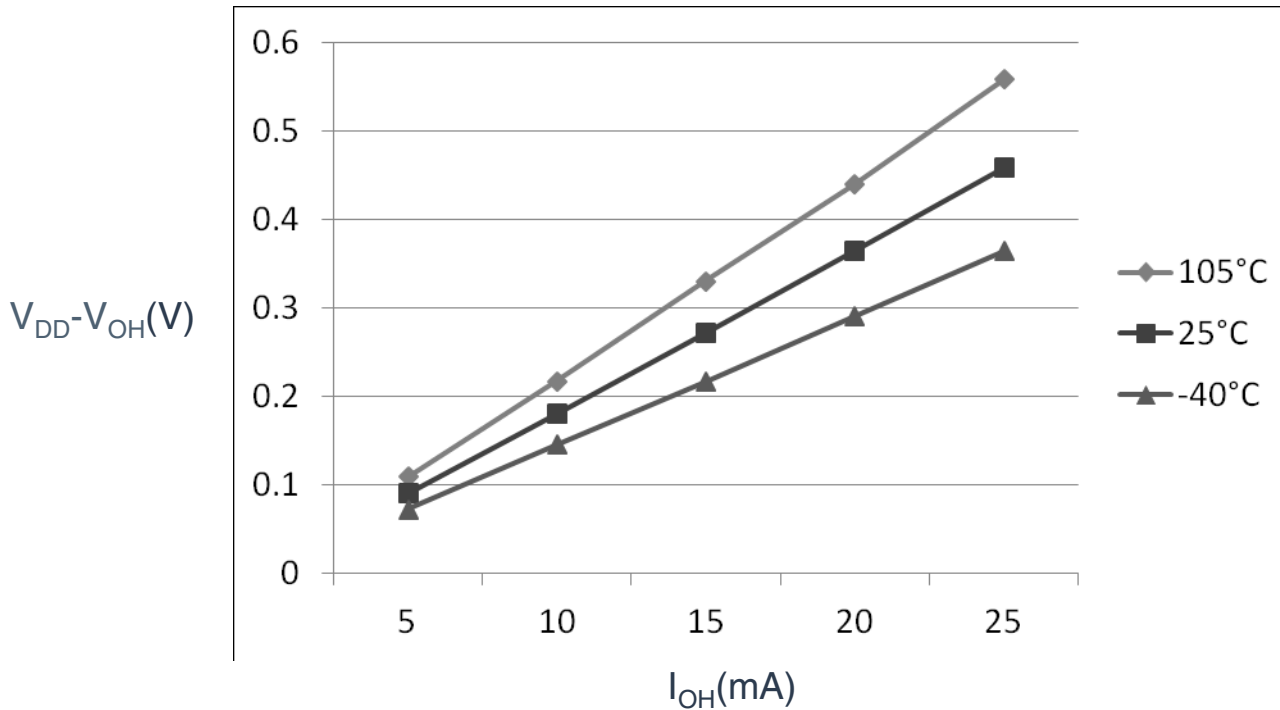


Figure 3. Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (high drive strength) ( $V_{DD} = 3\text{ V}$ )

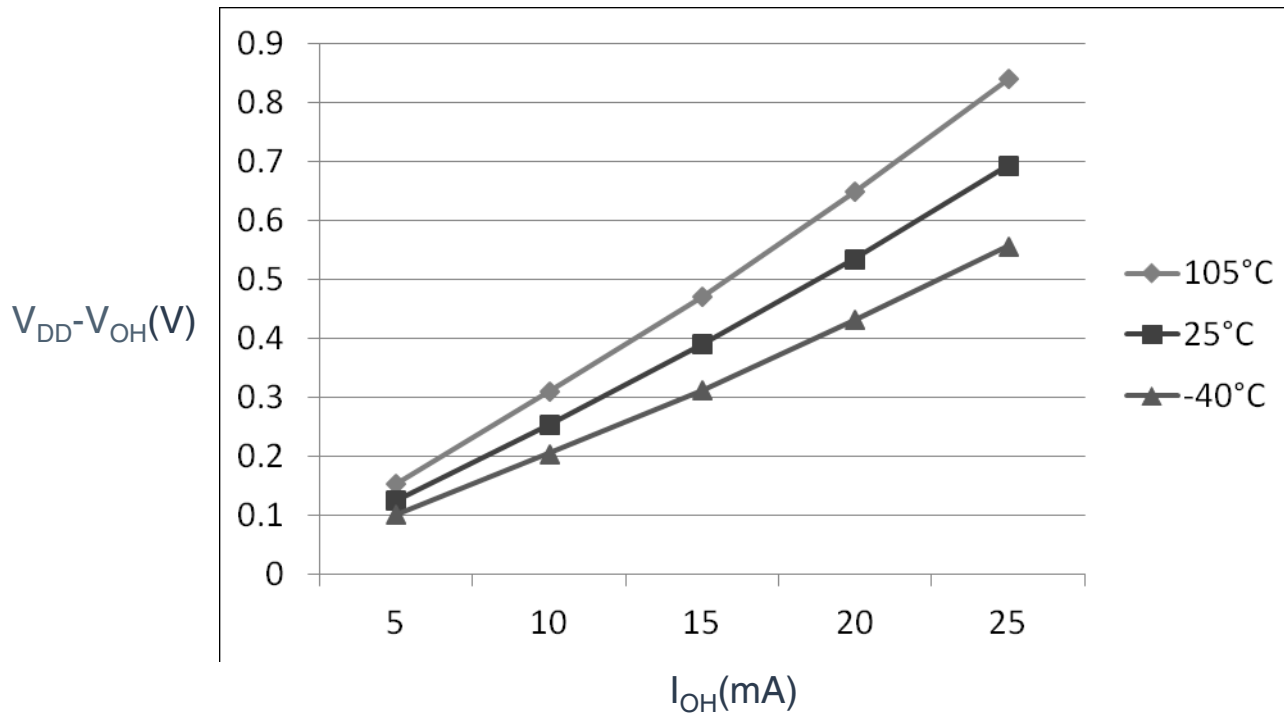


Figure 4. Typical  $I_{OH}$  Vs.  $V_{DD}-V_{OH}$  (high drive strength) ( $V_{DD} = 3\text{ V}$ )

Typical  $I_{OL}$  Vs.  $V_{OL}$  (standard drive strength) ( $V_{DD} = 5\text{ V}$ )

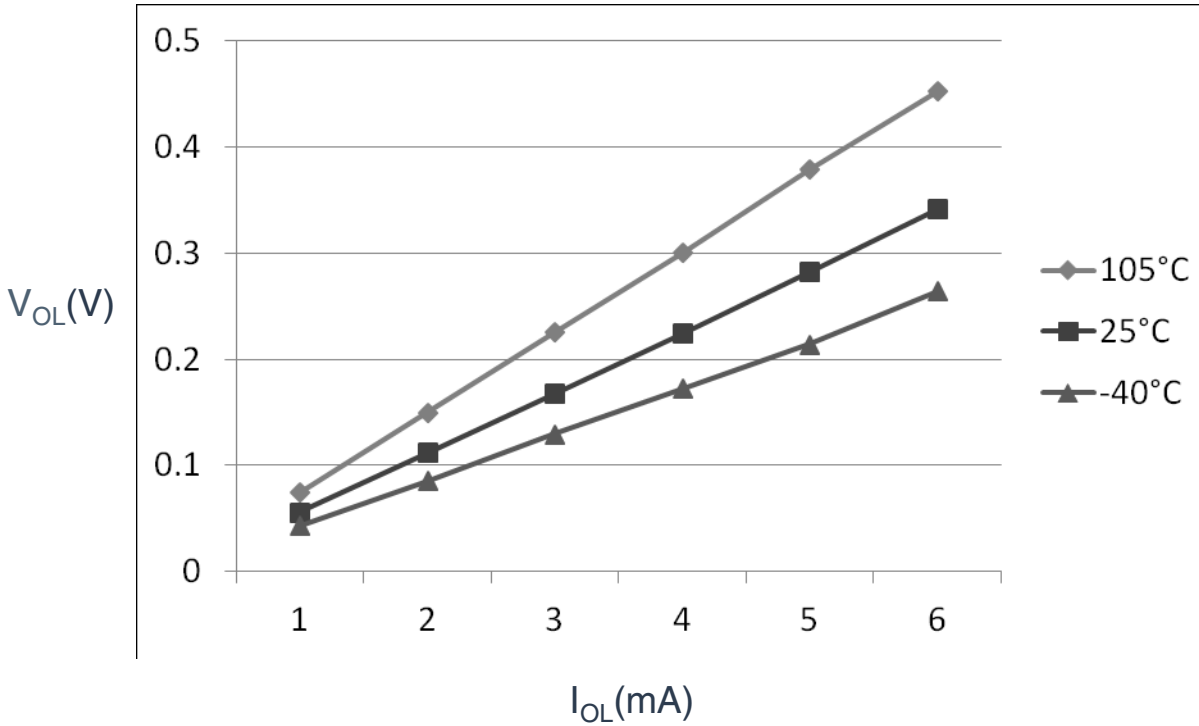


Figure 5. Typical  $I_{OL}$  Vs.  $V_{OL}$  (standard drive strength) ( $V_{DD} = 5\text{ V}$ )

Typical  $I_{OL}$  Vs.  $V_{OL}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

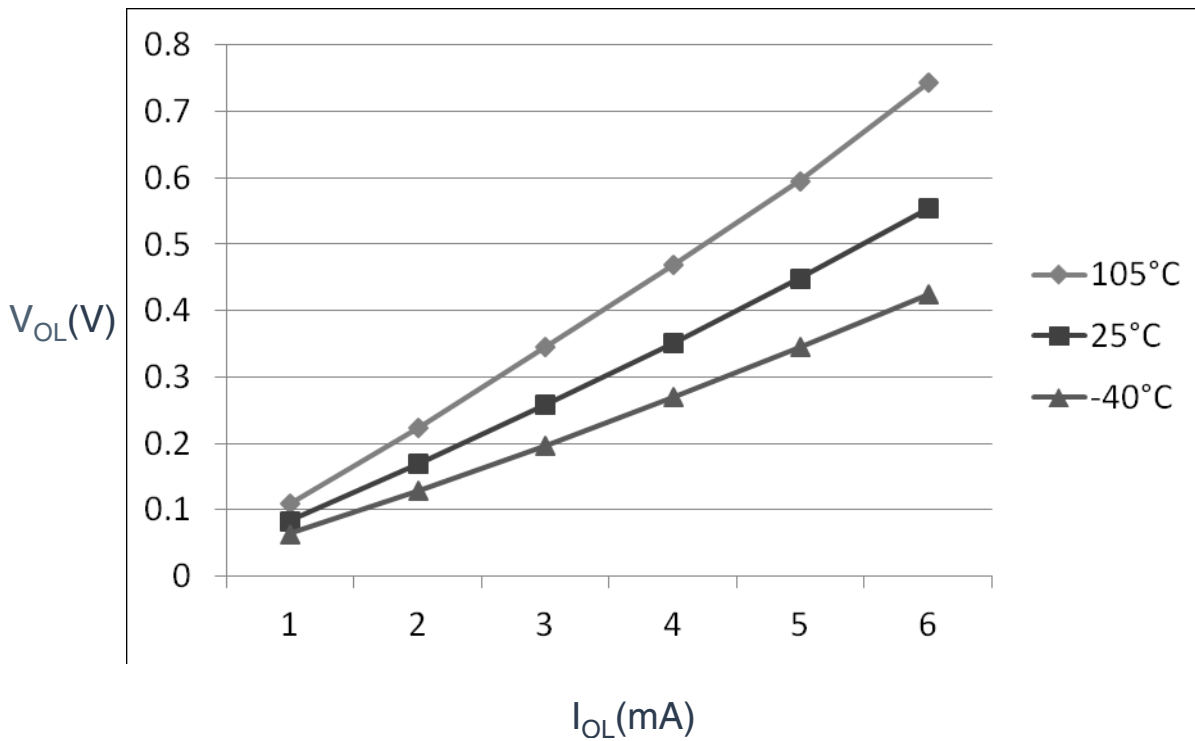


Figure 6. Typical  $I_{OL}$  Vs.  $V_{OL}$  (standard drive strength) ( $V_{DD} = 3\text{ V}$ )

Typical  $I_{OL}$  Vs.  $V_{OL}$ (high drive strength) ( $V_{DD} = 5\text{ V}$ )

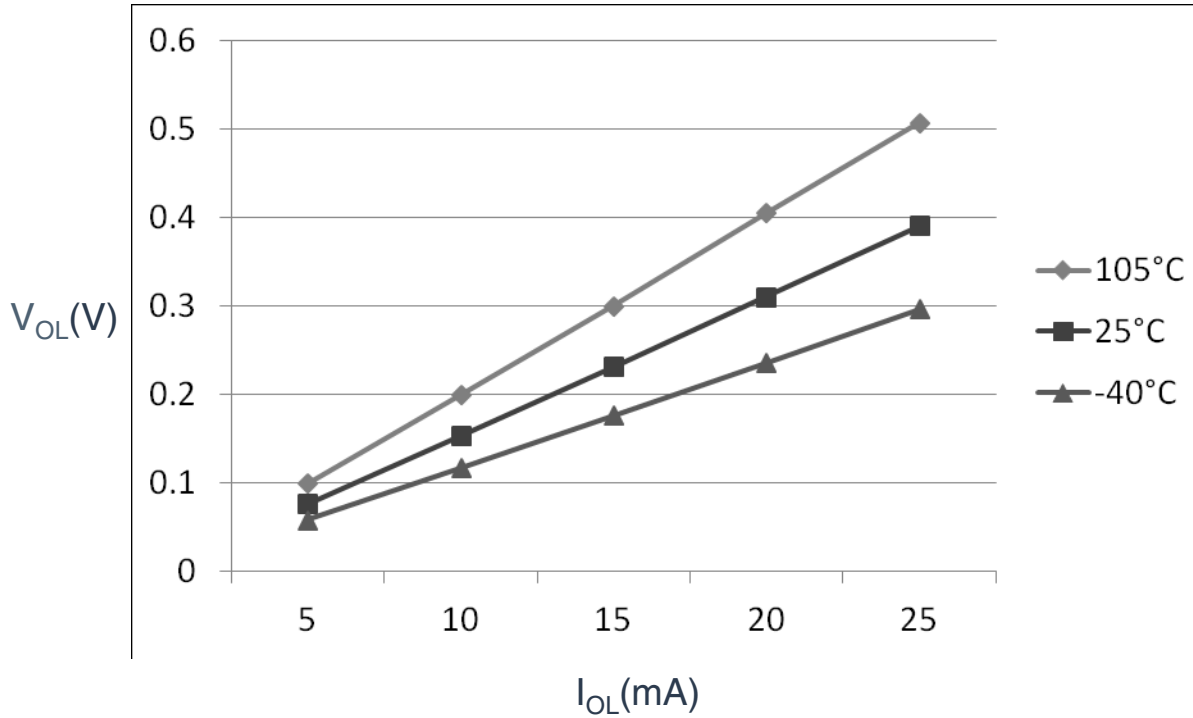


Figure 7. Typical  $I_{OL}$  Vs.  $V_{OL}$  (high drive strength) ( $V_{DD} = 5\text{ V}$ )

Typical  $I_{OL}$  Vs.  $V_{OL}$ (high drive strength) ( $V_{DD} = 3\text{ V}$ )

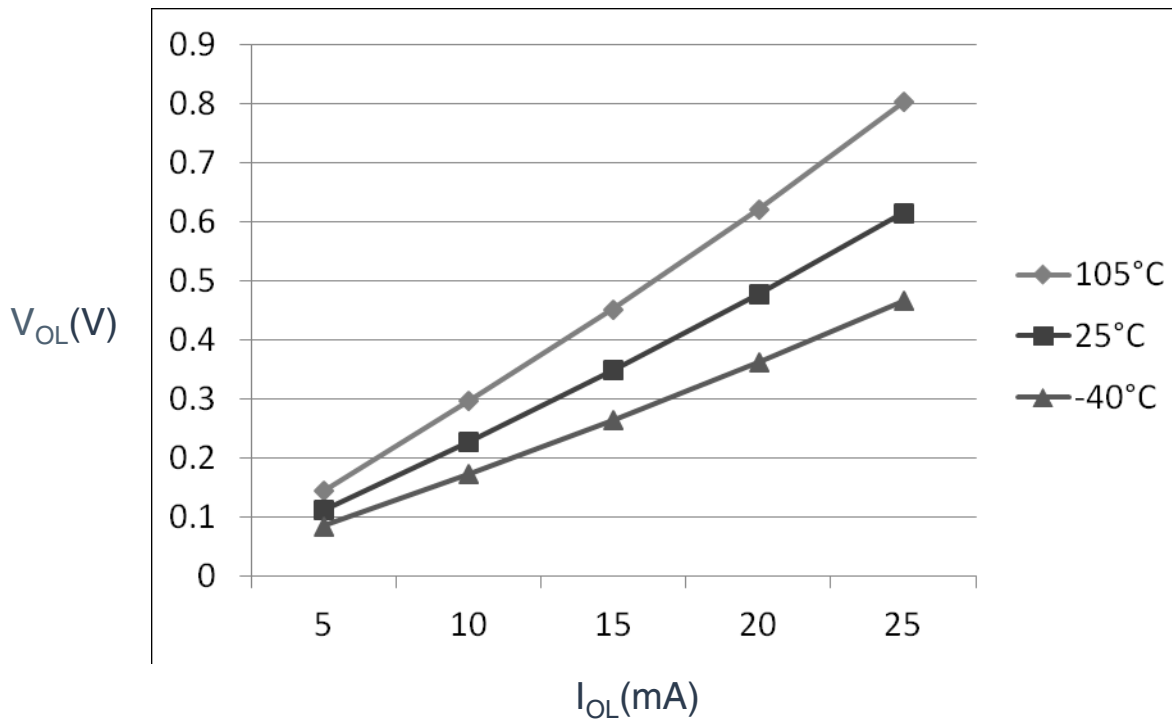


Figure 8. Typical  $I_{OL}$  Vs.  $V_{OL}$  (high drive strength) ( $V_{DD} = 3\text{ V}$ )

### 5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

**Table 5. Supply current characteristics**

C	Parameter	Symbol	Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	R <sub>I</sub> DD	20 MHz	5	6.7	—	mA	–40 to 105 °C
C			10 MHz		4.5	—		
C			1 MHz		1.5	—		
C			20 MHz	3	6.6	—		
C			10 MHz		4.4	—		
C			1 MHz		1.45	—		
C	Run supply current FEI mode, all modules clocks disabled; run from flash	R <sub>I</sub> DD	20 MHz	5	5.3	—	mA	–40 to 105 °C
C			10 MHz		3.7	—		
C			1 MHz		1.5	—		
C			20 MHz	3	5.3	—		
C			10 MHz		3.7	—		
C			1 MHz		1.4	—		
P	Run supply current FBE mode, all modules clocks enabled; run from RAM	R <sub>I</sub> DD	20 MHz	5	9	14.8	mA	–40 to 105 °C
C			10 MHz		5.2	—		
C			1 MHz		1.45	—		
P			20 MHz	3	8.8	11.8		
C			10 MHz		5.1	—		
C			1 MHz		1.4	—		
P	Run supply current FBE mode, all modules clocks disabled; run from RAM	R <sub>I</sub> DD	20 MHz	5	8	12.3	mA	–40 to 105 °C
C			10 MHz		4.4	—		
C			1 MHz		1.35	—		
P			20 MHz	3	7.8	9.2		
C			10 MHz		4.2	—		
C			1 MHz		1.3	—		
P	Wait mode current FEI mode, all modules clocks enabled	W <sub>I</sub> DD	20 MHz	5	5.5	—	mA	–40 to 105 °C
C			10 MHz		3.5	—		
C			1 MHz		1.4	—		
C			20 MHz	3	5.4	—		
C			10 MHz		3.4	—		
C			1 MHz		1.4	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock) <sup>2, 3</sup>	S <sub>I</sub> DD	—	5	2	85	µA	–40 to 105 °C
P			—	3	1.9	80		–40 to 105 °C
C	ADC adder to Stop ADLPC = 1	—	—	5	86 (64-, 44-pin packages)	—	µA	–40 to 105 °C

Table continues on the next page...

**Table 5. Supply current characteristics (continued)**

C	Parameter	Symbol	Bus Freq	V <sub>DD</sub> (V)	Typical <sup>1</sup>	Max	Unit	Temp
C	ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B				42 (32-pin package)			
				3	82 (64-, 44-pin packages) 41 (32-pin package)	—		
C	LVD adder to stop <sup>4</sup>	—	—	5	128	—	μA	-40 to 105 °C
C				3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder causes I<sub>DD</sub> to increase typically by less than 1 μA; RTC clock source is 1 kHz LPO clock.
3. ACMP adder causes I<sub>DD to</sub> increase typically by less than 1 μA.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

### 5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on [freescale.com](http://freescale.com) for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

## 5.2 Switching specifications

### 5.2.1 Control timing

Table 6. Control timing

Num	C	Rating	Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	P	Bus frequency ( $t_{cyc} = 1/f_{Bus}$ )	$f_{Bus}$	DC	—	20	MHz
2	P	Internal low power oscillator frequency	$f_{LPO}$	0.67	1.0	1.25	KHz
3	D	External reset pulse width	$t_{extrst}$	$1.5 \times t_{cyc}$	—	—	ns
4	D	Reset low drive	$t_{rstdrv}$	$34 \times t_{cyc}$	—	—	ns
5	D	IRQ pulse width	Asynchronous path <sup>2</sup>	$t_{LIH}$	100	—	ns
	D		Synchronous path	$t_{HIL}$	$1.5 \times t_{cyc}$	—	ns
6	D	Keyboard interrupt pulse width	Asynchronous path <sup>2</sup>	$t_{LIH}$	100	—	ns
	D		Synchronous path	$t_{HIL}$	$1.5 \times t_{cyc}$	—	ns
7	C	Port rise and fall time - Normal drive strength (load = 50 pF)	—	$t_{Rise}$	—	10.2	ns
	C		—	$t_{Fall}$	—	9.5	ns
	C	Port rise and fall time - high drive strength (load = 50 pF) <sup>3</sup>	—	$t_{Rise}$	—	5.4	ns
	C		—	$t_{Fall}$	—	4.6	ns

1. Typical values are based on characterization data at  $V_{DD} = 5.0\text{ V}$ ,  $25\text{ }^\circ\text{C}$  unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a RESET pin request.
3. Timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  levels. Temperature range  $-40\text{ }^\circ\text{C}$  to  $105\text{ }^\circ\text{C}$ .

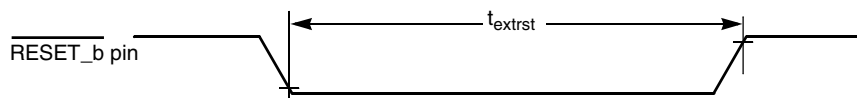


Figure 9. Reset timing

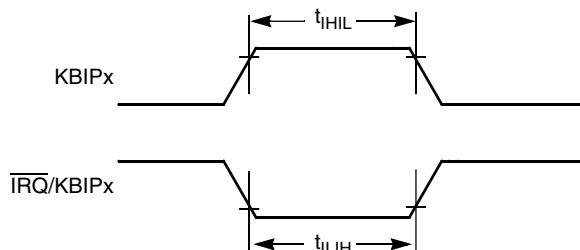


Figure 10. KBIPx timing

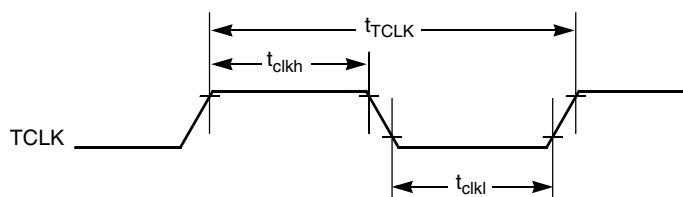


## 5.2.2 FTM module timing

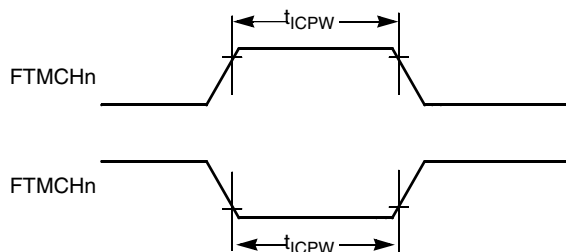
Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

**Table 7. FTM input timing**

No.	C	Function	Symbol	Min	Max	Unit
1	D	External clock frequency	$f_{TCLK}$	0	$f_{Bus}/4$	Hz
2	D	External clock period	$t_{TCLK}$	4	—	$t_{cyc}$
3	D	External clock high time	$t_{clkh}$	1.5	—	$t_{cyc}$
4	D	External clock low time	$t_{clkl}$	1.5	—	$t_{cyc}$
5	D	Input capture pulse width	$t_{iCPW}$	1.5	—	$t_{cyc}$



**Figure 11. Timer external clock**



**Figure 12. Timer input capture pulse**

## 5.3 Thermal specifications

### 5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take  $P_{I/O}$  into account in power calculations, determine the difference between actual pin voltage and  $V_{SS}$  or  $V_{DD}$  and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and  $V_{SS}$  or  $V_{DD}$  will be very small.

**Table 8. Thermal attributes**

Board type	Symbol	Description	64 LQFP	64 QFP	44 LQFP	32 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	61	75	86	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	47	53	57	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	50	62	72	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	41	47	51	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	32	34	33	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	23	20	24	°C/W	5
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	5	8	5	6	°C/W	6

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
- Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature ( $T_J$ ) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

$T_A$  = Ambient temperature, °C

$\theta_{JA}$  = Package thermal resistance, junction-to-ambient, °C/W

$$P_D = P_{int} + P_{I/O}$$

$P_{int} = I_{DD} \times V_{DD}$ , Watts - chip internal power

$P_{I/O}$  = Power dissipation on input and output pins - user determined

For most applications,  $P_{I/O} \ll P_{int}$  and can be neglected. An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is:

$$P_D = K \div (T_J + 273 \text{ °C})$$

Solving the equations above for K gives:

$$K = P_D \times (T_A + 273 \text{ °C}) + \theta_{JA} \times (P_D)^2$$

where K is a constant pertaining to the particular part. K can be determined by measuring  $P_D$  (at equilibrium) for an known  $T_A$ . Using this value of K, the values of  $P_D$  and  $T_J$  can be obtained by solving the above equations iteratively for any value of  $T_A$ .

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 SWD electricals

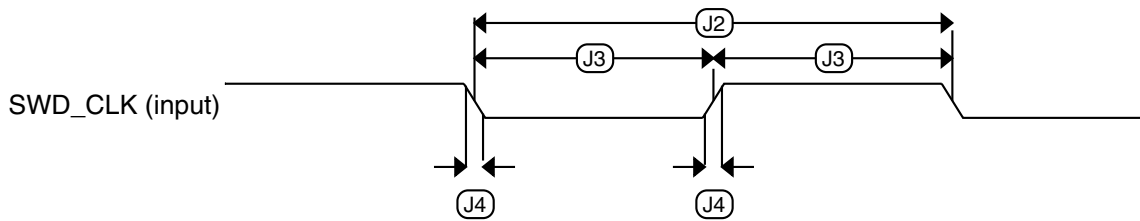
Table 9. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width	20	—	ns

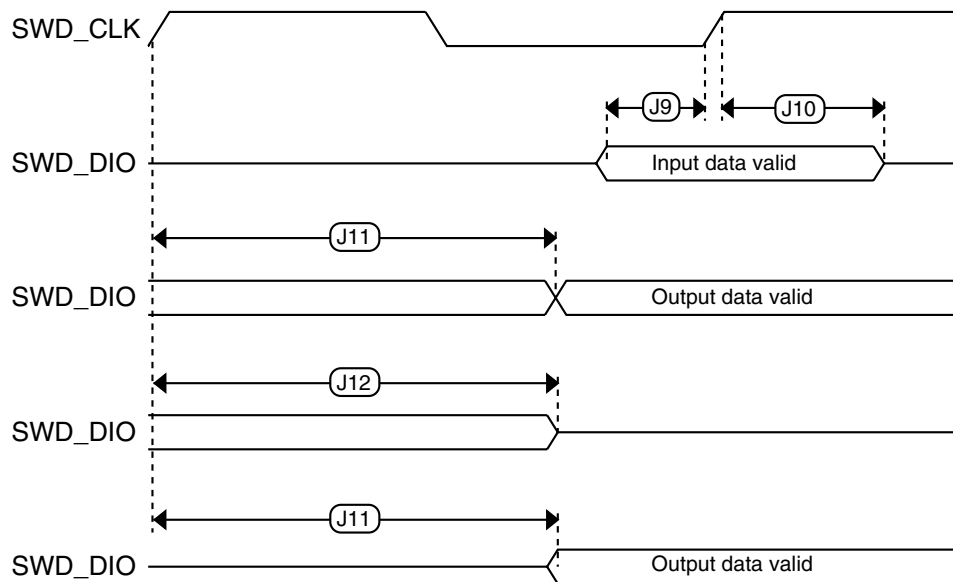
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**Table 9. SWD full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug			
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns



**Figure 13. Serial wire clock input timing**



**Figure 14. Serial wire data timing**

## 6.2 External oscillator (OSC) and ICS characteristics

Table 10. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)

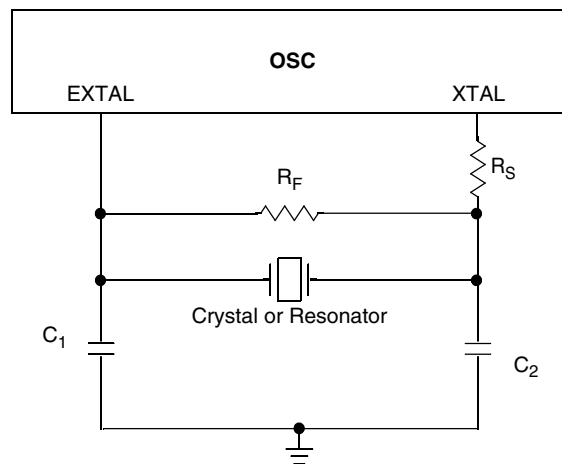
Num	C	Characteristic		Symbol	Min	Typical <sup>1</sup>	Max	Unit
1	C	Oscillator crystal or resonator	Low range (RANGE = 0)	$f_{lo}$	31.25	—	39.0625	kHz
	C		High range (RANGE = 1) FEE or FBE mode	$f_{hi}$	4	—	20	MHz
	C		High range (RANGE = 1), high gain (HGO = 1), FBELP mode	$f_{hi}$	4	—	20	MHz
	C		High range (RANGE = 1), low power (HGO = 0), FBELP mode	$f_{hi}$	4	—	20	MHz
2	D	Load capacitors		C1, C2	See Note <sup>3</sup>			
3	D	Feedback resistor	Low Frequency, Low-Power Mode	$R_F$	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode <sup>4</sup>	$R_S$	—	—	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode <sup>4</sup>	$R_S$	—	—	—	kΩ
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 31.25 kHz crystal; High range = 20 MHz crystal, <sup>6</sup>	Low range, low power	$t_{CSTL}$	—	1000	—	ms
	C		Low range, high power		—	800	—	ms
	C		High range, low power	$t_{CSTH}$	—	3	—	ms
	C		High range, high power		—	1.5	—	ms
7	T	Internal reference start-up time		$t_{IRST}$	—	20	50	μs
8	D	Square wave input clock frequency	FEE or FBE mode <sup>2</sup>	$f_{extal}$	0.03125	—	5	MHz
	D		FBELP mode		0	—	20	MHz
9	P	Average target internal reference frequency - trimmed		$f_{int\_t}$	—	31.25	—	kHz
10	P	DCO output frequency range - trimmed		$f_{dco\_t}$	16	—	20	MHz
11	P	Total deviation of DCO output from trimmed frequency <sup>5</sup>	Over full voltage and temperature range	$\Delta f_{dco\_t}$	—	—	±2.0	% $f_{dco}$
	C						±1.5	
	C		Over fixed voltage and temperature range of 0 to 70 °C				±1.0	
12	C	FLL acquisition time <sup>5, 7</sup>		$t_{Acquire}$	—	—	2	ms

Table continues on the next page...

**Table 10. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)  
(continued)**

Num	C	Characteristic	Symbol	Min	Typical <sup>1</sup>	Max	Unit
13	C	Long term jitter of DCO output clock (averaged over 2 ms interval) <sup>8</sup>	$C_{\text{Jitter}}$	—	0.02	0.2	% $f_{\text{dco}}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. When ICS is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.
3. See crystal or resonator manufacturer's recommendation.
4. Load capacitors ( $C_1, C_2$ ), feedback resistor ( $R_F$ ) and series resistor ( $R_S$ ) are incorporated internally when RANGE = HGO = 0.
5. This parameter is characterized and not tested on each device.
6. Proper PC board layout procedures must be followed to achieve specifications.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{\text{BUS}}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via  $V_{\text{DD}}$  and  $V_{\text{SS}}$  and variation in crystal oscillator frequency increase the  $C_{\text{Jitter}}$  percentage for a given interval.

**Figure 15. Typical crystal or resonator circuit**

## 6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

**Table 11. Flash and EEPROM characteristics**

C	Characteristic	Symbol	Min <sup>1</sup>	Typical <sup>2</sup>	Max <sup>3</sup>	Unit <sup>4</sup>
D	Supply voltage for program/erase -40 °C to 105 °C	$V_{\text{prog/erase}}$	2.7	—	5.5	V
D	Supply voltage for read operation	$V_{\text{Read}}$	2.7	—	5.5	V

Table continues on the next page...

**Table 11. Flash and EEPROM characteristics  
(continued)**

C	Characteristic	Symbol	Min <sup>1</sup>	Typical <sup>2</sup>	Max <sup>3</sup>	Unit <sup>4</sup>
D	NVM Bus frequency	f <sub>NVMBUS</sub>	1	—	25	MHz
D	NVM Operating frequency	f <sub>NVMOP</sub>	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t <sub>VFYALL</sub>	—	—	17338	t <sub>cyc</sub>
D	Erase Verify Flash Block	t <sub>RD1BLK</sub>	—	—	16913	t <sub>cyc</sub>
D	Erase Verify EEPROM Block	t <sub>RD1BLK</sub>	—	—	810	t <sub>cyc</sub>
D	Erase Verify Flash Section	t <sub>RD1SEC</sub>	—	—	484	t <sub>cyc</sub>
D	Erase Verify EEPROM Section	t <sub>DRD1SEC</sub>	—	—	555	t <sub>cyc</sub>
D	Read Once	t <sub>RDONCE</sub>	—	—	450	t <sub>cyc</sub>
D	Program Flash (2 word)	t <sub>PGM2</sub>	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t <sub>PGM4</sub>	0.20	0.21	0.46	ms
D	Program Once	t <sub>PGMONCE</sub>	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t <sub>DPGM1</sub>	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t <sub>DPGM2</sub>	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t <sub>DPGM3</sub>	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t <sub>DPGM4</sub>	0.32	0.33	0.77	ms
D	Erase All Blocks	t <sub>ERSALL</sub>	96.01	100.78	101.49	ms
D	Erase Flash Block	t <sub>ERSBLK</sub>	95.98	100.75	101.44	ms
D	Erase Flash Sector	t <sub>ERSPG</sub>	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t <sub>DERSPG</sub>	4.81	5.05	20.57	ms
D	Unsecure Flash	t <sub>UNSECU</sub>	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t <sub>VFYKEY</sub>	—	—	464	t <sub>cyc</sub>
D	Set User Margin Level	t <sub>MLOADU</sub>	—	—	407	t <sub>cyc</sub>
C	FLASH Program/erase endurance T <sub>L</sub> to T <sub>H</sub> = -40 °C to 105 °C	n <sub>FLPE</sub>	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C	n <sub>FLPE</sub>	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T <sub>Javg</sub> = 85°C after up to 10,000 program/erase cycles	t <sub>D_ret</sub>	15	100	—	years

1. Minimum times are based on maximum f<sub>NVMOP</sub> and maximum f<sub>NVMBUS</sub>
2. Typical times are based on typical f<sub>NVMOP</sub> and maximum f<sub>NVMBUS</sub>
3. Maximum times are based on typical f<sub>NVMOP</sub> and typical f<sub>NVMBUS</sub> plus aging
4. t<sub>cyc</sub> = 1 / f<sub>NVMBUS</sub>

Program and erase operations do not require any special power sources other than the normal V<sub>DD</sub> supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

## 6.4 Analog

### 6.4.1 ADC characteristics

Table 12. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symb	Min	Typ <sup>1</sup>	Max	Unit	Comment
Supply voltage	Absolute	$V_{DDA}$	2.7	—	5.5	V	—
	Delta to $V_{DD}$ ( $V_{DD}-V_{DDAD}$ )	$\Delta V_{DDA}$	-100	0	+100	mV	
Ground voltage	Delta to $V_{SS}$ ( $V_{SS}-V_{SSA}$ ) <sup>1</sup>	$\Delta V_{SSA}$	-100	0	+100	mV	
Input voltage		$V_{ADIN}$	$V_{REFL}$	—	$V_{REFH}$	V	
Input capacitance		$C_{ADIN}$	—	4.5	5.5	pF	
Input resistance		$R_{ADIN}$	—	3	5	k $\Omega$	—
Analog source resistance	12-bit mode	$R_{AS}$	—	—	2	k $\Omega$	External to MCU
	• $f_{ADCK} > 4$ MHz		—	—	5		
	• $f_{ADCK} < 4$ MHz		—	—	5		
10-bit mode	—	—	5	k $\Omega$	External to MCU		
• $f_{ADCK} > 4$ MHz	—	—	10				
• $f_{ADCK} < 4$ MHz	—	—	10				
8-bit mode (all valid $f_{ADCK}$ )			—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	$f_{ADCK}$	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25°C,  $f_{ADCK}=1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

1. DC potential difference.



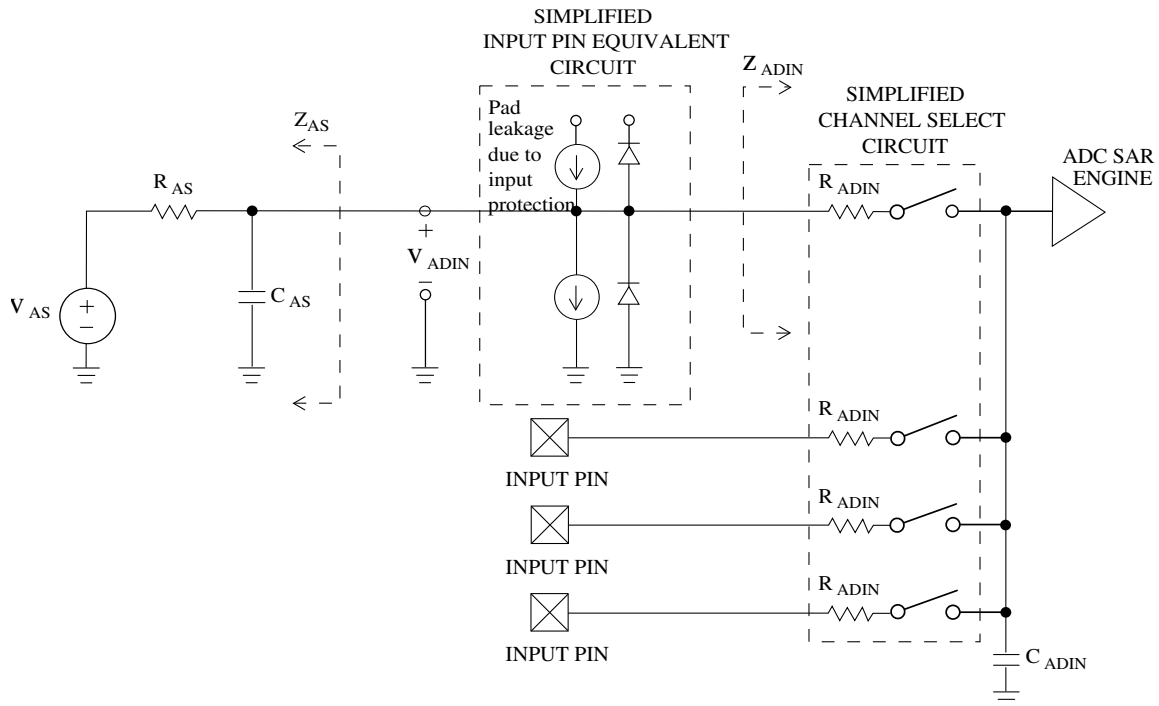


Figure 16. ADC input impedance equivalency diagram

Table 13. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	133	—	$\mu\text{A}$
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	$I_{DDA}$	—	218	—	$\mu\text{A}$
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	$I_{DDA}$	—	327	—	$\mu\text{A}$
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	$I_{DDAD}$	—	582	990	$\mu\text{A}$
Supply current	Stop, reset, module off	T	$I_{DDA}$	—	0.011	1	$\mu\text{A}$
ADC asynchronous clock source	High speed (ADLPC = 0)	P	$f_{ADACK}$	2	3.3	5	MHz

Table continues on the next page...

**Table 13. 12-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Characteristic	Conditions	C	Symb	Min	Typ <sup>1</sup>	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	$t_{ADC}$	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	$t_{ADS}$	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error	12-bit mode	T	$E_{TUE}$	—	$\pm 5.0$	—	LSB
	10-bit mode	P		—	$\pm 1.5$	$\pm 2.0$	
	8-bit mode	P		—	$\pm 0.7$	$\pm 1.0$	
Differential Non-Linearity	12-bit mode	T	DNL	—	$\pm 1.0$	—	LSB <sup>2</sup>
	10-bit mode	P		—	$\pm 0.25$	$\pm 0.5$	
	8-bit mode <sup>3</sup>	P		—	$\pm 0.15$	$\pm 0.25$	
Integral Non-Linearity	12-bit mode	T	INL	—	$\pm 1.0$	—	LSB <sup>2</sup>
	10-bit mode	T		—	$\pm 0.3$	$\pm 0.5$	
	8-bit mode	T		—	$\pm 0.15$	$\pm 0.25$	
Zero-scale error	12-bit mode	C	$E_{ZS}$	—	$\pm 2.0$	—	LSB <sup>2</sup>
	10-bit mode	P		—	$\pm 0.25$	$\pm 1.0$	
	8-bit mode	P		—	$\pm 0.65$	$\pm 1.0$	
Full-scale error <sup>6</sup>	12-bit mode	T	$E_{FS}$	—	$\pm 2.5$	—	LSB <sup>2</sup>
	10-bit mode	T		—	$\pm 0.5$	$\pm 1.0$	
	8-bit mode	T		—	$\pm 0.5$	$\pm 1.0$	
Quantization error	$\leq 12$ bit modes	D	$E_Q$	—	—	$\pm 0.5$	LSB <sup>2</sup>
Input leakage error <sup>7</sup>	all modes	D	$E_{IL}$	$I_{in} * R_{AS}$			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	$V_{TEMP25}$	—	1.396	—	V

1. Typical values assume  $V_{DDA} = 5.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$

3. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes

4.  $V_{ADIN} = V_{DDA}$

5.  $I_{in}$  = leakage current (refer to DC characteristics)

## 6.4.2 Analog comparator (ACMP) electricals

Table 14. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	$V_{DDA}$	2.7	—	5.5	V
T	Supply current (Operation mode)	$I_{DDA}$	—	10	20	$\mu\text{A}$
D	Analog input voltage	$V_{AIN}$	$V_{SS} - 0.3$	—	$V_{DDA}$	V
P	Analog input offset voltage	$V_{AIO}$	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	$V_H$	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	$V_H$	—	20	30	mV
T	Supply current (Off mode)	$I_{DDA\text{OFF}}$	—	60	—	nA
C	Propagation Delay	$t_D$	—	0.4	1	$\mu\text{s}$

## 6.5 Communication interfaces

### 6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20%  $V_{DD}$  and 70%  $V_{DD}$ , unless noted, and 100 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

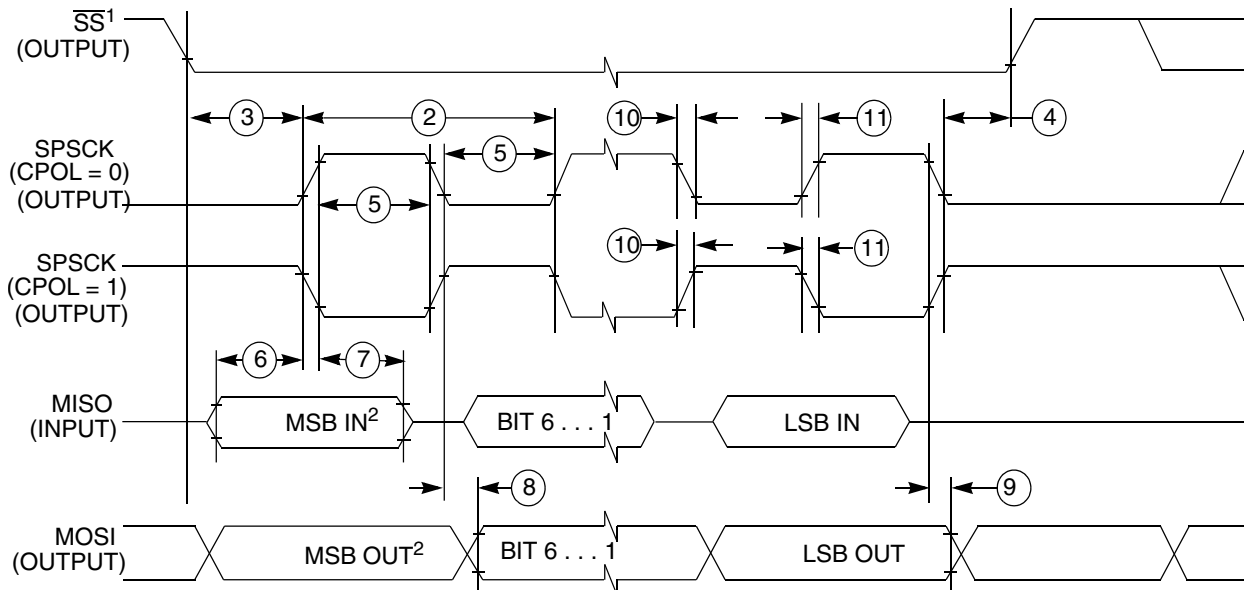
Table 15. SPI master mode timing

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	$f_{op}$	Frequency of operation	$f_{Bus}/2048$	$f_{Bus}/2$	Hz	$f_{Bus}$ is the bus clock
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{Bus}$	$2048 \times t_{Bus}$	ns	$t_{Bus} = 1/f_{Bus}$
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{Bus} - 30$	$1024 \times t_{Bus}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	15	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	25	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{Bus} - 25$	ns	—

Table continues on the next page...

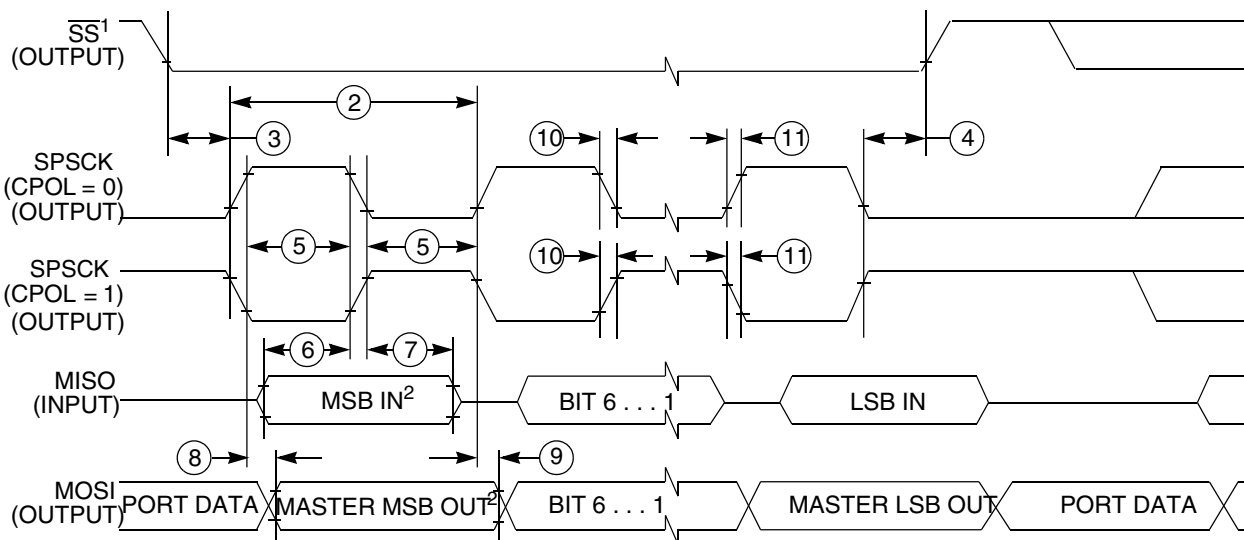
**Table 15. SPI master mode timing (continued)**

Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				



- 1. If configured as an output.
- 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 17. SPI master mode timing (CPHA=0)**

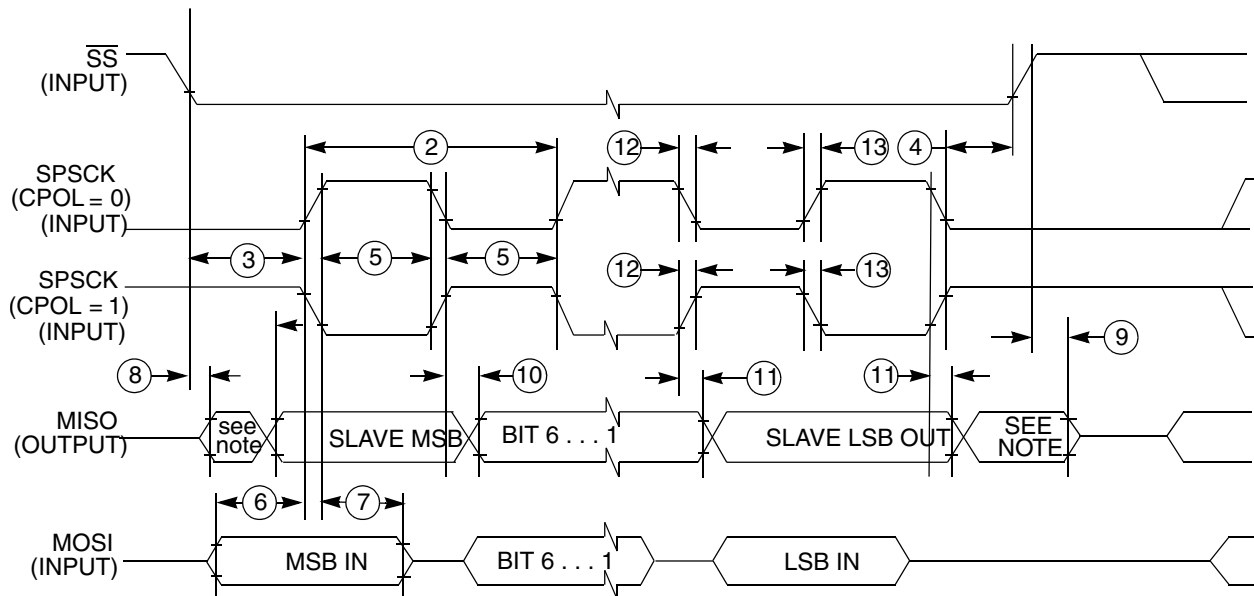


- 1. If configured as output
- 2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 18. SPI master mode timing (CPHA=1)**

Table 16. SPI slave mode timing

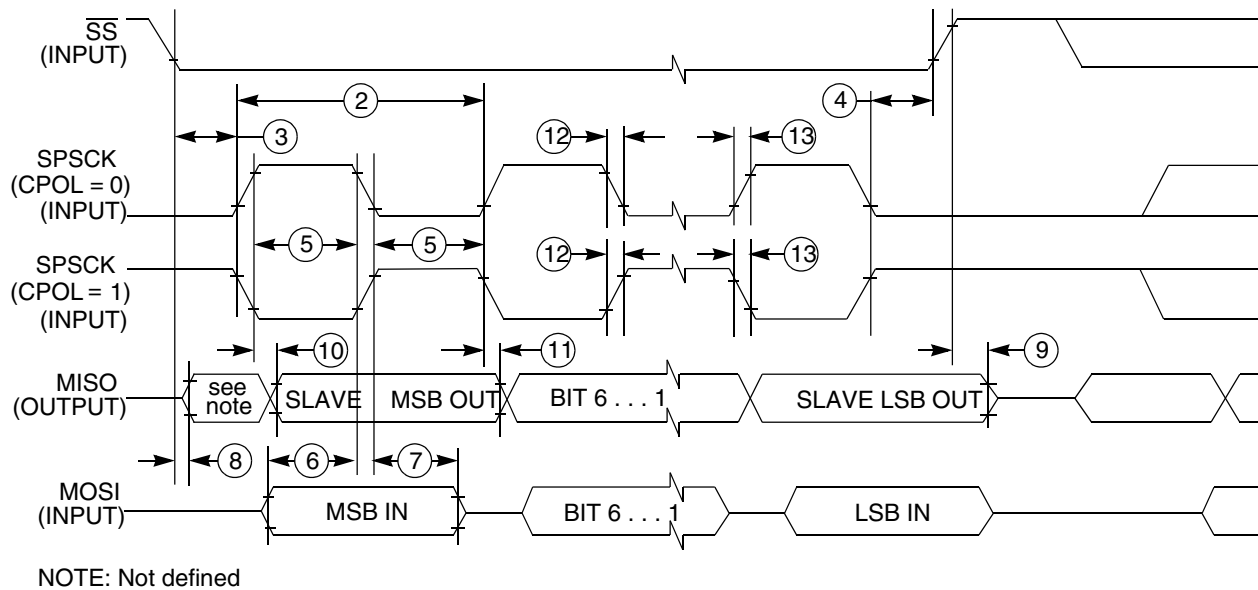
Nu m.	Symbol	Description	Min.	Max.	Unit	Comment
1	$f_{op}$	Frequency of operation	0	$f_{BUS}/4$	Hz	$f_{BUS}$ is the bus clock as defined in .
2	$t_{SPSCK}$	SPSCK period	$4 \times t_{BUS}$	—	ns	$t_{BUS} = 1/f_{BUS}$
3	$t_{Lead}$	Enable lead time	1	—	$t_{BUS}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{BUS}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{BUS} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	15	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	25	—	ns	—
8	$t_a$	Slave access time	—	$t_{BUS}$	ns	Time to data active from high-impedance state
9	$t_{dis}$	Slave MISO disable time	—	$t_{BUS}$	ns	Hold time to high-impedance state
10	$t_v$	Data valid (after SPSCK edge)	—	25	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{BUS} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				



NOTE: Not defined

Figure 19. SPI slave mode timing (CPHA = 0)

## Dimensions



**Figure 20. SPI slave mode timing (CPHA=1)**

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W

## 8 Pinout

### 8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

**Table 17. Pin availability by package pin-count**

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD1 <sup>1</sup>	KBI1_P1	FTM2_CH3	SPI1_MOSI	—
2	2	2	PTD0 <sup>1</sup>	KBI1_P0	FTM2_CH2	SPI1_SCK	—
3	—	—	PTH7	—	—	—	—
4	—	—	PTH6	—	—	—	—
5	3	—	PTE7	—	FTM2_CLK	—	FTM1_CH1
6	4	—	PTH2	—	BUSOUT	—	FTM1_CH0
7	5	3	—	—	—	—	VDD
8	6	4	—	—	—	VDDA	VREFH <sup>2</sup>
9	7	5	—	—	—	—	VREFL
10	8	6	—	—	—	VSSA	VSS <sup>3</sup>
11	9	7	PTB7	—	I2C0_SCL	—	EXTAL
12	10	8	PTB6	—	I2C0_SDA	—	XTAL
13	11	—	—	—	—	—	VSS
14	—	—	PTH1 <sup>1</sup>	—	FTM2_CH1	—	—
15	—	—	PTH0 <sup>1</sup>	—	FTM2_CH0	—	—
16	—	—	PTE6	—	—	—	—
17	—	—	PTE5	—	—	—	—
18	12	9	PTB5 <sup>1</sup>	FTM2_CH5	SPI0_PCS0	ACMP1_OUT	—
19	13	10	PTB4 <sup>1</sup>	FTM2_CH4	SPI0_MISO	NMI	ACMP1_IN2
20	14	11	PTC3	FTM2_CH3	—	—	ADC0_SE11
21	15	12	PTC2	FTM2_CH2	—	—	ADC0_SE10
22	16	—	PTD7	KBI1_P7	UART2_TX	—	—
23	17	—	PTD6	KBI1_P6	UART2_RX	—	—
24	18	—	PTD5	KBI1_P5	—	—	—
25	19	13	PTC1	—	FTM2_CH1	—	ADC0_SE9
26	20	14	PTC0	—	FTM2_CH0	—	ADC0_SE8
27	—	—	PTF7	—	—	—	ADC0_SE15

Table continues on the next page...

Table 17. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
28	—	—	PTF6	—	—	—	ADC0_SE14
29	—	—	PTF5	—	—	—	ADC0_SE13
30	—	—	PTF4	—	—	—	ADC0_SE12
31	21	15	PTB3	KBI0_P7	SPI0_MOSI	FTM0_CH1	ADC0_SE7
32	22	16	PTB2	KBI0_P6	SPI0_SCK	FTM0_CH0	ADC0_SE6
33	23	17	PTB1	KBI0_P5	UART0_TX	—	ADC0_SE5
34	24	18	PTB0	KBI0_P4	UART0_RX	—	ADC0_SE4
35	—	—	PTF3	—	—	—	—
36	—	—	PTF2	—	—	—	—
37	25	19	PTA7	—	FTM2_FLT2	ACMP1_IN1	ADC0_SE3
38	26	20	PTA6	—	FTM2_FLT1	ACMP1_IN0	ADC0_SE2
39	—	—	PTE4	—	—	—	—
40	27	—	—	—	—	—	VSS
41	28	—	—	—	—	—	VDD
42	—	—	PTF1	—	—	—	—
43	—	—	PTF0	—	—	—	—
44	29	—	PTD4	KBI1_P4	—	—	—
45	30	21	PTD3	KBI1_P3	SPI1_PCS0	—	—
46	31	22	PTD2	KBI1_P2	SPI1_MISO	—	—
47	32	23	PTA3 <sup>4</sup>	KBI0_P3	UART0_TX	I2C0_SCL	—
48	33	24	PTA2 <sup>4</sup>	KBI0_P2	UART0_RX	I2C0_SDA	—
49	34	25	PTA1	KBI0_P1	FTM0_CH1	ACMP0_IN1	ADC0_SE1
50	35	26	PTA0	KBI0_P0	FTM0_CH0	ACMP0_IN0	ADC0_SE0
51	36	27	PTC7	—	UART1_TX	—	—
52	37	28	PTC6	—	UART1_RX	—	—
53	—	—	PTE3	—	SPI0_PCS0	—	—
54	38	—	PTE2	—	SPI0_MISO	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—
57	—	—	PTG1	—	—	—	—
58	—	—	PTG0	—	—	—	—
59	39	—	PTE1 <sup>1</sup>	—	SPI0_MOSI	—	—
60	40	—	PTE0 <sup>1</sup>	—	SPI0_SCK	FTM1_CLK	—
61	41	29	PTC5	—	FTM1_CH1	—	RTCO
62	42	30	PTC4	RTCO	FTM1_CH0	ACMP0_IN2	SWD_CLK
63	43	31	PTA5	IRQ	FTM0_CLK	—	RESET
64	44	32	PTA4	—	ACMP0_OUT	—	SWD_DIO

1. This is a high-current drive pin when operated as output.

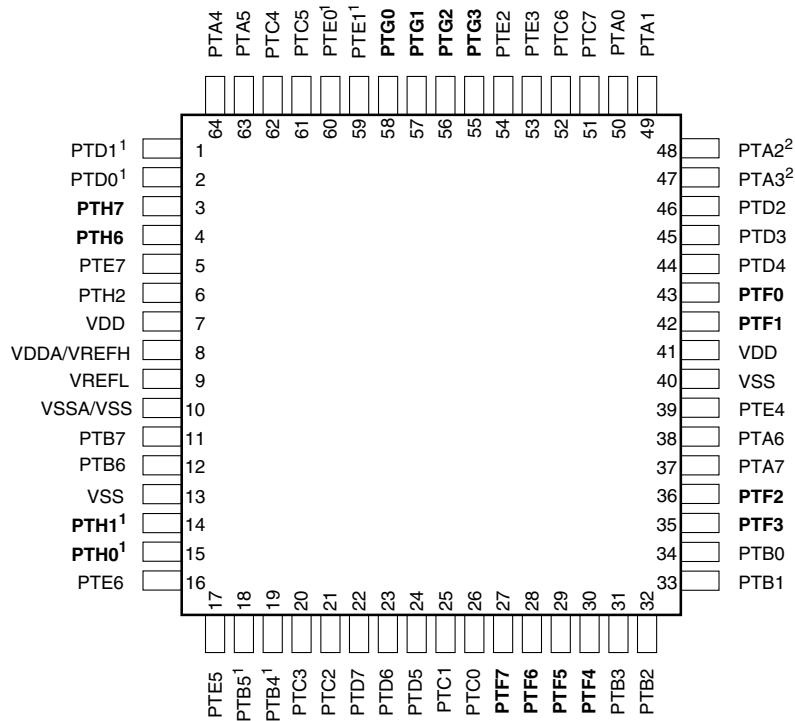


2. VREFH and VDDA are internally connected.
3. VSSA and VSS are internally connected.
4. This is a true open-drain pin when operated as output.

### Note

When an alternative function is first enabled, it is possible to get a spurious edge to the module. User software must clear any associated flags before interrupts are enabled. [Table 17](#) illustrates the priority if multiple modules are enabled. The highest priority module will have control over the pin. Selecting a higher priority pin function with a lower priority function already enabled can cause spurious edges to the lower priority module. Disable all modules that share a pin before enabling another module.

## 8.2 Device pin assignment

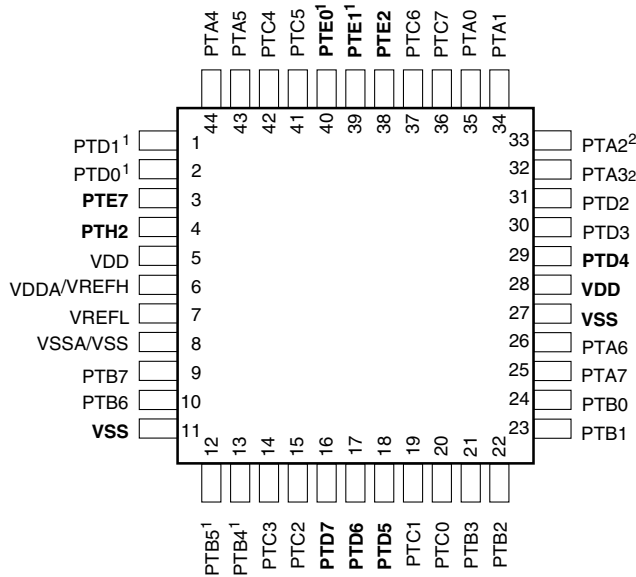


Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins

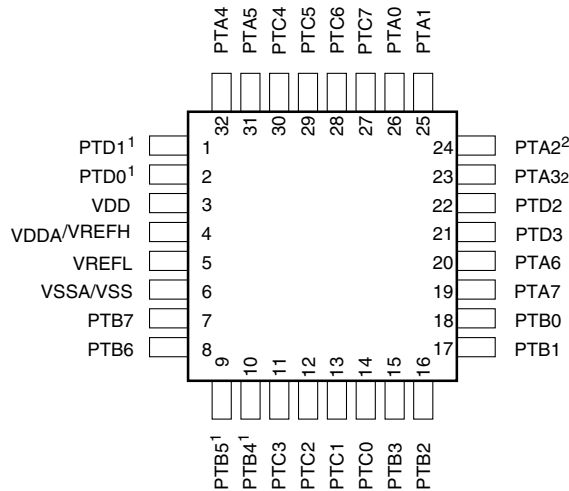
2. True open drain pins

**Figure 21. 64-pin QFP/LQFP packages**



Pins in **bold** are not available on less pin-count packages.  
 1. High source/sink current pins  
 2. True open drain pins

**Figure 22. 44-pin LQFP package**



1. High source/sink current pins  
 2. True open drain pins

**Figure 23. 32-pin LQFP package**

## 9 Revision history

The following table provides a revision history for this document.

**Table 18. Revision history**

<b>Rev. No.</b>	<b>Date</b>	<b>Substantial Changes</b>
3	07/2013	Initial public release.

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