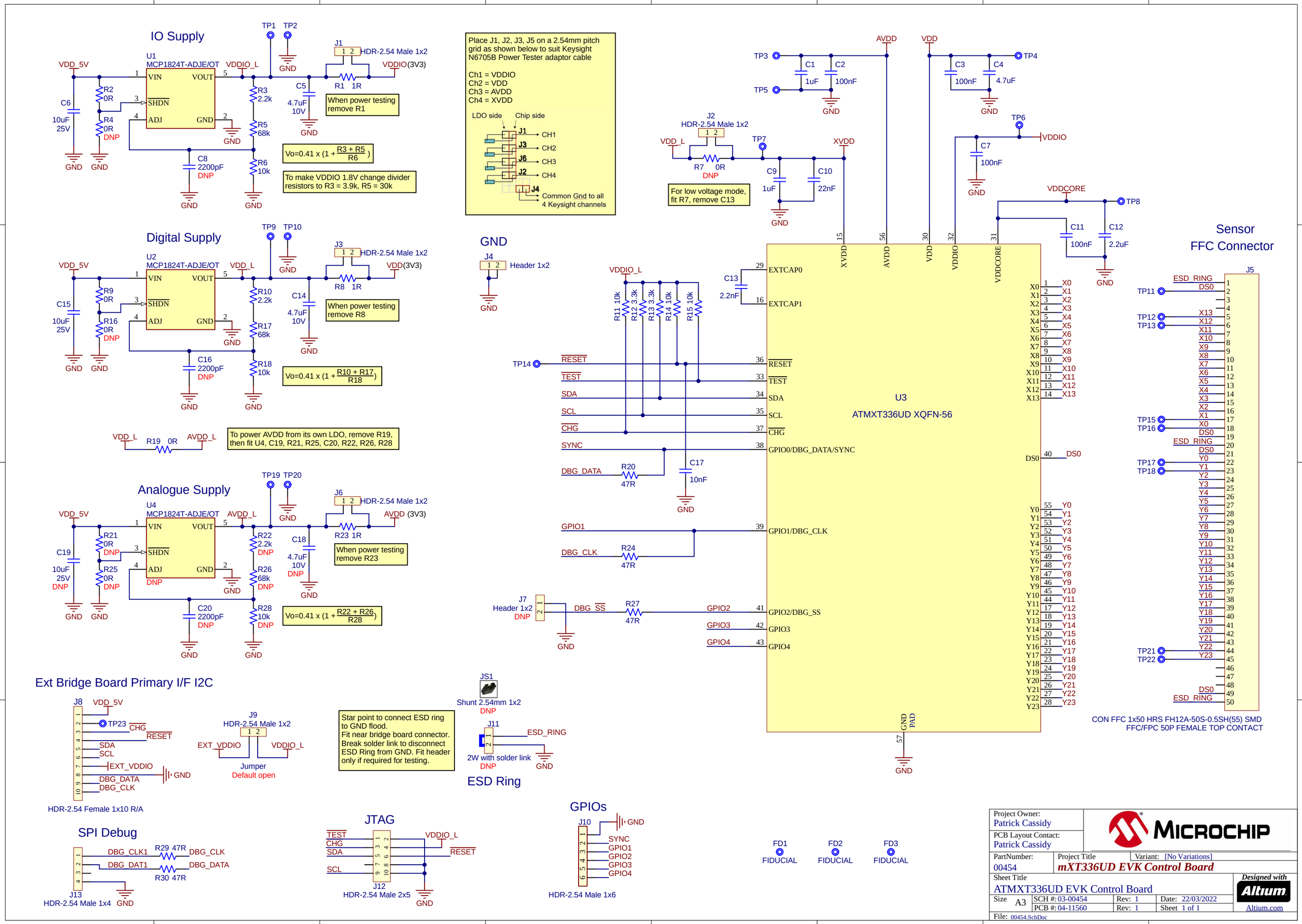
IO Supply
U1
MCP1824T-ADJE/OT
VDD_5V
VDDIO_L
VIN
VOUT
SHDN
ADJ
GND
TP1
TP2
J1
HDR-2.54 Male 1x2
VDDIO(3V3)
R1 1R
When power testing remove R1
C5
4.7uF
10V
R2 0R
R4 0R DNP
C6
10uF
25V
R3 2.2k
R5 68k
R6 10k
C8
2200pF
DNP
Vo=0.41 x (1 + (R3 + R5)/R6)
To make VDDIO 1.8V change divider resistors to R3 = 3.9k, R5 = 30k
Digital Supply
U2
MCP1824T-ADJE/OT
VDD_5V
VDD_L
TP9
TP10
J3
HDR-2.54 Male 1x2
VDD(3V3)
R8 1R
When power testing remove R8
C14
4.7uF
10V
R9 0R
R16 0R DNP
C15
10uF
25V
R10 2.2k
R17 68k
R18 10k
C16
2200pF
DNP
Vo=0.41 x (1 + (R10 + R17)/R18)
VDD_L
R19 0R
AVDD_L
To power AVDD from its own LDO, remove R19, then fit U4, C19, R21, R25, C20, R22, R26, R28
Analogue Supply
U4
MCP1824T-ADJE/OT
VDD_5V
AVDD_L
TP19
TP20
J6
HDR-2.54 Male 1x2
AVDD (3V3)
R23 1R
When power testing remove R23
C18
4.7uF
10V
DNP
R21 0R DNP
R25 0R DNP
C19
10uF
25V
DNP
R22 2.2k DNP
R26 68k DNP
R28 10k DNP
C20
2200pF
DNP
Vo=0.41 x (1 + (R22 + R26)/R28)
Place J1, J2, J3, J5 on a 2.54mm pitch grid as shown below to suit Keysight N6705B Power Tester adaptor cable
Ch1 = VDDIO
Ch2 = VDD
Ch3 = AVDD
Ch4 = XVDD
LDO side
Chip side
J1
J3
J6
J2
J4
CH1
CH2
CH3
CH4
Common Gnd to all 4 Keysight channels
GND
J4
Header 1x2
TP3
TP5
C1 1uF
C2 100nF
AVDD
VDD
C3 100nF
C4 4.7uF
TP4
J2
HDR-2.54 Male 1x2
VDD_L
R7 0R
DNP
TP7
C9 1uF
C10 22nF
XVDD
For low voltage mode, fit R7, remove C13
TP6
VDDIO
C7 100nF
VDDCORE
TP8
C11 100nF
C12 2.2uF
C13 2.2nF
EXTCAP0
EXTCAP1
RESET
TEST
SDA
SCL
CHG
SYNC
DBG_DATA
R20 47R
C17 10nF
GPIO1
DBG_CLK
R24 47R
J7
Header 1x2
DNP
DBG_SS
R27 47R
GPIO2
GPIO3
GPIO4
GPIO1/DBG_CLK
GPIO2/DBG_SS
GPIO0/DBG_DATA/SYNC
U3
ATMXT336UD XQFN-56
R11 10k
R12 3.3k
R13 3.3k
R14 10k
R15 10k
TP14
Sensor FFC Connector
J5
ESD_RING
DS0
TP11
TP12
TP13
TP15
TP16
TP17
TP18
TP21
TP22
CON FFC 1x50 HRS FH12A-50S-0.5SH(55) SMD
FFC/FPC 50P FEMALE TOP CONTACT
Ext Bridge Board Primary I/F I2C
J8
VDD_5V
TP23
CHG
RESET
SDA
SCL
EXT_VDDIO
DBG_DATA
DBG_CLK
HDR-2.54 Female 1x10 R/A
J9
HDR-2.54 Male 1x2
EXT_VDDIO
VDDIO_L
Jumper
Default open
Star point to connect ESD ring to GND flood.
Fit near bridge board connector.
Break solder link to disconnect ESD Ring from GND. Fit header only if required for testing.
JS1
Shunt 2.54mm 1x2
DNP
J11
ESD_RING
2W with solder link
DNP
ESD Ring
SPI Debug
J13
HDR-2.54 Male 1x4
DBG_CLK1
DBG_DAT1
R29 47R
R30 47R
DBG_CLK
DBG_DATA
JTAG
J12
HDR-2.54 Male 2x5
TEST
CHG
SDA
SCL
VDDIO_L
RESET
GPIOs
J10
HDR-2.54 Male 1x6
SYNC
GPIO1
GPIO2
GPIO3
GPIO4
FD1
FD2
FD3
FIDUCIAL
Project Owner:
Patrick Cassidy
PCB Layout Contact:
Patrick Cassidy
MICROCHIP
PartNumber:
00454
Project Title
mXT336UD EVK Control Board
Variant: [No Variations]
Sheet Title
ATMXT336UD EVK Control Board
Size A3
SCH #: 03-00454
PCB #: 04-11560
Rev: 1
Date: 22/03/2022
Sheet 1 of 1
File: 00454.SchDoc
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