

FEATURES

Very high dc precision

- 30 μV maximum offset voltage
- 0.3 $\mu\text{V}/^\circ\text{C}$ maximum offset voltage drift
- 0.35 μV p-p maximum voltage noise (0.1 Hz to 10 Hz)
- 5 million V/V minimum open-loop gain
- 130 dB minimum CMRR
- 120 dB minimum PSRR

Matching characteristics

- 30 μV maximum offset voltage match
- 0.3 $\mu\text{V}/^\circ\text{C}$ maximum offset voltage drift match
- 130 dB minimum CMRR match

Available in 8-lead narrow body, PDIP, and

hermetic CERDIP and CERDIP/883B packages

GENERAL DESCRIPTION

The AD708 is a high precision, dual monolithic operational amplifier. Each amplifier individually offers excellent dc precision with maximum offset voltage and offset voltage drift of any dual bipolar op amp.

The matching specifications are among the best available in any dual op amp. In addition, the AD708 provides 5 V/ μV minimum open-loop gain and guaranteed maximum input voltage noise of 350 nV p-p (0.1 Hz to 10 Hz). All dc specifications show excellent stability over temperature, with offset voltage drift typically 0.1 $\mu\text{V}/^\circ\text{C}$ and input bias current drift of 25 pA/ $^\circ\text{C}$ maximum.

The AD708 is available in four performance grades. The AD708J is rated over the commercial temperature range of 0 $^\circ\text{C}$ to 70 $^\circ\text{C}$ and is available in a narrow body, PDIP. The AD708A and AD708B are rated over the industrial temperature range of -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$ and are available in a CERDIP.

PIN CONFIGURATION

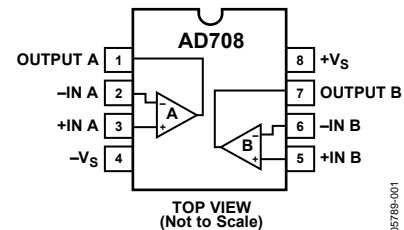


Figure 1. PDIP (N) and CERDIP (Q) Packages

The AD708S is rated over the military temperature range of -55 $^\circ\text{C}$ to +125 $^\circ\text{C}$ and is available in a CERDIP military version processed to MIL-STD-883B.

PRODUCT HIGHLIGHTS

1. The combination of outstanding matching and individual specifications make the AD708 ideal for constructing high gain, precision instrumentation amplifiers.
2. The low offset voltage drift and low noise of the AD708 allow the designer to amplify very small signals without sacrificing overall system performance.
3. The AD708 10 V/ μV typical open-loop gain and 140 dB common-mode rejection make it ideal for precision applications.

Rev. C

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REVISION HISTORY**1/06—Rev. B to Rev. C**

Updated Format.....	Universal
Removed TO-99 Package	Universal
Deleted AD707 References.....	Universal
Deleted LT1002 Reference.....	1
Deleted Figure 1.....	1
Deleted Metalization Photograph	5
Moved Figure 25, Figure 26, and Figure 27 to Theory of Operation section	10
Updated Outline Dimensions	13
Changes to Ordering Guide	13

2/91—Rev. A to Rev. B

SPECIFICATIONS

@ 25°C and ±15 V dc, unless otherwise noted.

Table 1.

Parameter	Conditions	AD708J/AD708A			AD708B			AD708S			Unit	
		Min ¹	Typ	Max ¹	Min ¹	Typ	Max ¹	Min ¹	Typ	Max ¹		
INPUT OFFSET VOLTAGE ²	T _{MIN} to T _{MAX}		30	100		5	50		5	30	μV	
		Drift		50	150		15	65		15	50	μV
		Long Term Stability		0.3	1.0		0.1	0.4		0.1	0.3	μV/°C
				0.3			0.3			0.3		μV/month
INPUT BIAS CURRENT	T _{MIN} to T _{MAX}		1.0	2.5		0.5	1.0		0.5	1	nA	
		Average Drift		2.0	4.0		1.0	2.0		1.0	4	nA
				15	40		10	25		10	30	pA/°C
OFFSET CURRENT	V _{CM} = 0 V T _{MIN} to T _{MAX}		0.5	2.0		0.1	1.0		0.1	1	nA	
		Average Drift		2.0	4.0		0.2	1.5		0.2	1.5	nA
				2	60		1	25		1	25	pA/°C
MATCHING CHARACTERISTICS ³	T _{MIN} to T _{MAX}	Offset Voltage		80			50			30	μV	
					150		75			50	μV	
			Offset Voltage Drift		1.0		0.4			0.3	μV/°C	
	T _{MIN} to T _{MAX}	Input Bias Current		4.0			1.0			1.0	nA	
					5.0		2.0			2.0	nA	
	T _{MIN} to T _{MAX}	Common-Mode Rejection		120	140		130	140		130	140	dB
				110			130			130		dB
T _{MIN} to T _{MAX}	Power Supply Rejection		110			120			120		dB	
			110			120			120		dB	
T _{MIN} to T _{MAX}	Channel Separation		135			140			140		dB	
INPUT VOLTAGE NOISE	0.1 Hz to 10 Hz	f = 10 Hz		0.23	0.6		0.23	0.6		0.23	0.35	μV p-p
		f = 100 Hz		10.3	18		10.3	12		10.3	12	nV/√Hz
		f = 1 kHz		10.0	13.0		10.0	11.0		10.0	11	nV/√Hz
				9.6	11.0		9.6	11.0		9.6	11	nV/√Hz
INPUT CURRENT NOISE	0.1 Hz to 10 Hz	f = 10 Hz		14	35		14	35		14	35	pA p-p
		f = 100 Hz		0.32	0.9		0.32	0.8		0.32	0.8	pA/√Hz
		f = 1 kHz		0.14	0.27		0.14	0.23		0.14	0.23	pA/√Hz
				0.12	0.18		0.12	0.17		0.12	0.17	pA/√Hz
COMMON-MODE REJECTION RATIO	V _{CM} = ±13 V T _{MIN} to T _{MAX}		120	140		130	140		130	140	dB	
			120	140		130	140		130	140	dB	
OPEN-LOOP GAIN	V _O = ±10 V R _{LOAD} ≥ 2 kΩ T _{MIN} to T _{MAX}		3	10		5	10		4	10	V/μV	
			3	10		5	10		4	7	V/μV	
POWER SUPPLY REJECTION RATIO	V _S = ±3 V to ±18 V T _{MIN} to T _{MAX}		110	130		120	130		120	130	dB	
			110	130		120	130		120	130	dB	
FREQUENCY RESPONSE	Closed-Loop Bandwidth Slew Rate		0.5	0.9		0.5	0.9		0.5	0.9	MHz	
			0.15	0.3		0.15	0.3		0.15	0.3	V/μs	
INPUT RESISTANCE	Differential Common Mode			60			200			200	MΩ	
				200			400			400	GΩ	

AD708

Parameter	Conditions	AD708J/AD708A			AD708B			AD708S			Unit
		Min ¹	Typ	Max ¹	Min ¹	Typ	Max ¹	Min ¹	Typ	Max ¹	
OUTPUT VOLTAGE	$R_{LOAD} \geq 10 \text{ k}\Omega$	13.5	14		13.5	14.0		13.5	14		$\pm V$
	$R_{LOAD} \geq 2 \text{ k}\Omega$	12.5	13.0		12.5	13.0		12.5	13		$\pm V$
	$R_{LOAD} \geq 1 \text{ k}\Omega$	12.0	12.5		12.0	12.5		12.0	12.5		$\pm V$
	T_{MIN} to T_{MAX}	12.0	13.0		12.0	13.0		12.0	13		$\pm V$
OPEN-LOOP OUTPUT RESISTANCE			60		60			60			Ω
POWER SUPPLY											
Quiescent Current			4.5	5.5		4.5	5.5		4.5	5.5	mA
Power Consumption	$V_S = \pm 15 \text{ V}$		135	165		135	165		135	165	mW
	$V_S = \pm 3 \text{ V}$		12	18		12	18		12	18	mW
Operating Range		± 3		± 18	± 3		± 18	± 3		± 18	V

¹ All min and max specifications are guaranteed. Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

² Input offset voltage specifications are guaranteed after five minutes of operation at $T_A = 25^\circ\text{C}$.

³ Matching is defined as the difference between parameters of the two amplifiers.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	± 22 V
Internal Power Dissipation ¹	
Input Voltage ²	$\pm V_S$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range (Q)	-65°C to $+150^\circ\text{C}$
Storage Temperature Range (N)	-65°C to $+125^\circ\text{C}$
Lead Temperature (Soldering 60 sec)	300°C

¹ Thermal Characteristics

8-lead PDIP: $\theta_{JC} = 33^\circ\text{C}/\text{W}$, $\theta_{JA} = 100^\circ\text{C}/\text{W}$

8-lead CERDIP: $\theta_{JC} = 30^\circ\text{C}/\text{W}$, $\theta_{JA} = 110^\circ\text{C}/\text{W}$

² For supply voltages less than ± 22 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TYPICAL PERFORMANCE CHARACTERISTICS

$V_S = \pm 15\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

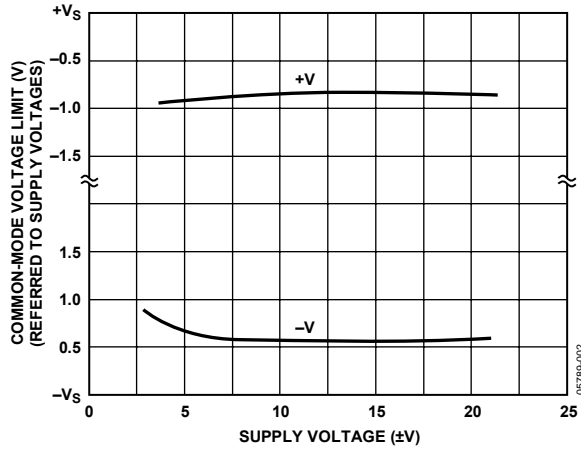


Figure 2. Input Common-Mode Range vs. Supply Voltage

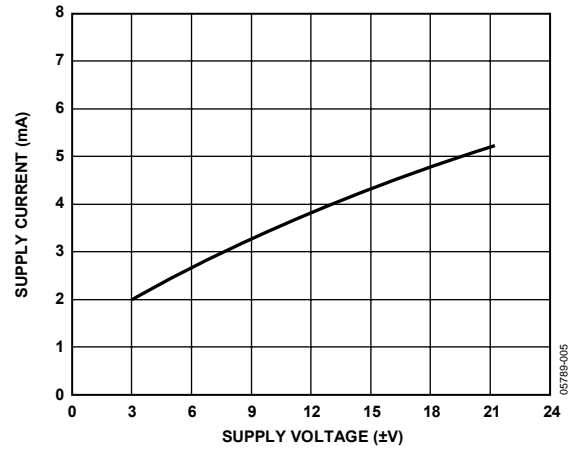


Figure 5. Supply Current vs. Supply Voltage

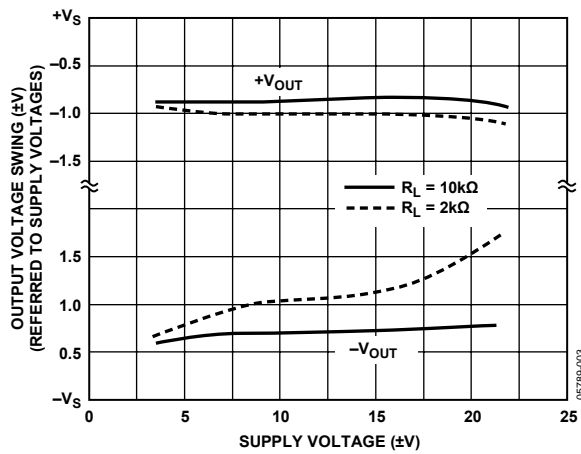


Figure 3. Output Voltage Swing vs. Supply Voltage

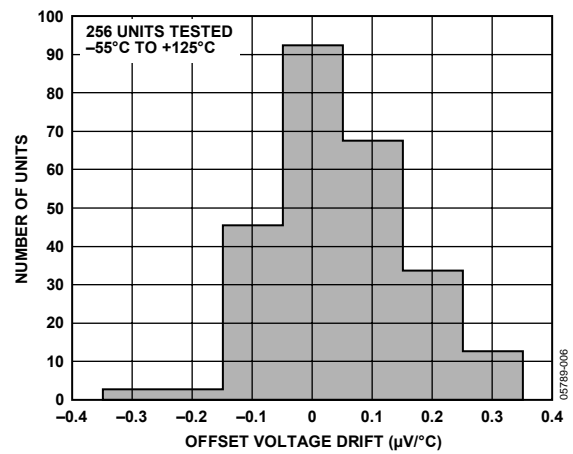


Figure 6. Typical Distribution of Offset Voltage Drift

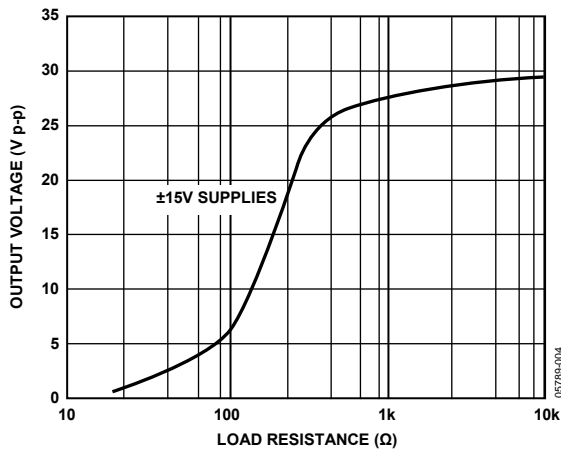


Figure 4. Output Voltage Swing vs. Load Resistance

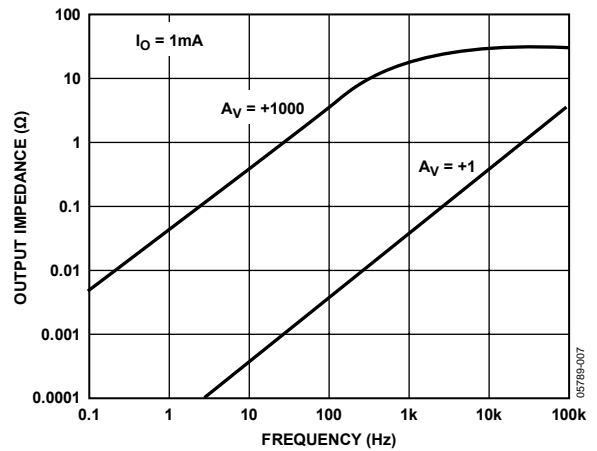


Figure 7. Output Impedance vs. Frequency

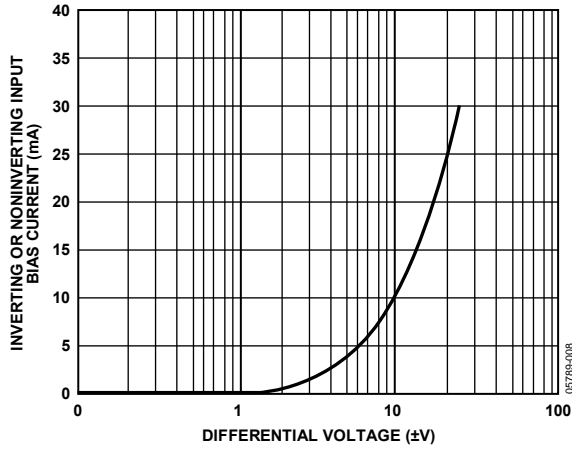


Figure 8. Input Bias Current vs. Differential Input Voltage

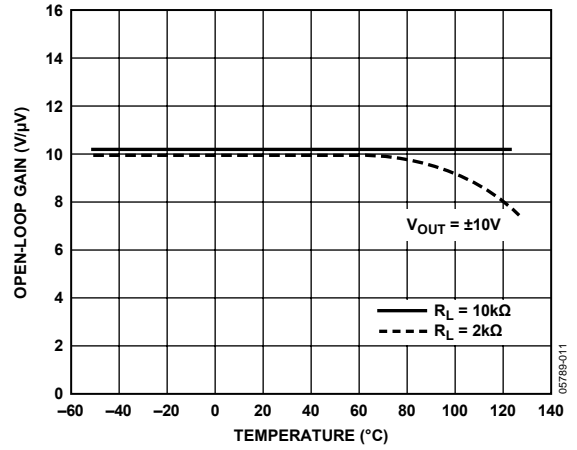


Figure 11. Open-Loop Gain vs. Temperature

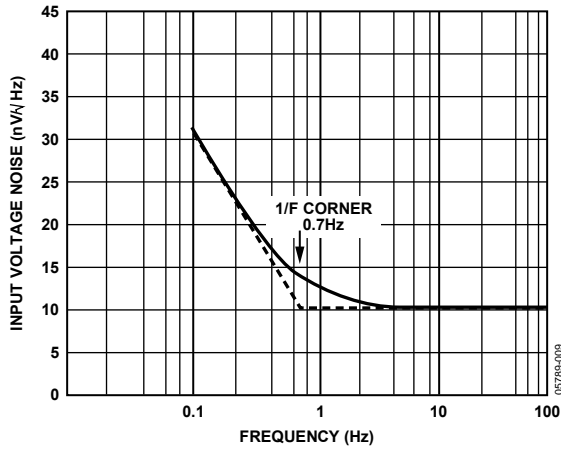


Figure 9. Input Noise Spectral Density

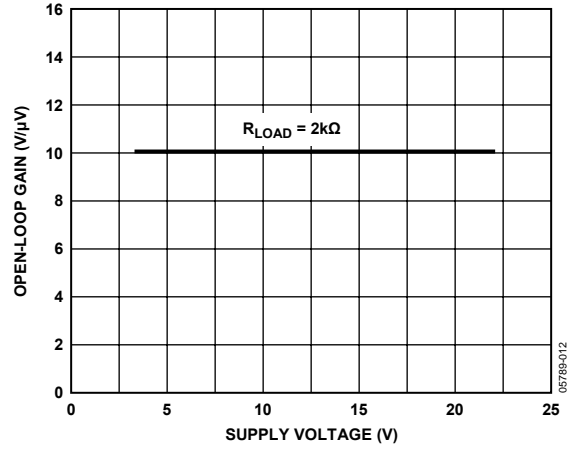


Figure 12. Open-Loop Gain vs. Supply Voltage

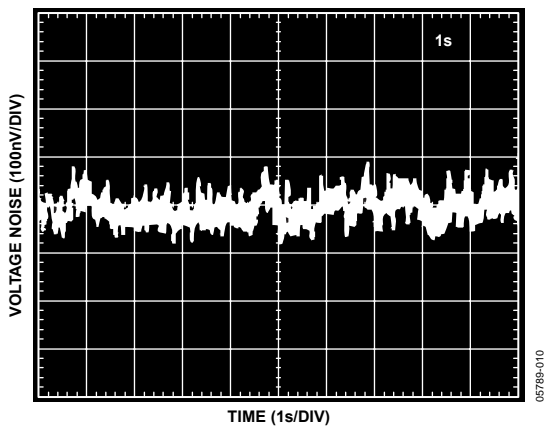


Figure 10. 0.1 Hz to 10 Hz Voltage Noise

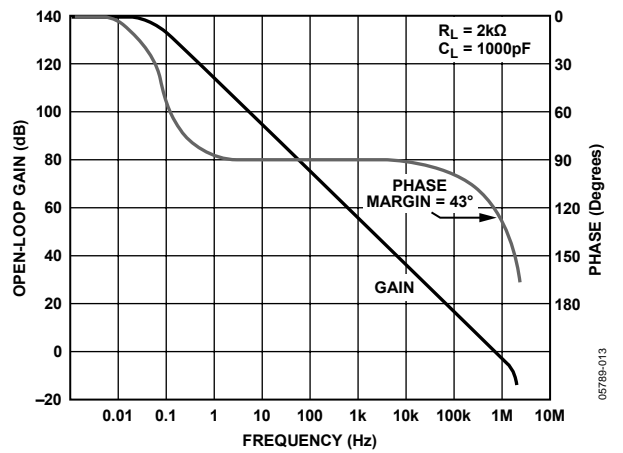


Figure 13. Open-Loop Gain and Phase vs. Frequency

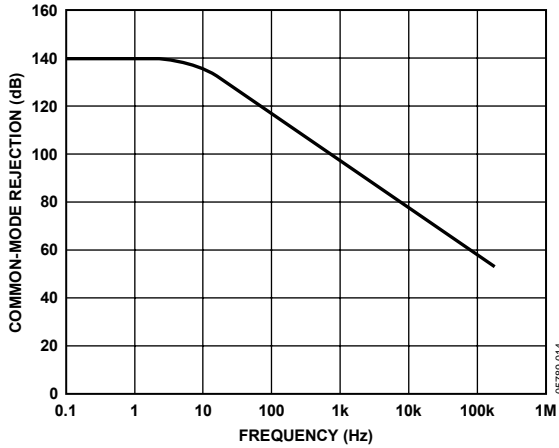


Figure 14. Common-Mode Rejection vs. Frequency

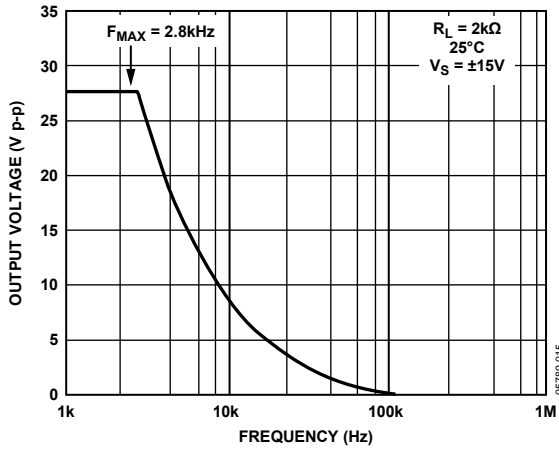


Figure 15. Large Signal Frequency Response

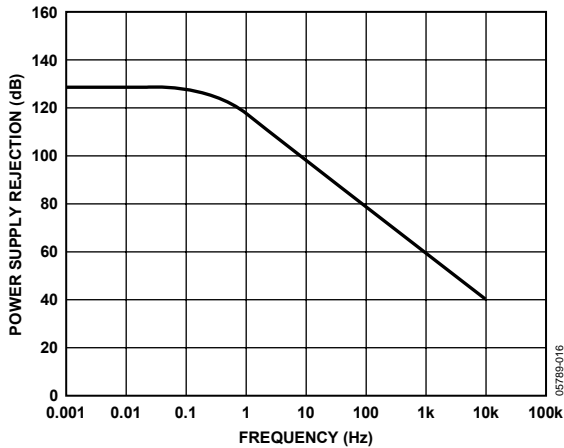


Figure 16. Power Supply Rejection vs. Frequency

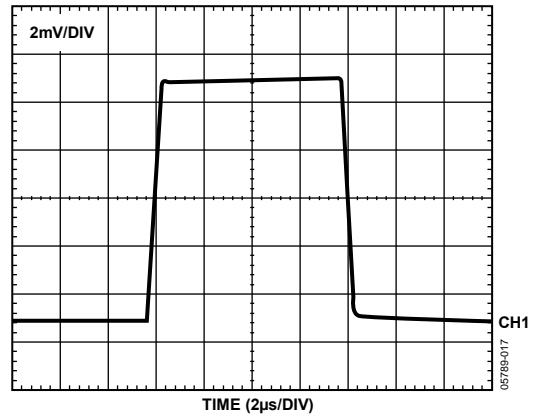


Figure 17. Small Signal Transient Response; $A_V = +1$, $R_L = 2\text{ k}\Omega$, $C_L = 50\text{ pF}$

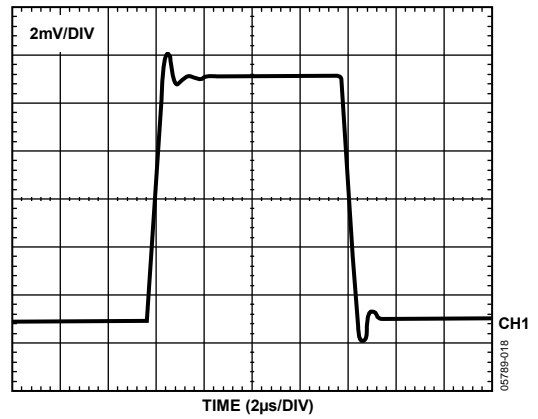


Figure 18. Small Signal Transient Response; $A_V = +1$, $R_L = 2\text{ k}\Omega$, $C_L = 1000\text{ pF}$

MATCHING CHARACTERISTICS

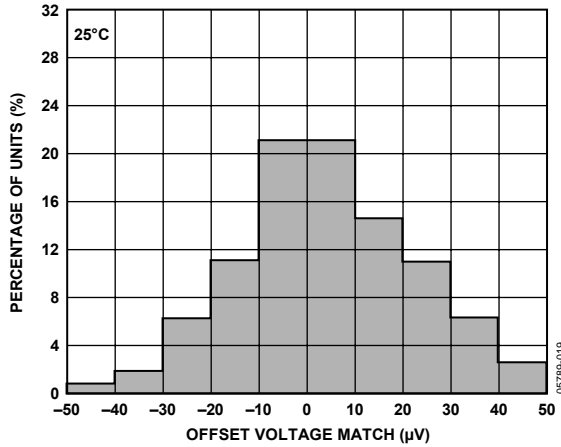


Figure 19. Typical Distribution of Offset Voltage Match

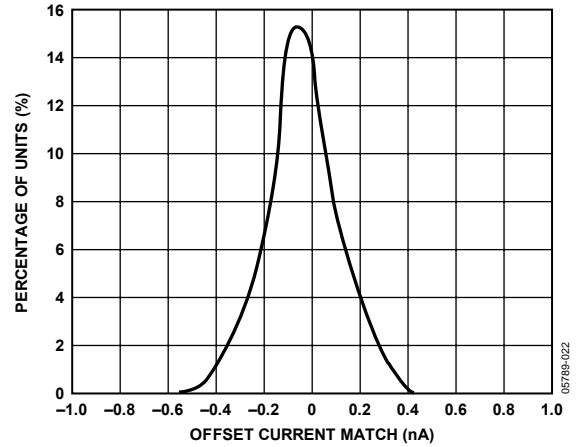


Figure 22. Typical Distribution of Input Offset Current Match

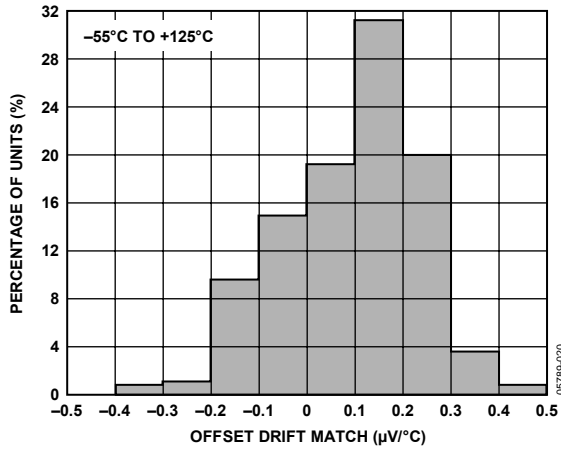


Figure 20. Typical Distribution of Offset Voltage Drift Match

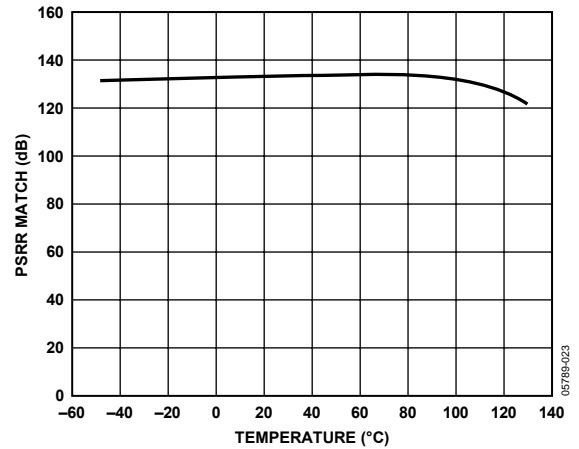


Figure 23. PSRR Match vs. Temperature

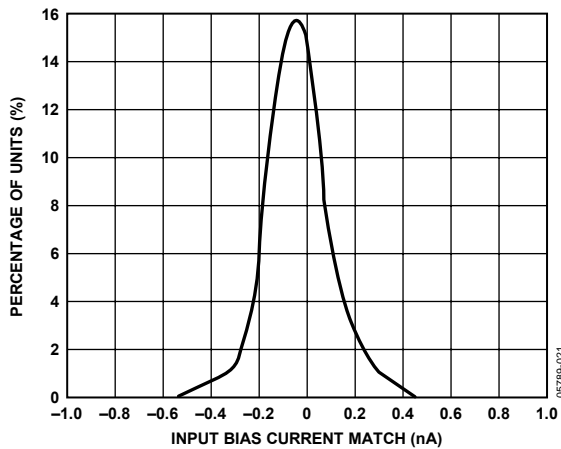


Figure 21. Typical Distribution of Input Bias Current Match

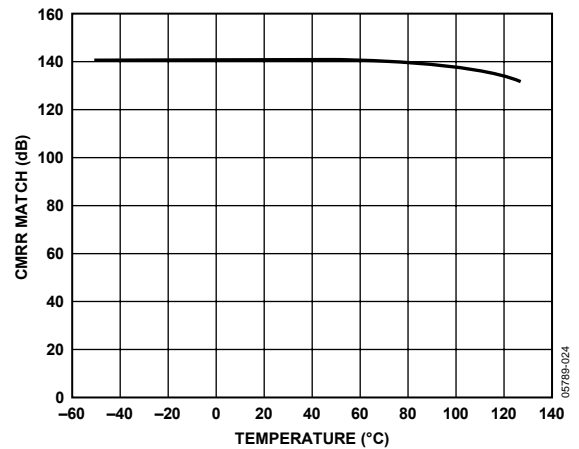


Figure 24. CMRR Match vs. Temperature

THEORY OF OPERATION

CROSSTALK PERFORMANCE

The AD708 exhibits very low crosstalk as shown in Figure 25, Figure 26, and Figure 27. Figure 25 shows the offset voltage induced on Side B of the AD708 when Side A output is moving slowly (0.2 Hz) from -10 V to $+10\text{ V}$ under no load. This is the least stressful situation to the part because the overall power in the chip does not change. Only the location of the power in the output device changes. Figure 26 shows the input offset voltage change to Side B when Side A is driving a $2\text{ k}\Omega$ load. Here the power changes in the chip with the maximum power change occurring at 7.5 V . Figure 27 shows crosstalk under the most severe conditions. Side A is connected as a follower with 0 V input, and is forced to sink and source $\pm 5\text{ mA}$ of output current.

$$\text{Power} = (30\text{ V})(5\text{ mA}) = 150\text{ mW}$$

Even this large change in power causes only an $8\text{ }\mu\text{V}$ (linear) change in the input offset voltage of Side B.

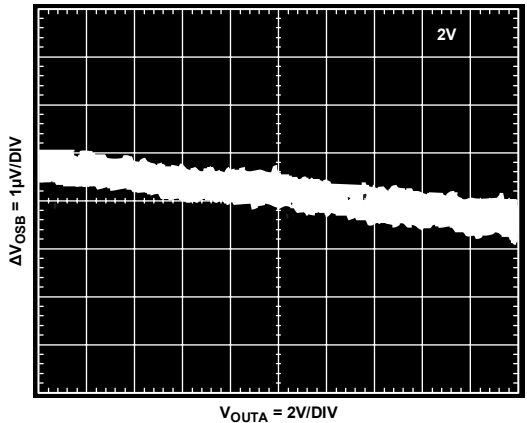
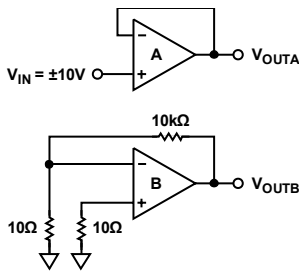


Figure 25. Crosstalk with No Load

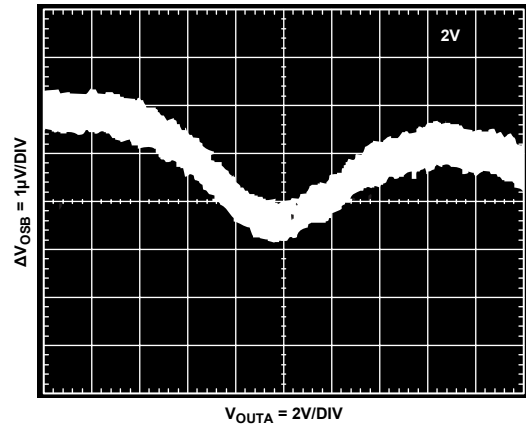
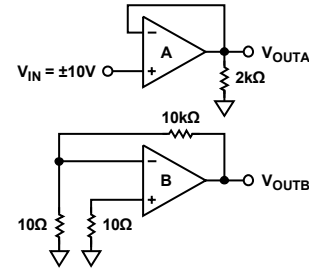


Figure 26. Crosstalk with $2\text{ k}\Omega$ Load

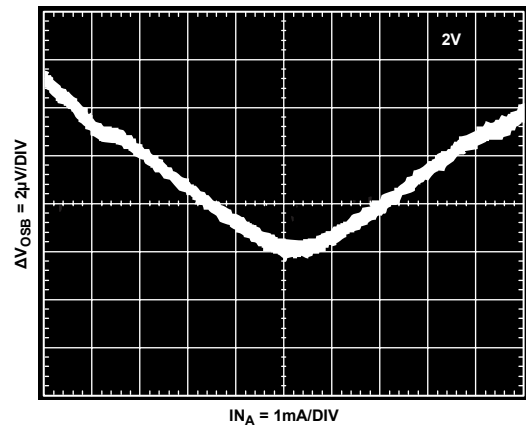
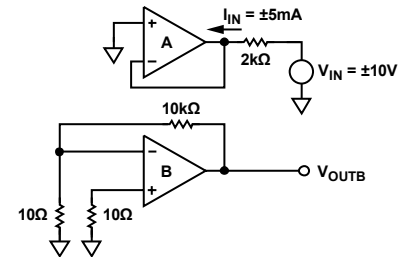


Figure 27. Crosstalk Under Forced Source and Sink Conditions

OPERATION WITH A GAIN OF –100

To show the outstanding dc precision of the AD708 in a real application, Table 3 shows an error budget calculation for a gain of –100. This configuration is shown in Figure 28.

Table 3.

Maximum Error Contribution $A_V = 100$ (S Grade) (Full Scale: $V_{OUT} = 10\text{ V}$, $V_{IN} = 100\text{ mV}$)	
Error Sources	
V_{OS}	$30\ \mu\text{V}/100\text{ mV} = 300\text{ ppm}$
I_{OS}	$(100\text{ k}\Omega)(1\text{ nA})/10\text{ V} = 10\text{ ppm}$
Gain (2 k Ω Load)	$10\text{ V}/(5 \times 10^6)/100\text{ mV} = 20\text{ ppm}$
Noise	$0.35\text{ mV}/100\text{ mV} = 4\text{ ppm}$
V_{OS} Drift	$(0.3\text{ mV}/^\circ\text{C})/100\text{ mV} = 3\text{ ppm}/^\circ\text{C}$
Total Unadjusted Error	
@ 25°C	$= 334\text{ ppm} > 11\text{ bits}$
–55°C to +125°C	$= 634\text{ ppm} > 10\text{ bits}$
With Offset Calibrated Out	
@ 25°C	$= 34\text{ ppm} > 14\text{ bits}$
–55°C to +125°C	$= 334\text{ ppm} > 11\text{ bits}$

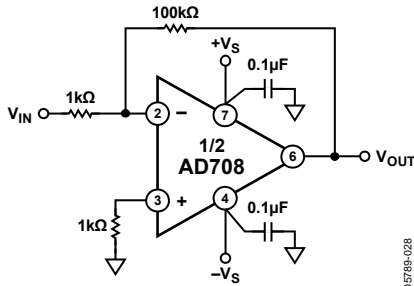


Figure 28. Gain of –100 Configuration

This error budget assumes no error in the resistor ratio and no error from power supply variation (the 120 dB minimum PSRR of the AD708S makes this a good assumption). The external resistors can cause gain error from mismatch and drift over temperature.

HIGH PRECISION PROGRAMMABLE GAIN AMPLIFIER

The three op amp programmable gain amplifier shown in Figure 29 takes advantage of the outstanding matching characteristics of the AD708 to achieve high dc precision.

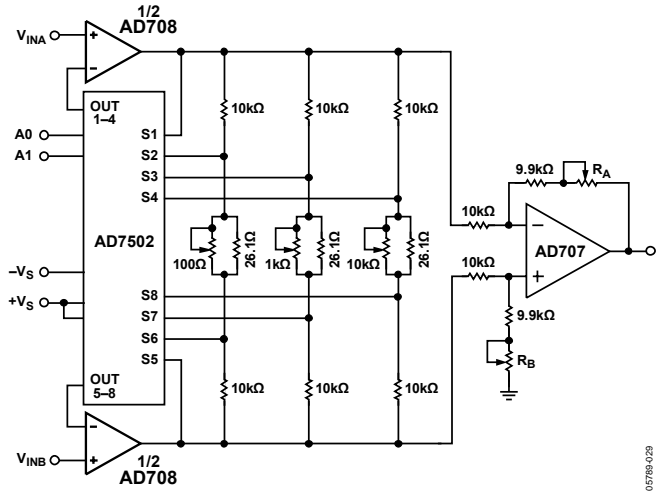


Figure 29. Precision PGA

The gains of the circuit are controlled by the select lines, A0 and A1, of the AD7502 multiplexer, and are 1, 10, 100, and 1000 in this design.

The input stage attains very high dc precision due to the 30 μV maximum offset voltage match of the AD708S and the 1 nA maximum input bias current match. The accuracy is maintained over temperature because of the ultralow drift performance of the AD708.

To achieve 0.1% gain accuracy, along with high common-mode rejection, the circuit should be trimmed.

To maximize common-mode rejection

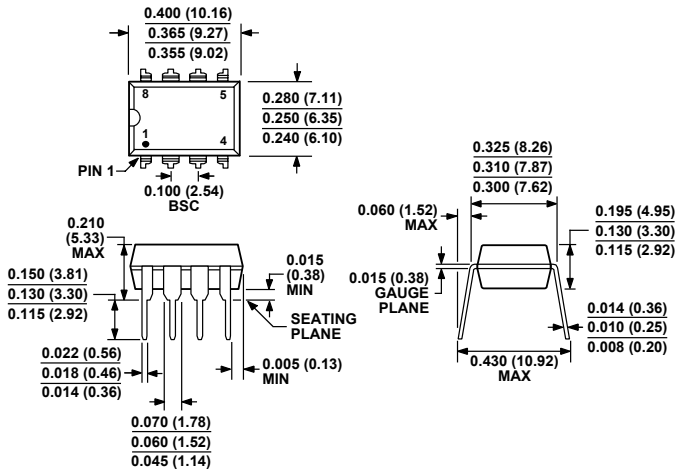
1. Set the select lines for gain = 1 and ground V_{INB} .
2. Apply a precision dc voltage to V_{INA} and trim R_A until $V_O = -V_{INA}$ to the required precision.
3. Connect V_{INB} to V_{INA} and apply an input voltage equal to the full-scale common mode expected.
4. Trim R_B until $V_O = 0\text{ V}$.

To minimize gain errors

1. Select gain = 10 with the control lines and apply a differential input voltage.
2. Adjust the 100 Ω potentiometer to $V_O = 10 V_{IN}$ (adjust V_{IN} magnitude as necessary).
3. Repeat Step 1 and Step 2 for gain = 100 and gain = 1000, adjusting the 1 k Ω and 10 k Ω potentiometers, respectively.

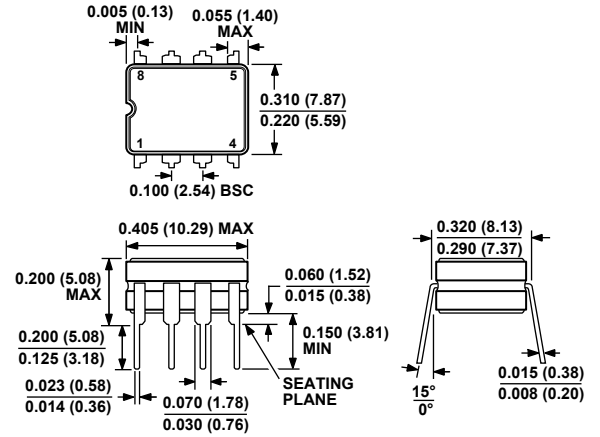
The design shown in Figure 29 should allow for 0.1% gain accuracy and 0.1 $\mu\text{V}/\text{V}$ common-mode rejection when $\pm 1\%$ resistors and $\pm 5\%$ potentiometers are used.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-001-BA
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 33. 8-Lead Plastic Dual In-Line Package [PDIP]
 Narrow Body
 (N-8)
 Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 34. 8-Lead Ceramic Dual In-Line Package [CERDIP]
 (Q-8)
 Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD708JN	0°C to +70°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD708JNZ ¹	0°C to +70°C	8-Lead Plastic Dual In-Line Package [PDIP]	N-8
AD708AQ	-40°C to +85°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8
AD708BQ	-40°C to +85°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8
AD708SQ/883B	-55°C to +125°C	8-Lead Ceramic Dual In-Line Package [CERDIP]	Q-8

¹ Z = Pb-free part.

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