



STS11NF30L

N-CHANNEL 30V - 0.0085 Ω - 11A SO-8 LOW GATE CHARGE STripFET™ POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STS11NF30L	30 V	<0.0105 Ω	11 A

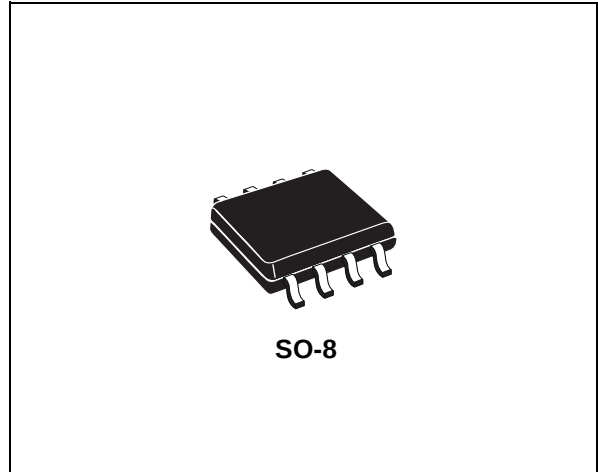
- TYPICAL R_{DS(on)} = 0.0085 Ω @ 10 V
- TYPICAL Q_g = 22.5 nC @ 5 V
- OPTIMAL R_{DS(on)} x Q_g TRADE-OFF
- CONDUCTION LOSSES REDUCED

DESCRIPTION

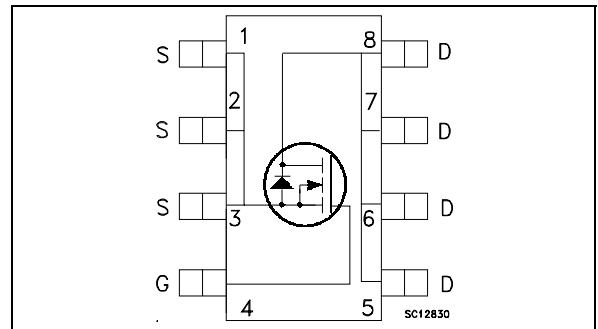
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS
- AUTOMOTIVE



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	30	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	30	V
V _{GS}	Gate- source Voltage	± 18	V
I _D (●)	Drain Current (continuous) at T _C = 25°C	11	A
I _D	Drain Current (continuous) at T _C = 100°C	7	A
I _{DM} (●●)	Drain Current (pulsed)	44	A
P _{tot}	Total Dissipation at T _C = 25°C	2.5	W
	Derating Factor	0.02	W/°C
dV/dt (1)	Peak Diode Recovery voltage slope	5.5	V/ns
T _{stg}	Storage Temperature	-55 to 150	°C
T _J	Max. Operating Junction Temperature	150	°C

(●●) Pulse width limited by safe operating area.
(●) Current limited by the package

(1) I_{SD} ≤ 11A, di/dt ≤ 370A/ μ s, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ T_{JMAX}

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THERMAL DATA

Rthj-amb T_I	(*)Thermal Resistance Junction-ambient Maximum Lead Temperature For Soldering Purpose	Max Typ	50 150	°C/W °C
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(*) When Mounted on 1 inch² FR-4 board, 2 oz of Cu and $t \leq 10$ sec.

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^\circ\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_C = 125^\circ\text{C}$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 18\ \text{V}$			± 100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\ \mu\text{A}$	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\ \text{V}$ $I_D = 5.5\ \text{A}$ $V_{GS} = 5\ \text{V}$ $I_D = 5.5\ \text{A}$		0.0085 0.0145	0.0105 0.0190	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS}=25\text{V}$ $I_D = 5.5\ \text{A}$		15		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		1440 560 135		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15\text{ V}$ $I_D = 55\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 3)		22 39		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 15\text{ V}$ $I_D = 11\text{ A}$ $V_{GS} = 5\text{ V}$		22.5 9 12	30	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 15\text{ V}$ $I_D = 5.5\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ (Resistive Load, Figure 3)		23 16		ns ns

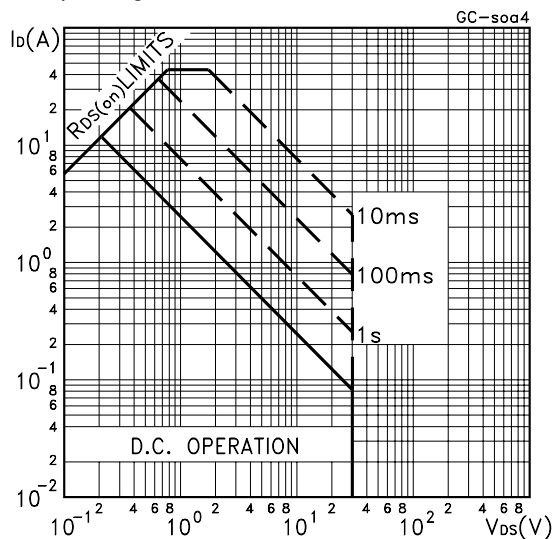
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				11 44	A A
$V_{SD}^(*)$	Forward On Voltage	$I_{SD} = 11\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 11\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		42 52 2.5		ns nC A

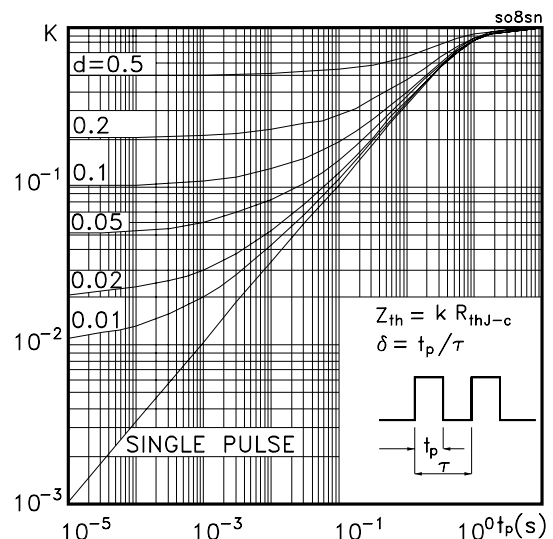
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

($\bullet$) Pulse width limited by safe operating area.

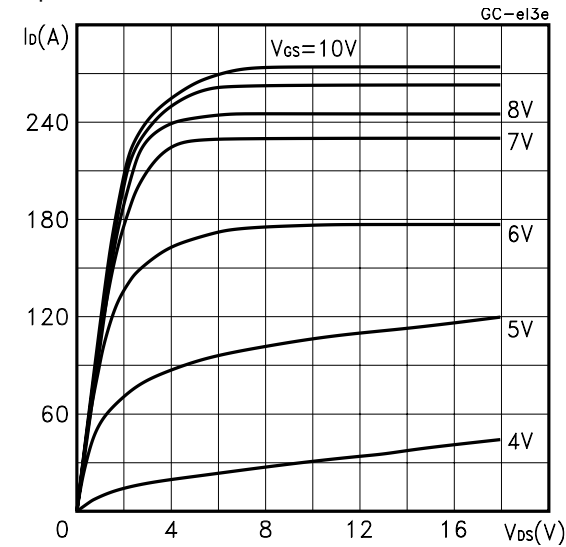
Safe Operating Area



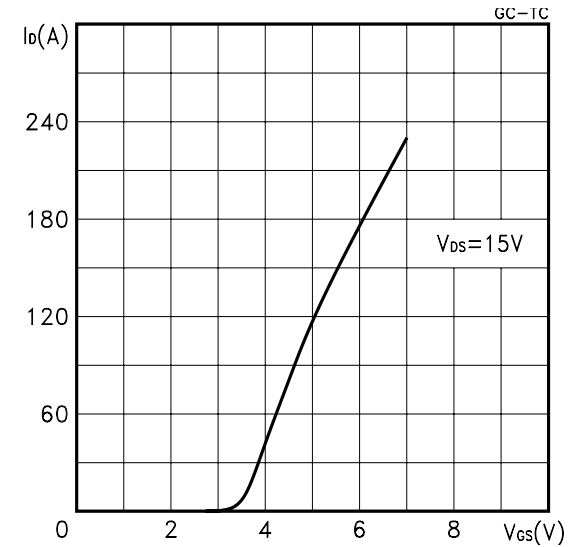
Thermal Impedance



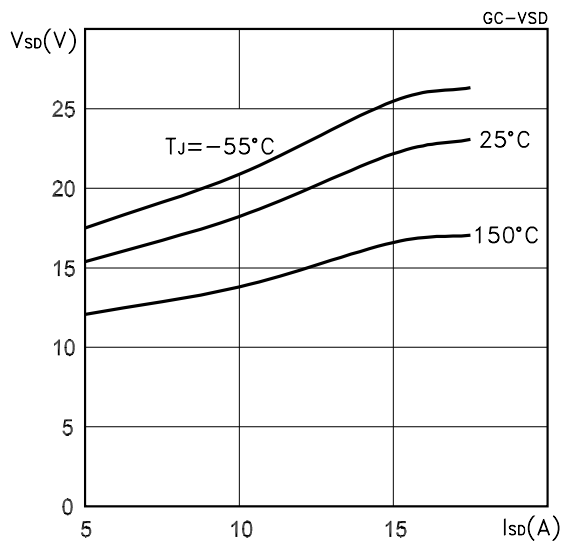
Output Characteristics



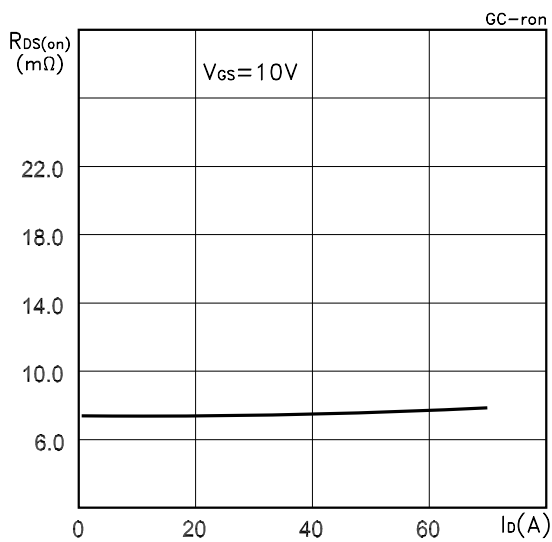
Transfer Characteristics



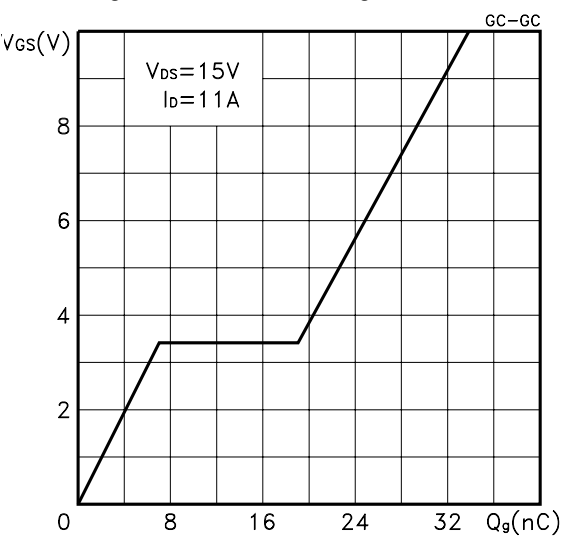
Transconductance



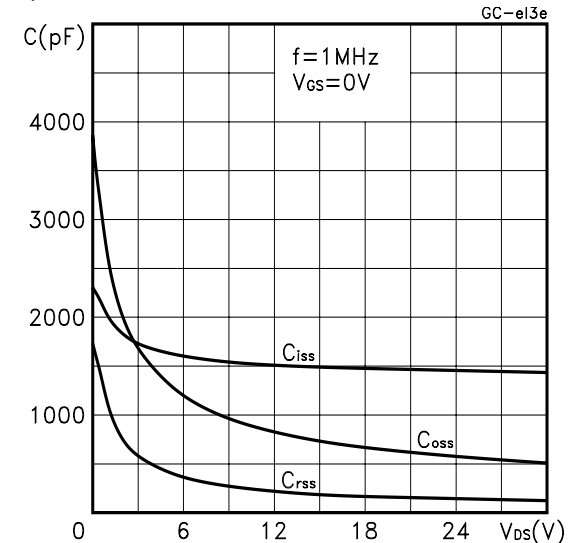
Static Drain-source On Resistance



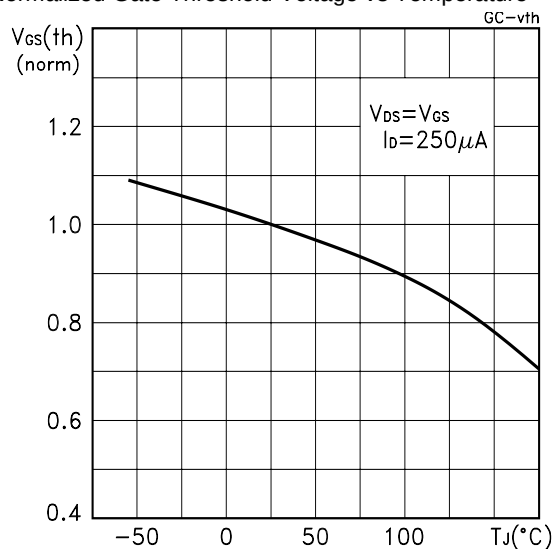
Gate Charge vs Gate-source Voltage



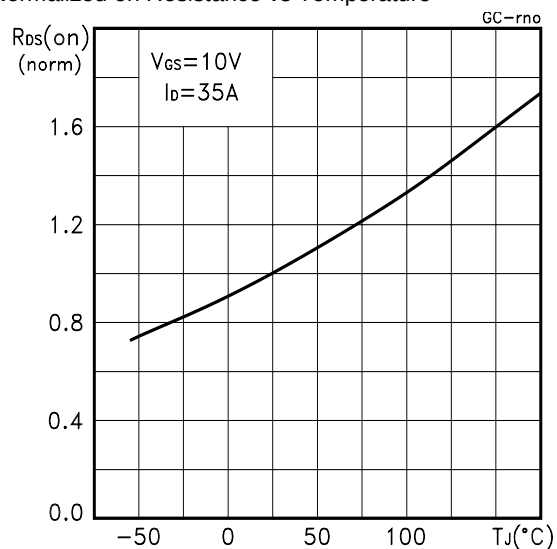
Capacitance Variations



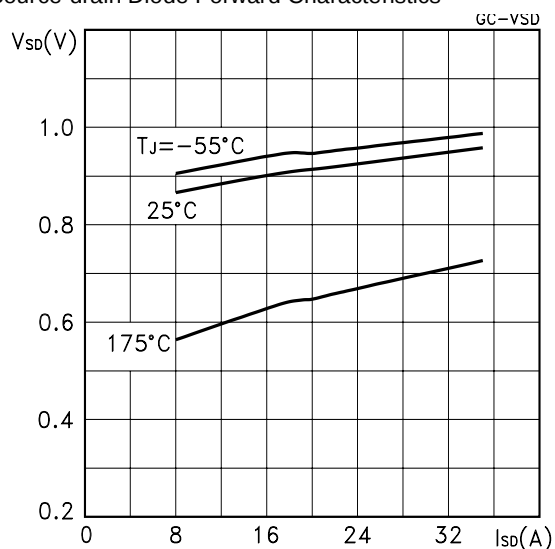
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature.

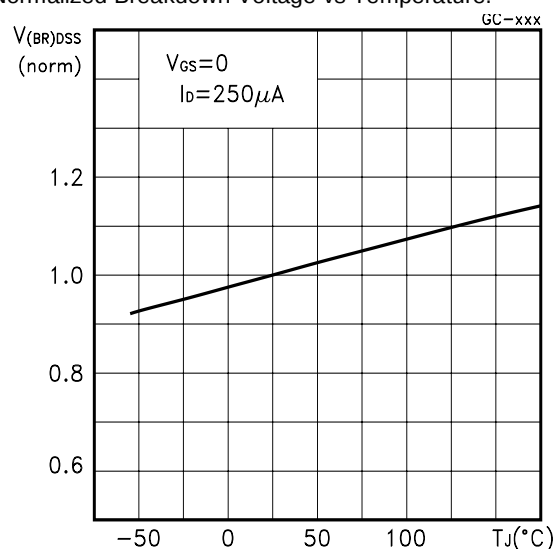


Fig. 1: Unclamped Inductive Load Test Circuit

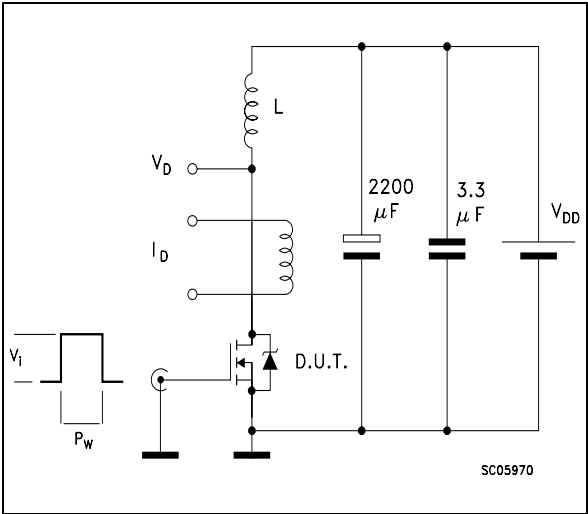


Fig. 2: Unclamped Inductive Waveform

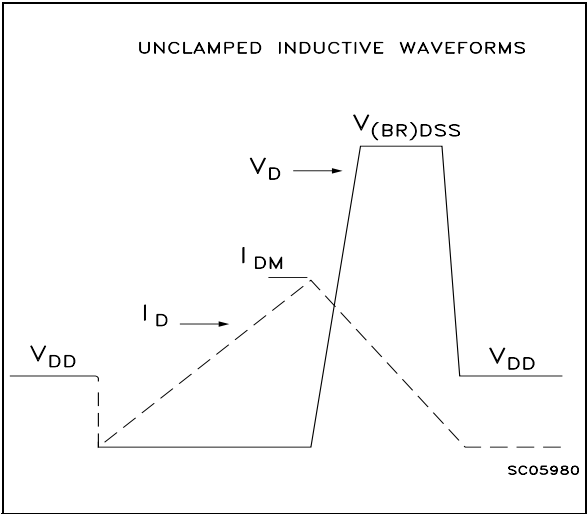


Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

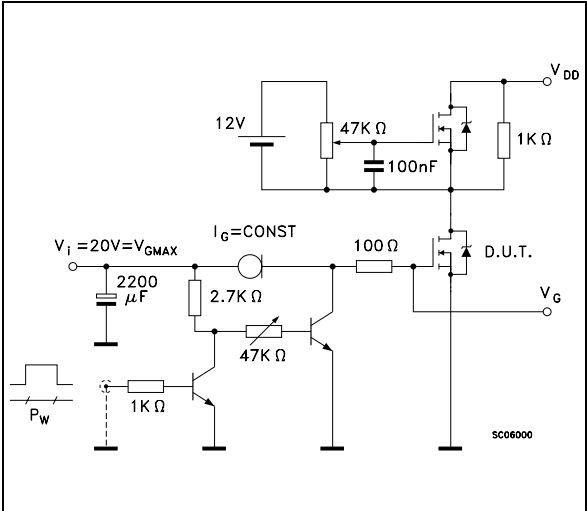
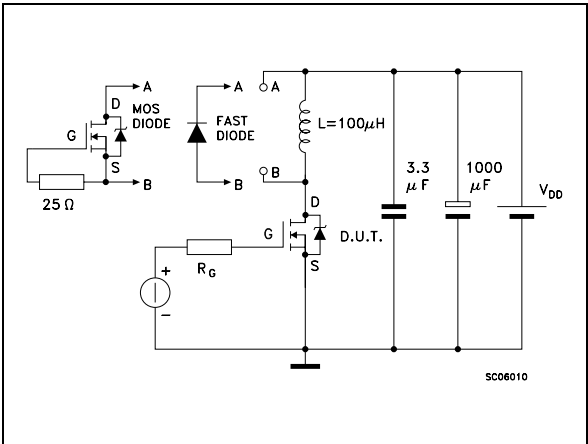
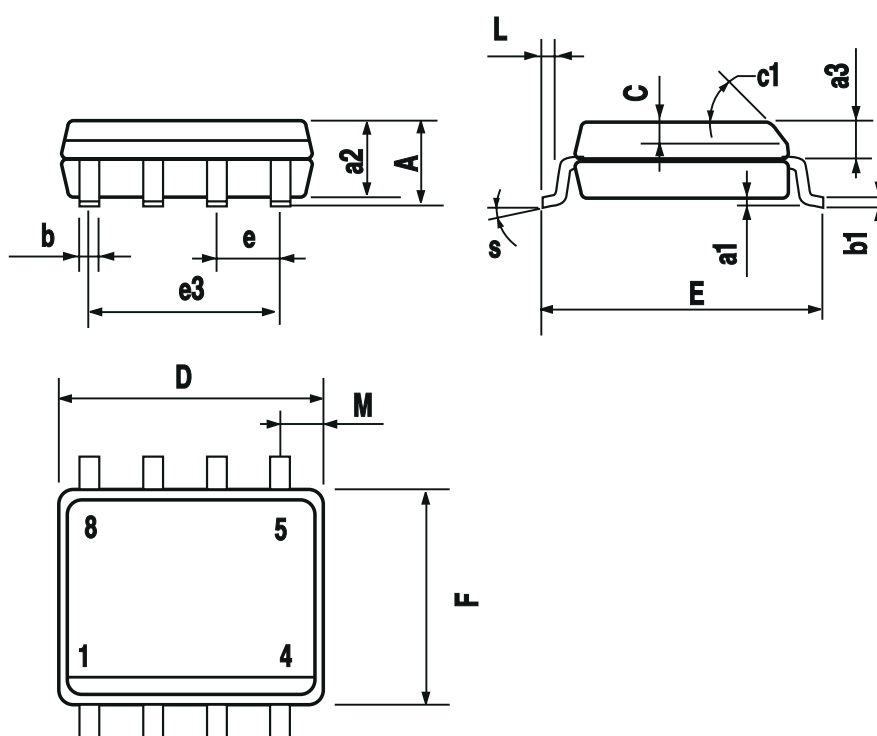


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



SO-8 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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