

HD74LV1GT00A

2-input NAND Gate / CMOS Logic Level Shifter

REJ03D0115-0900 Rev.9.00 Mar 21, 2008

Description

The HD74LV1GT00A is high-speed CMOS two input NAND gate using silicon gate CMOS process. With CMOS low power dissipation, it provides high-speed equivalent to LS-TTL series. The internal circuit of three stages construction with buffer provides wide noise margin and stable output. The input protection circuitry on this device allows over voltage tolerance on the input, allowing the device to be used as a logic-level translator from 3.0 V CMOS Logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high-voltage power supply. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

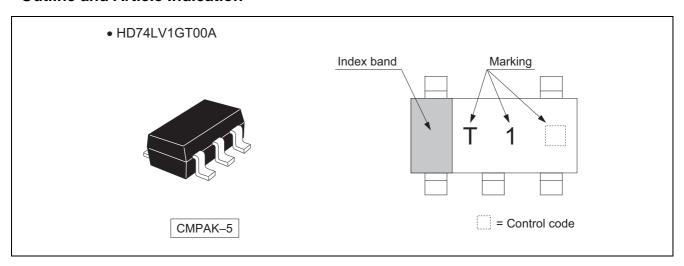
Features

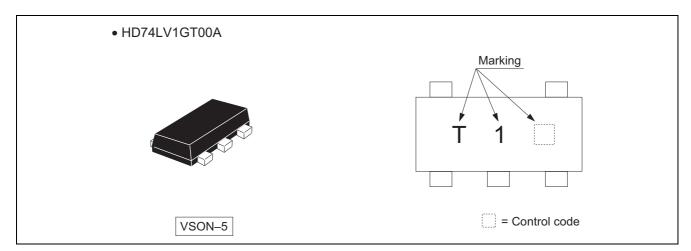
- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.
 - Supply voltage range: 3.0 to 5.5 V
 - Operating temperature range : -40 to +85°C
- Logic-level translate function
 - 3.0 V CMOS logic \rightarrow 5.0 V CMOS logic (@V_{CC} = 5.0 V)
 - 1.8 V or 2.5 V CMOS logic \rightarrow 3.3 V CMOS logic (@V_{CC} = 3.3 V)
- All inputs V_{IH} (Max.) = 5.5 V (@ V_{CC} = 0 V to 5.5 V)
 - All outputs V_0 (Max.) = 5.5 V (@V_{CC} = 0 V)
- Output current $\pm 6 \text{ mA}$ (@V_{CC} = 3.0 V to 3.6 V), $\pm 12 \text{ mA}$ (@V_{CC} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV1GT00ACME	CMPAK-5 pin	PTSP0005ZC-A (CMPAK-5V)	СМ	E (3000 pcs/reel)
HD74LV1GT00AVSE	VSON-5 pin	PUSN0005KA-A (TNP-5DV)	VS	E (3000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Outline and Article Indication



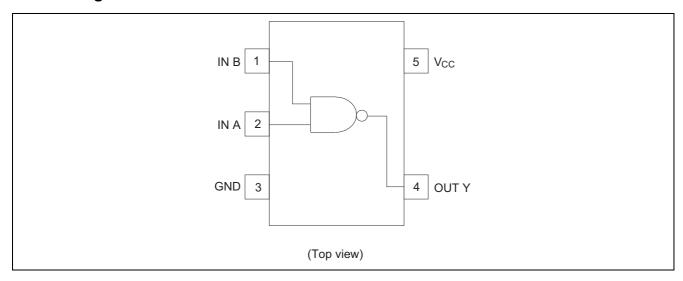


Function Table

Inp	Output Y	
Α	В	Output 1
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

H : High level L : Low level

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	Vcc	-0.5 to 7.0	V	
Input voltage range *1	Vı	-0.5 to 7.0	V	
Output voltage range *1, 2		-0.5 to V _{CC} + 0.5	V	Output : H or L
Output voltage range	Vo	-0.5 to 7.0	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	V _{CC} : OFF
Input clamp current	I _{IK}	-20	mA	V ₁ < 0
Output clamp current	I _{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I _O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through Vcc or GND	I _{CC} or I _{GND}	±50	mA	
Maximum power dissipation at Ta = 25°C (in still air) *3	P _T	200	mW	
Storage temperature	Tstg	-65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

- 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. This value is limited to 5.5 V maximum.
- 3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V _{CC}	3.0	5.5	V	
Input voltage range	VI	0	5.5	V	
Output voltage range	Vo	0	V _{CC}	V	
	I _{OL}	_	6		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
Outrast assument	IOL	_	12	mA	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Output current	Іон	_	-6		$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
		_	-12]	$V_{CC} = 4.5 \text{ to } 5.5 \text{ V}$
Input transition rise or fall rate	Δt / Δν	0	100	ns / V	$V_{CC} = 3.0 \text{ to } 3.6 \text{ V}$
input transition rise of fall rate	Δι / Δν	0	20	115/V	V _{CC} = 4.5 to 5.5 V
Operating free-air temperature	Ta	-40	85	°C	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristic

• $Ta = -40 \text{ to } 85^{\circ}\text{C}$

Item	Symbol	V _{CC} (V) *	Min	Тур	Max	Unit	Test condition
	V _{IH}	3.0 to 3.6	1.5	_	_		
Input voltage	VIH	4.5 to 5.5	2.0	_	_	V	
Input voltage	V _{IL}	3.0 to 3.6		_	0.6	V	
	V IL	4.5 to 5.5		_	0.8		
Hysteresis voltage	V _H	3.3		0.10		V	$V_T^+ - V_T^-$
li iysteresis voitage	VH	5.0	_	0.15	_	V	VT - VT
		Min to Max	V _{CC} -0.1	_	_		$I_{OH} = -50 \mu A$
	V _{OH}	3.0	2.48	_	_		$I_{OH} = -6 \text{ mA}$
Output voltage		4.5	3.8	_	_	V	$I_{OH} = -12 \text{ mA}$
Output voltage	V _{OL}	Min to Max	_	_	0.1		$I_{OL} = 50 \mu A$
		3.0	_	_	0.44		$I_{OL} = 6 \text{ mA}$
		4.5	_	_	0.55		$I_{OL} = 12 \text{ mA}$
Input current	I _{IN}	0 to 5.5	_	_	±1	μΑ	$V_{IN} = 5.5 \text{ V or GND}$
Quiescent	Icc	5.5	_		10	μА	$V_{IN} = V_{CC}$ or GND,
supply current	icc	5.5			10	μΛ	$I_{O} = 0$
	Δl_{CC}	5.5	_	_	1.5	mA	One input $V_{IN} = 3.4 \text{ V}$,
	Δi(C	0.0			1.0	1117 (other input V _{CC} or GND
Output leakage current	I _{OFF}	0	_	_	5	μΑ	V_{IN} or $V_O = 0$ to 5.5 V
Input capacitance	C _{IN}	5.0		2.5		pF	$V_{IN} = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

• $V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40	to 85°C	Unit	Test	FROM	ТО
iteiii	Syllibol	Min	Тур	Max	Min	Max	Ollit	Conditions	(Input)	(Output)
Propagation	t _{PLH}	_	7.0	10.0	1.0	12.0	ne	$C_L = 15 pF$	A or B	>
delay time	t _{PHL}	_	7.5	12.0	1.0	14.0	ns	$C_L = 50 pF$	AUID	'

 $\bullet \quad V_{CC} = 5.0 \pm 0.5 \ V$

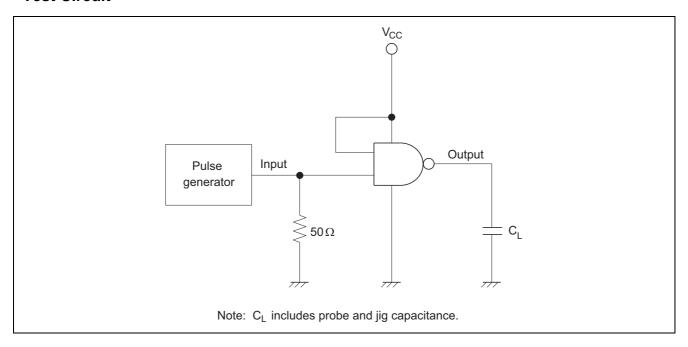
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test	FROM	ТО
item	Syllibol	Min	Тур	Max	Min	Max	Onit	Conditions	(Input)	(Output)
Propagation	t _{PLH}	_	5.0	6.9	1.0	8.0	nc	$C_L = 15 pF$	A or B	V
delay time	t _{PHL}	_	5.5	7.9	1.0	9.0	ns	$C_L = 50 \text{ pF}$	AUID	

Operating Characteristics

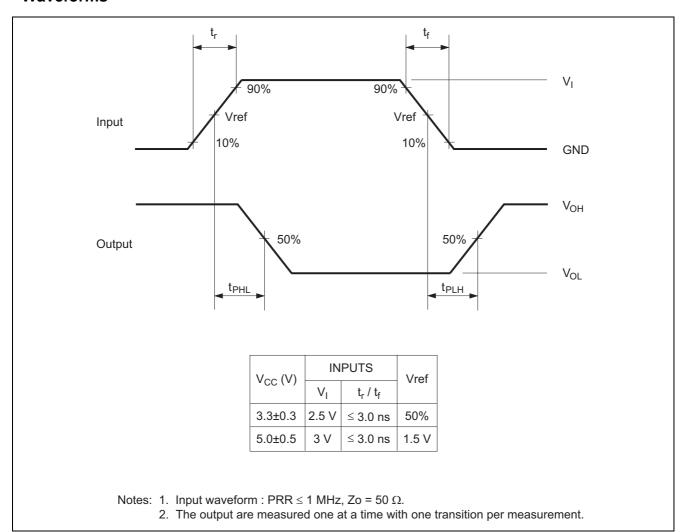
• $C_L = 50 \text{ pF}$

ltem	Symbol	Symbol V _{cc} (V)		Ta = 25°C			Test Conditions	
iteiii	Syllibol	ACC (A)	Min	Тур	Max	Unit	rest conditions	
Power dissipation capacitance	C _{PD}	5.0		11.0		pF	f = 10 MHz	

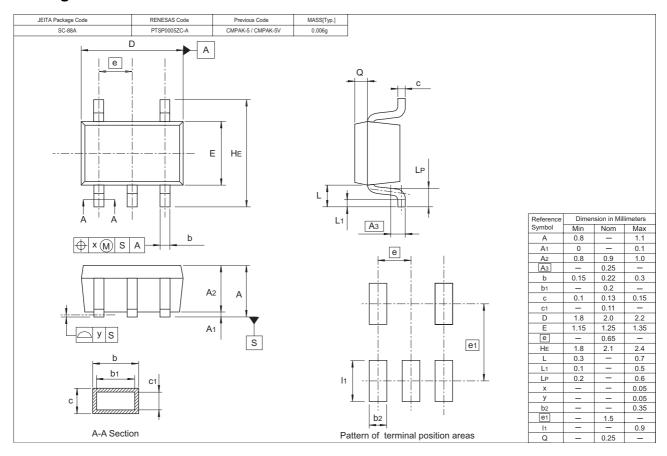
Test Circuit

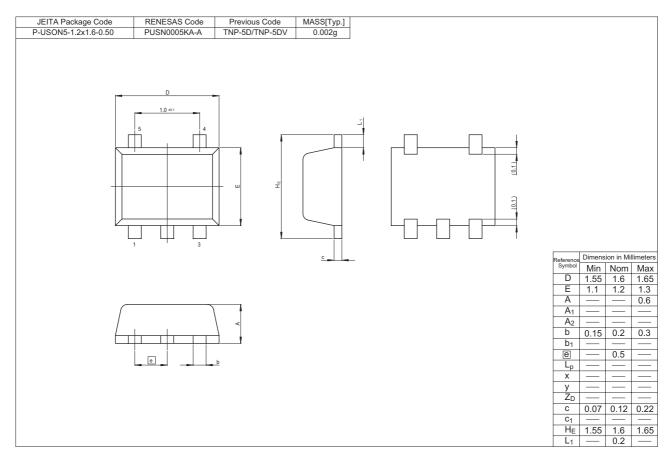


Waveforms



Package Dimensions





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- Renesas lechnology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan Notes:

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