EiceDRIVER™ 1ED31xxMU12H (1ED-X3 Compact)

Technical description

1ED312xMU12H, 1ED3131MU12H

Single-channel 5.7 kV (rms) isolated gate driver IC with active Miller clamp or separate output

About this document

The Infineon EiceDRIVER™ 1ED-X3 Compact products are single-channel high-voltage gate driver ICs with integrated coreless transformer (CLT) technology and a maximum offset voltage of 1200 V. The ICs are designed for use with 600 V, 650 V and 1200 V IGBTs, silicon and silicon-carbide MOSFETs.

Scope and purpose

The scope of this application note includes an explanation of general gate driver input and output features, and a description of how to use them in an application.

Intended audience

This document is intended for application circuit designers and concept engineers in power electronics.

Table of contents

1 Introduction

The Infineon EiceDRIVER™ 1ED-X3 Compact products are available in a 300 mil package with UL 1577 certification with either separated source sink outputs or a single output with an additional clamping function.

1ED31xx Compact UL 1577 certified device types

There are six variants in the wide body PG-DSO-8 (300 mil) package. Please refer to the data sheet for their individual isolation ratings.

Product type	Typical output current and configuration	UVLO ($V_{UVLOL2,min}$)	Certification (planned)	Package
1ED3120MU12H	5.5 A separate source and sink	8.0 V	UL	PG-DSO-8
1ED3121MU12H	5.5 A separate source and sink	10.5 V	UL	PG-DSO-8
1ED3122MU12H	10.0 A and 3.0 A clamp	8.0 V	UL	PG-DSO-8
1ED3123MU12H	14.0 A separate source and sink	8.0 V	UL	PG-DSO-8
1ED3124MU12H	14.0 A separate source and sink	10.5 V	UL	PG-DSO-8
1ED3131MU12H	5.5 A separate source and sink, 180 ns minimum input pulse suppression time	10.5 V	UL	PG-DSO-8

2 Input features

The input features of the gate driver IC include undervoltage lockout of input supply, pull-up and pull-down resistors of logic inputs, and signal filtering.

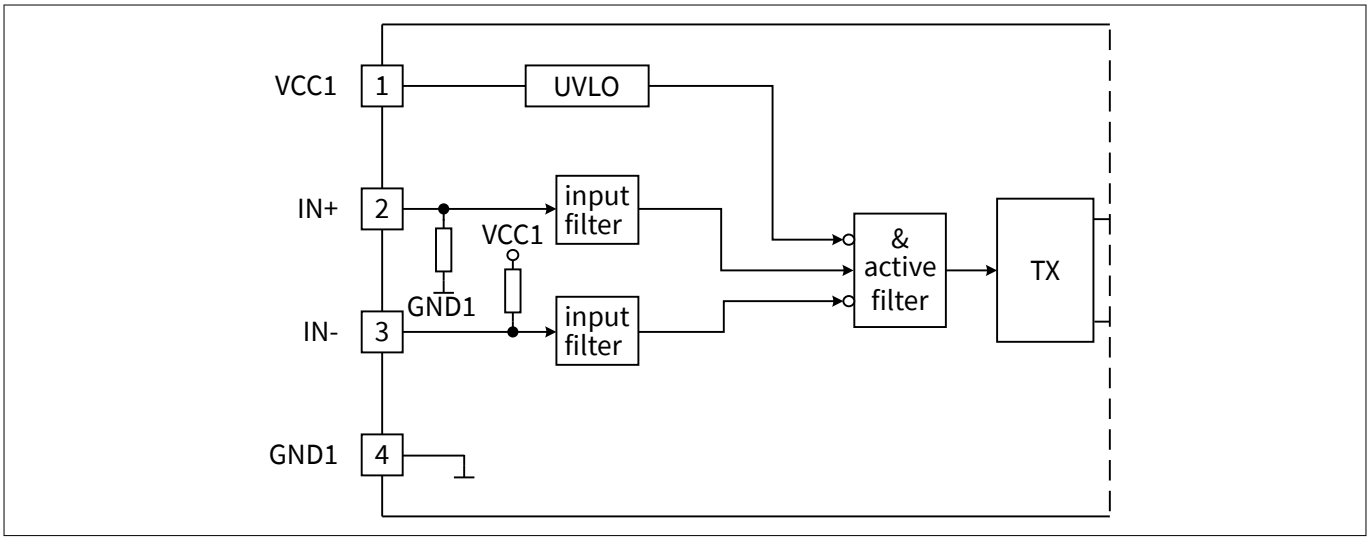

Figure 1 Block diagram of input section

The gate driver IC input section consists of the following functional blocks:

- input undervoltage lockout circuit
- signal filtering
- pull-up resistor for inverting input
- pull-down resistor for non-inverting input
- signal transmission to isolated output section

2.1 Input supply and undervoltage lockout (UVLO)

The input supply range has absolute maximum ratings of -0.3 V to 17 V. Static operation beyond the absolute maximum voltage (abs max) damages internal structures and is therefore considered a forbidden area.

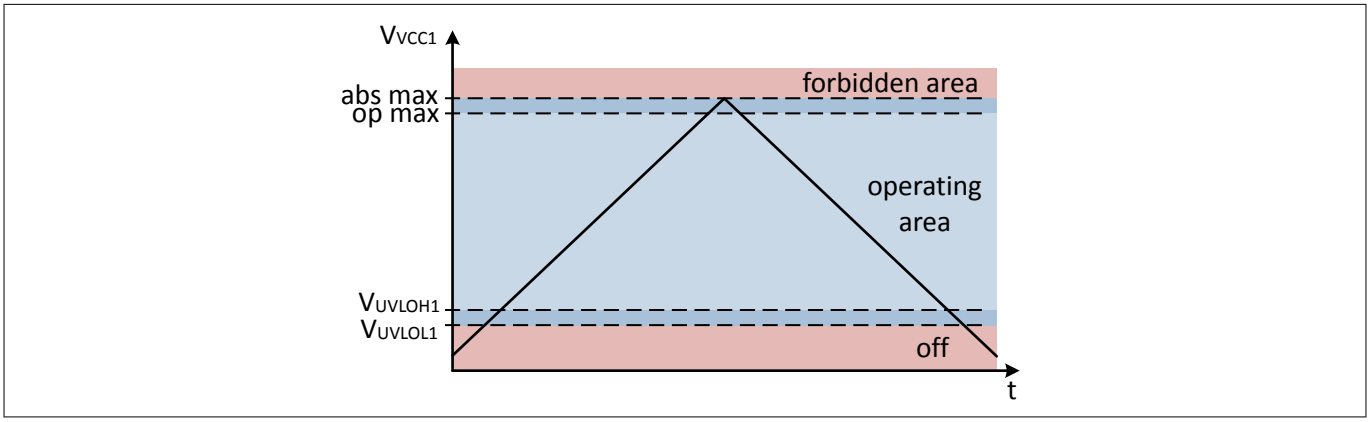

Figure 2 Input supply areas and UVLO threshold

At a crossing of the turn on undervoltage lockout threshold(V_{UVLOH1}) during a positive ramp at *VCC1* pin, the input section starts to operate. It evaluates the input signals *IN+* and *IN-* and transmits their current state to the output section. During V_{VCC1} ramp down and crossing of the turn-off undervoltage lockout threshold (V_{UVLOL1}), the input section will send a final off signal regardless of the *IN+* or *IN-* state. V_{UVLOL1} and V_{UVLOH1} form a hysteresis which offers stable operation even at low levels.

Any voltage overshoot above the absolute maximum voltage (abs max) rating can damage the driver circuits. In this area, the current consumption increases dramatically and therefore results in a violation of the maximum allowed input power loss. The operating area is defined between the turn-on undervoltage lockout threshold (V_{UVLOH1}) and the maximum operating voltage (op max).

2.2 Pull-up and pull-down resistor for input signals

The input pull-up or pull-down resistors ensure an off state in case the corresponding input is not connected. These resistors have a minimum value of 50 kΩ. Even with the maximum allowed voltage at *VCC1* pin, the input current due to these resistors stays below 1 mA.

The pull-up and pull-down resistors are designed to be connected to an external supply or ground potential for permanent activation of the individual driver input.

2.3 Input signal filtering (active filter)

The input section of the driver IC filters both input signals to suppress short pulses triggered by external influences.

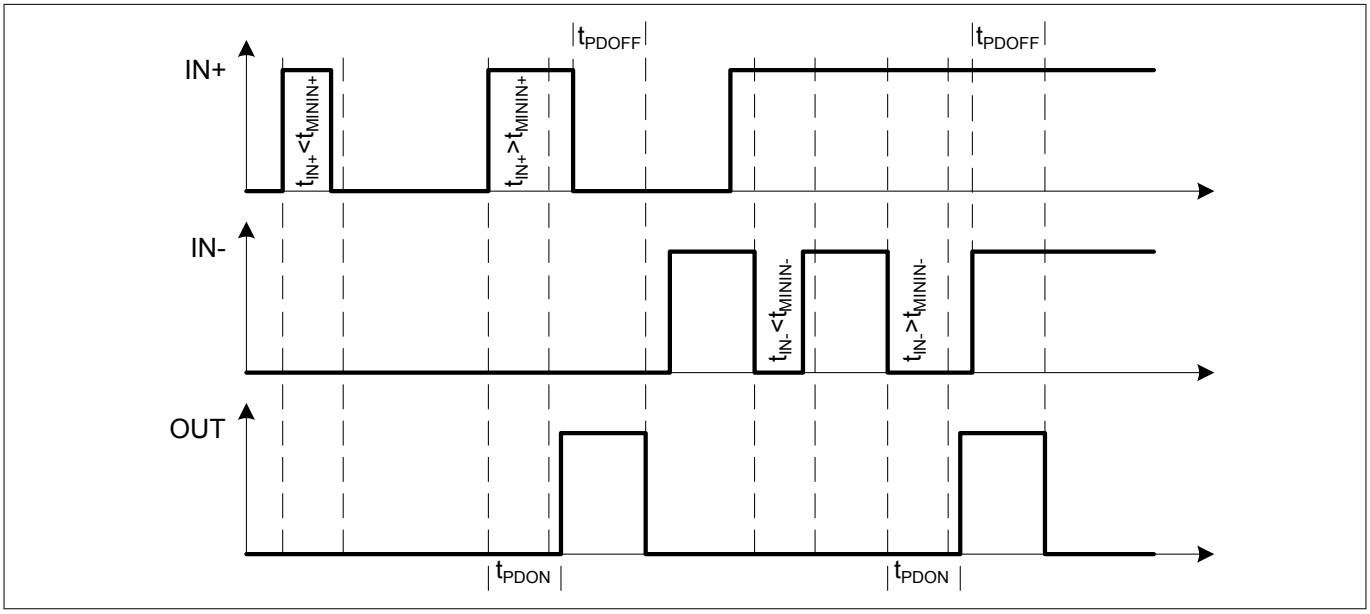

Figure 3 Input pulse suppression and turn-on/turn-off propagation delay

Every pulse at *IN+* shorter than the input pulse suppression time for pin *IN+* (t_{MININ+}) will be filtered and won't be transmitted to the output chip. Longer pulses will be sent to the output with the shown propagation delay t_{PDON} and t_{PDOFF}. The same behavior is implemented at *IN-*. Every pulse shorter than the input pulse suppression time for *IN-* (t_{MININ-}) will be omitted, and longer pulses transmitted with the same propagation delay.

Table 1 Typical filter and propagation delay times

The 1ED-X3 Compact family offers two dedicated input filter times resulting also in two different propagation delay times.

Product name	Input pulse suppression time (typical)	Propagation delay time (typical)
1ED3131MU12H	200 ns	270 ns
1ED312xMU12H	35 ns	90 ns

2.4 Application usage of *IN+* and *IN-*

The inverting (*IN-*) and non-inverting (*IN+*) input pins offer multiple possibilities to connect PWM input and logic signals for various control and protection uses.

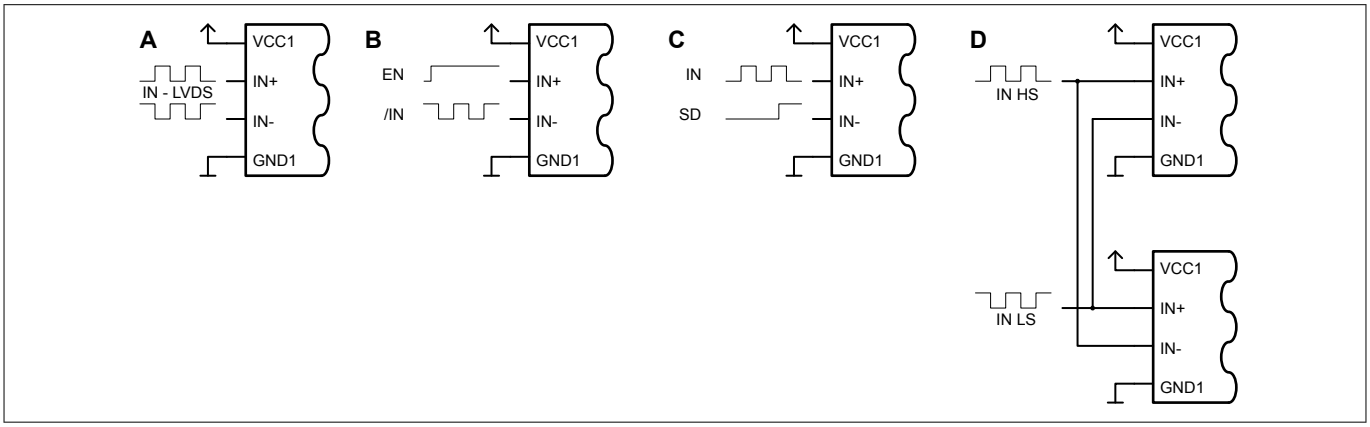

Figure 4 Input *IN+* and *IN-* usage

Apart from using both inputs with a differential signal (A) (*VCC1* and *GND1* levels), using only one input signal for actual switch control leaves the second input available for functions like Enable (B), Shutdown (C) or Interlock (D).

A) Differential signal

Applying a logic-level differential signal on both *IN+* and *IN-* with the positive level of *VCC1* pin and the negative level of *GND1* pin improves common-mode noise rejection.

B) Enable

Using the *IN+* pin as enable signal leaves the *IN-* to control the output PWM with an inverted logic input signal. The enable signal can then be shared between gate driver ICs of a complete inverter to start operation with a single control signal.

C) Shutdown

Using the *IN-* pin as shutdown signal leaves the *IN+* to control the output PWM with a non-inverted logic input signal. The shutdown signal can then be shared between gate driver ICs of a complete inverter to interrupt operation with a single control signal.

D) Interlock

Interlocking is often used in half-bridge configurations to avoid a shoot through current from the high-voltage DC bus supply. Connecting the following input signal pins of the top and bottom driver IC together inhibits a static turn-on for both channels at the same time

- top driver non-inverting input (*IN+*) with the bottom driver inverting input (*IN-*)
- bottom driver non-inverting input (*IN+*) with the top driver inverting input (*IN-*)

Dynamic turn-on and off characteristics of gate drivers and power switches can still lead to short-term shoot though. To avoid overlapping turn-on times at the power switches, a proper deadtime setting for the PWM generation at the microcontroller is recommended.

3 Output features

This section describes the gate driver output section of the variants with separate source/sink outputs and variants with single output and active Miller clamp functionality.

3.1 Output supply and undervoltage lockout (UVLO)

The output supply range has a positive absolute maximum rating of 40 V for all variants. The gate driver ICs are therefore capable of providing a bipolar gate voltage to a connected power switch.

Table 2 Output undervoltage lockout threshold levels

The undervoltage lockout thresholds of the different gate driver variants are optimized to be used with either IGBT or MOS-based switches. Nevertheless, all variants provide unlimited functionality for use with both IGBT as well as MOSFETs.

Parameter	Symbol	Value	Unit
1ED3120, 1ED3122, and 1ED3123 maximum turn-on level	$V_{UVLOH2,1}$	10.0	V
1ED3120, 1ED3122, and 1ED3123 minimum turn-off level	$V_{UVLOL2,1}$	8.0	V
1ED3121, 1ED3124, 1ED3125, and 1ED3131 maximum turn-on level	$V_{UVLOH2,2}$	12.5	V
1ED3121, 1ED3124, 1ED3125, and 1ED3131 minimum turn-off level	$V_{UVLOL2,2}$	10.5	V

3.2 Active shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a free-floating gate of a connected power switch to trigger a turn-on.

An external R_{GE} usually provides this protection. The active shutdown function is implemented in all variants and renders the use of this external resistor unnecessary.

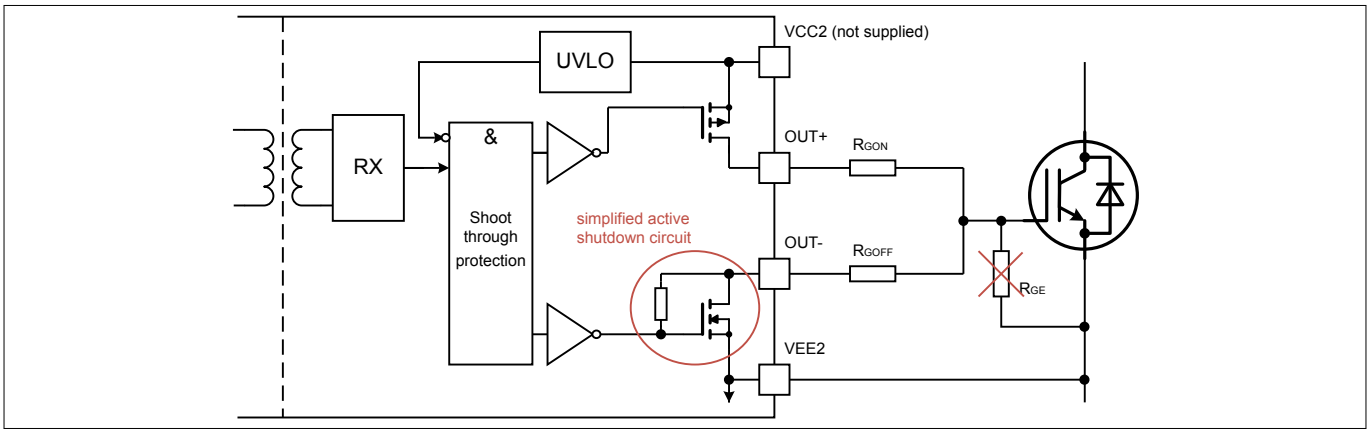

Figure 5 Block diagram of separate output variant showing active shutdown

In case of a missing or collapsing power supply at the *VCC2* pin, the output section of the driver operates in the active shutdown mode. In this case the driver uses the floating voltage of the connected gate to supply this internal circuit. The maximum pull-down current in this mode is approximately 10% of the rated output current of the individual driver variant. This solution is by far stronger than using the external R_{GE}.

3.3 Separate source and sink output variants

With separated outputs for current sourcing and sinking in a gate driver IC, individual gate resistors can be used for turning a power switch on and off.

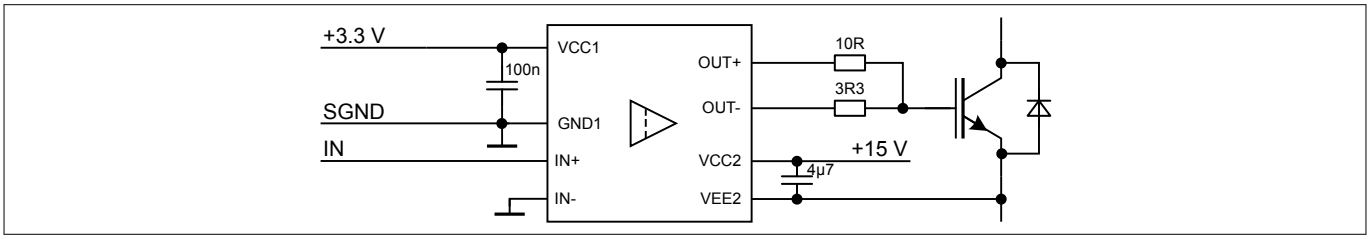

Figure 6 Circuit example for separate output variants

This optimization for a dedicated application saves a bypass diode for each power switch used.

It also helps reduce the gate loop by minimizing the number of components between the gate driver and the power switch. It minimizes as well the required PCB space as well. An additional benefit of two separated gate resistors is the power loss distribution. Because each of the two resistors is only active during turn-on or turn-off, the power loss in each individual resistor is only halved compared to a single gate-resistor solution.

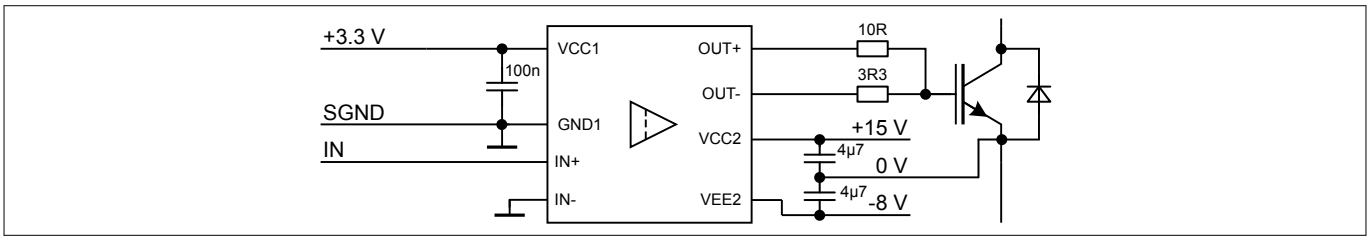

Figure 7 Circuit example for separate output variants for bipolar supply

The variants with separate outputs are able to operate with a supply voltage of up to 35 V between *VCC2* and *VEE2* pins. This allows a gate switching with for example 0 V to +15 V, -8 V to +15 V or -15 V to +15 V.

The connection of any voltage supply needs to connect the positive voltage to *VCC2* pin, the negative voltage to *VEE2* pin, and the reference supply pin to the emitter of an IGBT. This common ground level is then unknown to the driver IC, and therefore the UVLO protection is referenced to the negative supply.

3.4 *OUT* with *CLAMP* variants

In these variants a common output for turn-on and turn-off is combined with a separate pin for active Miller clamping. The variants with output and *CLAMP* are able to operate with a supply voltage of up to 35 V between *VCC2* and *VEE2*

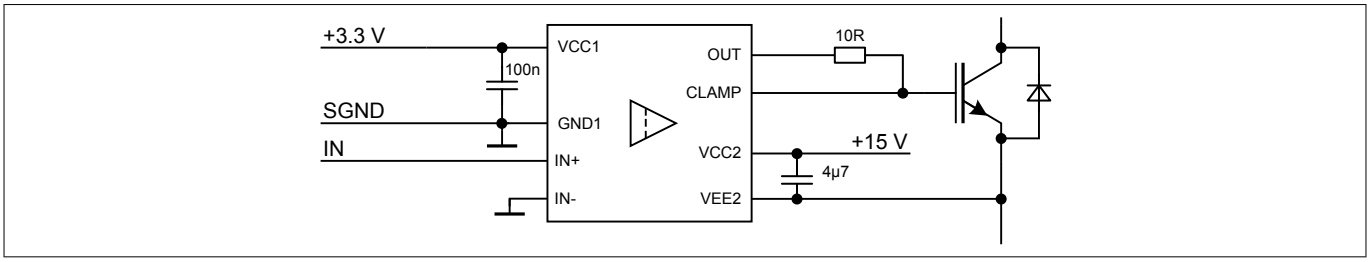

Figure 8 Circuit example for output with CLAMP variants

The active Miller clamping function reduces the risk of a parasitic turn-on during a high dv_{CE}/dt transition at the connected IGBT. Displacement currents through the intrinsic gate-collector (C_{GC}) and gate-emitter (C_{GE}) capacitances can lead to an increase at v_{GATE}. If the voltage reaches the IGBT threshold, a dynamic turn-on of

the power switch occurs. It stays on until the regular discharge path through R_G can reduce the gate voltage again.

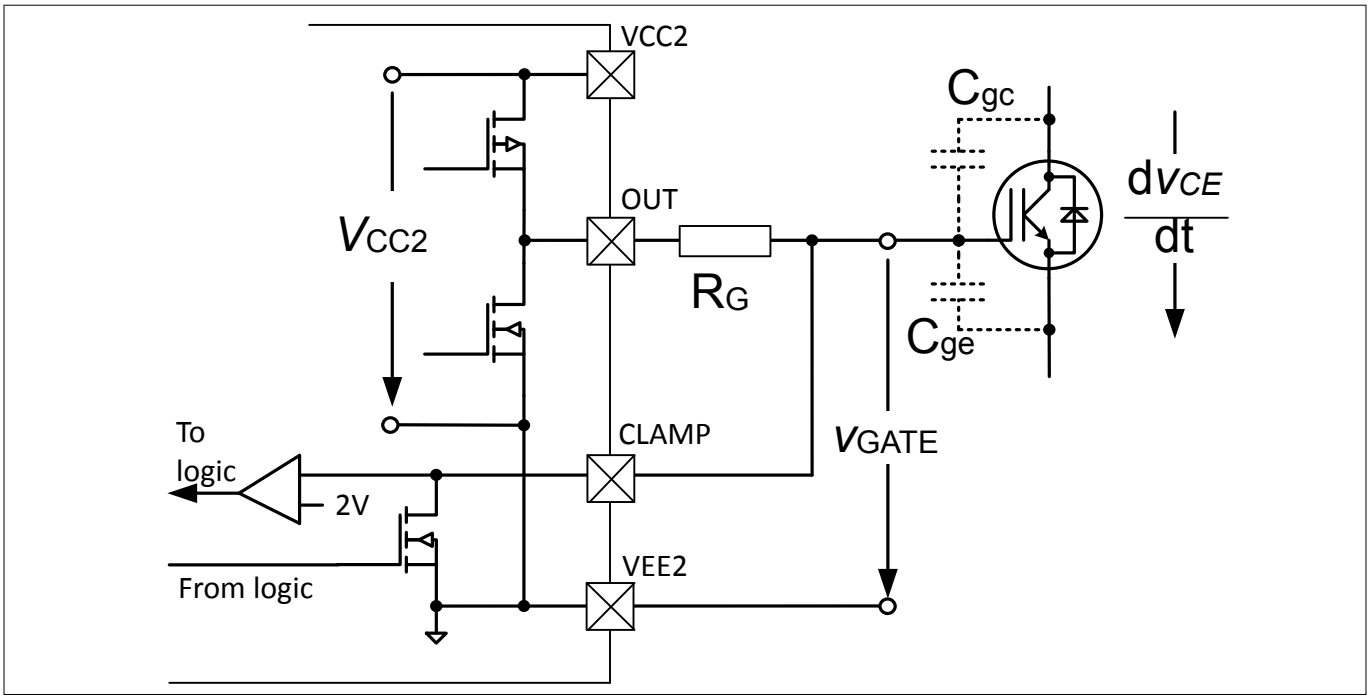

Figure 9 Output block diagram for CLAMP variants

The implemented CLAMP function of this gate driver IC monitors the gate voltage during driver off state. It activates the additional discharge path between *CLAMP* and *VEE2* as soon as the gate voltage drops below 2 V. The clamping circuit stays active until the gate driver is turned on again. To achieve the most effective clamping results, the circuit layout between the gate and *CLAMP* pin has to be optimized for lowest possible inductance.

4 Design aspects

The design aspects describe gate resistor and output supply capacitor selection as well as the power dissipation estimation for a selected design.

4.1 Output supply capacitor selection

A general design rule for the location of the driver output supply capacitor is always as close to the IC's supply pins *VCC2* and *VEE2* as possible.

Additionally, the value of the capacitor needs to be big enough to limit the voltage drop during the power switch turn-on. The following equation helps to calculate a first approximation for this capacitor.

$$C_2 = \frac{I_{Q2} \cdot t_p + Q_G}{\Delta V_{CC}} \cdot 1.2$$

Equation 1

I_{Q2} is the gate driver supply current, t_P the period of the switching frequency, Q_G the total gate charge at the selected operating condition, and ΔV_{CC} the maximum allowable voltage variation. The additional margin of 20% covers typical tolerances of capacitor and gate charge parameters.

Calculating this for the 100 A module FP100R12KT4 with Q_G = 800 nC, a switching frequency of f_{sw} = 15 kHz and an acceptable voltage variation of ΔV_{CC} = 0.2 V results in

$$C_2 = \frac{4\ \text{mA} \cdot 67\ \mu\text{s} + 800\ \text{nC}}{200\ \text{mV}} \cdot 1.2$$

$$C_2 = 5.6\ \mu\text{F}$$

Equation 2

4.2 Gate resistor selection

To optimize the gate resistor, it is recommended to have the appropriate gate charge diagram of the IGBT used and the output characteristic of the gate driver available. Both diagrams depend on operation conditions such as DC-link voltage (V_{DC}), collector current (I_C) and operating temperature.

The following representative diagrams show typical behaviors of an IGBT and the gate driver IC output without scale.

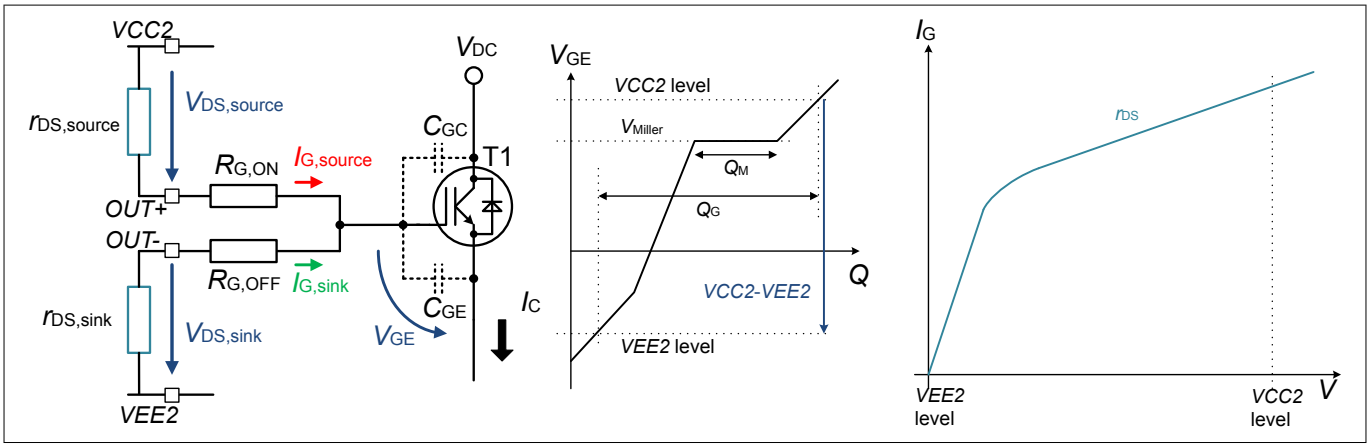

Figure 10 Simplified gate circuit, IGBT gate charge diagram and driver output characteristics

The MOSFET-based gate driver outputs can be simplified as dynamic resistors ($r_{DS,source}$; $r_{DS,sink}$) with a voltage drop ($V_{DS,source}$; $V_{DS,sink}$) during switching. The total gate charge (Q_G) and the Miller charge (Q_M) can be extracted from the gate charge diagram using the given gate driver supply V_{CC2} and DC-link voltage.

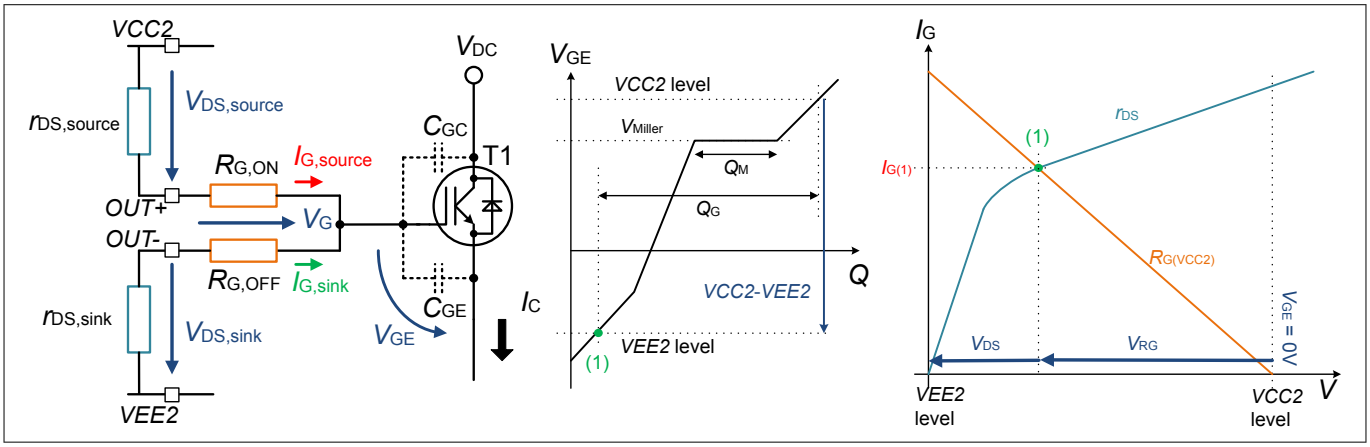

Figure 11 Simplified gate circuit turn-on event: Initial phase

In the initial phase of an IGBT turn-on event the gate is discharged and at the level of the *VEE2* pin. In the diagram this is marked with (1). Therefore the total gate supply voltage is split between the inner gate driver resistance ($r_{DS,source}$) and the turn-on gate resistor ($R_{G,ON}$). The graphical solution shows the initial gate current ($I_{G(1)}$) which can be located in the linear or in the saturated region of the gate driver output characteristic. This maximum current can also be used to select the appropriate pulse current class for the gate resistor.

Immediately after the initial phase, the gate current starts to fall, following the crossing point of the output characteristic curve and the parallel translated gate resistor line while the gate-emitter voltage (V_{GE}) charges up.

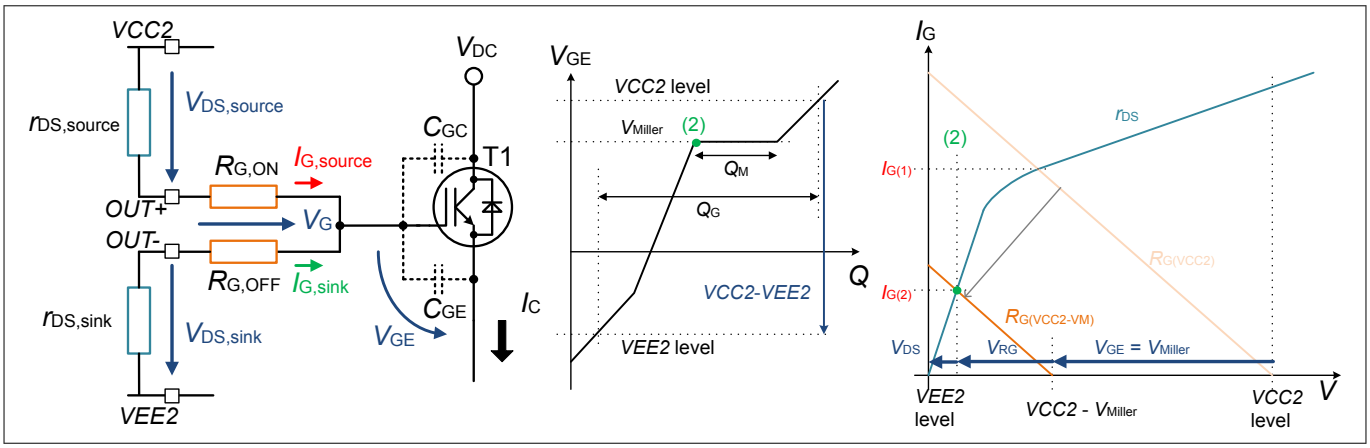

Figure 12 Simplified gate circuit turn-on event at Miller plateau

Beginning with the Miller plateau, marked with (2) above, the gate-emitter voltage remains nearly constant while the transistor is reducing the collector-emitter voltage to its saturation level.

Given the condition at that phase, the resulting gate current is constant allowing a collector-emitter voltage transition time (t_{ON}) calculation with the following formula:

$$t_{ON} = \frac{\left(R_{G,ON} + r_{DS,source(2)}\right)}{\left(V_{CC2} - V_M\right)} \cdot Q_M$$

$$t_{ON} = \frac{1}{I_{G(2)}} \cdot Q_M$$

Equation 3

Tuning the value of a gate resistor requires extensive knowledge of all the parasitics in the gate circuit. It is therefore an iterative process of adjusting between switching losses and EMI.

4.3 Power dissipation estimation

Apart from the power losses in the gate resistor during switching of any power switch, there is also considerable power loss inside the driver IC.

Every package can achieve a maximum power dissipation at a certain operating condition without exceeding the maximum junction temperature. The internal power loss of the output section (P_{OUT}) of the gate driver IC can be estimated as follows:

$$P_{OUT} = P_Q + P_{source} + P_{sink}$$

Equation 4

P_Q is the operating power loss of the driver output stage. It is easily calculated by the operating supply current (I_{Q2}) and the supply voltage V_{CC2}between *VCC2* and *VEE2* pins:

$$P_Q = I_{Q2} \cdot V_{CC2}$$

Equation 5

The turn-on (P_{source}) and turn-off (P_{sink}) losses can be estimated using the resistive voltage divider between inner gate driver resistance (R_{DS}) and outer gate resistor (R_G) with the total gate charge (Q_G) and switching frequency (f_{sw}):

4 Design aspects

$$P_{source} = \frac{1}{2} Q_G \cdot f_{sw} \cdot V_{CC2} \cdot \frac{R_{DS,source}}{R_{DS,source} + R_{G,ON}}$$

$$P_{sink} = \frac{1}{2} Q_G \cdot f_{sw} \cdot V_{CC2} \cdot \frac{R_{DS,sink}}{R_{DS,sink} + R_{G,OFF}}$$

Equation 6

Table 3 Gate driver output resistance

Driver type	$R_{DS,source}$ output resistance		$R_{DS,sink}$ output resistance	
	typ [Ω]	max [Ω]	typ [Ω]	max [Ω]
1ED3120MU12H, 1ED3121MU12H, 1ED3131MU12H	0.95	4.3	0.75	5.0
1ED3122MU12H	0.55	2.2	0.45	2.7
1ED3123MU12H, 1ED3124MU12H	0.45	1.4	0.35	1.7

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-04-07

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-imf1564570884580

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury