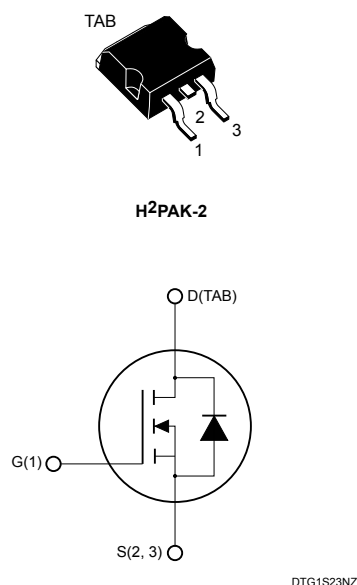


Automotive N-channel 100 V, 1.9 mΩ max., 292 A STripFET F8 Power MOSFET in an H²PAK-2 package



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH285N10F8-2AG	100 V	1.9 mΩ	292 A

- AEC-Q101 qualified
- 175 °C maximum operating junction temperature
- 100% avalanche tested
- Excellent FoM (figure of merit)

Applications

- Automotive motor control
- Electro mobility

Description

The **STH285N10F8-2AG** is a 100 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure. It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.



Product status link

[STH285N10F8-2AG](#)

Product summary

Order code	STH285N10F8-2AG
Marking ⁽¹⁾	285N10F8
Package	H ² PAK-2
Packing	Tape and reel

1. Engineering samples are clearly identified with a dedicated special symbol in the marking of each unit.

1 Electrical ratings

Table 1. Absolute maximum ratings (at $T_C = 25\text{ °C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$ ⁽²⁾	292	A
	Drain current (continuous) at $T_C = 100\text{ °C}$ ⁽²⁾	206	
	Drain current (continuous) at $T_C = 25\text{ °C}$ ⁽³⁾	240	
$I_{DM}^{(1)(2)(4)}$	Drain current (pulsed), $t_P = 10\text{ }\mu\text{s}$	1170	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	341	W
I_{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	90	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = 90\text{ A}$, $R_G = 25\text{ }\Omega$)	600	mJ
T_J	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

1. Specified by design, not tested in production.
2. This is the theoretical current value only related to the silicon.
3. This current value is limited by package.
4. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	14.8	$^{\circ}\text{C/W}$
R_{thJC}	Thermal resistance, junction-to-case	0.44	$^{\circ}\text{C/W}$

1. Defined according to JEDEC standards (JESD51-5, -7).

2 Electrical characteristics

$T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 90\text{ A}$		1.5	1.9	m Ω

1. Specified by design and evaluated by characterization, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	11200	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	2400	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	99	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 180\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	177	-	nC
$Q_{gs}^{(1)}$	Gate-source charge		-	53	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge		-	44	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 90\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	40	-	ns
$t_r^{(1)}$	Rise time		-	40	-	ns
$t_{d(off)}^{(1)}$	Turn-off delay time		-	95	-	ns
$t_f^{(1)}$	Fall time		-	35	-	ns

1. Specified by design and evaluated by characterization, not tested in production.

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)(2)}$	Forward on current (continuous)	$T_C = 25\text{ °C}$	-		227	A
V_{SD}	Forward on voltage	$I_{SD} = 90\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.2	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_D = 90\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$	-	87		ns
$Q_{rr}^{(2)}$	Reverse recovery charge		-	212		nC
$I_{RRM}^{(2)}$	Reverse recovery current		-	4.9		A

1. This is the theoretical current value only related to the silicon.
2. Specified by design and evaluated by characterization, not tested in production.

2.1 Electrical characteristics (curves)

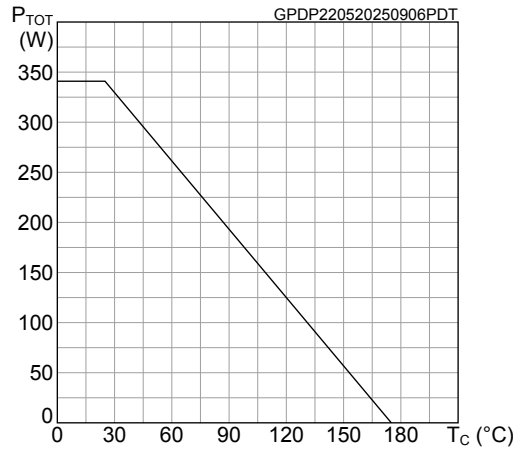
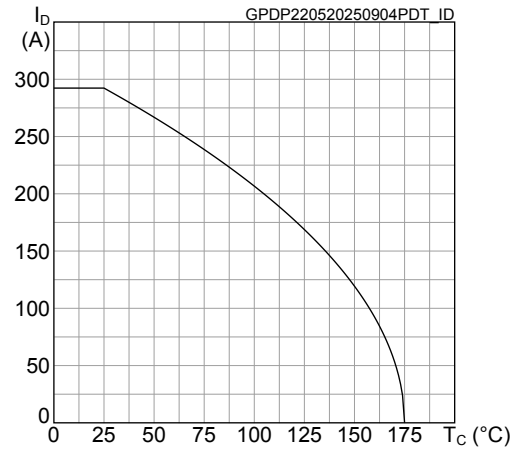
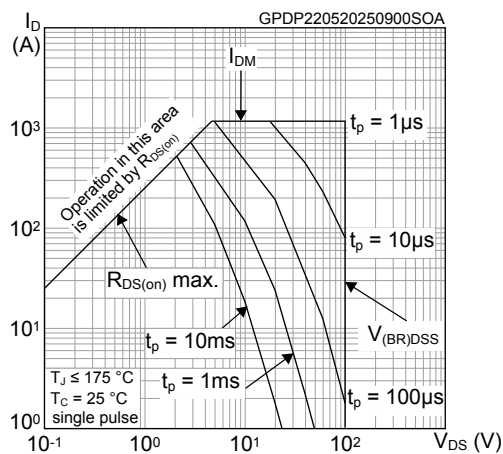
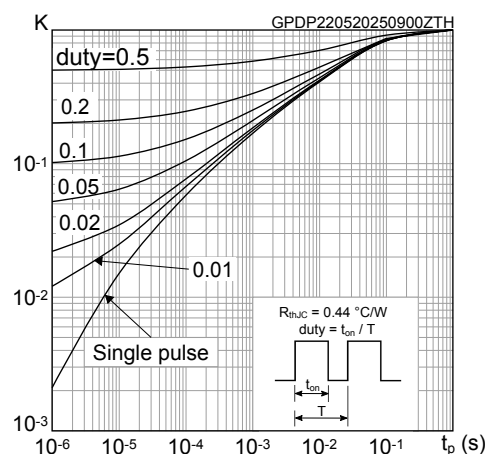
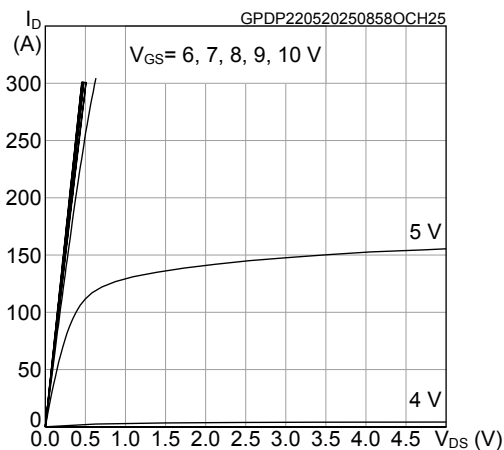
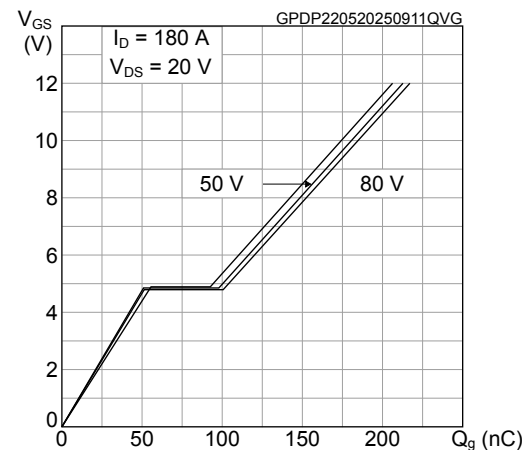
Figure 1. Total power dissipation vs temperature

Figure 2. Drain current vs case temperature

Figure 3. Safe operating area

Figure 4. Normalized transient thermal impedance

Figure 5. Typical output characteristics

Figure 6. Typical gate charge characteristics


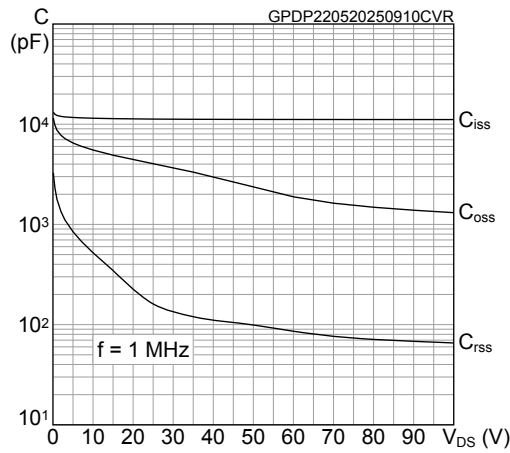
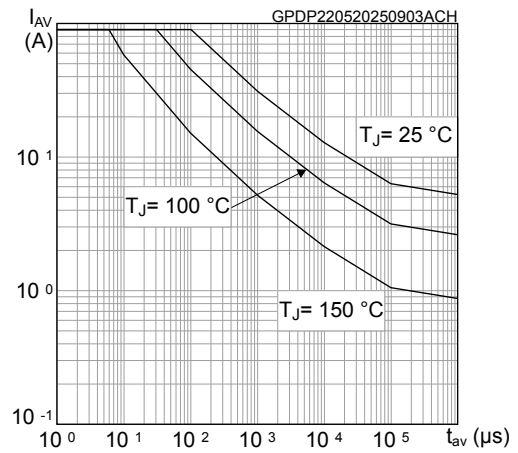
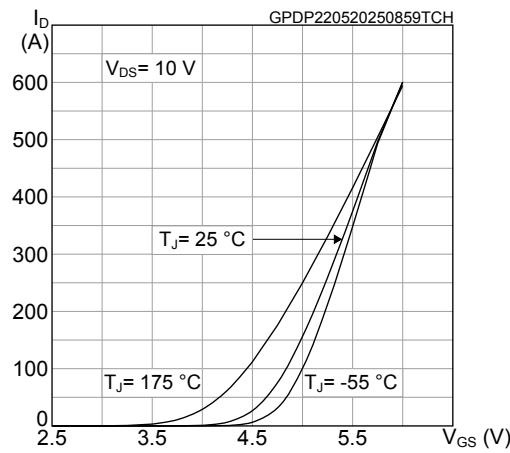
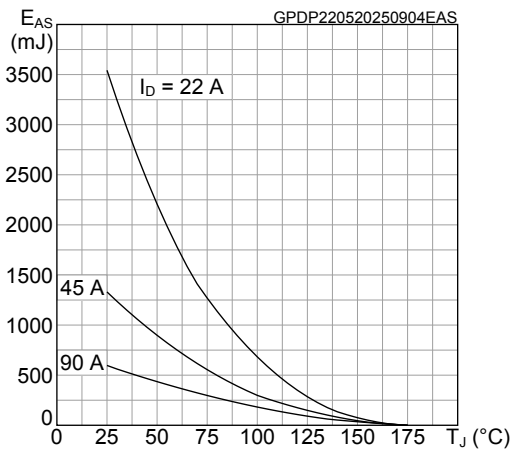
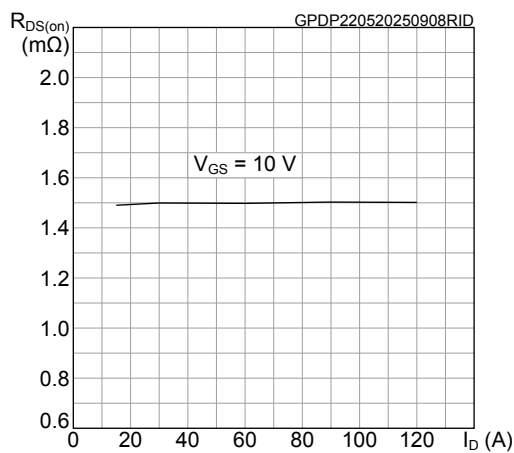
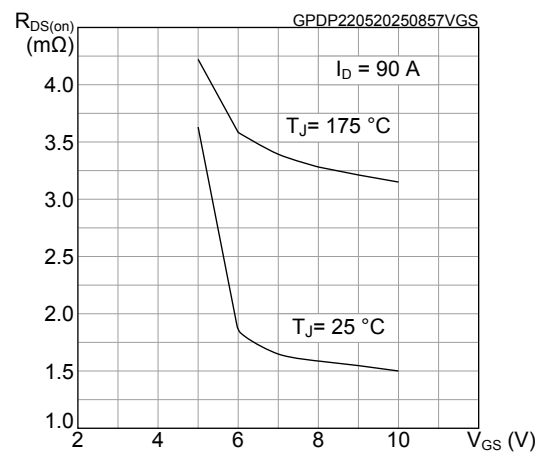
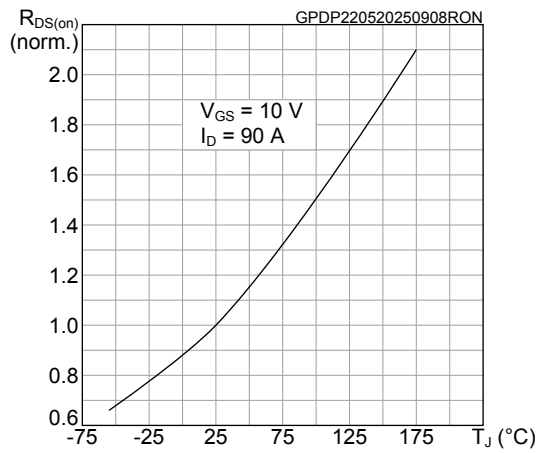
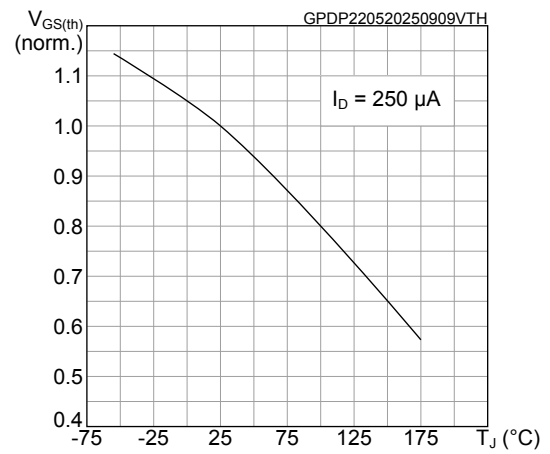
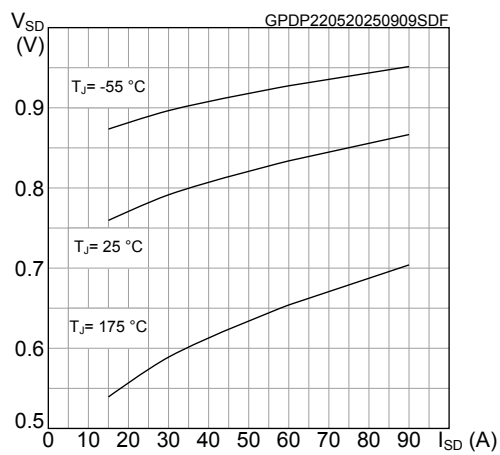
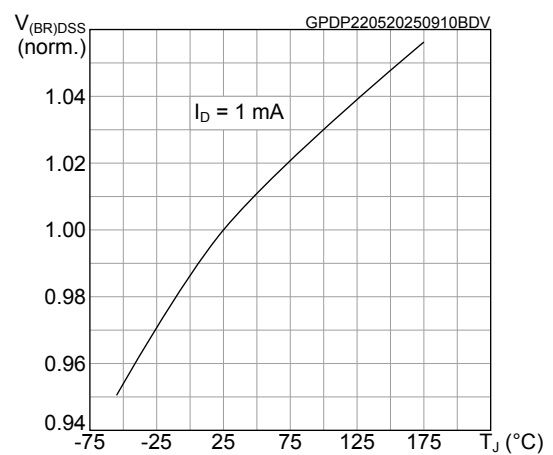
Figure 7. Typical capacitance characteristics

Figure 8. Avalanche characteristics

Figure 9. Typical transfer characteristics

Figure 10. Avalanche energy

Figure 11. Typical drain-source on-resistance

Figure 12. Typical on-resistance vs gate-source voltage


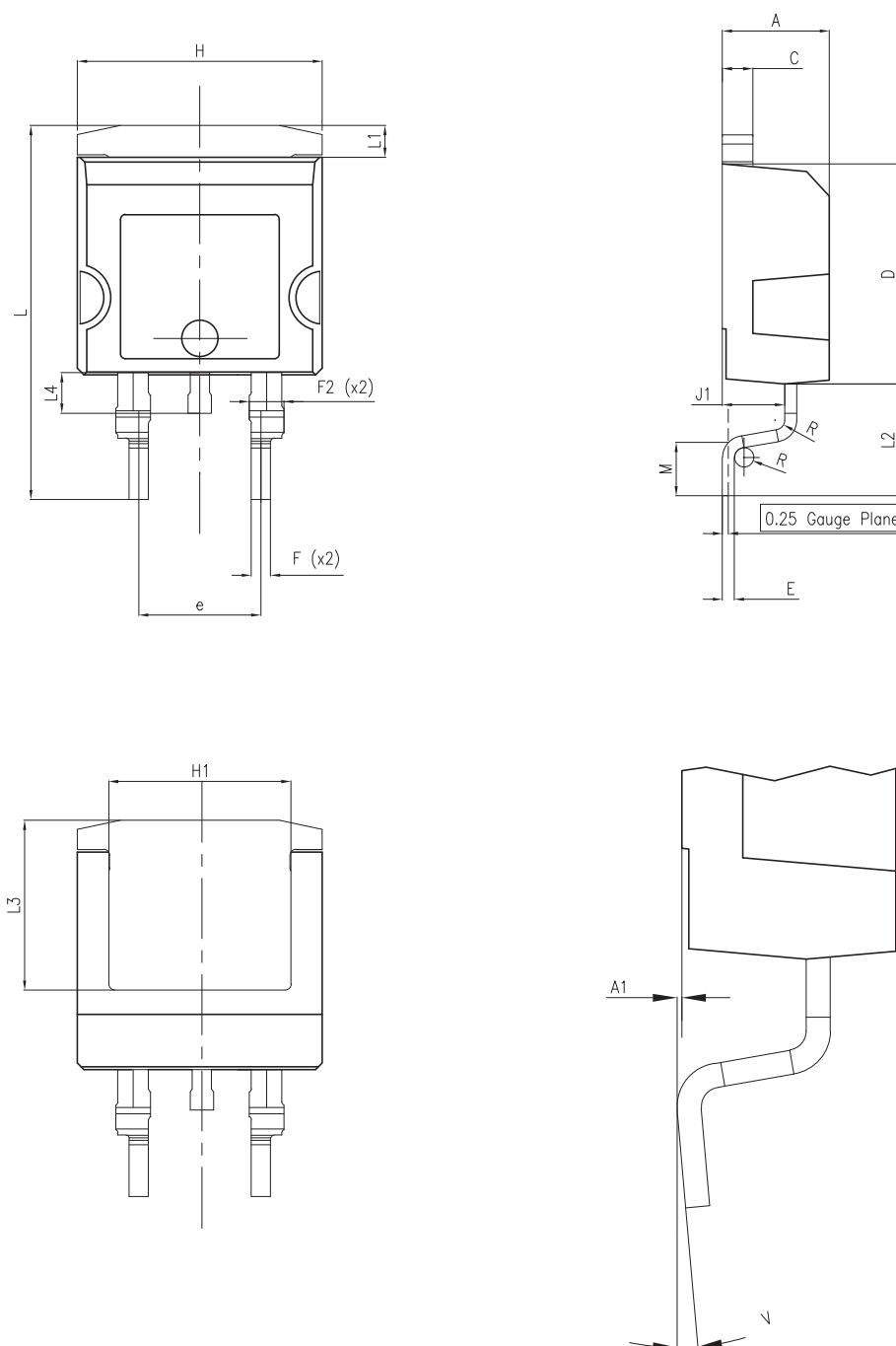
Figure 13. Normalized on-resistance vs temperature

Figure 14. Normalized gate threshold voltage vs temperature

Figure 15. Typical reverse diode forward characteristics

Figure 16. Normalized $V_{(BR)DSS}$ vs temperature


3 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 H²PAK-2 package information

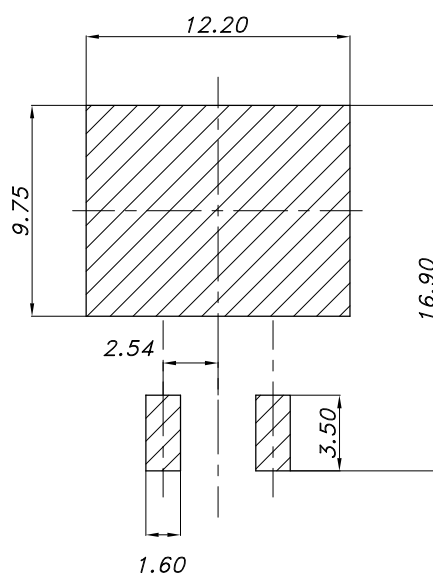
Figure 17. H²PAK-2 package outline



8159712_10

Table 7. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40		7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

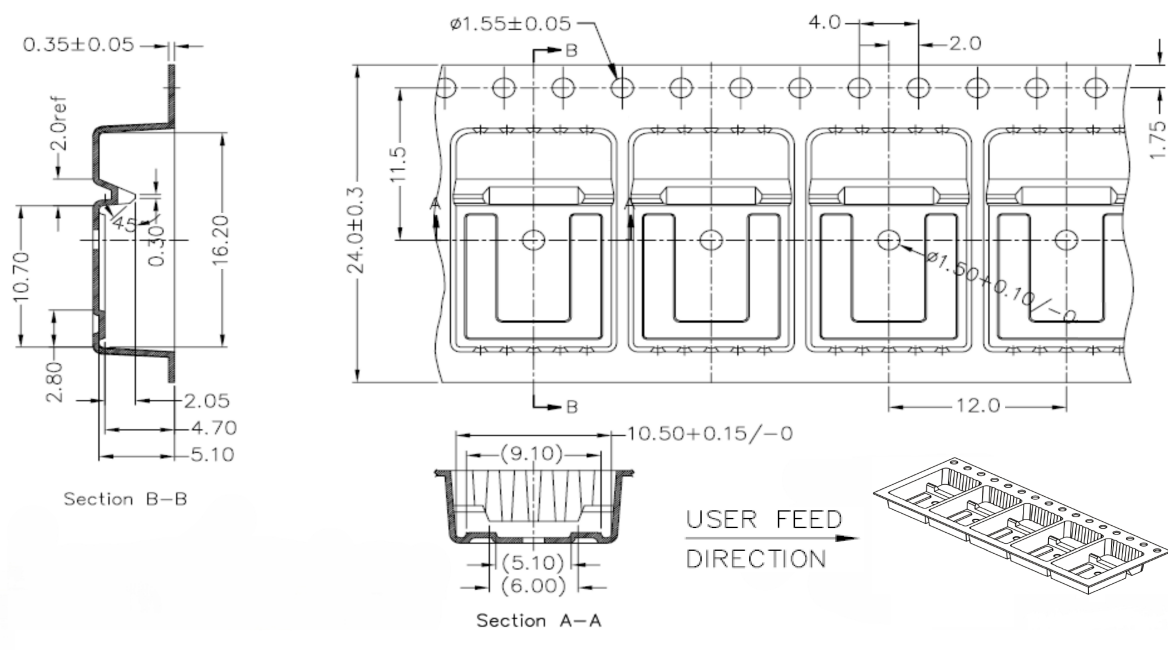
Figure 18. H²PAK-2 recommended footprint


8159712_10

Note: Dimensions are in mm.

3.2 H²PAK-2 packing information

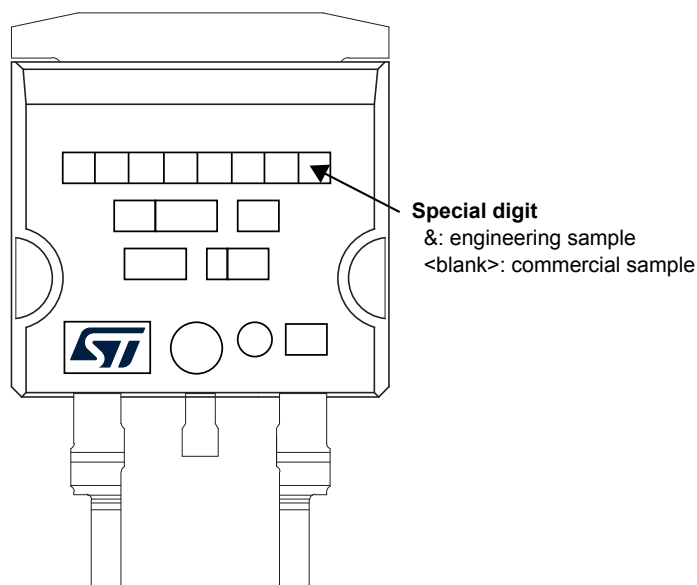
Figure 19. H²PAK-2 tape drawing (dimensions are in mm)



DM01095771_2

3.3 H²PAK-2 marking information

Figure 20. H²PAK-2 marking information



Note: *Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 8. Document revision history

Date	Revision	Changes
06-Nov-2024	1	First release.
02-Sep-2025	2	Updated title in cover page. Updated <i>Section 1: Electrical ratings</i> , <i>Section 2: Electrical characteristics</i> and <i>Section 2.1: Electrical characteristics (curves)</i> .
10-Nov-2025	3	Updated Table 2. Thermal data and Section 2.1: Electrical characteristics (curves) . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves)	5
3	Package information.....	8
3.1	H ² PAK-2 package information	8
3.2	H ² PAK-2 packing information.....	10
3.3	H ² PAK-2 marking information	10
	Revision history	11

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved