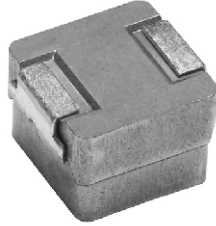


Low Profile, High Current IHLP® Inductors



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
 Several foreign patents, and other patents pending.

| STANDARD ELECTRICAL SPECIFICATIONS | | | | |
|---|------------------------------|------------------------------|--|--|
| L ₀ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (μH) | DCR TYP. 25 °C (mΩ) | DCR MAX. 25 °C (mΩ) | HEAT RATING CURRENT DC TYP. (A) ⁽³⁾ | SATURATION CURRENT DC TYP. (A) ⁽⁴⁾ |
| 0.56 | 3.4 | 3.6 | 20 | 12 |
| 0.68 | 4.2 | 4.5 | 18 | 11.5 |
| 0.82 | 4.6 | 4.9 | 16.5 | 13 |
| 1.0 | 5.6 | 6.5 | 13 | 15 |
| 1.5 | 8.6 | 9.0 | 12 | 12 |
| 2.2 | 13.0 | 13.6 | 10 | 10 |
| 3.3 | 19.9 | 20.9 | 8 | 8 |
| 4.7 | 28.9 | 30.3 | 6.5 | 7 |
| 5.6 | 32.7 | 34.4 | 6 | 7 |
| 6.8 | 42.5 | 44.6 | 5.5 | 5.5 |
| 8.2 | 48.3 | 50.7 | 5.0 | 5.0 |
| 10.0 | 67.9 | 71.3 | 4.5 | 4.5 |

Notes

- (1) All test data is referenced to 25 °C ambient
- (2) Operating temperature range - 55 °C to + 125 °C
- (3) DC current (A) that will cause an approximate ΔT of 40 °C
- (4) DC current (A) that will cause L₀ to drop approximately 20 %
- (5) The part temperature (ambient + temp rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.

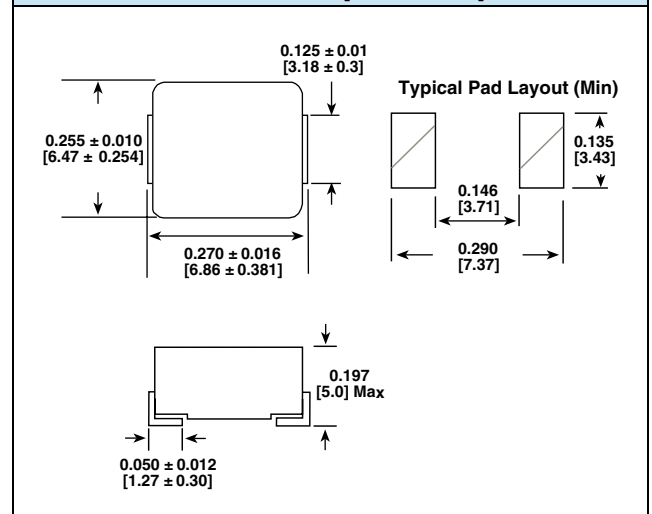
FEATURES

- Shielded construction
- Frequency range below 1.0 MHz
- Lowest DCR/μH, in this package size
- Powdered iron composition provides soft saturation
- Handles high transient current spikes without saturation
- Saturation and inductance extremely stable over temperature
- Ultra low buzz noise, due to composite construction
- Compliant to RoHS directive 2002/95/EC


RoHS
COMPLIANT

APPLICATIONS

- Notebook/desktop/server applications
- High current POL converters
- Low profile, high current power supplies
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)

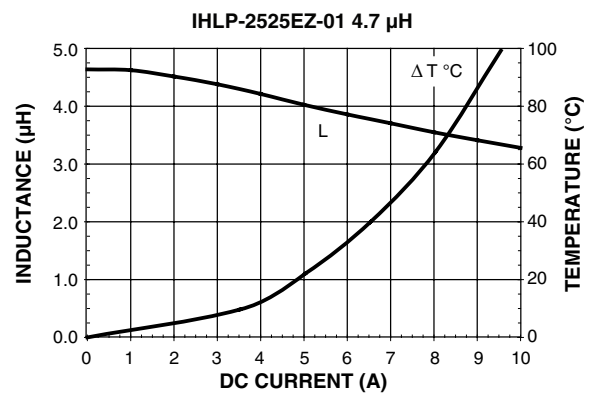
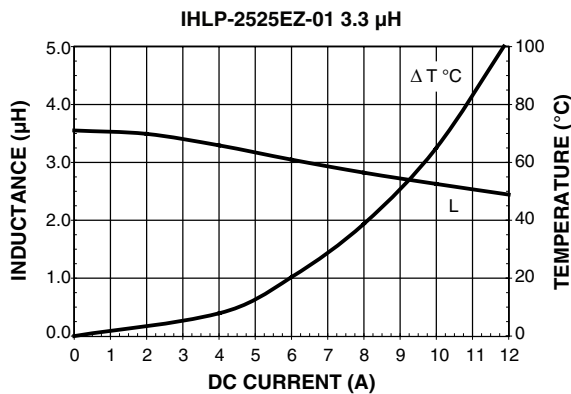
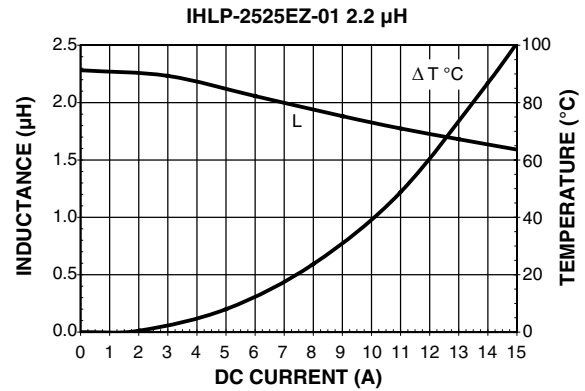
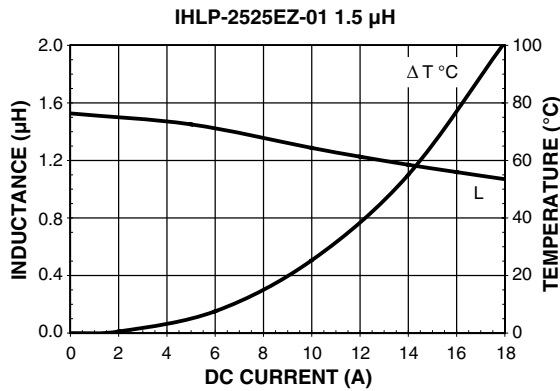
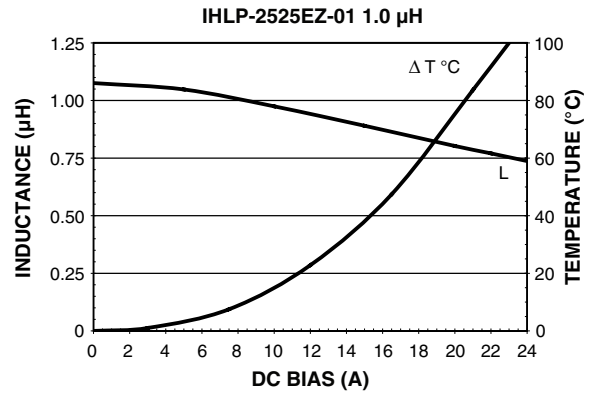
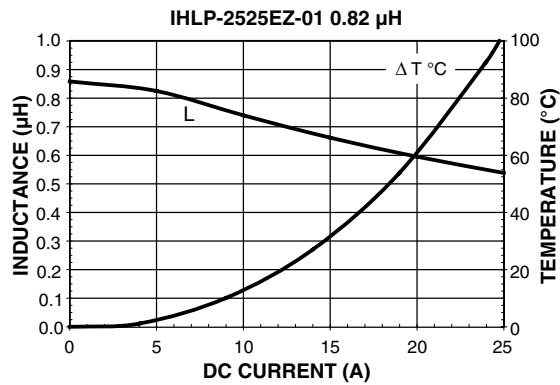
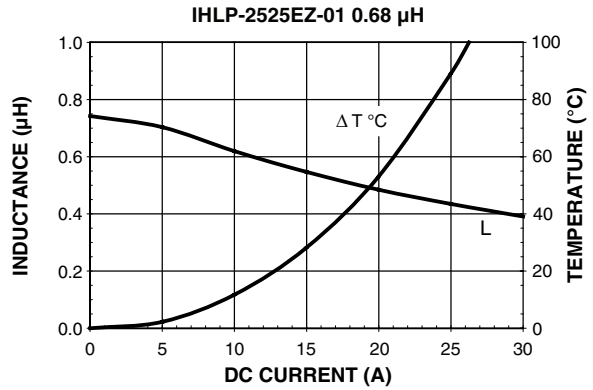
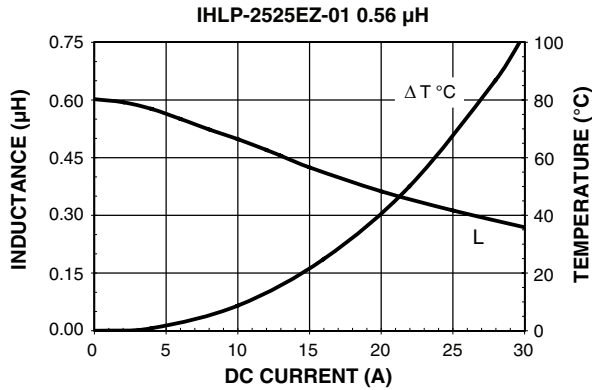
DIMENSIONS in inches [millimeters]

DESCRIPTION

| | | | | |
|----------------|------------------|----------------------|--------------|-------------------------------|
| IHLP-2525EZ-01 | 1.0 μH | ± 20 % | ER | e3 |
| MODEL | INDUCTANCE VALUE | INDUCTANCE TOLERANCE | PACKAGE CODE | JEDEC LEAD (Pb)-FREE STANDARD |

GLOBAL PART NUMBER

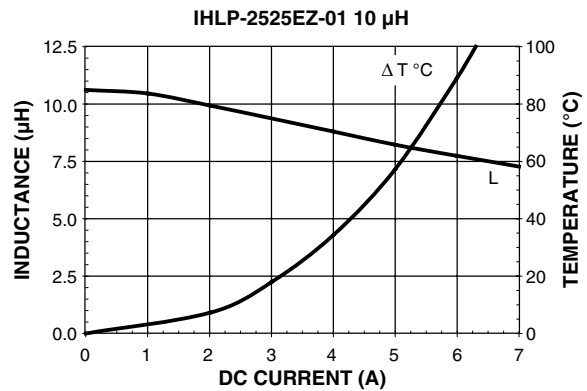
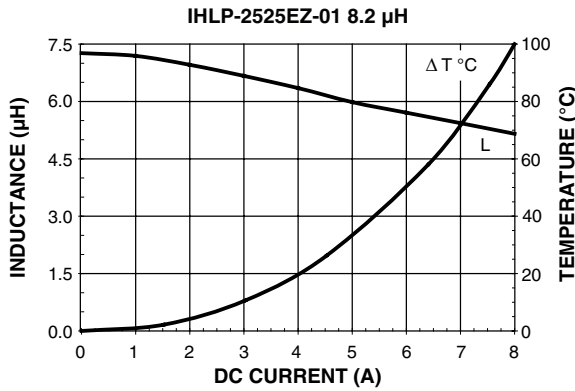
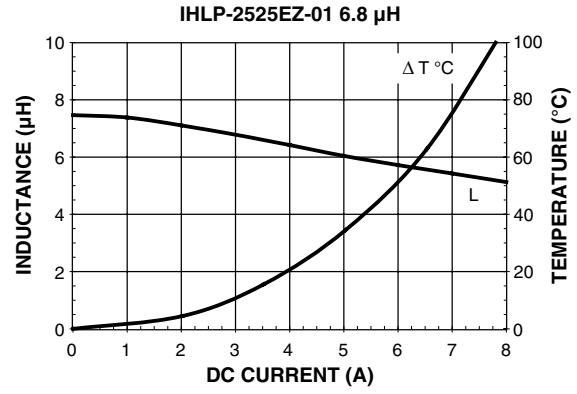
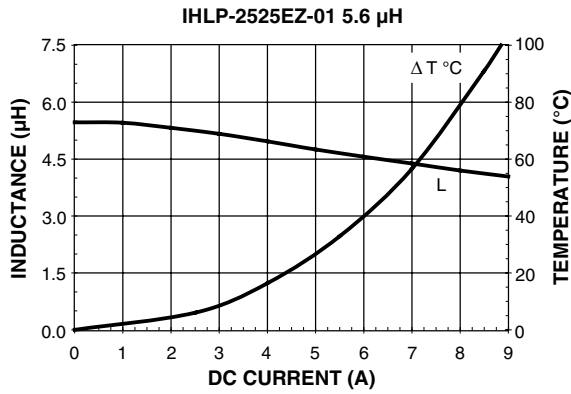
| | | | | | | | | | | | | | | | | | |
|----------------|---|---|---|------|---|---|---|--------------|---|------------------|---|---|------|---|--------|---|---|
| I | H | L | P | 2 | 5 | 2 | 5 | E | Z | E | R | 1 | R | 0 | M | 0 | 1 |
| PRODUCT FAMILY | | | | SIZE | | | | PACKAGE CODE | | INDUCTANCE VALUE | | | TOL. | | SERIES | | |

PERFORMANCE GRAPHS





PERFORMANCE GRAPHS





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