



MICROCHIP

**LAN8842 EDS2
Daughter Card
User Guide**

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at <https://www.microchip.com/en-us/about/legal-information/microchip-trademarks>.

ISBN: 979-8-3371-2497-1

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Table of Contents

Preface	5
Introduction.....	5
Document Layout	5
Conventions Used in this Guide	6
Warranty Registration.....	7
The Microchip Web Site	7
Development Systems Customer Change Notification Service	7
Customer Support	8
Document Revision History	8
 Chapter 1. Overview	
1.1 Introduction	9
1.2 Features	10
1.3 References	10
1.4 Acronyms and Definitions	10
 Chapter 2. Getting Started	
2.1 Introduction	13
2.2 Daughter Card Installation	13
2.3 Quick Start	17
2.4 LAN8842 EDS2 Daughter Card Removal	18
 Chapter 3. Hardware	
3.1 Introduction	19
3.2 Connectors	20
3.3 Test Points	21
3.4 LEDS	22
3.5 Configuration Straps	22
3.6 Reset	22
3.7 Clocks	23
3.8 Power	23
3.9 LAN8842 EDS2 Daughter Card EEPROM	24
 Chapter 4. System Boot	
4.1 Introduction	27
4.2 LAN8842 EDS2 System Power-Up	27
 Appendix A. Schematics	
A.1 Introduction	35

Appendix B. Bill of Materials

B.1 Introduction	41
------------------------	----

Appendix C. PCB Layers

C.1 Introduction	45
------------------------	----

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXA”, where “XXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the LAN8842 EDS2 Daughter Card User Guide. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [Warranty Registration](#)
- [The Microchip Web Site](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

This document features the LAN8842 EDS2 Daughter Card. The manual layout is as follows:

- **Chapter 1. “Overview”** – This chapter provides an overview of the LAN8842 EDS2 Daughter Card and a brief description of the card’s features.
- **Chapter 2. “Getting Started”** – This chapter provides information on the setup and operation of the LAN8842 EDS2 Daughter Card.
- **Chapter 3. “Hardware”** – This chapter shows the different connection types found on the LAN8842 EDS2 Daughter Card.
- **Chapter 4. “System Boot”** – This chapter explains how to utilize device tree overlays when booting the host system.
- **Appendix A. “Schematics”** – This section shows the schematic drawings of the LAN8842 EDS2 Daughter Card.
- **Appendix B. “Bill of Materials”** – This section shows the Bill of Materials (BOM) for the LAN8842 EDS2 Daughter Card.
- **Appendix C. “PCB Layers”** – This section shows the PCB layers of the LAN8842 EDS2 Daughter Card.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB[®] IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	<i>file.o</i> , where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] <i>file</i> [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending the Warranty Registration Card entitles users to receive new product updates. Interim software releases are available at the Microchip web site.

THE MICROCHIP WEB SITE

Microchip provides online support via our web site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

DEVELOPMENT SYSTEMS CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com, click on Customer Change Notification and follow the registration instructions.

The Development Systems product group categories are:

- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLAB C compilers; all MPLAB assemblers (including MPASM assembler); all MPLAB linkers (including MPLINK object linker); and all MPLAB librarians (including MPLIB object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICKit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at:

<http://www.microchip.com/support>

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003989A (12-05-25)	Initial release.	

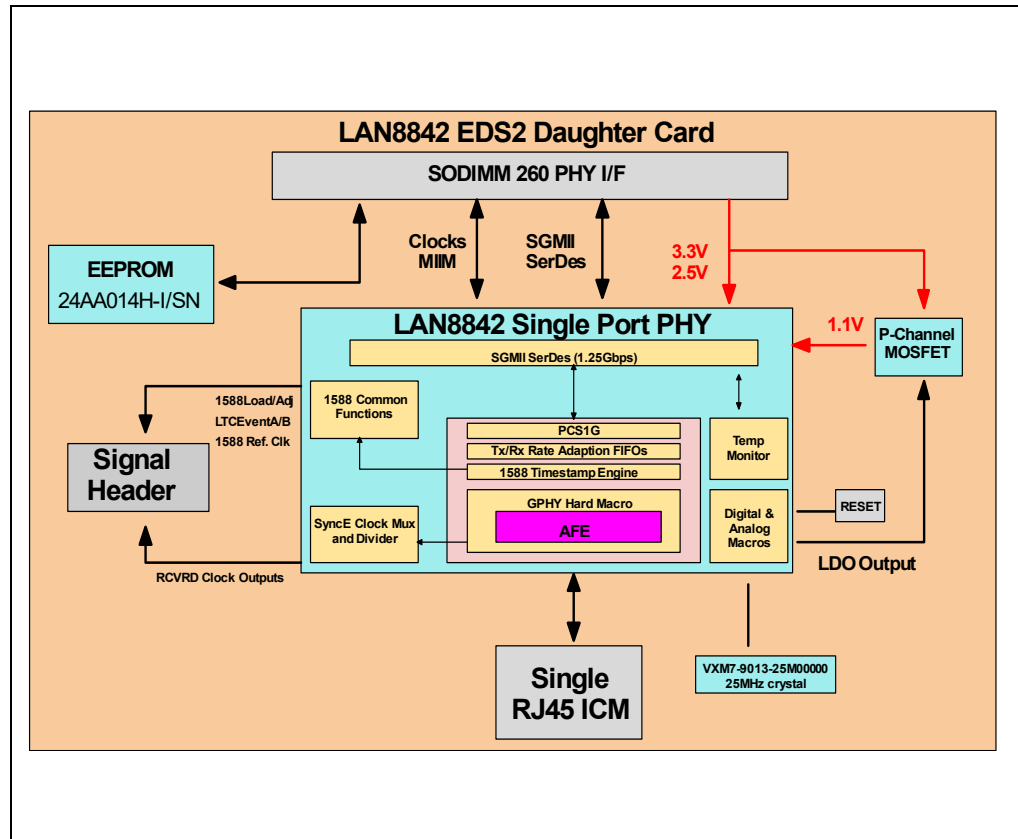
Chapter 1. Overview

1.1 INTRODUCTION

The LAN8842 EDS2 Daughter Card is designed for evaluation of the Microchip LAN8842 Gigabit Ethernet SGMII PHY when used with a Microchip EVB-LAN9668 EDS2 (EV83E85A) or other compatible host board. A SODIMM 260-pin socket (board fingers for the EDS2 host), the LAN8842 EDS2 Daughter Card interface is used due to its high performance, high pin count, and low cost.

This document describes the LAN8842 EDS2 Daughter Card setup and use with the EVB-LAN9668 EDS2 host. A simplified block diagram is shown in [Figure 1-1](#).

FIGURE 1-1: LAN8842 EDS2 DAUGHTER CARD BLOCK DIAGRAM



1.2 FEATURES

Below are the features of the LAN8842 EDS2 Daughter Card:

- Microchip LAN8842 Gigabit Ethernet PHY with SGMII
- Microchip VXM7-9032-25M0000 crystal for 25 MHz
- Microchip MIC33153 4 MHz Internal Inductor PWM regulator for 1.1V generation
- Microchip MIC2790N Reset supervisor with Reset LED indicator
- Microchip 24AA014H I²C Serial EEPROM for board identification
- Single 10/100/1000Mb RJ45 Integrated Connector and Magnetics with LEDs
- MDIO Management interface
- Compliant with the SODIMM EDS2 Interface Specification
- One position SPST DIP Switch with Reset feature to keep the LAN8842 in Reset. Useful for development.
- 1x3 header to select between 3.3V and 2.5V VDDAH transceiver voltage
- 1x3 header to select between 3.3V and 2.5V VDDIO transceiver voltage
- 1x3 header to select internal VDDAH bypass
- 1x3 header to select between 1.1V output from internal LDO or external regulator
- 1x3 header to enable or disable Coma mode
- 2x2 header for buffered 25 MHz clock output and SOF indicator
- Green LED indicator for 1.1V
- Test points for Power rails and GND
- GPIO test points for IEEE1588 (Precision Time Protocol) timestamp capture and clearing event interrupts
- TX SMAs which can be used in conjunction with RX SMAs on the LAN9668 Host board

1.3 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN8842 Data Sheet*
- *LAN8842 EDS2 Daughter Card Schematics*
- *LAN8842 Hardware Design Checklist*
- *LAN8842 Silicon Errata and Data Sheet Clarification*
- *EVB-LAN9668 EDS2 Schematics*
- *EVB-LAN9668 EDS2 User Guide*

1.4 ACRONYMS AND DEFINITIONS

[Table 1-1](#) shows the terms used in this user guide.

TABLE 1-1: ACRONYMS AND DEFINITIONS

Term	Definition
ARP	Address Resolution Protocol
COM	Communications Port
DHCP	Dynamic Host Configuration Protocol
DIP	Dual In-line Package
DSUB	D - Subminiature
EP	Extended Page

TABLE 1-1: ACRONYMS AND DEFINITIONS (CONTINUED)

Term	Definition
GPIO	General Purpose Input/Output
ICM	Integrated Connector Magnetic
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
IP	Internet Protocol
LAN	Local Area Network
LSB	Least Significant Byte/Bit
MAC	Media Access Controller
MDIO	Management/Data Input/Output
MII	Media Independent Interface
NIC	Network Interface Card
OUI	Organizationally Unique Identifier
PC	Personal Computer
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PHY	Physical Layer Transceiver
PDU	Payload Data Unit
PN	Part Number
SMA	Sub-Miniature version A
TCXO	Temperature-Compensated Crystal Oscillator
TFTP	Trivial File Transfer Protocol
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VDFN	Very-small Dual Flat, No Leads
VM	Virtual Machine
VREG	Voltage regulator
XO	Crystal oscillator
SODIMM	Small Outline Dual In-line Memory Module

LAN8842 EDS2 Daughter Card User Guide

NOTES:

Chapter 2. Getting Started

2.1 INTRODUCTION

This chapter provides a quick start guide for the installation and use of the LAN8842 EDS2 Daughter Card.

2.2 DAUGHTER CARD INSTALLATION

Figure 2-1 shows the LAN8842 EDS2 Daughter Card. Figure 2-2 shows the EVB-LAN9668 EDS2.

FIGURE 2-1: LAN8842 EDS2 DAUGHTER CARD

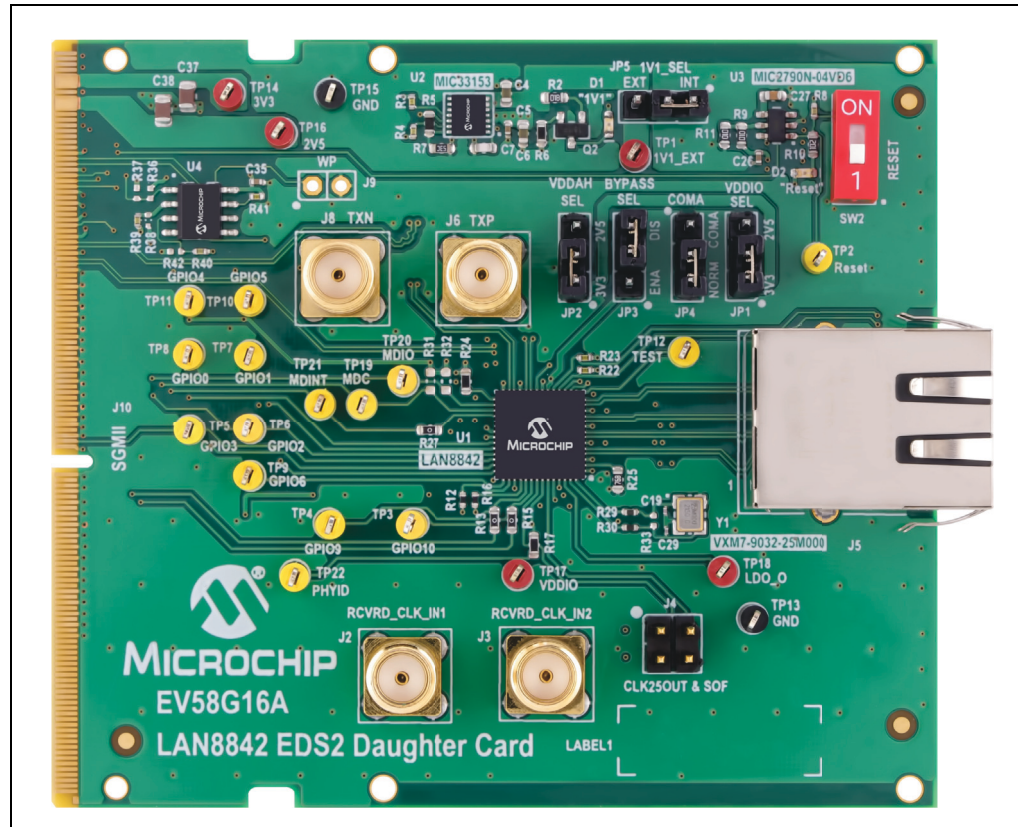
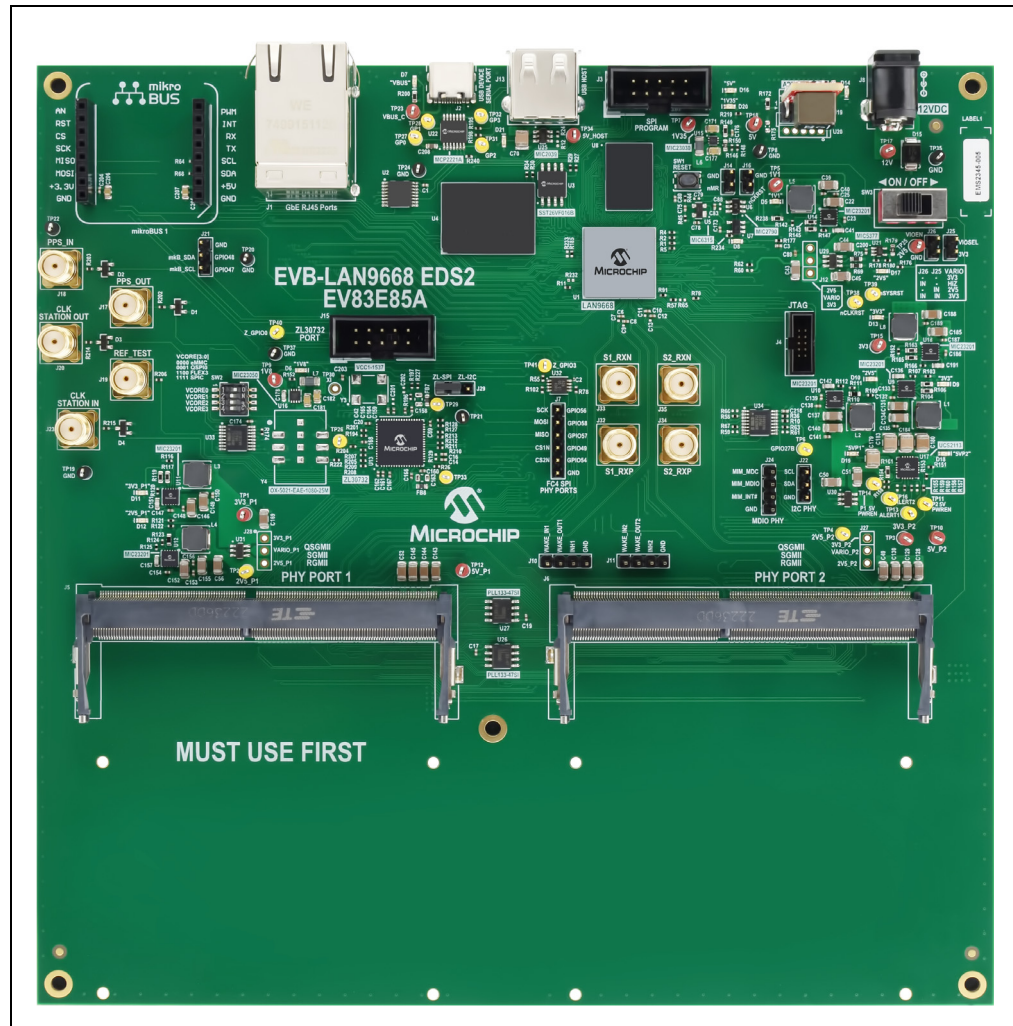


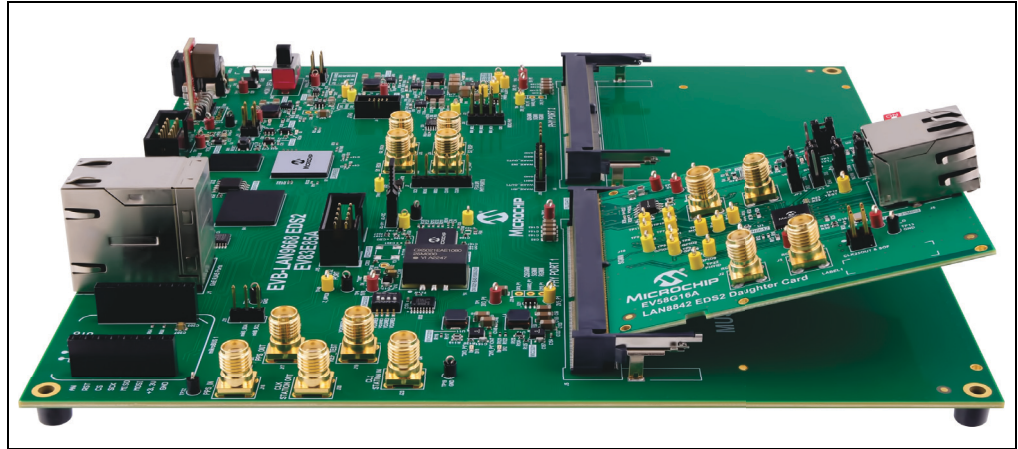
FIGURE 2-2: LAN8842 EDS2 DAUGHTER CARD HOST



Perform the following steps to install the LAN8842 EDS2 Daughter Card in the left (PHY1 PORT 1) SODIMM EDS2 socket:

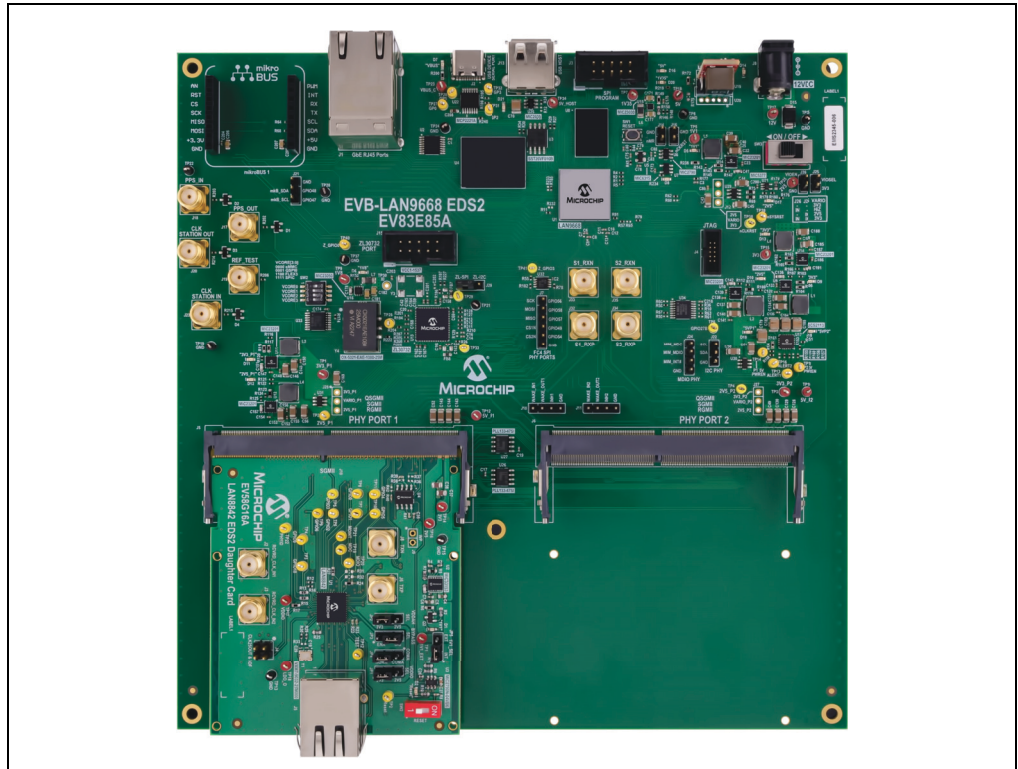
1. Verify that the host board power is OFF.
2. Hold the daughter card by its board edges. Align to SODIMM EDS2 socket and insert the board fingers' edge at a 45-degree angle into the SODIMM socket as shown in [Figure 2-3](#).

FIGURE 2-3: LAN8842 EDS2 DAUGHTER CARD INSTALLATION



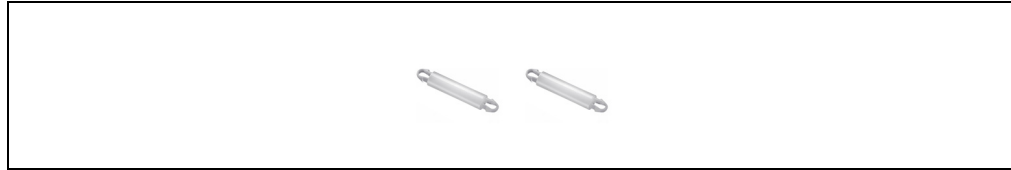
3. Push daughter card down until it latches into the SODIMM receptacle latches.
4. After installation, the boards should appear as shown in [Figure 2-4](#).

FIGURE 2-4: LAN8842 EDS2 DAUGHTER CARD INSTALLED



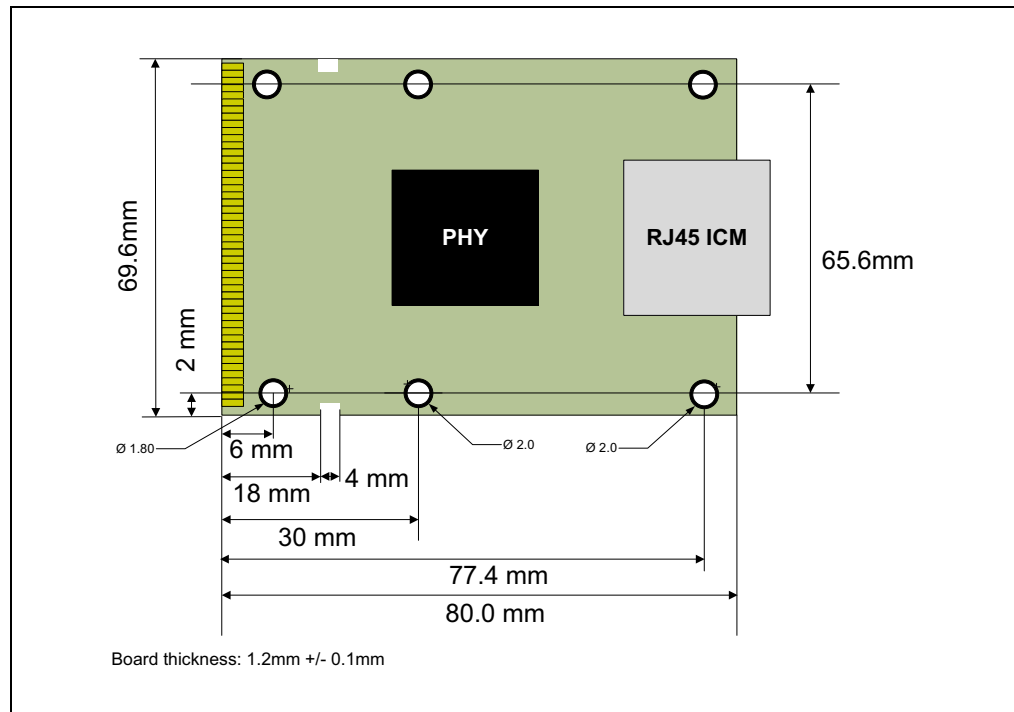
- (Optional step) Secure the board with two snap lock pins (Würth Elektronik part number 709652500, included in the kit). These pins prevent board movement and remove stress from the SODIMM socket due to the RJ45 cable weight and movement. See [Figure 2-5](#).

FIGURE 2-5: SNAP LOCK PINS



- The LAN8842 EDS2 Daughter Card has four (4) snap lock mounting holes, two (2) at 30 mm from the board fingers' edge, and two (2) at 77.4 mm from the board fingers' edge as shown in [Figure 2-6](#). For the EVB-LAN9668 EDS2 Host, use the mounting holes at 77.4 mm. Other hosts may only have the mounting holes at 30 mm.

FIGURE 2-6: LAN8842 EDS2 DAUGHTER CARD SNAP LOCK MOUNTING HOLES



- To use the snap lock pins, first install the snap lock pins on the host board, and then insert the daughter card into the SODIMM EDS2 receptacle. Align the snap locks with the corresponding mounting holes and press the daughter card down until the snap locks are fastened. A pair of long-nose pliers can be used to close the pin locks for easy board installation and removal.

2.3 QUICK START

Perform the following steps to start using the LAN8842 EDS2 Daughter Card:

1. Verify if the SW2 slide switch is set as shown in [Figure 2-7](#). This setting does not hold the PHY in a Reset state.

FIGURE 2-7: SW1 SLIDE SWITCH



2. Check if there is a shunt jumper at JP2[1-2] as shown in [Figure 2-8](#).

FIGURE 2-8: VDDAH_SEL HEADER



3. Check if there is a shunt jumper at JP3[2-3] as shown in [Figure 2-9](#).

FIGURE 2-9: BYPASS_SEL HEADER



4. Check if there is a shunt jumper at JP4[2-3] as shown in [Figure 2-10](#).

FIGURE 2-10: COMA HEADER



5. Check if there is a shunt jumper at JP1[1-2] as shown in [Figure 2-11](#).

FIGURE 2-11: VDDIO_SEL HEADER



6. Connect a USB-C[®] serial cable to the EVB-LAN9668 EDS2 host board and host PC for the terminal console.
7. Connect a 12V supply with a DC plug to the EVB-LAN9668 EDS2 host board.
8. Power up the EVB-LAN9668 EDS2 host board.
9. Connect the Ethernet cable to the RJ45 connector on the LAN8842 EDS2 Daughter Card.
10. Complete the steps in the boot process as shown in [Chapter 4. "System Boot"](#).

2.4 LAN8842 EDS2 DAUGHTER CARD REMOVAL

To remove the LAN8842 EDS2 Daughter Card from the SODIMM EDS2 receptacle:

1. Verify that the host board power is OFF.
2. Disconnect the RJ45 cable.
3. If snap locks are used, release them from the daughter card. A pair of long-nose pliers can be used to close the latch pins for easy release.
4. Gently pull the SODIMM receptacle arms away from the daughter card. It should swivel upwards.
5. Hold the daughter card by its edges and remove it from the SODIMM EDS2 receptacle.

Chapter 3. Hardware

3.1 INTRODUCTION

This section provides a description of the LAN8842 EDS2 Daughter Card hardware, including headers, test points, LEDs, and switches on the board.

The top side and bottom side of the LAN8842 EDS2 Daughter Card are shown in [Figure 3-1](#) and [Figure 3-2](#), respectively.

FIGURE 3-1: LAN8842 EDS2 DAUGHTER CARD (TOP SIDE)

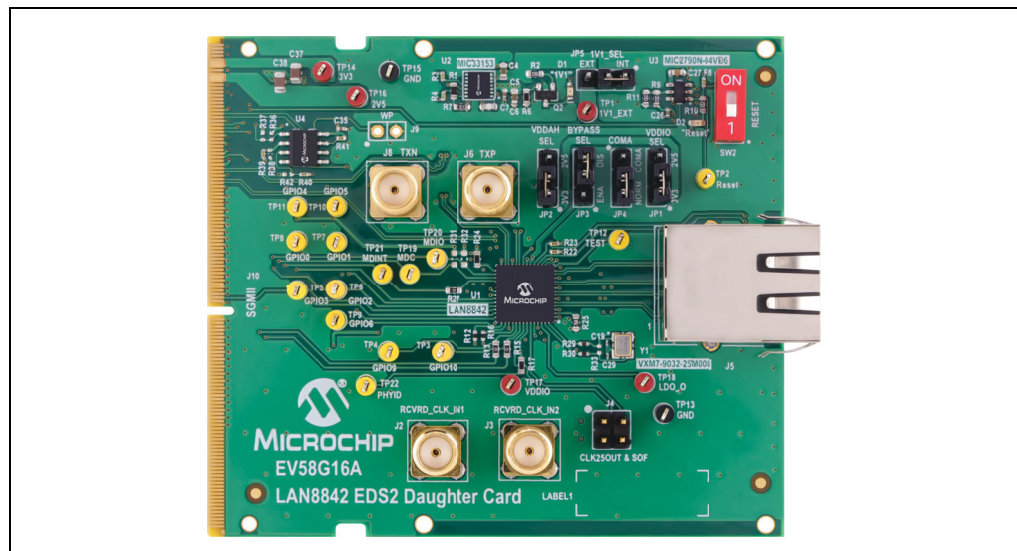
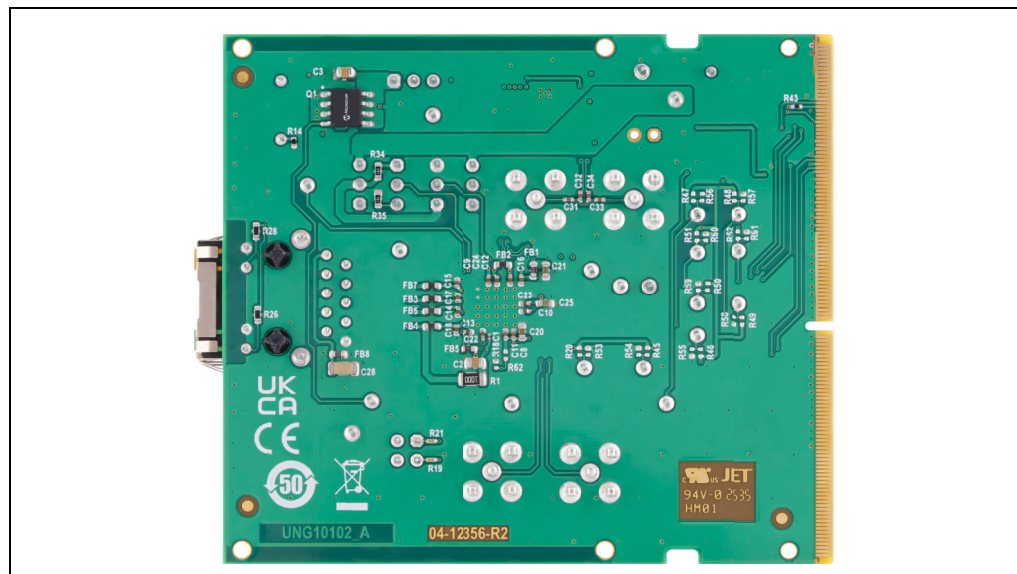


FIGURE 3-2: LAN8842 EDS2 DAUGHTER CARD (BOTTOM SIDE)



3.2 CONNECTORS

Table 3-1 describes the connectors on the LAN8842 EDS2 Daughter Card.

TABLE 3-1: LAN8842 EDS2 DAUGHTER CARD CONNECTORS

Reference Designator	Name	Description
J10	SODIMM-260 pin Edge Connector	Provides power and signals for operation. Connects to Microchip EDS2-compatible host.
J5	RJ45 ICM	Ethernet RJ45 connector with integrated magnetics for a 1 Gb port.
J6	TXP SMA	SMA Breakout for the MAC interface transmit positive line.
J8	TXN SMA	SMA Breakout for the MAC interface transmit negative line.
J9	WP Header 1x2	EEPROM Write Protect footprint (header not installed). Used to disable write protection during factory programming.
JP1	VDDIO Header 1x2	Used to select the LAN8842 VDDAH power. [1-2] 3.3V (Default) [2-3] 2.5V
JP2	VDDAH Header 1x2	Used to select the LAN8842 VDDAH power. [1-2] 3.3V (Default) [2-3] 2.5V
JP3	Bypass Header ¹ 1x2	Used to configure circuit bypass for SERDES, PVT Monitor, and 1588 PLL within LAN8842. [1-2] When VDDAH = 2.5V [2-3] When VDDAH = 3.3V (Default)
JP4	COMA Header	Used to enable/disable Coma mode for LAN8842. [1-2] Coma mode [2-3] Normal mode (Default)
JP5	1V1 Rail Selection	Used to select the source of 1.1V power for LAN8842. [1-2] Internal LDO 1V1 [2-3] External Reg 1V1 (Default)
J4	CLK25OUT, SOF, and PHYAD header	Used to either probe signals or change the default PHYAD strapping for LAN8842. [Unpopulated] (Default)

Note 1: Bypass header is attached to a live pin called SEL_2V5_VDDAH. The pin must not only be strapped during Reset but also be tied high or low at all times during device operation.

3.3 TEST POINTS

Table 3-2 lists the test points on the LAN8842 EDS2 Daughter Card.

TABLE 3-2: LAN8842 EDS2 DAUGHTER CARD TEST POINTS

Test Point	Color	Description
TP1	Red	1V1_EXT
TP2	Yellow	RESET
TP3	Yellow	GPIO10/RCVRD_CLK_OUT2
TP4	Yellow	GPIO9/RCVRD_CLK_OUT1
TP5	Yellow	GPIO3/1588_LD_ADJ
TP6	Yellow	GPIO2/CLK125M_P
TP7	Yellow	GPIO1/1588_EVENT_B
TP8	Yellow	GPIO0/1588_EVENT_A
TP9	Yellow	GPIO6/MODE_SEL4
TP10	Yellow	GPIO5/MODE_SEL3
TP11	Yellow	GPIO4/MODE_SEL2
TP12	Yellow	TEST
TP13	Black	GND
TP14	Red	3V3
TP15	Black	GND
TP16	Red	2V5
TP17	Red	VDDIO
TP18	Red	LDO_O
TP19	Yellow	MDC
TP20	Yellow	MDIO
TP21	Yellow	MDINT

3.4 LEDS

Table 3-3 describes the LEDES on the LAN8842 EDS2 Daughter Card.

TABLE 3-3: LAN8842 EDS2 DAUGHTER CARD LEDES

Reference Designator	Name	Description
D1	1V1	External Regulator 1.1 voltage output detected
D2	RESET	Red LED RESET indicator
J5 - Left	RJ45 - Left	Green LED activity indicator
J5 - Right	RJ45 - Right	Yellow LED link indicator

3.5 CONFIGURATION STRAPS

Table 3-4 lists the configuration straps on the LAN8842 EDS2 Daughter Card.

TABLE 3-4: LAN8842 EDS2 DAUGHTER CARD CONFIGURATION STRAPS

Reference Designator PU/PD	Name	Description
R52/R61	LED_MODE	0* – Enable Tri-Color LEDs 1 – Enable Individual LEDs
R51/R60	MODE_SEL Bit 0	MODE_SEL [4:0] 11000* - default mode set by internal straps. See Table 3-10 in the device data sheet, which details all possible configurations.
R49/R58	MODE_SEL Bit 1	
R48/R57	MODE_SEL Bit 2	
R47/R56	MODE_SEL Bit 3	
R46/R55	MODE_SEL Bit 4	
See J4	PHYAD Bit 0	PHYAD[4:0] 000x0* - default address where x = PHYID
R62/R18	PHYAD Bit 1	
See J4	PHYAD Bit 2	
None/R22	PHYAD Bit 3	
None/R23	PHYAD Bit 4	

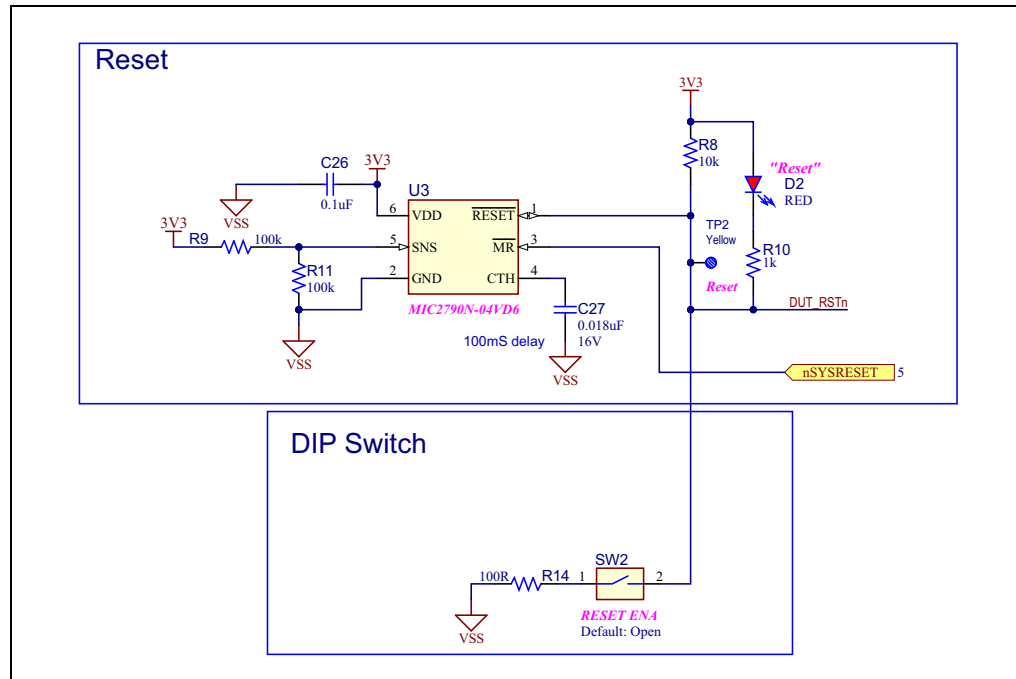
Note 1: Only one of the two PU/PD resistors is installed.

2: * indicates default.

3.6 RESET

The LAN8842 EDS2 Daughter Card includes a Reset circuit using the Microchip MIC2790 Reset supervisor as shown in Figure 3-3. The system Reset signal, nSYS-RESET, is driven from the SODIMM EDS2 host interface and is connected to the MIC2790 master Reset input MR. When MR goes low, the MIC2790 Reset output on net RST_INDY_N goes low, resetting the LAN8842 and turning on the Reset LED D2. The RST_INDY_N net will go high 100 milliseconds after nSYSRESET goes high, turning the Reset LED off and releasing the LAN8842 from Reset. The configuration straps are sampled when RST_INDY_N goes high.

FIGURE 3-3: LAN8842 EDS2 DAUGHTER CARD RESET CIRCUIT



The DIP Switch (SW2), as shown in [Figure 3-3](#), can be used to place the LAN8842 EDS2 Daughter Card in Reset without affecting the rest of the system. This feature is useful when testing and updating the LAN8842 Linux[®] driver after the system has booted up.

3.7 CLOCKS

The LAN8842 EDS2 Daughter Card uses a Microchip VXM7-9013-25M0000 25 MHz crystal for the LAN8842 clock reference.

3.8 POWER

The LAN8842 EDS2 Daughter Card requires 3.3V, 2.5V, and 1.1V. The EDS2 SODIMM EDS2 interface provides 3.3V, 2.5V, and VARIO (3.3V or 2.5V). An on-board Microchip MIC33153 switching regulator is used to generate the 1.1V required by the LAN8842 analog, digital core, and PLL power inputs.

LAN8842 EDS2 Daughter Card User Guide

3.9 LAN8842 EDS2 DAUGHTER CARD EEPROM

The LAN8842 EDS2 Daughter Card includes a Microchip 24AA014H EEPROM with half-array write protection (40H to 7Fh) for identification. Only some locations in the protected area starting at 40h are programmed as shown in [Figure 3-4](#). Details on these fields are specified in [Table 3-5](#).

FIGURE 3-4: EEPROM CONTENTS

Address	0	1	2	3	4	5	6	7	8	9	a	b	c	d	e	f	Dump
00000000	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	yyyyyyyyyyyyyyyy
00000010	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	yyyyyyyyyyyyyyyy
00000020	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	yyyyyyyyyyyyyyyy
00000030	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	yyyyyyyyyyyyyyyy
00000040	a3	01	00	01	04	10	88	42	01	00	45	56	35	38	33	31	E.....^B..EV5831
00000050	36	41	42	31	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	6AB1yyyyyyyyyyyy
00000060	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	yyyyyyyyyyyyyyyy
00000070	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	ff	aa	00	00	aa	yyyyyyyyyyyyy ^a .. ^a

TABLE 3-5: EDS2 DAUGHTER CARD EEPROM

Byte Address	Name	Type	Description
40	KEY	INT	Magic number = A3h
41	REV	INT	EEPROM Revision
42	DCTYPE	INT	Daughter Card type: 0 = PHY, 1 = SWITCH
43	NPORTS	INT	Number of ports
44	MACIF	INT	MAC Interface: RMII 07h RGMII 09h RGMII_ID 0Ah RGMII_RXID 0Bh RGMII_TXID 0Ch SGMII 04h
45	DPN_PNUM	INT	Device Part number: 23:20 Product Family 0 = KSZ 1 = LAN 2 = VSC 19:16 Part Number upper 4 bits
46			Device Part number bits 15:8
47			Device Part number bits 7:0
48	CTRLIF	INT	Control interface: 7 = 5 Reserved 4 = 3 SPI Mode 2 = SPI Control available 1 = I ² C Control available 0 = MIIM Control available
49	SPIR	INT	SPI rate

TABLE 3-5: EDS2 DAUGHTER CARD EEPROM (CONTINUED)

Byte Address	Name	Type	Description
4A	DEVT	ASCII	Dev Tools Part number
4B			
4C			
4D			
4E			
4F			
50			
51			
52	BREVU	ASCII	UNG Board Revision Letter
53	BREVD	ASCII	Dev Tools Board Revision Number
7C	IDBYTE0	INT	ID BYTE 1 = AAh
7D	IDBYTE1	INT	ID BYTE 2 = 00h
7E	IDBYTE2	INT	ID BYTE 3 = 00h
7F	CHECKSUM	INT	CHECKSUM = AAh

LAN8842 EDS2 Daughter Card User Guide

NOTES:

Chapter 4. System Boot

4.1 INTRODUCTION

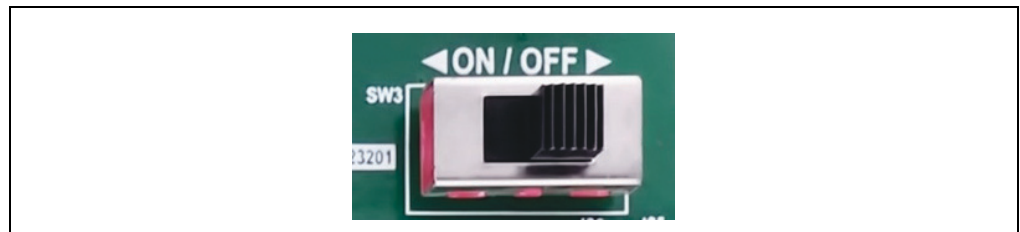
This chapter describes the boot process using the EVB-LAN9668 EDS2 (EV83E85A) host using Linux software factory configuration. Refer to the software documentation for each EDS2 host platform for specific configuration and software details.

4.2 LAN8842 EDS2 SYSTEM POWER-UP

The LAN8842 EDS2 Daughter Card should be installed as shown in [Figure 2-3](#). Perform the following steps to power up the LAN8842 EDS2:

1. Verify that the EVB-LAN9668 EDS2 power switch is set to OFF (right) position. See [Figure 4-1](#).

FIGURE 4-1: LAN9668 POWER SWITCH



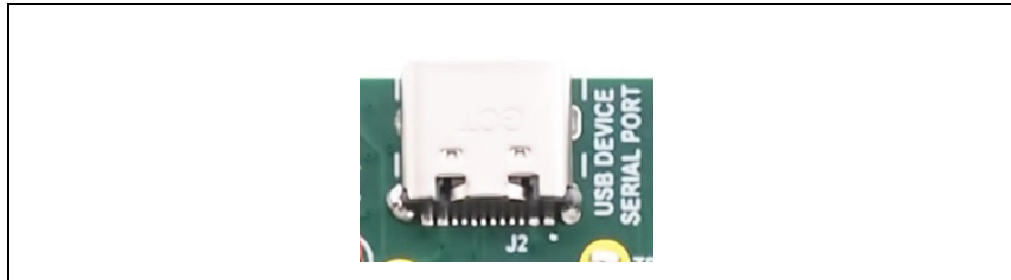
2. Connect a 12V 1A (minimum) power supply with a DC plug to DC Jack J8 on the EVB-LAN9668 EDS2. See [Figure 4-2](#).

FIGURE 4-2: LAN9668 DC JACK



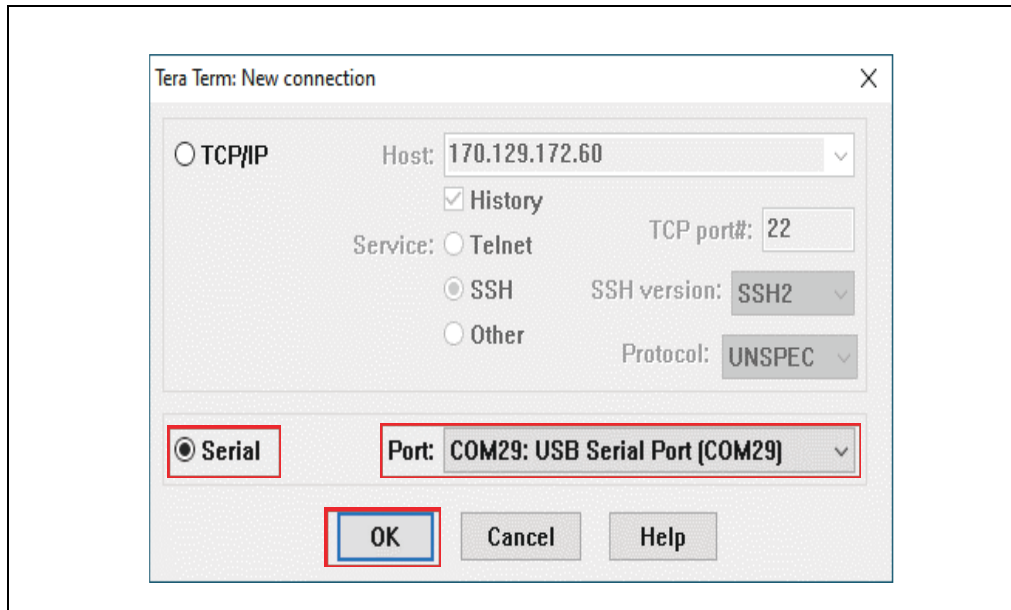
3. Connect a USB-C cable into the USB-C receptacle J2 on the EVB-LAN9668 EDS2 and then insert the other end into a PC. See [Figure 4-3](#).

FIGURE 4-3: EVB-LAN9696 REFERENCE BOARD USB-C® SERIAL PORT



- Slide the EVB-LAN9668 EDS2 power switch SW3 to the left ON position to turn on board power.
- Open Tera Term. Select the Serial radial button and look for COMx:USB Serial Port. COM29 is shown in [Figure 4-4](#). Windows may assign a different port number.

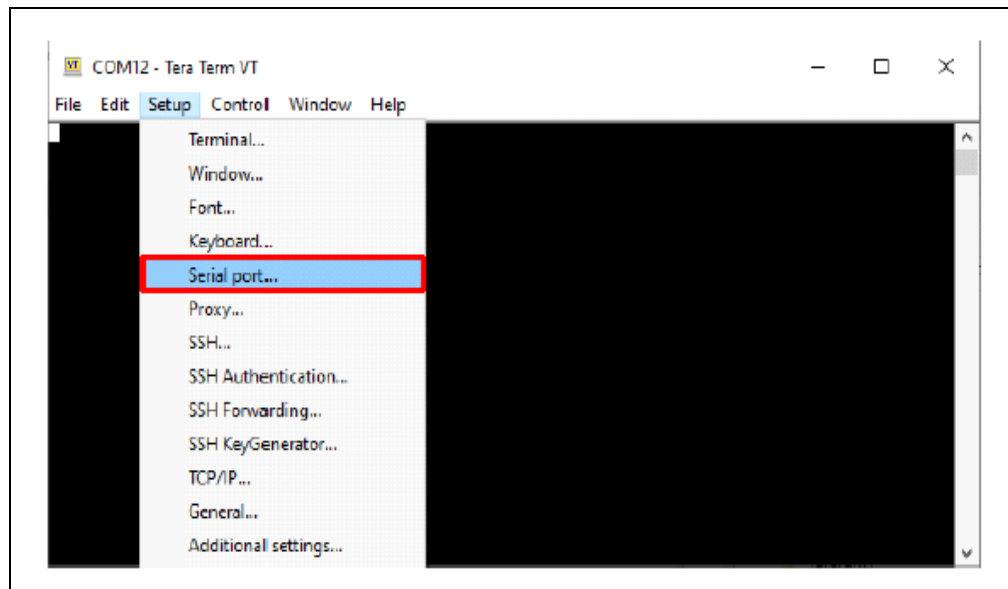
FIGURE 4-4: TERA TERM SERIAL PORT SELECTION



- Click on **OK**.

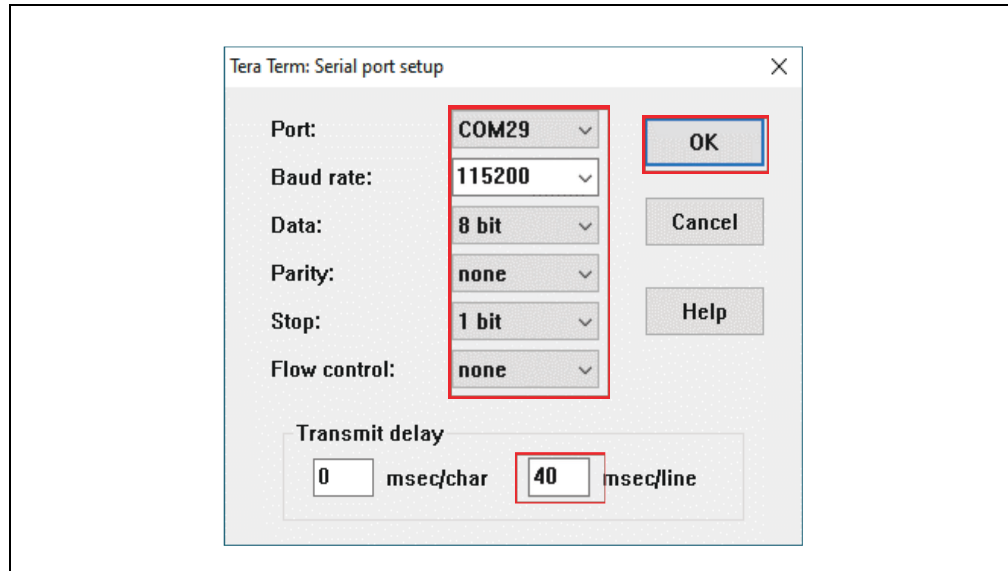
7. Go to the Setup menu and select Serial port. See [Figure 4-5](#).

FIGURE 4-5: TERA TERM SETUP MENU



8. Set the selected port to 115200, 8-bit, no parity, 1 stop bit, no flow control, and 40 msec/line. Click on **OK**. See [Figure 4-6](#).

FIGURE 4-6: TERA TERM SERIAL PORT SETUP



- Slide the EVB-LAN9668 EDS2 power switch SW3 to the right OFF position. Wait for a few seconds and then slide it back to the left ON position. Immediately begin tapping the space bar on the keyboard until the terminal halts within a U-boot environment. See [Figure 4-7](#).

FIGURE 4-7: U-BOOT ENVIRONMENT

```
NOTICE: Booting Trusted Firmware
NOTICE: BL1: v2.4(release):laguna-transplant-base-v0-23-g225acd2
NOTICE: BL1: Built : 12:48:51, Dec 6 2021
INFO: BL1: RAM 0x116000 - 0x120000
INFO: CPRCL 0: 0x02100101
INFO: Using crypto library 'LAN9668 crypto core'
INFO: Loading image id=6 at address 0x100000
INFO: Image id=6 loaded: 0x100000E: DDR: lan966x 2023-08-14-10:53:11 416024f90cff, 1200 MHz, 896MiB, ECC enabled
NOTICE: OTP: Available for non-secure provisioning
NOTICE: BL1: Booting BL32
INFO: Entry point address = 0x60000000
INFO: SPSR = 0x0
NOTICE: SP_MIN: lts-v2.8.8(release):v2.8.8-mchp1
NOTICE: SP_MIN: Built : 13:56:16, Apr 5 2024
NOTICE: Direct boot of BL33 binary image
board type: 5

U-Boot 2024.04 (Sep 22 2025 - 12:19:49 +0200). Build: jenkins-UNGE-sw-buildroot-layer-2025.09-soak-7
CPU: Cortex ARM A7
board type: 5
DRAM: 894 MiB
Cache: 34 devices, 17 uclasses, devicetree: fit
MMC: sdhci-host@0030000: 0, emmc@e0830000: 1
Loading Environment from SPIFlash... SF: Detected sst26vf016h with page size 256 Bytes, erase size 4 KiB, total 2 MiB
OK
In: serial
Out: serial
Err: serial
Net: eth0: vnet0, eth1: vnet1

Hit any key to stop autoboot: 0
a =>
```

- Use the following command to review environment variables which are set from the factory:
`#printenv`

FIGURE 4-8: #PRINTENV COMMAND

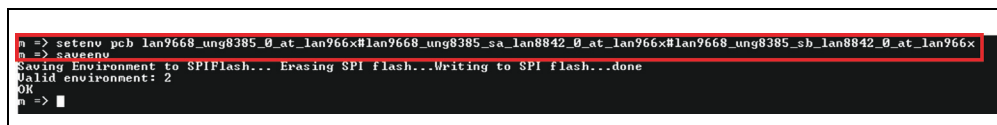
```
a => printenv
bootargs=console=ttys0,115200 root=/dev/rand loglevel=4 qio_pdrv_genirq.of_id=generic-uio
bootargs_extra=qio_pdrv_genirq.of_id=generic-uio loglevel=1
bootcmd=run mmc_boot
bootdelay=3
console=ttys0,115200n8
div_512=setexpr _tmp_ ${filesize} + 0x1fff; setexpr filesize_512 ${_tmp_} / 0x200; env set _tmp_
ethaddr=62:1e:3a:31:66:b3
ethact=pcap0
ethaddr=d6:51:6c:ca:10:c4
fdt_high=0xffffffff
fdtcontroladdr=70660800
fileaddr=64000000
filesize=940000
filesize_512=46440
fip_fw_d1=dhcp ${loadaddr} ${fip_fw}
fip_fw_d1=dhcp ${loadaddr} ${fip_fw}
gatewvip=10.132.26.1
initrd_high=0xffffffff
loadaddr=10.132.26.1f3
loadaddr=0x64000000
mmc_bak=5
mmc_boot=run mmc_tryboot; run mmc_swap; run mmc_tryboot
mmc_boot0_d1up=run mmc_d1; run mmc_boot0_upd; run mmc_boot1_upd
mmc_boot0_d1up=run mmc_d1; run mmc_boot0_upd
mmc_boot0_upd=run div_512; mmc write ${mmc_unzip_loadaddr} ${mmc_offset_boot0} ${filesize_512}
mmc_boot1_d1up=run mmc_d1; run mmc_boot1_upd
mmc_boot1_upd=run div_512; mmc write ${mmc_unzip_loadaddr} ${mmc_offset_boot1} ${filesize_512}
mmc_cur=6
mmc_dev=mmc 0
mmc_dhcp_d1=dhcp ${loadaddr} ${mmc_fw}; unzip ${loadaddr} ${mmc_unzip_loadaddr}
mmc_d1=fipboot ${loadaddr} ${mmc_fw}; unzip ${loadaddr} ${mmc_unzip_loadaddr}
mmc_fip0_d1up=run fip_fw_d1; if test $? = 0; then run mmc_fip0_upd; run mmc_fip1_upd; fi
mmc_fip0_d1up=run fip_fw_d1; if test $? = 0; then run mmc_fip0_upd; fi
mmc_fip0_upd=run div_512; mmc write ${loadaddr} ${mmc_offset_fip0} ${filesize_512}
mmc_fip1_d1up=run fip_fw_d1; if test $? = 0; then run mmc_fip1_upd; fi;
mmc_fip1_upd=run div_512; mmc write ${loadaddr} ${mmc_offset_fip1} ${filesize_512}
mmc_format_spt_guid ${mmc_dev} mmc_guid; spt write ${mmc_dev} ${mmc_part}; env save
mmc_fw=mgwyder/eds2/brsdk_standalone_arm2509_ext4.gz
mmc_fw_template_old=mgwyder/eds2/mchp-brsdk-arm-2025.06/arm-cortex_a8-linux-gnu/standalone/release/brsdk_standalone_arm.ext4.gz
mmc_guid=3d5f16af-4541-edba-f957b2540e75
mmc_load=ext4load ${mmc_dev}:${mmc_cur} ${loadaddr} Image.ith
mmc_offset_boot0=0x82040
mmc_offset_boot1=0x482040
mmc_offset_data=0x482040
mmc_offset_fip0=0x40
mmc_offset_fip1=0x4040
mmc_part=uid_disk ${mmc_guid}; name=fip,start=32K,size=128MiB,type=system;name=fip_bak,size=128MiB,type=system;name=Env,size=2MiB,type=data;
mmc_data,size=-,type=linux
mmc_static_d1=ftptboot ${loadaddr} ${mmc_fw}; unzip ${loadaddr} ${mmc_unzip_loadaddr}
mmc_swap=env set _mmc_tmp ${mmc_bak}; env set mmc_bak ${mmc_cur}; env set _mmc_tmp; env save
mmc_tryboot=run mmc_d1; if test $? = 0; then setenv mtdroot root_next=/dev/mmcblk0p${mmc_cur}; run randboot; fi;
mmc_unzip_loadaddr=0x80000000
mtids=nr0=pi0
mtdparts=mtids:spi0:1536k(fip),256k(Env),256k(Env.bk)
netack=255.255.255.0
nor_fip_upd=run fip_fw_d1; if test $? = 0; then run nor_fip_upd; fi;
nor_fip_upd=run probe; sf update ${loadaddr} 0 ${filesize}
partid=8504
pcblan9668_ung8385_0_at_lan966x1lan9668_ung8385_sa_lan8814_0_at_lan966x1lan9668_ung8385_sb_lan8840_0_at_lan966x
randboot=bootn start ${loadaddr}#5(pcb) = bootn lan966x ${loadaddr}#5(pcb); bootn ramdisk ${loadaddr}#5(pcb); run set_rootargs; run setup; run set_rootargs; run setenv rootargs root=/dev/mmcblk0p${mmc_cur} no rootwait
rootargs=run=setenv rootargs root=/dev/rand ro rootwait
serial_number=21979713528110
serverip=10.132.26.30
set_rootargs=if test $initrd_start = 0; then run rootargs_mmc; else; run rootargs_ran; fi;
setup=setenv bootargs console=${console} ${mtdroot} fis_act=${active} boot_source=${boot_source} ${bootargs_extra}
ver=U-Boot 2024.04 (Sep 22 2025 - 12:19:49 +0200)

Environment size: 3782/262139 bytes
a =>
```

11. Change the device tree overlay, so that EVB-LAN9668 EDS2 can recognize the LAN8842 EDS2 daughter cards plugged into both slots. Save the new environment, so that it remains in place after power cycles. See [Figure 4-9](#).

```
setenv pcb  
lan9668_ung8385_0_at_lan966x#lan9668_ung8385_sa_lan8842_0_at  
_lan966x#lan9668_ung8385_sb_lan8842_0_at  
_lan966x  
#saveenv
```

FIGURE 4-9: SETENV PCB AND SAVENV



```
n -> setenv pcb lan9668_ung8385_0_at_lan966x#lan9668_ung8385_sa_lan8842_0_at_lan966x#lan9668_ung8385_sb_lan8842_0_at_lan966x  
n -> saveenv  
Saving Environment to SPIFlash... Erasing SPI flash...Writing to SPI flash...done  
Valid environment: 2  
OK  
n ->
```

12. Boot into the kernel. See [Figure 4-10](#).

```
#boot
```

FIGURE 4-10: #BOOT

```
n => boot
556038 Bytes read in 392 ms (13.5 MiB/s)
## Loading kernel from FIT Image at 64000000 ...
Using 'lan9668_ung8385_0_at_lan966x' configuration
Trying 'kernel' kernel subimage
  Description: Kernel
  Type: Kernel Image
  Compression: uncompressed
  Data Start: 0x640000c8
  Data Size: 5312344 Bytes = 5.1 MiB
  Architecture: ARM
  OS: Linux
  Load Address: 0x60208000
  Entry Point: 0x60208000
Verifying Hash Integrity ... OK
## Loading fdt from FIT Image at 64000000 ...
Using 'lan9668_ung8385_0_at_lan966x' configuration
Trying 'fdt_lan9668_ung8385_0_at_lan966x' fdt subimage
  Description: Flattened Device Tree
  Type: Flat Device Tree
  Compression: uncompressed
  Data Start: 0x64528288
  Data Size: 19341 Bytes = 18.9 KiB
  Architecture: ARM
  Load Address: 0x67e00000
Verifying Hash Integrity ... OK
Loading fdt from 0x64528288 to 0x67e00000
## Loading fdt from FIT Image at 64000000 ...
Using 'lan9668_ung8385_sa_lan8842_0_at_lan966x' configuration
Trying 'fdt_lan9668_ung8385_sa_lan8842_0_at_lan966x' fdt subimage
  Description: Flattened Device Tree Overlay
  Type: Flat Device Tree
  Compression: uncompressed
  Data Start: 0x645412a4
  Data Size: 1429 Bytes = 1.4 KiB
  Architecture: ARM
  Load Address: 0x67e80000
Verifying Hash Integrity ... OK
## Loading fdt from FIT Image at 64000000 ...
Using 'lan9668_ung8385_sb_lan8842_0_at_lan966x' configuration
Trying 'fdt_lan9668_ung8385_sb_lan8842_0_at_lan966x' fdt subimage
  Description: Flattened Device Tree Overlay
  Type: Flat Device Tree
  Compression: uncompressed
  Data Start: 0x645418f0
  Data Size: 1429 Bytes = 1.4 KiB
  Architecture: ARM
  Load Address: 0x67e80000
Verifying Hash Integrity ... OK
Bootimg using the fdt blob at 0x67e00000
Working FDT set to 67e00000
Loading Kernel Image to 60208000
Using Device Tree in place at 67e00000, end 67e07da6
Working FDT set to 67e00000
Using Device Tree in place at 67e00000, end 67e0ada6
Working FDT set to 67e00000

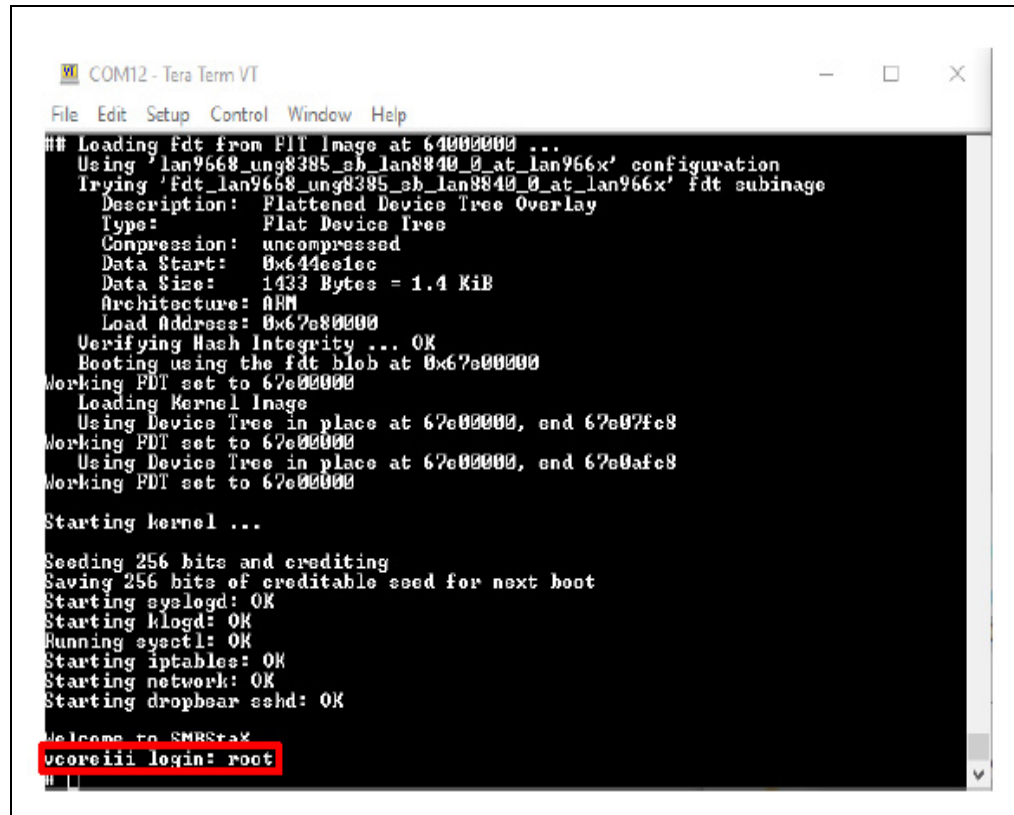
Starting kernel ...

Seeding 256 bits and crediting
Saving 256 bits of creditable seed for next boot
Starting syslogd: OK
Starting klogd: OK
Running sysctl: OK
Starting iptables: OK
Starting network: OK
Starting crond: OK
Starting dropbear sshd: OK

Welcome to SMBStaX
ucoreiii login: █
```

13. At login prompt, enter `root`. See [Figure 4-11](#).

FIGURE 4-11: TERA TERM LOGIN PROMPT



```
COM12 - Tera Term VT
File Edit Setup Control Window Help
## Loading fdt from PII Image at 64000000 ...
Using 'lan9668_ung8385_sb_lan8840_0_at_lan966x' configuration
Trying 'fdt_lan9668_ung8385_sb_lan8840_0_at_lan966x' fdt subimage
Description: Flattened Device Tree Overlay
Type: Flat Device Tree
Compression: uncompressed
Data Start: 0x644e1ec
Data Size: 1433 Bytes = 1.4 KiB
Architecture: ARM
Load Address: 0x67e80000
Verifying Hash Integrity .. OK
Booting using the fdt blob at 0x67e00000
Working FDT set to 67e00000
Loading Kernel Image
Using Device Tree in place at 67e00000, end 67e07fc8
Working FDT set to 67e00000
Using Device Tree in place at 67e00000, end 67e0afe8
Working FDT set to 67e00000

Starting kernel ...

Seeding 256 bits and crediting
Saving 256 bits of creditable seed for next boot
Starting syslogd: OK
Starting klogd: OK
Running sycht1: OK
Starting iptables: OK
Starting network: OK
Starting dropbear sshd: OK

Welcome to SMRStax
ucoreiii login: root
```

Note: For the succeeding steps, it is assumed that a host PC with an Ethernet port that can be pinged at 192.168.0.80 is available.

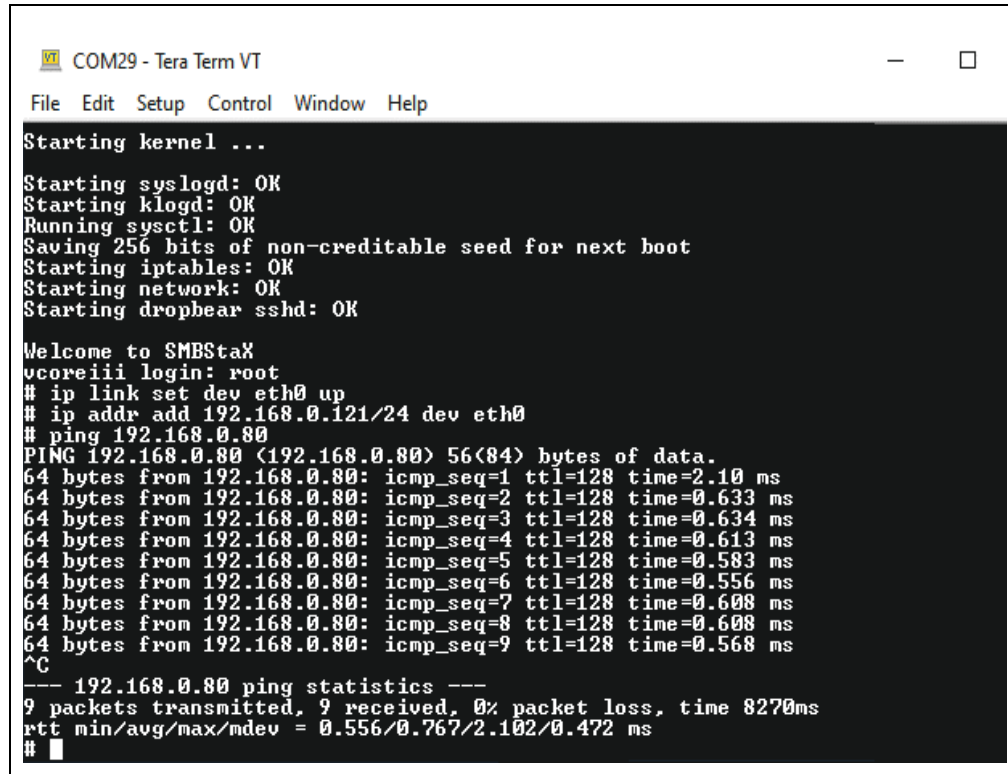
14. Enter the following commands to assign an IP address to the upstream port on the switch:

```
#ip link set dev eth0 up
#ip addr add 192.168.0.121/24 dev eth0
```

15. Connect an Ethernet cable to the LAN8842 EDS2 Daughter Card RJ45 port.
Then, enter the following command:

```
#ping 192.168.0.80
```

FIGURE 4-12: LINUX® PING



```
COM29 - Tera Term VT
File Edit Setup Control Window Help
Starting kernel ...
Starting syslogd: OK
Starting klogd: OK
Running sysctl: OK
Saving 256 bits of non-creditable seed for next boot
Starting iptables: OK
Starting network: OK
Starting dropbear sshd: OK

Welcome to SMBStax
vcoreiii login: root
# ip link set dev eth0 up
# ip addr add 192.168.0.121/24 dev eth0
# ping 192.168.0.80
PING 192.168.0.80 (192.168.0.80) 56(84) bytes of data.
64 bytes from 192.168.0.80: icmp_seq=1 ttl=128 time=2.10 ms
64 bytes from 192.168.0.80: icmp_seq=2 ttl=128 time=0.633 ms
64 bytes from 192.168.0.80: icmp_seq=3 ttl=128 time=0.634 ms
64 bytes from 192.168.0.80: icmp_seq=4 ttl=128 time=0.613 ms
64 bytes from 192.168.0.80: icmp_seq=5 ttl=128 time=0.583 ms
64 bytes from 192.168.0.80: icmp_seq=6 ttl=128 time=0.556 ms
64 bytes from 192.168.0.80: icmp_seq=7 ttl=128 time=0.608 ms
64 bytes from 192.168.0.80: icmp_seq=8 ttl=128 time=0.608 ms
64 bytes from 192.168.0.80: icmp_seq=9 ttl=128 time=0.568 ms
^C
--- 192.168.0.80 ping statistics ---
9 packets transmitted, 9 received, 0% packet loss, time 8270ms
rtt min/avg/max/mdev = 0.556/0.767/2.102/0.472 ms
# █
```



Appendix A. Schematics

A.1 INTRODUCTION

This appendix shows the LAN8842 EDS2 Daughter Card schematics.

FIGURE A-1: LAN8842 EDS2 DAUGHTER CARD OVERVIEW

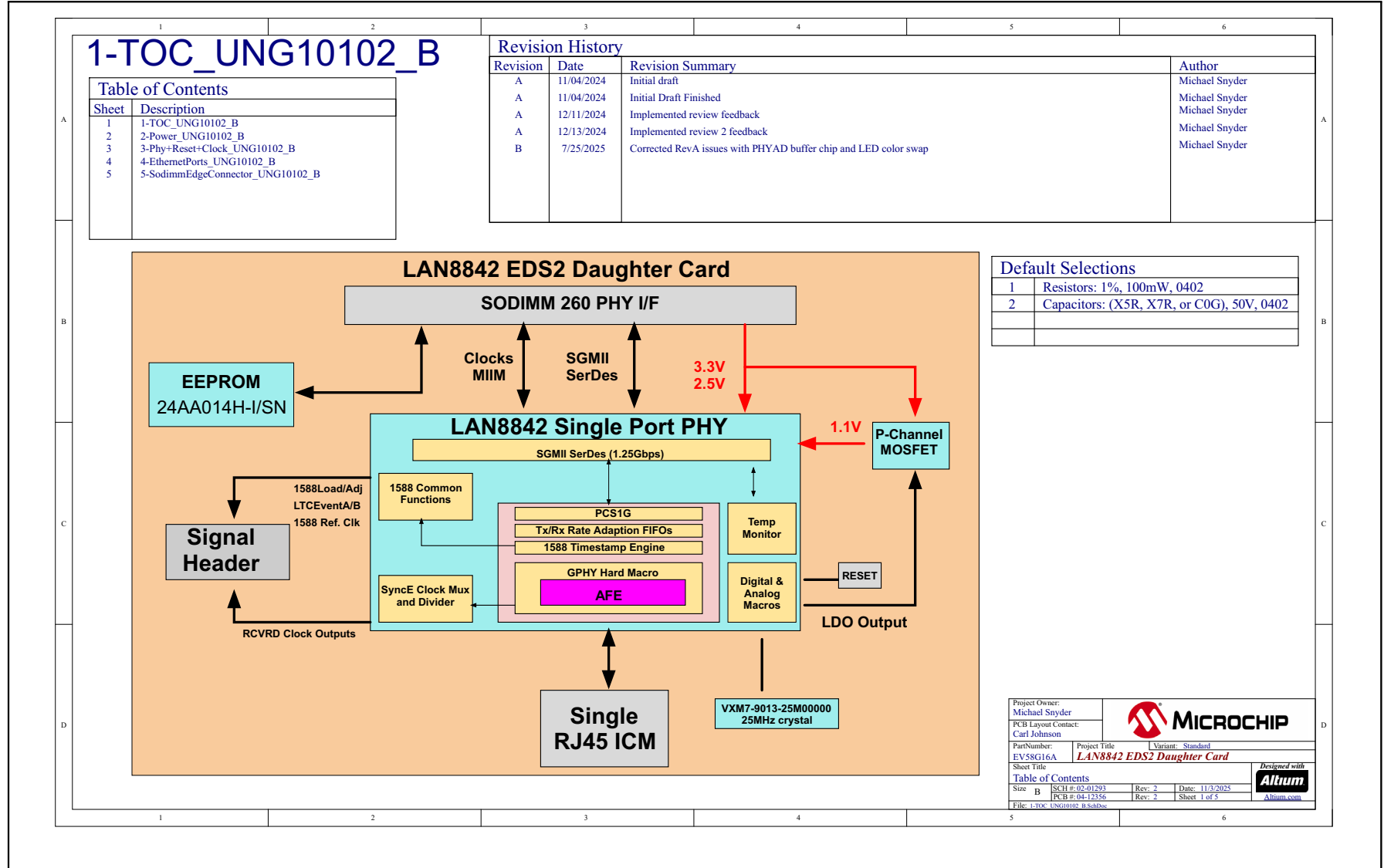


FIGURE A-2: LAN8842 EDS2 DAUGHTER CARD POWER

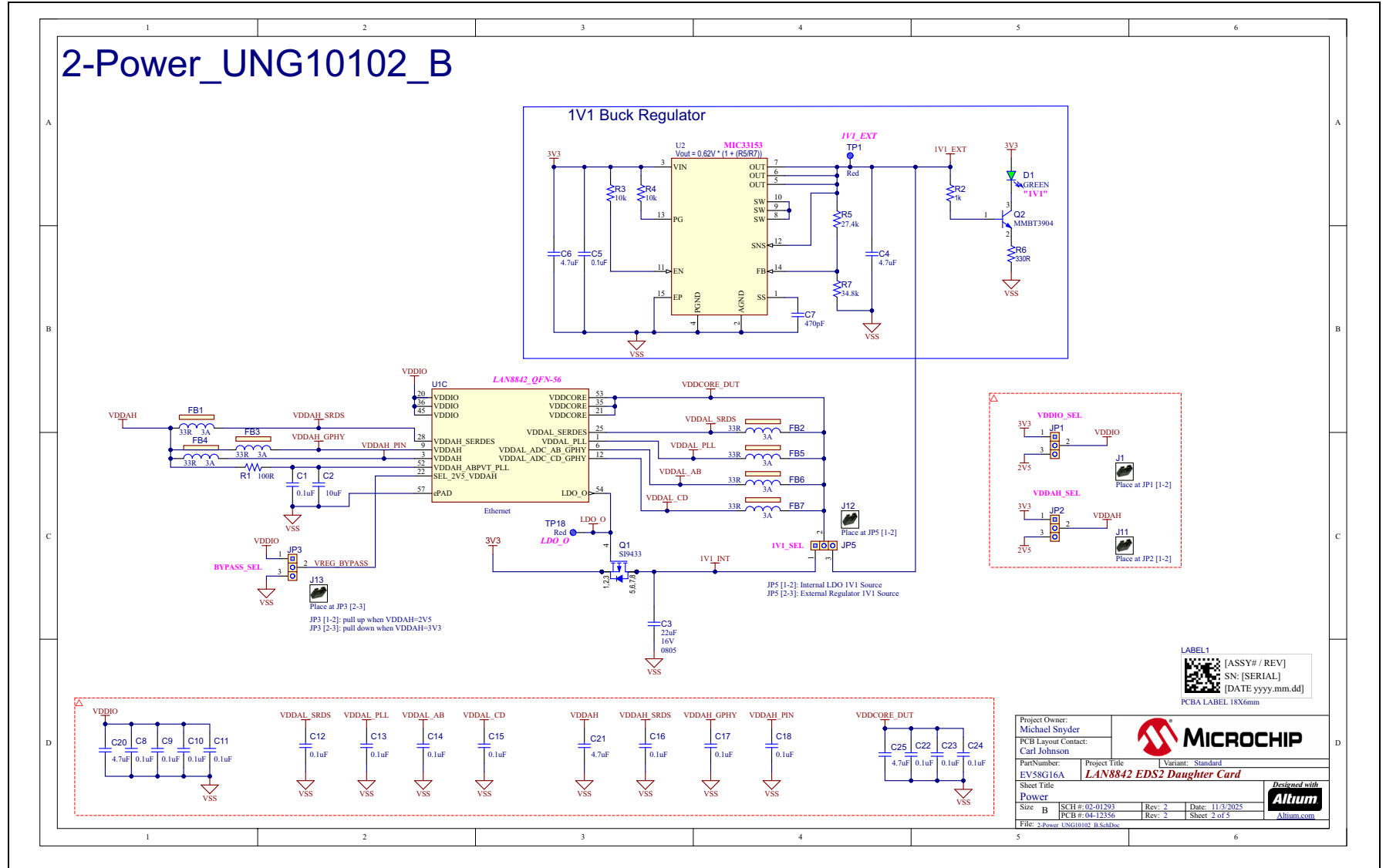
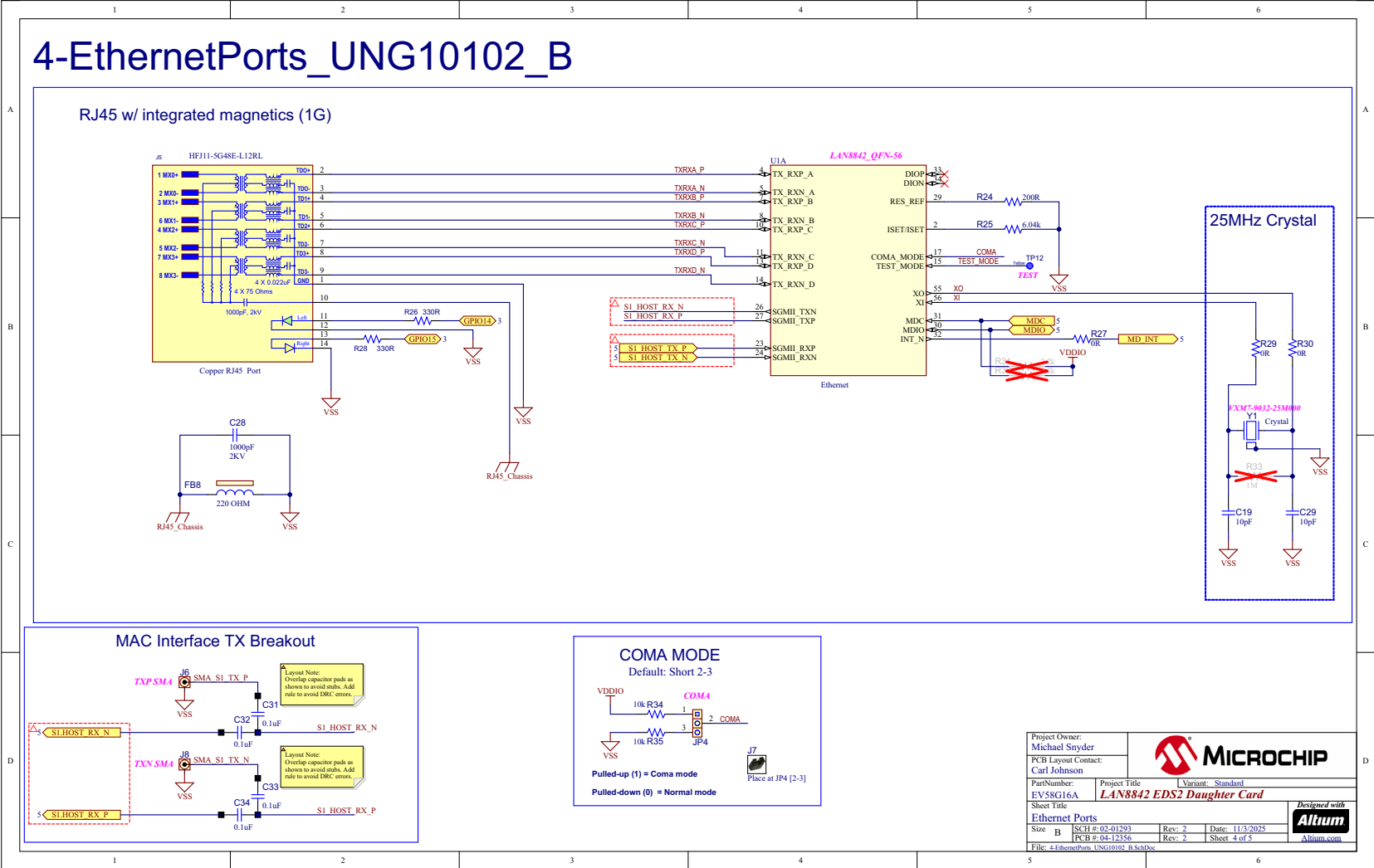


FIGURE A-4: LAN8842 EDS2 DAUGHTER CARD ETHERNET PORTS

4-EthernetPorts_UNG10102_B

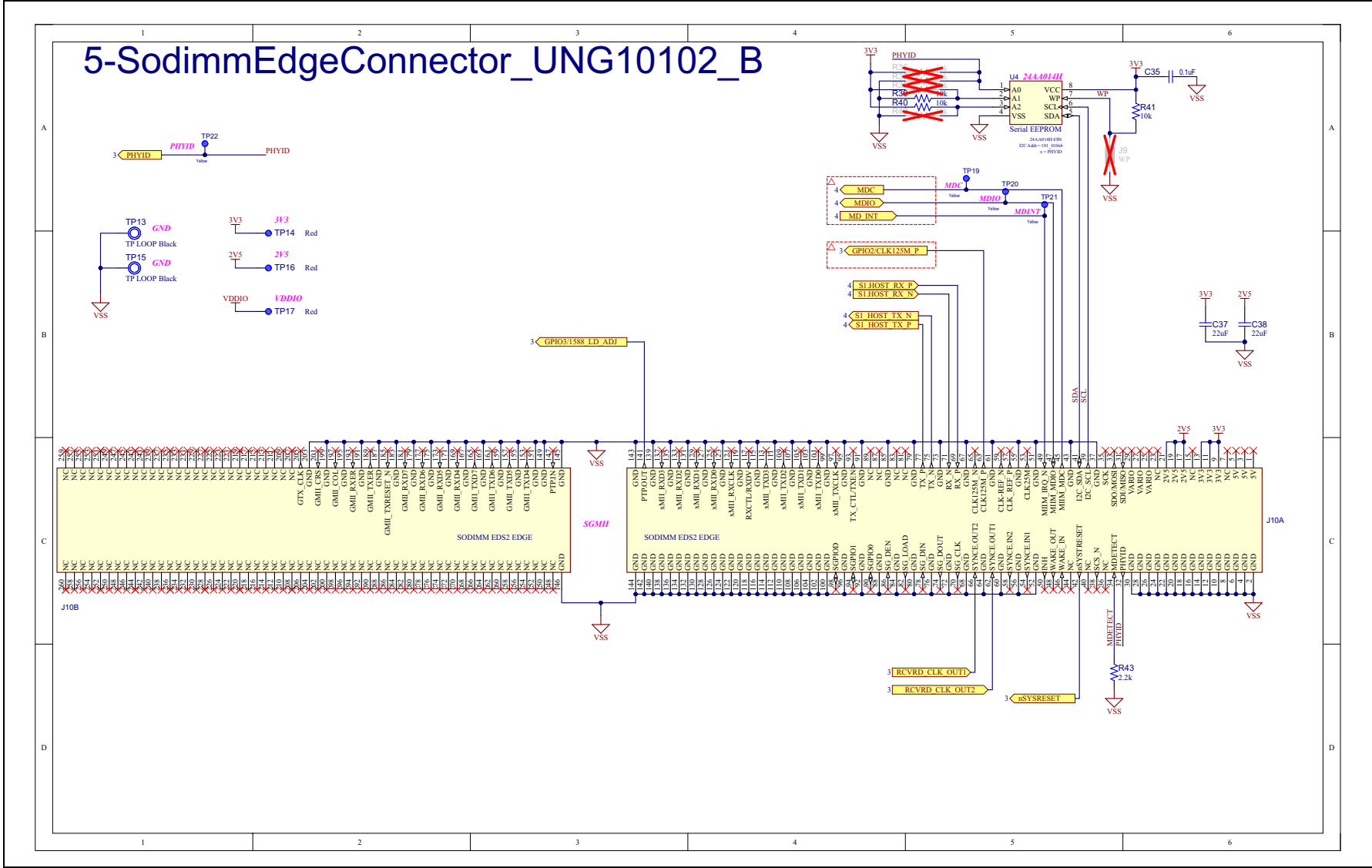
RJ45 w/ integrated magnetics (1G)



Project Owner: Michael Snyder	
PCB Layout Contact: Carl Johnson	
PartNumber: EV58G16A	Project Title: LAN8842 EDS2 Daughter Card
Sheet Title: Ethernet Ports	Variant: Standard
Size: B	SCH #: 02-01293
PCB #: 04-12356	Rev: 2
File: 4-ethernet_ports_UNG10102_B.SchDoc	Date: 11/3/2025
	Rev: 2
	Sheet 4 of 5

Designed with Altium.com

FIGURE A-5: LAN8842 EDS2 DAUGHTER CARD SODIMM EDGE CONNECTOR AND I²C MEMORY





Appendix B. Bill of Materials

B.1 INTRODUCTION

This appendix contains the LAN8842 Bill of Materials (BOM).

TABLE B-1: BILL OF MATERIALS (BOM)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
1	1	C1	CAP CER 0.1uF 16V 10% X5R SMD 0201	Yes	Murata	GRM033R61C104KE84D
2	1	C2	CAP CER 10uF 10V 10% X7R SMD 0805	Yes	Samsung Electro-Mechanics	CL21B106KPQNFNE
3	3	C3, C37, C38	CAP CER 22uF 16V 10% X5R SMD 0805	Yes	Samsung Electro-Mechanics, TDK Corporation	CL21A226KOQNNNG, C2012X5R1C226K125AC
4	5	C4, C6, C20, C21, C25	CAP CER 4.7uF 10V 10% X5R SMD 0603	Yes	KEMET	C0603C475K8PACTU
5	3	C5, C26, C35	CAP CER 0.1uF 50V 10% X7R SMD 0402	Yes	TDK Corporation, Taiyo Yuden	C1005X7R1H104K050BB, UMK105B7104KV-FR
6	1	C7	CAP CER 470pF 25V 5% NP0 SMD 0603	Yes	AVX	06033A471JAT2A
7	18	C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C22, C23, C24, C31, C32, C33, C34	CAP CER 0.1uF 35V 10% X7R SMD 0402	Yes	TDK Corporation	CGA2B3X7R1V104K050BB
8	2	C19, C29	CAP HiQ 10pF 25V 5% NP0 3.15GHz SMD 0201	Yes	Johanson Technology	250R05L100JV4T
9	1	C27	CAP CER 0.018uF 16V 10% X7R SMD 0603	Yes	Kemet	C0603C183K4RAC7867
10	1	C28	CAP CER 1000pF 2KV 10% X7R SMD 1206	Yes	Johanson Dielectrics Inc	202R18W102KV4E
11	1	D1	DIO LED GREEN 2V 30mA 35mcd Clear SMD 0603	Yes	Lite-On Inc	LTST-C191KGKT
12	1	D2	DIO RED 2V 20mA 54mcd CLEAR SMD 0603	Yes	Lite-On Inc.	LTST-C191KRKT
13	7	FB1, FB2, FB3, FB4, FB5, FB6, FB7	FERRITE 33R@100MHz 3A SMD 0603	Yes	Murata	BLM18PG330SN1D
14	1	FB8	FERRITE 500mA 220R SMD 0603	Yes	Murata Electronics North America	BLM18AG221SN1D
15	5	J1, J7, J11, J12, J13	MECH HW JUMPER 2.54mm 1x2 GOLD	MECH	Sullins Connector Solutions	QPC02SXGN-RC
16	4	J2, J3, J6, J8	CON RF Coaxial SMA Female 2P TH VERT	Yes	Adam Tech	RF2-04A-T-00-50-G
17	1	J4	CON HDR-2.54 Male 2x2 Gold 6.0MH TH VERT	Yes	JAMECO VALUEPRO	2X2SG-R
18	1	J5	CON MODULAR JACK RJ45 5G POE/FASTJACK 2xLEDs SHIELD TH	Yes	HALO Electronics	HFJ11-5G48E-L12RL
19	0	J9	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	Yes	FCI	77311-118-02LF
20	5	JP1, JP2, JP3, JP4, JP5	CON HDR-2.54 Male 1x3 Tin 6.75MH TH VERT	Yes	Molex Inc	90120-0123
21	1	LABEL1	LABEL PCBA 18x6mm Datamatrix Assy# / Rev / Serial / Date	MECH	ACT Logimark AS	505462
22	1	Q1	TRANS FET P-CH SI9433 20V 4.5A 1.3W 0.040R SOIC-8	Yes	Vishay	SI9433BDY-T1-GE3
23	1	Q2	TRANS BJT NPN MMBT3904 40V 200mA 310mW SOT-23-3	Yes	Micro Commercial Components Corporation	MMBT3904-TP
24	1	R1	RES TKF 100R 1% 1/4W SMD 1206	Yes	Yageo	RC1206FR-07100RL
25	1	R2	RES TKF 1k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1001V
26	10	R3, R4, R8, R19, R21, R22, R23, R39, R40, R41	RES TKF 10k 1% 1/10W SMD 0402	Yes	Panasonic	ERJ-2RK1002X
27	1	R5	RES TKF 27.4k 1% 1/10W SMD 0603 AEC-Q200	Yes	Panasonic Electronic Components	ERJ-3EKF2742V
28	4	R6, R17, R26, R28	RES TKF 330R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF3300V

TABLE B-1: BILL OF MATERIALS (BOM)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
29	1	R7	RES TKF 34.8k 1% 1/10W SMD 0603	Yes	Panasonic Electronic Components	ERJ-3EKF3482V
30	2	R9, R11	RES TKF 100k 1% 1/10W AEC-Q200 SMD 0603	Yes	Panasonic Electronic Components	ERJ-3EKF1003V
31	1	R10	RES TKF 1k 5% 1/10W SMD 0603	Yes	Panasonic	ERJ-3GEYJ102V
32	2	R12, R16	RES TKF 22R 1% 1/20W SMD 0402	Yes	Panasonic Electronic Components	ERJ-2RKF22R0X
33	3	R13, R15, R27	RES TKF 0R 1/10W SMD 0603	Yes	Panasonic	ERJ-3GSY0R00V
34	1	R14	RES TKF 100R 1% 1/10W SMD 0402 AEC-Q200	Yes	Panasonic Electronic Components	ERJ-2RKF1000X
35	0	R18, R20, R36, R37, R38, R42, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62	RES TKF 10k 1% 1/10W SMD 0402	Yes	Panasonic	ERJ-2RKF1002X
36	1	R24	RES TKF 200R 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF2000V
37	1	R25	RES TKF 6.04k 1% 1/10W SMD 0603 AEC-Q200	Yes	Vishay	CRCW06036K04FKEA
38	2	R29, R30	RES TKF 0R 1/5W SMD 0402 AEC-Q200	Yes	Vishay	CRCW04020000Z0EDHP
39	0	R31, R32	RES TF 2.2k 1% 1/10W SMD 0603 AEC-Q200	Yes	TE Connectivity Passive Product	CRGCQ0603F2K2
40	0	R33	RES TKF 1M 5% 1/16W SMD 0402	Yes	Yageo	RC0402JR-071ML
41	2	R34, R35	RES TKF 10k 5% 1/10W SMD 0603	Yes	Panasonic	ERJ-3GEYJ103V
42	1	R43	RES TKF 2.2k 1% 1/10W SMD 0402	Yes	Panasonic	ERJ-2RKF2201X
43	1	SW2	SWITCH DIP 1 SPST 24V 25mA 418117270901 TH	Yes	Würth Elektronik	418117270901
44	5	TP1, TP14, TP16, TP17, TP18	MISC, TEST POINT MULTI PURPOSE MINI RED	Yes	Keystone	5000
45	15	TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP19, TP20, TP21, TP22	MISC, TEST POINT PC MINI, 0.040" D YELLOW	Yes	Keystone	5004
46	2	TP13, TP15	MISC, TEST POINT MULTI PURPOSE MINI BLACK	Yes	Keystone	5001
47	1	U1	MCHP INTERFACE ETHERNET LAN8842 QFN-56	Yes	Microchip Production	IC2707
48	1	U2	MCHP ANALOG SWITCHER Buck 0.6V to 3.6V MIC33153YHJ-TR VFDFN-14	Yes	Microchip Technology	MIC33153YHJ-TR
49	1	U3	MCHP ANALOG SUPERVISOR 0.4V to 5.5V MIC2790N-04VD6 SOT-23-3	Yes	Microchip Technology	MIC2790N-04VD6
50	1	U4	MCHP MEMORY SERIAL EEPROM 1kb I2C 24AA014H-I/SN 8SOIC	Yes	Microchip Technology	24AA014H-I/SN
51	1	Y1	MCHP CRYSTAL 25Mhz +/-20ppm 10pF SMD L3.2W2.5H0.8	Yes	Microchip Technology	VXM7-9032-25M0000000

LAN8842 EDS2 Daughter Card User Guide

NOTES:



Appendix C. PCB Layers

C.1 INTRODUCTION

This appendix contains the LAN8842 EDS2 Daughter Card's PCB layers.

FIGURE C-1: LAN8842 EDS2 DAUGHTER CARD TOP SILK

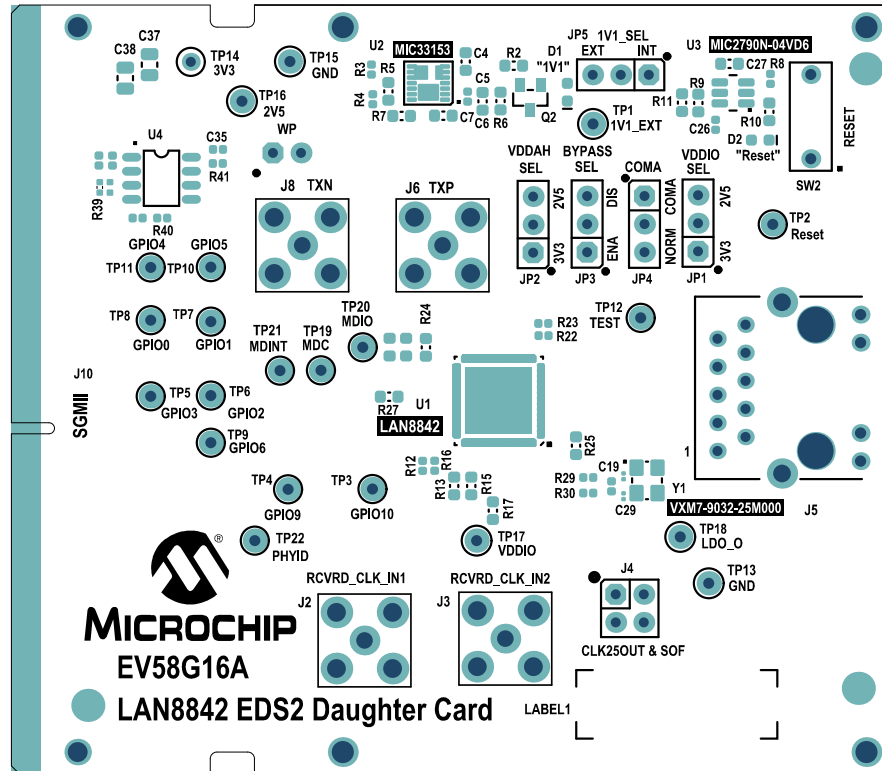


FIGURE C-2: LAN8842 EDS2 DAUGHTER CARD TOP COPPER AND SILK

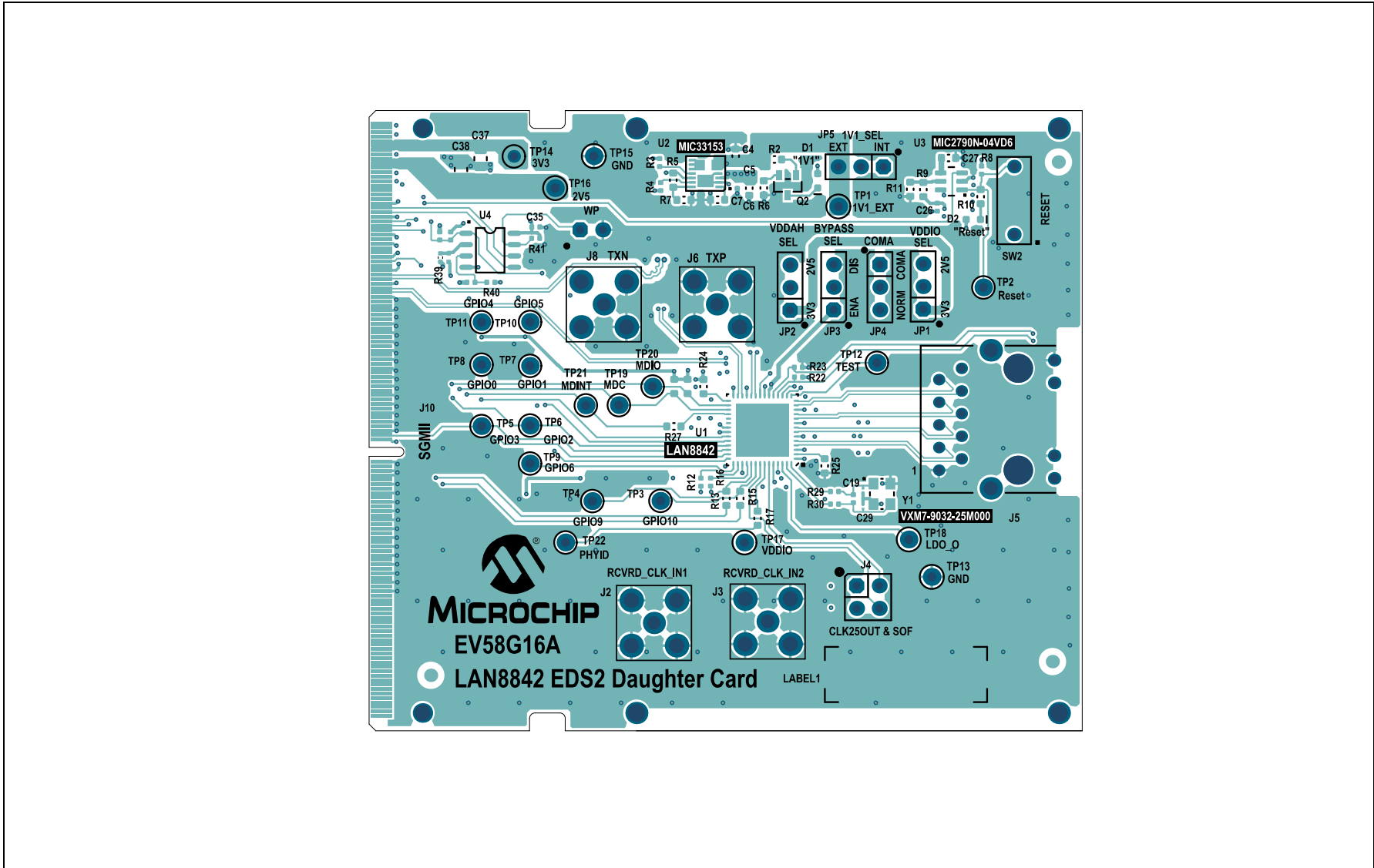


FIGURE C-3: LAN8842 EDS2 DAUGHTER CARD TOP COPPER

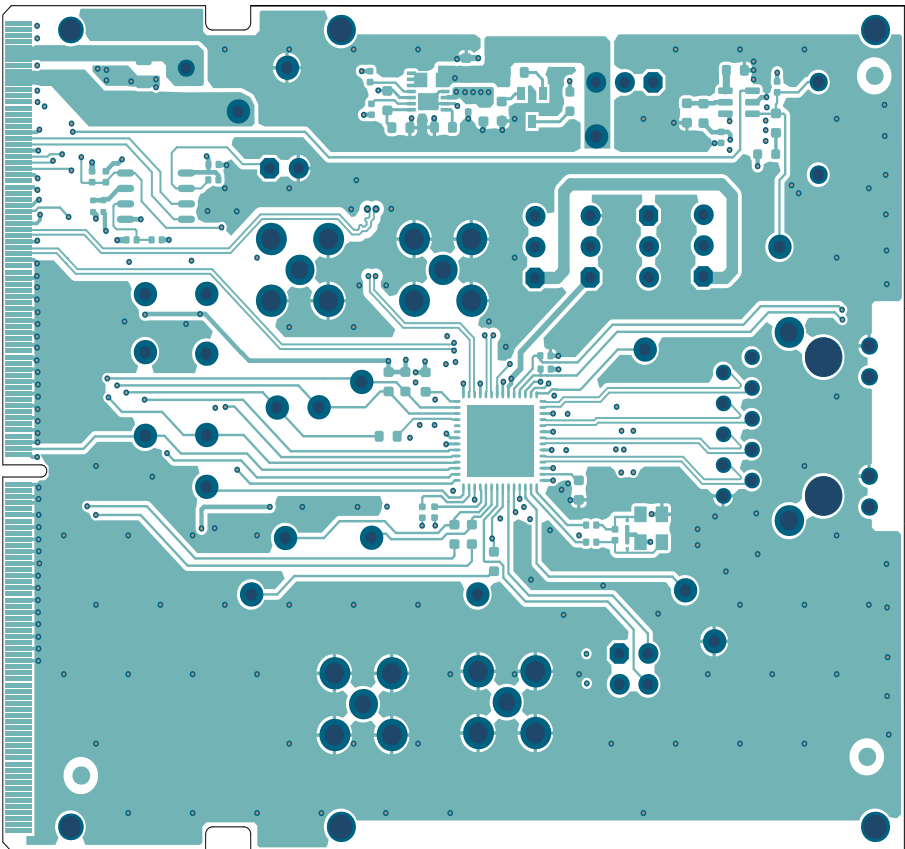


FIGURE C-4: LAN8842 EDS2 DAUGHTER CARD BOTTOM COPPER

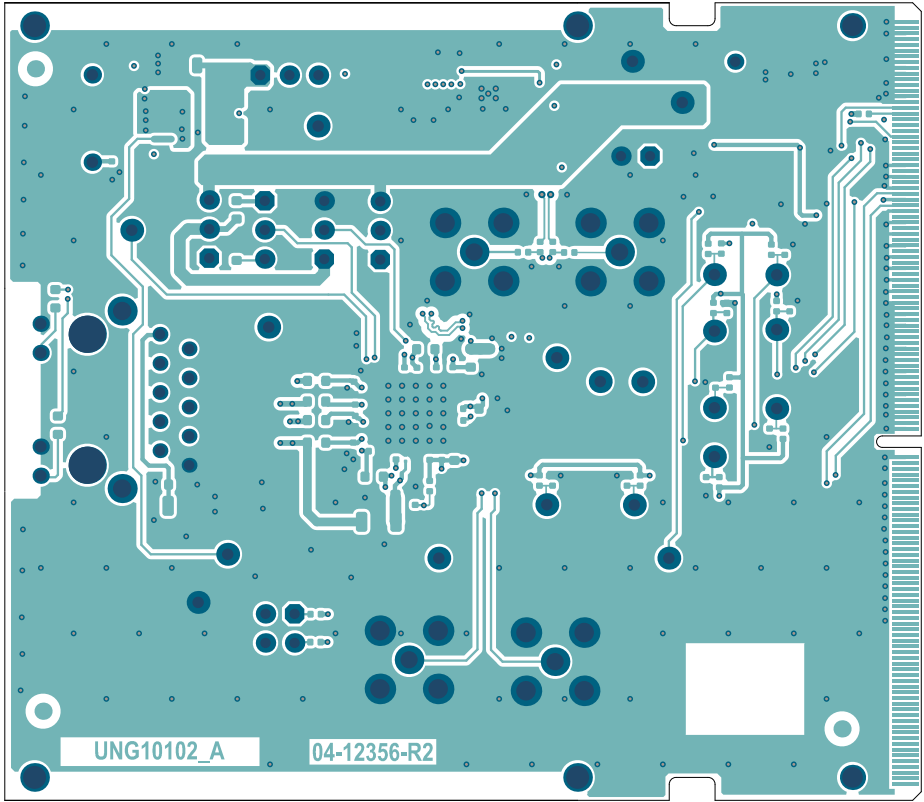


FIGURE C-5: LAN8842 EDS2 DAUGHTER CARD BOTTOM COPPER AND SILK

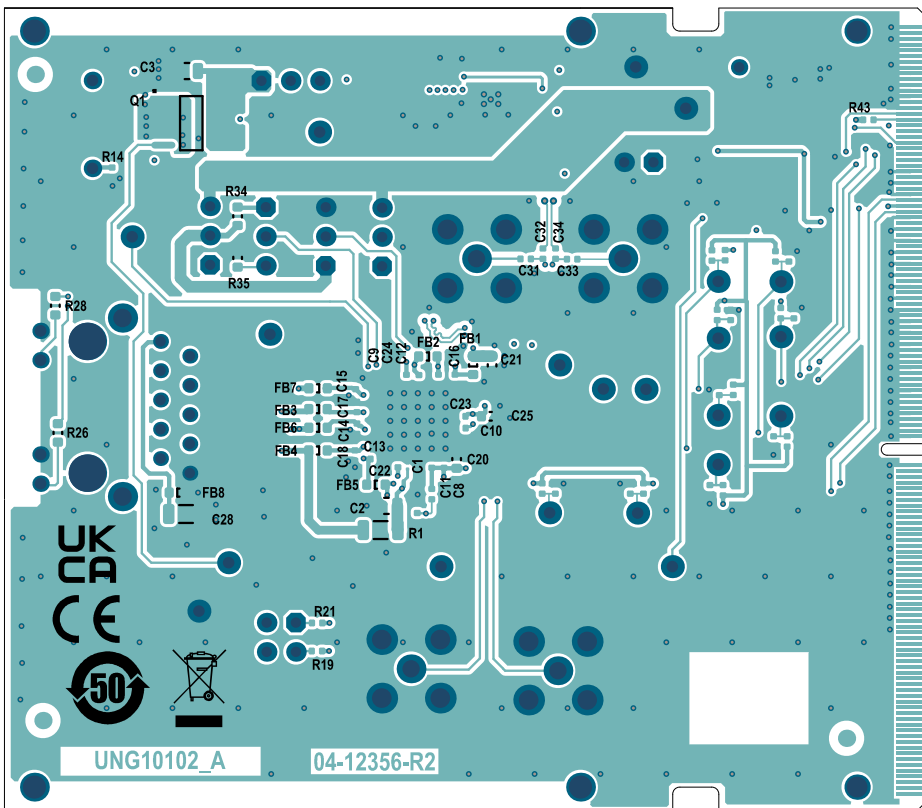


FIGURE C-6: LAN8842 EDS2 DAUGHTER CARD BOTTOM SILK

