

# High-Input Voltage, Adjustable 3-Terminal Linear Regulator

#### **Features**

- · 13.2V to 100V Input Voltage Range
- · Stable with a 100 nF Output Capacitor
- · Adjustable 1.20V to 88V Output Regulation
- 5% Reference Voltage Tolerance
- · 50 mA Minimum Output Current Limiting
- 10 µA Typical ADJ Current
- · Overtemperature Protection
- · Available in Three Different Packages

#### **Applications**

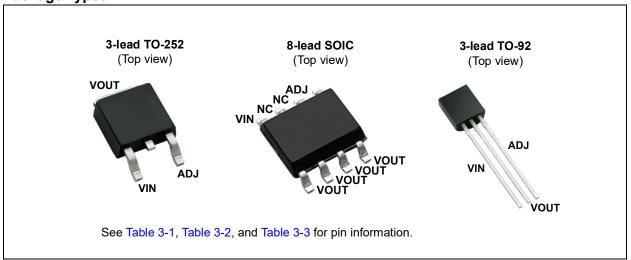
- · DC/DC SMPS Startup Circuits
- Adjustable High-voltage Constant-current Sources
- · Industrial Controls
- Motor Controls
- · Battery-powered Systems
- · Power Supplies
- Telecommunications Applications
- LED Drivers
- · Automotive Applications

#### **General Description**

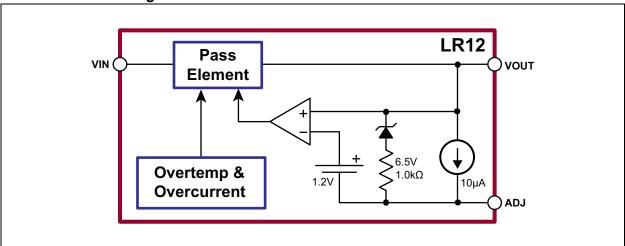
The LR12 is a high-voltage, low-output current and adjustable linear regulator. It has a wide operating input voltage range of 13.2V to 100V. The output voltage can be adjusted between 1.2V and 88V, provided that the input voltage is at least 12V greater than the output voltage. The output voltage can be adjusted by means of two external resistors,  $R_1$  and  $R_2$ , as shown in the-Typical Application Circuit diagrams. The LR12 regulates the voltage difference between  $V_{OUT}$  and ADJ pins to a nominal value of 1.2V, which is amplified by the external resistor ratio,  $R_1$  and  $R_2$ . A typical internal constant bias current of 10  $\mu A$  is connected to the ADJ pin. This increases  $V_{OUT}$  by a constant voltage of 10  $\mu A$  times  $R_2$ .

The LR12 is current limiting and temperature limiting. The output current limit is 100 mA maximum, and the minimum temperature limit is 125°C. An output short-circuit current will therefore be limited to 100 mA maximum. When the junction temperature reaches its temperature limit, the output current and/or output voltage will decrease to keep the junction temperature from exceeding the limit. For SMPS startup circuit applications, the LR12 turns off when an external voltage greater than the output voltage of the LR12 is applied to  $V_{OUT}$  of the LR12. To maintain stability, a bypass capacitor of 100 nF or larger and a minimum DC output current of 500  $\mu$ A are required.

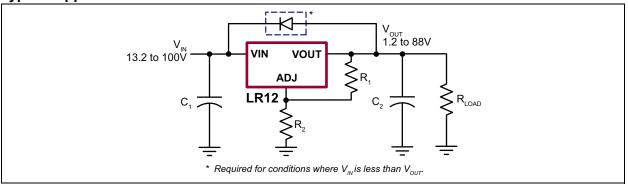
#### **Package Types**



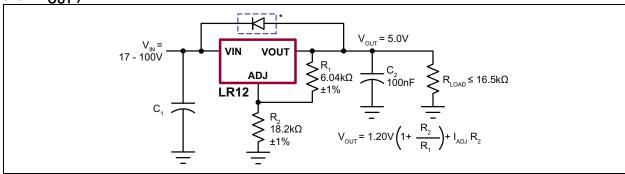
# **Functional Block Diagram**



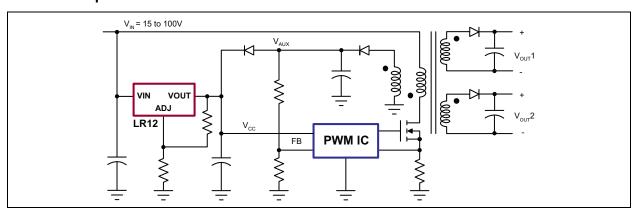
# **Typical Application Circuit**



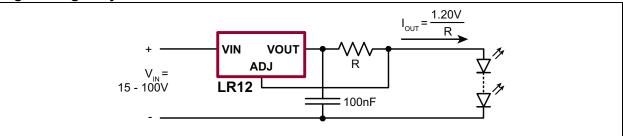
# High-input Voltage, 5V Output Linear Regulator (Required for conditions where $V_{\text{IN}}$ is less than $V_{\text{OUT}}$ .).



## **SMPS Startup Circuit**



# **High-voltage Adjustable Constant Current Source**



## 1.0 ELECTRICAL CHARACTERISTICS

## **Absolute Maximum Ratings†**

V <sub>IN-ADJ</sub>	-0.5V to +120V
V <sub>OUT-ADJ</sub>	10V to +10V
V <sub>IN</sub> V <sub>OLIT</sub>	-0.5V to +120V
Operating Ambient Temperature, T <sub>A</sub>	–40°C to +85°C
Operating Junction Temperature, T <sub>1</sub>	40°C to +125°C
Storage Temperature, T <sub>S</sub>	
Power Dissipation at T <sub>A</sub> = 25°C:	
3-lead TO-252 (DPAK)	2W
8-lead SOIC	1.8W3-la
3-lead TO-92	0.6W

**† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## **ELECTRICAL CHARACTERISTICS**

Electrical Specifications: Test conditions unless otherwise specified: -40°C < TA < +85°C										
Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions				
Input-to-output Voltage Difference	V <sub>IN</sub> –V <sub>OUT</sub>	12	_	98.8	>					
Overall Output Voltage Regulation	V <sub>OUT</sub>	1.14	1.2	1.26	>	13.2V < $V_{IN}$ < 100V, $R_1$ = 2.4 kΩ, $R_2$ = 0				
Line Regulation		_	0.003	0.03	%/V	15V < V <sub>IN</sub> < 100V, V <sub>OUT</sub> = 5V, I <sub>OUT</sub> = 0.5A				
Load Regulation	$\Delta V_{OUT}$	_	1.4	3	%	V <sub>IN</sub> = 15V, V <sub>OUT</sub> = 5V, 0.5 mA < I <sub>OUT</sub> < 50 mA				
Temperature Regulation		-1	_	+1	%	V <sub>IN</sub> = 15V, V <sub>OUT</sub> = 5V, I <sub>OUT</sub> = 10 mA, -40°C < T <sub>A</sub> < 85°C				
Output Current Limit		50	_	100	mA	$T_J$ < 85°C, $V_{IN}$ – $V_{OUT}$ < 12V				
Output Current Limit	I <sub>OUT</sub>	_	_	-0.5	IIIA	T <sub>J</sub> < 125°C, V <sub>IN</sub> -V <sub>OUT</sub> < 100V				
Minimum Output Current		0.5	_	_	mA	Includes R <sub>1</sub> and load current				
Adjust Output Current	I <sub>ADJ</sub>	5	10	15	μΑ					
Minimum Output Load Capacitance	C2	100			nF					
Ripple Rejection Ratio	DV <sub>OUT</sub> /D <sub>VIN</sub>	50	60	_	dB	120 Hz, V <sub>OUT</sub> = 5V				

## **TEMPERATURE SPECIFICATIONS**

Parameter	Sym.	Min.	Тур.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T <sub>A</sub>	-40	_	+85	°C	
Operating Junction Temperature	$T_J$	-40	_	+125	°C	
Storage Temperature	T <sub>S</sub>	-65	_	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead TO-252 (DPAK)	$\theta_{JA}$	_	81	_	°C/W	
8-lead SOIC	$\theta_{JA}$	_	101	_	°C/W	
3-lead TO-92	$\theta_{JA}$	_	132	_	°C/W	

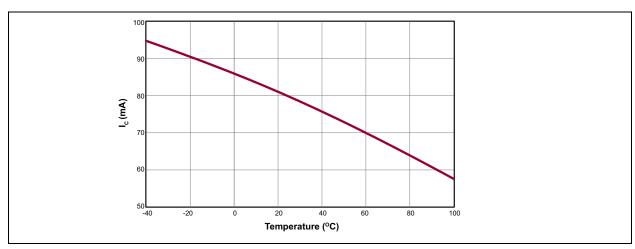


FIGURE 1-1: Current Limit.

#### 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

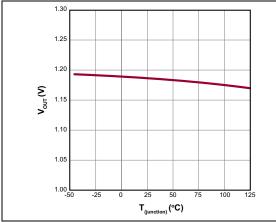


FIGURE 2-1: Temperature Variation (See Figure 4-1.).

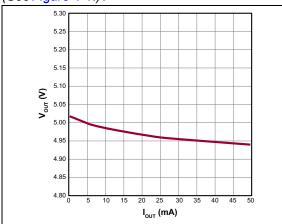
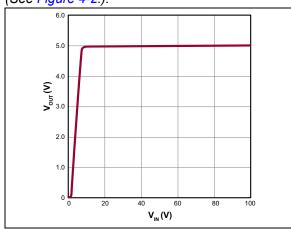


FIGURE 2-2: Load Regulation (See Figure 4-2.).



**FIGURE 2-3:**  $V_{OUT}$  vs.  $V_{IN}$  (See Figure 4-3.).

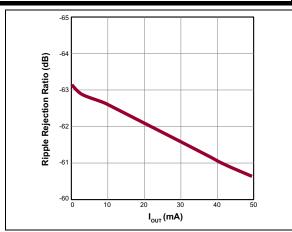
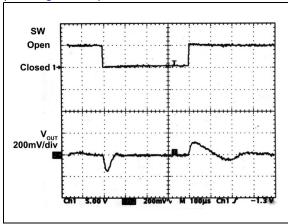


FIGURE 2-4: Ripple Rejection (See Figure 4-4.).



**FIGURE 2-5:** Load Transient Response, Load =  $509\Omega$  (See Figure 4-5.).

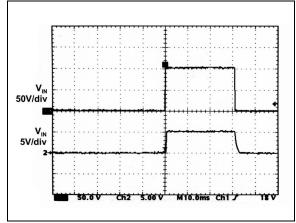


FIGURE 2-6: Line Turn-on/off Response (See Figure 4-6.).

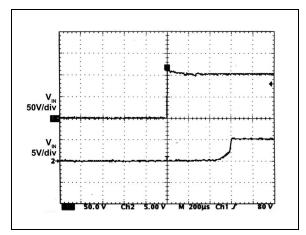


FIGURE 2-7: Line Power-up Transient (See Figure 4-6.).

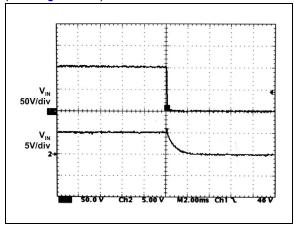


FIGURE 2-8: Line Power-down Transient (See Figure 4-6.).

## 3.0 PIN DESCRIPTION

The details on the pins of LR12 3-lead TO-252 (DPAK), 8-lead SOIC, and 3-lead TO-92 packages are listed in Table 3-1, Table 3-2, and Table 3-3, respectively. Refer to **Package Types** for the location of pins.

TABLE 3-1: 3-LEAD TO-252 (DPAK) PIN FUNCTION TABLE

Pin Number	Pin Name	Description						
1	VIN	Regulator Input Voltage						
2	VOUT	Regulator Output Voltage						
3	ADJ	Adjustment pin						
4	VOUT	Regulator Output Voltage						

#### TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE

Pin Number	Pin Name	Description					
1	VOUT	Regulator Output Voltage					
2	VOUT	Regulator Output Voltage					
3	VOUT	Regulator Output Voltage					
4	VOUT	Regulator Output Voltage					
5	ADJ	Adjustment pin					
6	NC	No connection					
7	NC	No connection					
8	VIN	Regulator Input Voltage					

#### TABLE 3-3: 3-LEAD TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description							
1	VIN	Regulator Input Voltage							
2	VOUT	Regulator Output Voltage							
3	ADJ	Adjustment pin							

#### 4.0 APPLICATION INFORMATION

#### 4.1 Measurement Circuits

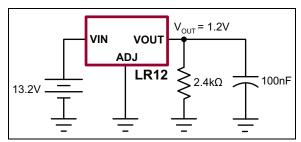


FIGURE 4-1: Temperature Variation Diagram (See Figure 2-1.).

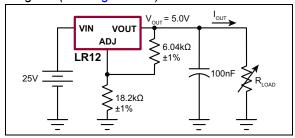
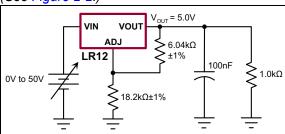
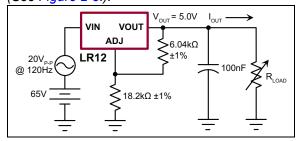


FIGURE 4-2: Load Regulation Diagram (See Figure 2-2.)



**FIGURE 4-3:**  $V_{OUT}$ vs.  $V_{IN}$  Diagram (See Figure 2-3.).



**FIGURE 4-4:** Ripple Rejection Diagram (See Figure 2-4.).

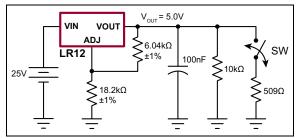


FIGURE 4-5: Load Transient Response Diagram (See Figure 2-5.).

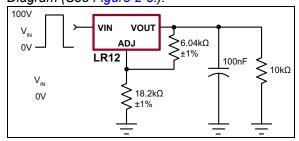
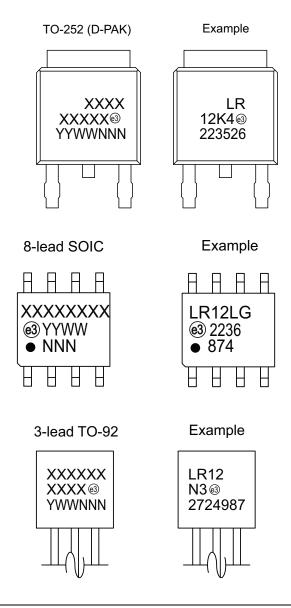


FIGURE 4-6: Line Transient Response (See Figure 2-6, Figure 2-7, and Figure 2-8.).

#### 5.0 PACKAGING INFORMATION

# 5.1 Package Marking Information

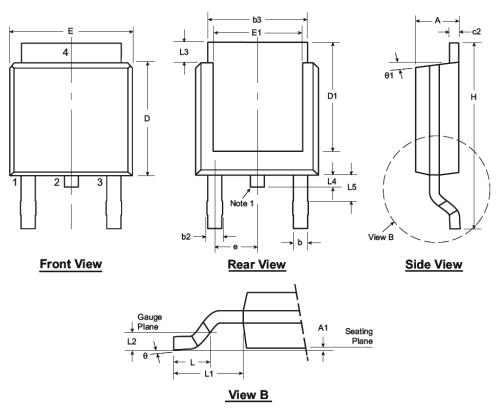


Legend: XX...X Product Code or Customer-specific information
Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')
NNN Alphanumeric traceability code

(e3) Pb-free JEDEC® designator for Matte Tin (Sn)
\* This package is Pb-free. The Pb-free JEDEC designator ((e3))
can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

# 3-Lead TO-252 (D-PAK) Package Outline (K4)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

#### Note:

Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.

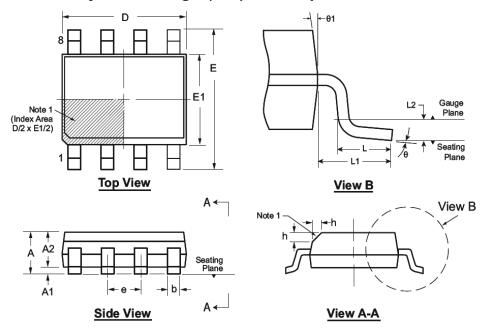
Symb	ol	Α	A1	b	b2	b3	c2	D	D1	E	E1	е	н	L	L1	L2	L3	L4	L5	θ	θ1
Dimen-	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170		.370	.055			.035	.025*	.035 <sup>†</sup>	00	00
sion	NOM	-	-	-	-	-	-	.240	-	-	-	.090 BSC	-	.060	.108 REF	.020 BSC	-	-	-	-	-
(inches)	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.200*		.410	.070			.050	.040	.060	10°	15°

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
\* This dimension is not specified in the JEDEC drawing.
† This dimension differs from the JEDEC drawing.

Drawings not to scale.

# 8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

#### Note:

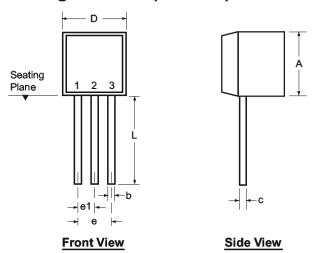
This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

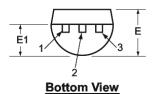
Symbo	ı	Α	A1	A2	b	D	E	E1	е	h	L	L1	L2	θ	θ1		
	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	[		0.25 0		0.40			<b>0</b> o	5º
Dimension (mm)	NOM	-	-	-	-	4.90	6.00	3.90	1.27 BSC	-	-	1.04 REF	0.25 BSC	-	-		
()	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			<b>8</b> º	15º		

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

# 3-Lead TO-92 Package Outline (L/LL/N3)





Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symb	ool	Α	b	С	D	Е	E1	е	e1	L
	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
Dimensions (inches)	NOM	-	-	-	-	-	-	-	-	-
()	MAX	.210	.022 <sup>†</sup>	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
\* This dimension is not specified in the JEDEC drawing.
† This dimension differs from the JEDEC drawing.

Drawings not to scale.

	D	4	7
L	$oldsymbol{\Gamma}$		

NOTES:

## APPENDIX A: REVISION HISTORY

## Revision A (August 2022)

- Converted Supertex Doc# DSFP-LR12 to Microchip DS20005735A
- · Updated package marking format
- Changed the quantity of the 8-lead SOIC LG package from 2500/Reel to 3300/Reel to align packaging specifications with the actual BQM
- Removed the TO-92 N3 P002,P003,P005, P013, and P014 media types to align packaging specifications with the actual BQM
- Made minor text changes throughout the document

# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	<u> </u>		- <u>X</u> - <u>X</u>	Examples:	
Device	Package Options		Environmental Media Type	a) LR12K4-G:	High-Input Voltage, Adjustable 3- Terminal Linear Regulator, 3-lead DPAK, 2000/Reel
Device:	LR12	=	High-Input Voltage, Adjustable 3-Terminal Linear Regulator	b) LR12LG-G:	High-Input Voltage, Adjustable 3- Terminal Linear Regulator, 8-lead SOIC, 3300/Reel
Packages:	K4	=	3-lead DPAK		
	LG	=	8-lead SOIC	c) LR12N3-G:	High-Input Voltage, Adjustable
	N3		3-lead TO-92	,	3-Terminal Linear Regulator, 3-lead TO-92, 1000/Bag
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package		
Media Types:	(blank)	=	2000/Reel for a K4 Package		
,,	( ,	=	3300/Reel for an LG Package		
		=	1000/Bag for an N3 Package		
			3		

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