



# LIS331HH

## MEMS digital output motion sensor ultra low-power high full-scale 3-axes “nano” accelerometer

Preliminary data

### Features

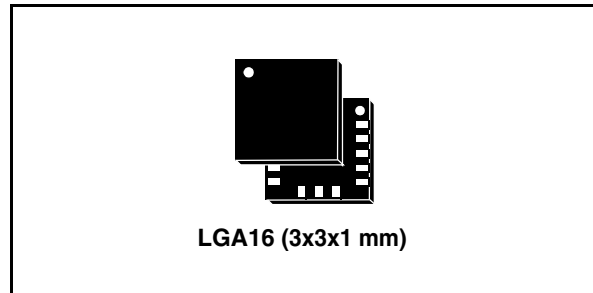
- Wide supply voltage, 2.16 V to 3.6 V
- Low voltage compatible IOs, 1.8 V
- Ultra low-current mode consumption down to 10  $\mu$ A
- $\pm 6g/\pm 12g/\pm 24g$  dynamically selectable full-scale
- I<sup>2</sup>C/SPI digital output interface
- 16 bit data output
- 2 independent programmable interrupt engines
- Sleep to wake-up function
- 6D orientation detection
- Embedded self-test
- 10000 g high shock survivability
- ECOPACK<sup>®</sup> RoHS and “Green” compliant (see [Section 8](#))

### Applications

- Pedometer
- Gaming and virtual reality input devices
- Motion activated functions
- Impact recognition and logging
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation

### Description

The LIS331HH is an ultra low-power high performance high full-scale three axes linear



accelerometer belonging to the “nano” family, with digital I<sup>2</sup>C/SPI serial interface standard output.

The device features ultra low-power operational modes that allow advanced power saving and smart sleep to wake-up functions.

The LIS331HH has dynamically user selectable full scales of  $\pm 6g/\pm 12g/\pm 24g$  and it is capable of measuring accelerations with output data rates from 0.5 Hz to 1 kHz. The self-test capability allows the user to check the functioning of the sensor in the final application.

The device contains 2 independent interrupt engines able to recognize dedicated inertial events.

Thresholds and timing of interrupt generators are programmable by the end user on the fly.

The LIS331HH is available in small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

| Order codes | Temperature range [°C] | Package | Packaging     |
|-------------|------------------------|---------|---------------|
| LIS331HH    | -40 to +85             | LGA16   | Tray          |
| LIS331HHTR  | -40 to +85             | LGA16   | Tape and reel |

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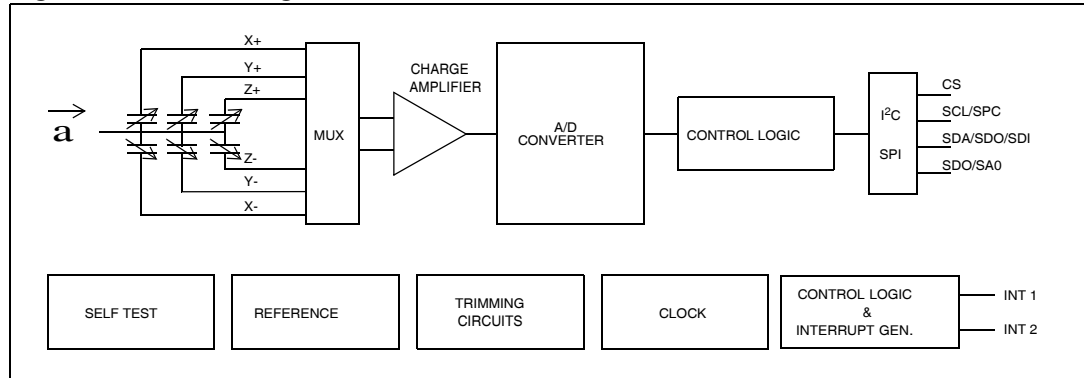
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# 1 Block diagram and pin description

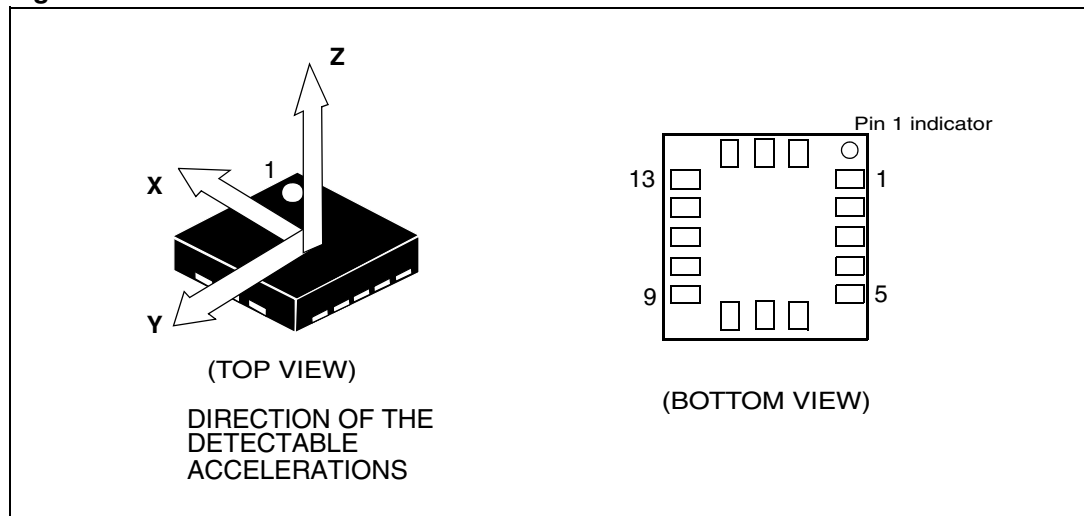
## 1.1 Block diagram

Figure 1. Block diagram



## 1.2 Pin description

Figure 2. Pin connection



**Table 2. Pin description**

| Pin# | Name              | Function   |
|------|-------------------|--|
| 1    | Vdd_IO            | Power supply for I/O pins  |
| 2    | NC                | Not connected  |
| 3    | NC                | Not connected  |
| 4    | SCL<br>SPC        | I <sup>2</sup> C serial clock (SCL)<br>SPI serial port clock (SPC)   |
| 5    | GND               | 0V supply  |
| 6    | SDA<br>SDI<br>SDO | I <sup>2</sup> C serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |
| 7    | SDO<br>SA0        | SPI serial data output (SDO)<br>I <sup>2</sup> C less significant bit of the device address (SA0)              |
| 8    | CS                | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: I <sup>2</sup> C mode; 0: SPI enabled)                   |
| 9    | INT 2             | Inertial interrupt 2   |
| 10   | Reserved          | Connect to GND   |
| 11   | INT 1             | Inertial interrupt 1   |
| 12   | GND               | 0 V supply   |
| 13   | GND               | 0 V supply   |
| 14   | Vdd               | Power supply   |
| 15   | Reserved          | Connect to Vdd   |
| 16   | GND               | 0 V supply   |



## 2 Mechanical and electrical specifications

### 2.1 Mechanical characteristics

**Table 3. Mechanical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted <sup>(1)</sup>**

| Symbol | Parameter   | Test conditions                           | Min. | Typ. <sup>(2)</sup> | Max. | Unit     |
|--------|---|---|------|---------------------|------|----------|
| FS     | Measurement range <sup>(3)</sup>                                | FS bit set to 00                          |      | ±6                  |      | g        |
|        |   | FS bit set to 01                          |      | ±12                 |      |          |
|        |   | FS bit set to 11                          |      | ±24                 |      |          |
| So     | Sensitivity   | FS bit set to 00<br>12 bit representation |      | 3                   |      | mg/digit |
|        |   | FS bit set to 01<br>12 bit representation |      | 6                   |      |          |
|        |   | FS bit set to 11<br>12 bit representation |      | 12                  |      |          |
| TCSO   | Sensitivity change vs temperature                               | FS bit set to 00                          |      | ±0.01               |      | %/°C     |
| TyOff  | Typical zero- <i>g</i> level offset accuracy <sup>(4),(5)</sup> | FS bit set to 00                          |      | ±70                 |      | mg       |
| TCOff  | Zero- <i>g</i> level change vs temperature                      | Max delta from 25 °C                      |      | ±0.4                |      | mg/°C    |
| An     | Acceleration noise density                                      | FS bit set to 00                          |      | 650                 |      | µg/√Hz   |
| Vst    | Self-test output change <sup>(6),(7),(8)</sup>                  | FS bit set to 00<br>X axis                | 50   | 110                 | 180  | LSb      |
|        |   | FS bit set to 00<br>Y axis                | -50  | -100                | -180 | LSb      |
|        |   | FS bit set to 00<br>Z axis                | 220  | 290                 | 370  | LSb      |
| Top    | Operating temperature range                                     |   | -40  |                     | +85  | °C       |
| Wh     | Product weight  |   |      | 20                  |      | mgram    |

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.
2. Typical specifications are not guaranteed
3. Verified by wafer level test and measurement of initial offset and sensitivity
4. Typical zero-*g* level offset value after MSL3 preconditioning
5. Offset can be eliminated by enabling the built-in high pass filter
6. The sign of "Self-test output change" is defined by CTRL\_REG4 STsign bit ([Table 27](#)), for all axes.
7. Self-test output changes with the power supply. "Self-test output change" is defined as  $OUTPUT[LSb]_{(CTRL\_REG4\ ST\ bit=1)} - OUTPUT[LSb]_{(CTRL\_REG4\ ST\ bit=0)}$ . 1LSb=12g/4096 at 12bit representation, ±6 g Full-scale
8. Output data reach 99% of final value after 1/ODR+1ms when enabling self-test mode, due to device filtering

## 2.2 Electrical characteristics

**Table 4. Electrical characteristics @ Vdd = 2.5 V, T = 25 °C unless otherwise noted <sup>(1)</sup>**

| Symbol            | Parameter                              | Test conditions   | Min.       | Typ. <sup>(2)</sup> | Max.       | Unit |
|-------------------|--|-------------------|------------|---------------------|------------|------|
| Vdd               | Supply voltage                         |                   | 2.16       | 2.5                 | 3.6        | V    |
| Vdd_IO            | I/O pins supply voltage <sup>(3)</sup> |                   | 1.71       |                     | Vdd+0.1    | V    |
| Idd               | Current consumption in normal mode     |                   |            | 250                 |            | µA   |
| IddLP             | Current consumption in low-power mode  |                   |            | 10                  |            | µA   |
| IddPdn            | Current consumption in power-down mode |                   |            | 1                   |            | µA   |
| VIH               | Digital high level input voltage       |                   | 0.8*Vdd_IO |                     |            | V    |
| VIL               | Digital low level input voltage        |                   |            |                     | 0.2*Vdd_IO | V    |
| VOH               | High level output voltage              |                   | 0.9*Vdd_IO |                     |            | V    |
| VOL               | Low level output voltage               |                   |            |                     | 0.1*Vdd_IO | V    |
| ODR               | Output data rate in normal mode        | DR bit set to 00  |            | 50                  |            | Hz   |
|                   |  | DR bit set to 01  |            | 100                 |            |      |
|                   |  | DR bit set to 10  |            | 400                 |            |      |
|                   |  | DR bit set to 11  |            | 1000                |            |      |
| ODR <sub>LP</sub> | Output data rate in low-power mode     | PM bit set to 010 |            | 0.5                 |            | Hz   |
|                   |  | PM bit set to 011 |            | 1                   |            |      |
|                   |  | PM bit set to 100 |            | 2                   |            |      |
|                   |  | PM bit set to 101 |            | 5                   |            |      |
|                   |  | PM bit set to 110 |            | 10                  |            |      |
| BW                | System bandwidth <sup>(4)</sup>        |                   |            | ODR/2               |            | Hz   |
| Ton               | Turn-on time <sup>(5)</sup>            | ODR = 100 Hz      |            | 1/ODR+1ms           |            | s    |
| Top               | Operating temperature range            |                   | -40        |                     | +85        | °C   |

1. The product is factory calibrated at 2.5 V. The operational power supply range is from 2.16 V to 3.6 V.
2. Typical specification are not guaranteed
3. It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication busses, in this condition the measurement chain is powered off.
4. Refer to [Table 19](#) for filter cut-off frequency
5. Time to obtain valid data after exiting power-down mode

## 2.3 Communication interface characteristics

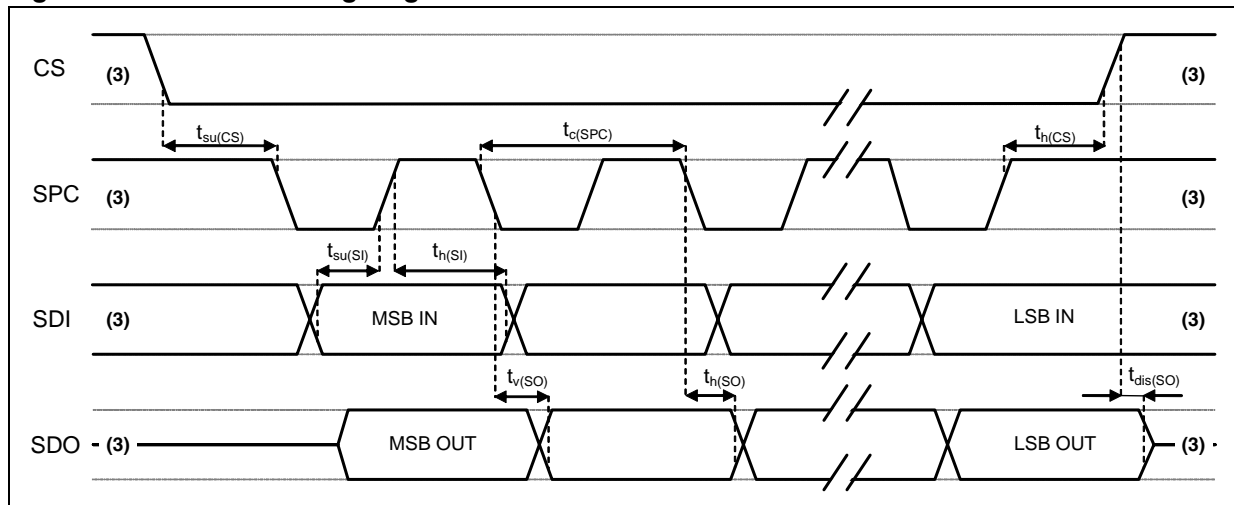
### 2.3.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

**Table 5. SPI slave timing values**

| Symbol   | Parameter               | Value <sup>(1)</sup> |     | Unit |
|----------|-------------------------|----------------------|-----|------|
|          |                         | Min                  | Max |      |
| tc(SPC)  | SPI clock cycle         | 100                  |     | ns   |
| fc(SPC)  | SPI clock frequency     |                      | 10  | MHz  |
| tsu(CS)  | CS setup time           | 6                    |     | ns   |
| th(CS)   | CS hold time            | 8                    |     |      |
| tsu(SI)  | SDI input setup time    | 5                    |     |      |
| th(SI)   | SDI input hold time     | 15                   |     |      |
| tv(SO)   | SDO valid output time   |                      | 50  |      |
| th(SO)   | SDO output hold time    | 9                    |     |      |
| tdis(SO) | SDO output disable time |                      | 50  |      |

**Figure 3. SPI slave timing diagram <sup>(2)</sup>**



1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production
2. Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both Input and output port
3. When no communication is on-going, data on CS, SPC, SDI and SDO are driven by internal pull-up resistors

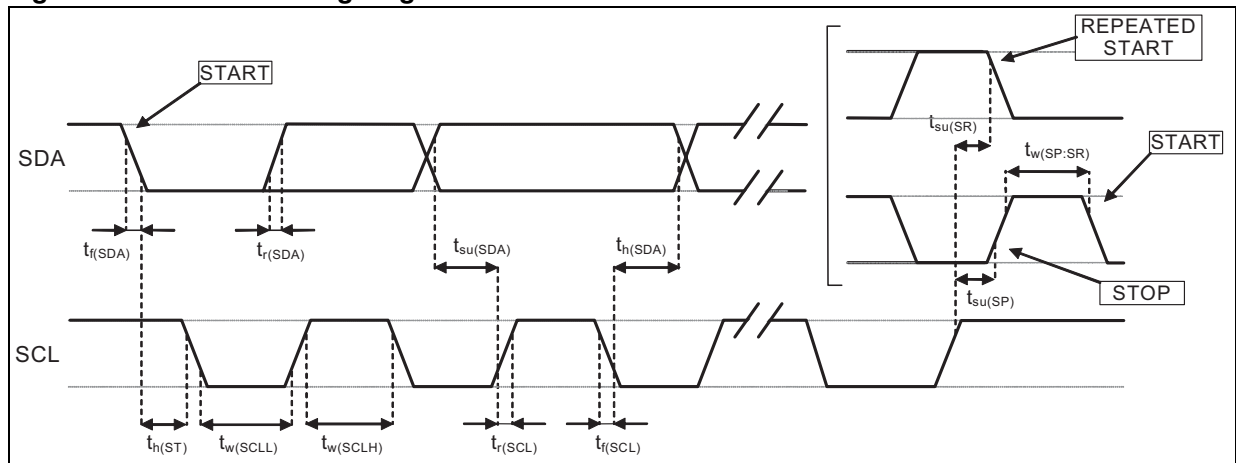
### 2.3.2 I<sup>2</sup>C - inter IC control interface

Subject to general operating conditions for Vdd and Top.

Table 6. I<sup>2</sup>C slave timing values

| Symbol                                  | Parameter                                      | I <sup>2</sup> C standard mode (1) |      | I <sup>2</sup> C fast mode (1) |     | Unit |
|---|--|------------------------------------|------|--------------------------------|-----|------|
|   |  | Min                                | Max  | Min                            | Max |      |
| f <sub>(SCL)</sub>                      | SCL clock frequency                            | 0                                  | 100  | 0                              | 400 | KHz  |
| t <sub>w(SCLL)</sub>                    | SCL clock low time                             | 4.7                                |      | 1.3                            |     | μs   |
| t <sub>w(SCLH)</sub>                    | SCL clock high time                            | 4.0                                |      | 0.6                            |     |      |
| t <sub>su(SDA)</sub>                    | SDA setup time                                 | 250                                |      | 100                            |     | ns   |
| t <sub>h(SDA)</sub>                     | SDA data hold time                             | 0                                  | 3.45 | 0.01                           | 0.9 | μs   |
| t <sub>r(SDA)</sub> t <sub>r(SCL)</sub> | SDA and SCL rise time                          |                                    | 1000 | 20 + 0.1C <sub>b</sub> (2)     | 300 | ns   |
| t <sub>f(SDA)</sub> t <sub>f(SCL)</sub> | SDA and SCL fall time                          |                                    | 300  | 20 + 0.1C <sub>b</sub> (2)     | 300 |      |
| t <sub>h(ST)</sub>                      | START condition hold time                      | 4                                  |      | 0.6                            |     | μs   |
| t <sub>su(SR)</sub>                     | Repeated START condition setup time            | 4.7                                |      | 0.6                            |     |      |
| t <sub>su(SP)</sub>                     | STOP condition setup time                      | 4                                  |      | 0.6                            |     |      |
| t <sub>w(SP:SR)</sub>                   | Bus free time between STOP and START condition | 4.7                                |      | 1.3                            |     |      |

Figure 4. I<sup>2</sup>C slave timing diagram (3)



1. Data based on standard I<sup>2</sup>C protocol requirement, not tested in production
2. C<sub>b</sub> = total capacitance of one bus line, in pF
3. Measurement points are done at 0.2·Vdd\_IO and 0.8·Vdd\_IO, for both port

## 2.4 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 7. Absolute maximum ratings**

| Symbol             | Ratings   | Maximum value                   | Unit |
|--------------------|---|---------------------------------|------|
| V <sub>dd</sub>    | Supply voltage  | -0.3 to 6                       | V    |
| V <sub>dd_IO</sub> | I/O pins Supply voltage   | -0.3 to 6                       | V    |
| V <sub>in</sub>    | Input voltage on any control pin<br>(CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0) | -0.3 to V <sub>dd_IO</sub> +0.3 | V    |
| A <sub>POW</sub>   | Acceleration (any axis, powered, V <sub>dd</sub> = 2.5 V)               | 3000 g for 0.5 ms               |      |
|                    |   | 10000 g for 0.1 ms              |      |
| A <sub>UNP</sub>   | Acceleration (any axis, unpowered)                                      | 3000 g for 0.5 ms               |      |
|                    |   | 10000 g for 0.1 ms              |      |
| T <sub>OP</sub>    | Operating temperature range   | -40 to +85                      | °C   |
| T <sub>STG</sub>   | Storage temperature range   | -40 to +125                     | °C   |
| ESD                | Electrostatic discharge protection                                      | 4 (HBM)                         | kV   |
|                    |   | 1.5 (CDM)                       | kV   |
|                    |   | 200 (MM)                        | V    |

*Note:* Supply voltage on any pin should never exceed 6.0 V



This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part



This is an ESD sensitive device, improper handling can cause permanent damages to the part

## 2.5 Terminology

### 2.5.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so,  $\pm 1$  *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of Sensitivities of a large population of sensors.

### 2.5.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* in X axis and 0 *g* in Y axis whereas the Z axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

### 2.5.3 Self-test

Self-test allows to check the sensor functionality without moving it. The self-test function is off when the self-test bit (ST) of CTRL\_REG4 (control register 4) is programmed to '0'. When the self-test bit of CTRL\_REG4 is programmed to '1' an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs will exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside [Table 3](#), then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

### 2.5.4 Sleep to wake-up

The "sleep to wake-up" function, in conjunction with low-power mode, allows to further reduce the system power consumption and develop new smart applications.

LIS331HH may be set in a low-power operating mode, characterized by lower data rates refreshments. In this way the device, even if sleeping, keep on sensing acceleration and generating interrupt requests.

When the "sleep to wake-up" function is activated, LIS331HH is able to automatically wake-up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth.

With this feature the system may be efficiently switched from low-power mode to full-performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

## 3 Functionality

The LIS331HH is a “nano”, low-power, high full-scale digital output 3-axis linear accelerometer packaged in a LGA package. The complete device includes a sensing element and an IC interface able to take the information from the sensing element and to provide a signal to the external world through an I<sup>2</sup>C/SPI serial interface.

### 3.1 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the moulding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady state the nominal value of the capacitors are few pF and when an acceleration is applied the maximum variation of the capacitive load is in the fF range.

### 3.2 IC interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage that is finally available to the user by an analog-to-digital converter.

The acceleration data may be accessed through an I<sup>2</sup>C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS331HH features a Data-Ready signal (RDY) which indicates when a new set of measured acceleration data is available thus simplifying data synchronization in the digital system that uses the device.

The LIS331HH may also be configured to generate an inertial dedicated interrupt signals accordingly to a programmed acceleration event along the enabled axes. Both interrupt can be available simultaneously on two different pins.

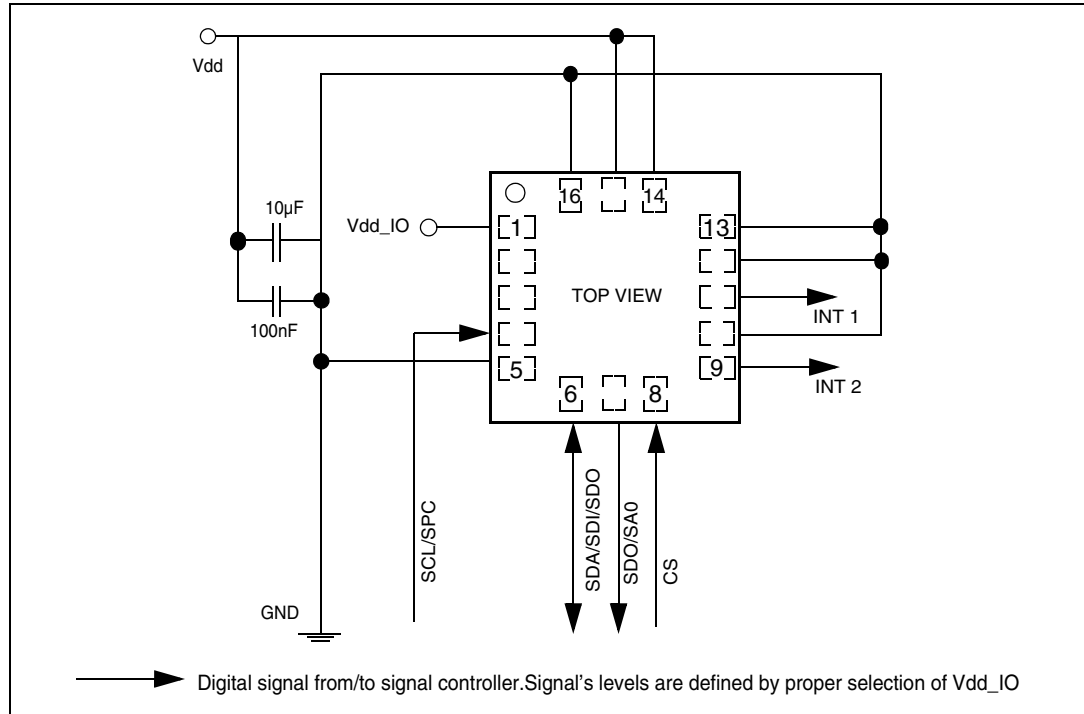
### 3.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-g level (TyOff).

The trimming values are stored inside the device in a non volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows to use the device without further calibration.

## 4 Application hints

**Figure 5. LIS331HH electrical connection**



The device core is supplied through Vdd line while the I/O pads are supplied through Vdd\_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF Aluminum) should be placed as near as possible to the pin 14 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd maintaining Vdd\_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I<sup>2</sup>C or SPI interfaces. When using the I<sup>2</sup>C, CS must be tied high.

The functions, the threshold and the timing of the two interrupt pins (INT 1 and INT 2) can be completely programmed by the user through the I<sup>2</sup>C/SPI interface.

### 4.1 Soldering information

The LGA package is compliant with the ECOPACK<sup>®</sup>, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020C.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at [www.st.com](http://www.st.com).



## 5 Digital interfaces

The registers embedded inside the LIS331HH may be accessed through both the I<sup>2</sup>C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I<sup>2</sup>C interface, CS line must be tied high (i.e. connected to Vdd\_IO).

**Table 8. Serial interface pin description**

| Pin name | Pin description  |
|----------|--|
| CS       | SPI enable<br>I <sup>2</sup> C/SPI mode selection (1: I <sup>2</sup> C mode; 0: SPI enabled) |
| SCL      | I <sup>2</sup> C serial clock (SCL)  |
| SPC      | SPI serial port clock (SPC)  |
| SDA      | I <sup>2</sup> C serial data (SDA)   |
| SDI      | SPI serial data input (SDI)  |
| SDO      | 3-wire interface serial data output (SDO)  |
| SA0      | I <sup>2</sup> C less significant bit of the device address (SA0)                            |
| SDO      | SPI serial data output (SDO)   |

### 5.1 I<sup>2</sup>C serial interface

The LIS331HH I<sup>2</sup>C is a bus slave. The I<sup>2</sup>C is employed to write data into registers whose content can also be read back.

The relevant I<sup>2</sup>C terminology is given in the table below.

**Table 9. Serial interface pin description**

| Term        | Description  |
|-------------|--|
| Transmitter | The device which sends data to the bus   |
| Receiver    | The device which receives data from the bus  |
| Master      | The device which initiates a transfer, generates clock signals and terminates a transfer |
| Slave       | The device addressed by the master   |

There are two signals associated with the I<sup>2</sup>C bus: the serial clock line (SCL) and the Serial DATA line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines are connected to Vdd\_IO through a pull-up resistor embedded inside the LIS331HH. When the bus is free both the lines are high.

The I<sup>2</sup>C interface is compliant with fast mode (400 kHz) I<sup>2</sup>C standards as well as with the normal mode.

### 5.1.1 I<sup>2</sup>C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADDRESS (SAD) associated to the LIS331HH is 001100xb. **SDO/SA0** pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSb is '1' (address 0011001b) else if SA0 pad is connected to ground, LSb value is '0' (address 0011000b). This solution permits to connect and address two different accelerometers to the same I<sup>2</sup>C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I<sup>2</sup>C embedded inside the LIS331HH behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged. [Table 10](#) explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

**Table 10. SAD+Read/Write patterns**

| Command | SAD[6:1] | SAD[0] = SA0 | R/W | SAD+R/W        |
|---------|----------|--------------|-----|----------------|
| Read    | 001100   | 0            | 1   | 00110001 (31h) |
| Write   | 001100   | 0            | 0   | 00110000 (30h) |
| Read    | 001100   | 1            | 1   | 00110011 (33h) |
| Write   | 001100   | 1            | 0   | 00110010 (32h) |

**Table 11. Transfer when master is writing one byte to slave**

|        |    |         |     |     |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |    |

**Table 12. Transfer when master is writing multiple bytes to slave:**

|        |    |         |     |     |     |      |     |      |     |    |
|--------|----|---------|-----|-----|-----|------|-----|------|-----|----|
| Master | ST | SAD + W |     | SUB |     | DATA |     | DATA |     | SP |
| Slave  |    |         | SAK |     | SAK |      | SAK |      | SAK |    |

**Table 13. Transfer when master is receiving (reading) one byte of data from slave:**

|        |    |         |     |     |     |    |         |     |      |      |    |
|--------|----|---------|-----|-----|-----|----|---------|-----|------|------|----|
| Master | ST | SAD + W |     | SUB |     | SR | SAD + R |     |      | NMAK | SP |
| Slave  |    |         | SAK |     | SAK |    |         | SAK | DATA |      |    |

**Table 14. Transfer when Master is receiving (reading) multiple bytes of data from slave**

|        |    |       |     |     |     |    |       |     |      |     |      |     |      |      |    |
|--------|----|-------|-----|-----|-----|----|-------|-----|------|-----|------|-----|------|------|----|
| Master | ST | SAD+W |     | SUB |     | SR | SAD+R |     |      | MAK |      | MAK |      | NMAK | SP |
| Slave  |    |       | SAK |     | SAK |    |       | SAK | DATA |     | DATA |     | DATA |      |    |

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

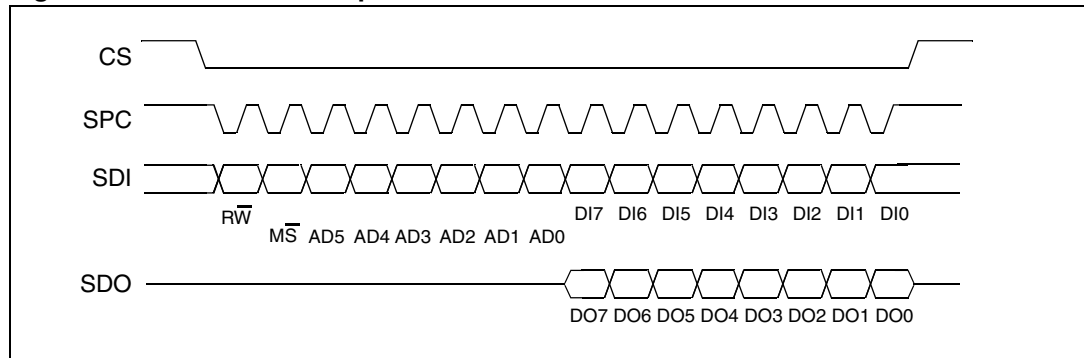
In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

## 5.2 SPI bus interface

The LIS331HH SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

**Figure 6. Read and write protocol**



**CS** is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

**bit 0:**  $\overline{RW}$  bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

**bit 1:**  $\overline{MS}$  bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

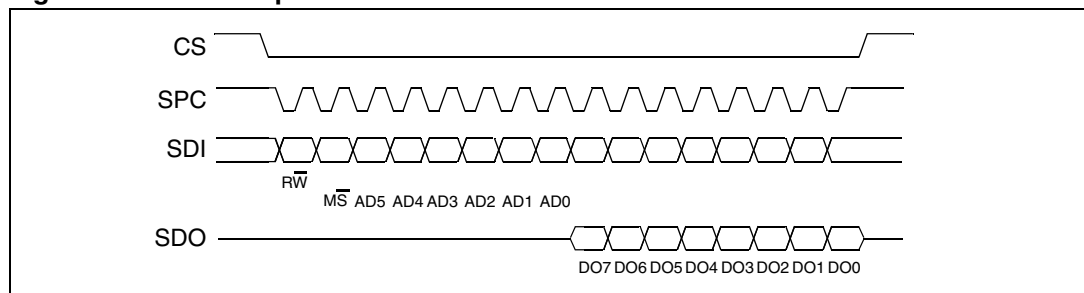
**bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When  $\overline{MS}$  bit is '0' the address used to read/write data remains the same for every block. When  $\overline{MS}$  bit is '1' the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

### 5.2.1 SPI read

**Figure 7. SPI read protocol**



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

**bit 0:** READ bit. The value is 1.

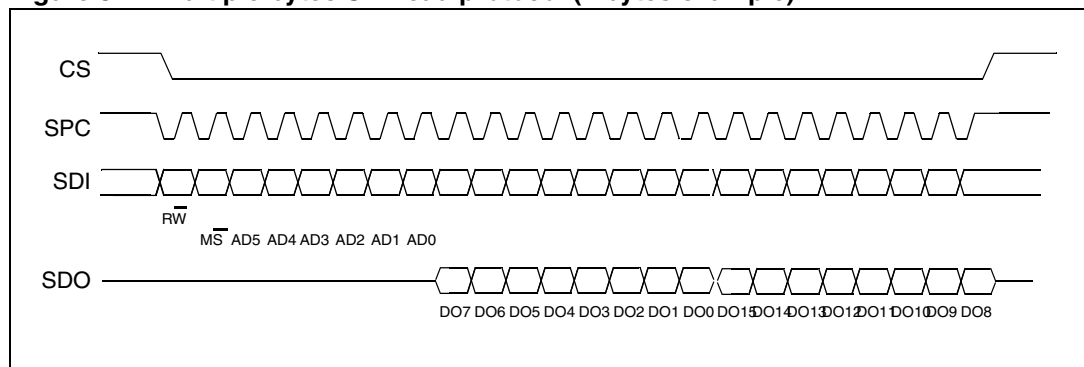
**bit 1:**  $\overline{MS}$  bit. When 0 do not increment address, when 1 increment address in multiple reading.

**bit 2-7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

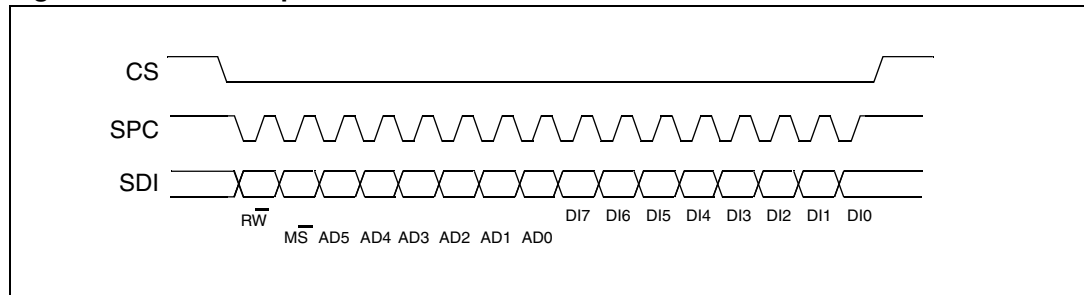
**bit 16-...** : data DO(...-8). Further data in multiple byte reading.

**Figure 8. Multiple bytes SPI read protocol (2 bytes example)**



### 5.2.2 SPI write

**Figure 9. SPI write protocol**



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

**bit 0:** WRITE bit. The value is 0.

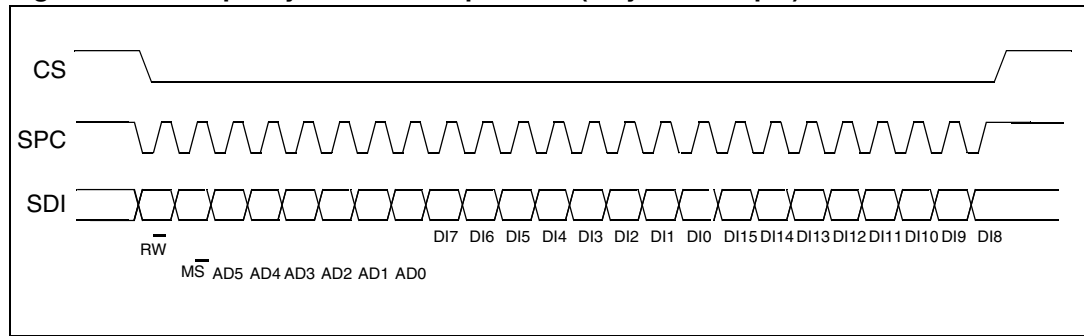
**bit 1:**  $\overline{MS}$  bit. When 0 do not increment address, when 1 increment address in multiple writing.

**bit 2 -7:** address AD(5:0). This is the address field of the indexed register.

**bit 8-15:** data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

**bit 16-...** : data DI(...-8). Further data in multiple byte writing.

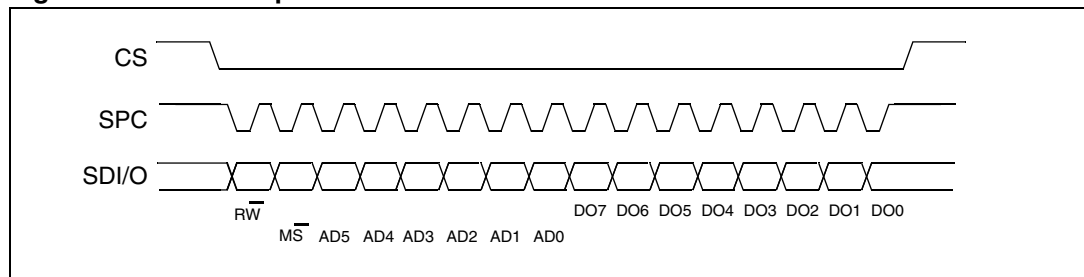
**Figure 10. Multiple bytes SPI write protocol (2 bytes example)**



### 5.2.3 SPI read in 3-wires mode

3-wires mode is entered by setting to '1' bit SIM (SPI serial interface mode selection) in CTRL\_REG4.

**Figure 11. SPI read protocol in 3-wires mode**



The SPI read command is performed with 16 clock pulses:

- bit 0:** READ bit. The value is 1.
  - bit 1:**  $\overline{MS}$  bit. When 0 do not increment address, when 1 increment address in multiple reading.
  - bit 2-7:** address AD(5:0). This is the address field of the indexed register.
  - bit 8-15:** data DO(7:0) (read mode). This is the data that is read from the device (MSb first).
- Multiple read command is also available in 3-wires mode.

## 6 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

**Table 15. Register address map**

| Name                     | Type | Register address |          | Default  | Comment        |
|--------------------------|------|------------------|----------|----------|----------------|
|                          |      | Hex              | Binary   |          |                |
| Reserved (do not modify) |      | 00 - 1F          |          |          | Reserved       |
| CTRL_REG1                | rw   | 20               | 010 0000 | 00000111 |                |
| CTRL_REG2                | rw   | 21               | 010 0001 | 00000000 |                |
| CTRL_REG3                | rw   | 22               | 010 0010 | 00000000 |                |
| CTRL_REG4                | rw   | 23               | 010 0011 | 00000000 |                |
| CTRL_REG5                | rw   | 24               | 010 0100 | 00000000 |                |
| HP_FILTER_RESET          | r    | 25               | 010 0101 |          | Dummy register |
| REFERENCE                | rw   | 26               | 010 0110 | 00000000 |                |
| STATUS_REG               | r    | 27               | 010 0111 | 00000000 |                |
| OUT_X_L                  | r    | 28               | 010 1000 | output   |                |
| OUT_X_H                  | r    | 29               | 010 1001 | output   |                |
| OUT_Y_L                  | r    | 2A               | 010 1010 | output   |                |
| OUT_Y_H                  | r    | 2B               | 010 1011 | output   |                |
| OUT_Z_L                  | r    | 2C               | 010 1100 | output   |                |
| OUT_Z_H                  | r    | 2D               | 010 1101 | output   |                |
| Reserved (do not modify) |      | 2E - 2F          |          |          | Reserved       |
| INT1_CFG                 | rw   | 30               | 011 0000 | 00000000 |                |
| INT1_SOURCE              | r    | 31               | 011 0001 | 00000000 |                |
| INT1_THS                 | rw   | 32               | 011 0010 | 00000000 |                |
| INT1_DURATION            | rw   | 33               | 011 0011 | 00000000 |                |
| INT2_CFG                 | rw   | 34               | 011 0100 | 00000000 |                |
| INT2_SOURCE              | r    | 35               | 011 0101 | 00000000 |                |
| INT2_THS                 | rw   | 36               | 011 0110 | 00000000 |                |
| INT2_DURATION            | rw   | 37               | 011 0111 | 00000000 |                |
| Reserved (do not modify) |      | 38 - 3F          |          |          | Reserved       |

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

## 7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

### 7.1 CTRL\_REG1 (20h)

**Table 16. CTRL\_REG1 register**

|     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|
| PM2 | PM1 | PM0 | DR1 | DR0 | Zen | Yen | Xen |
|-----|-----|-----|-----|-----|-----|-----|-----|

**Table 17. CTRL\_REG1 description**

|           |   |
|-----------|---|
| PM2 - PM0 | Power mode selection. Default value: 000<br>(000: Power-down; Others: refer to <a href="#">Table 18</a> ) |
| DR1, DR0  | Data rate selection. Default value: 00<br>(00:50 Hz; Others: refer to <a href="#">Table 19</a> )          |
| Zen       | Z axis enable. Default value: 1<br>(0: Z axis disabled; 1: Z axis enabled)                                |
| Yen       | Y axis enable. Default value: 1<br>(0: Y axis disabled; 1: Y axis enabled)                                |
| Xen       | X axis enable. Default value: 1<br>(0: X axis disabled; 1: X axis enabled)                                |

**PM** bits allow to select between power-down and two operating active modes. The device is in power-down mode when PD bits are set to “000” (default value after boot). [Table 18](#) shows all the possible power mode configurations and respective output data rates. Output data in the low-power modes are computed with low-pass filter cut-off frequency defined by DR1, DR0 bits.

**DR** bits, in the normal-mode operation, select the data rate at which acceleration samples are produced. In low-power mode they define the output data resolution. [Table 19](#) shows all the possible configuration for DR1 and DR0 bits.

**Table 18. Power mode and low-power output data rate configurations**

| PM2 | PM1 | PM0 | Power mode selection | Output data rate [Hz]<br>ODR <sub>LP</sub> |
|-----|-----|-----|----------------------|--|
| 0   | 0   | 0   | Power-down           | --   |
| 0   | 0   | 1   | Normal mode          | ODR  |
| 0   | 1   | 0   | Low-power            | 0.5  |
| 0   | 1   | 1   | Low-power            | 1  |
| 1   | 0   | 0   | Low-power            | 2  |



**Table 18. Power mode and low-power output data rate configurations (continued)**

| PM2 | PM1 | PM0 | Power mode selection | Output data rate [Hz]<br>ODR <sub>LP</sub> |
|-----|-----|-----|----------------------|--|
| 1   | 0   | 1   | Low-power            | 5  |
| 1   | 1   | 0   | Low-power            | 10   |

**Table 19. Normal-mode output data rate configurations and low-pass cut-off frequencies**

| DR1 | DR0 | Output Data Rate [Hz]<br>ODR | Low-pass filter cut-off<br>frequency [Hz] |
|-----|-----|------------------------------|---|
| 0   | 0   | 50                           | 37  |
| 0   | 1   | 100                          | 74  |
| 1   | 0   | 400                          | 292                                       |
| 1   | 1   | 1000                         | 780                                       |

## 7.2 CTRL\_REG2 (21h)

**Table 20. CTRL\_REG2 register**

| BOOT | HPM1 | HPM0 | FDS | HPen2 | HPen1 | HPCF1 | HPCF0 |
|------|------|------|-----|-------|-------|-------|-------|
|------|------|------|-----|-------|-------|-------|-------|

**Table 21. CTRL\_REG2 description**

|              |  |
|--------------|--|
| BOOT         | Reboot memory content. Default value: 0<br>(0: normal mode; 1: reboot memory content)  |
| HPM1, HPM0   | High pass filter mode selection. Default value: 00<br>(00: normal mode; Others: refer to <a href="#">Table 22</a> )              |
| FDS          | Filtered data selection. Default value: 0<br>(0: internal filter bypassed; 1: data from internal filter sent to output register) |
| HPen2        | High pass filter enabled for interrupt 2 source. Default value: 0<br>(0: filter bypassed; 1: filter enabled)                     |
| HPen1        | High pass filter enabled for interrupt 1 source. Default value: 0<br>(0: filter bypassed; 1: filter enabled)                     |
| HPCF1, HPCF0 | High pass filter cut-off frequency configuration. Default value: 00<br>(00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64)           |

**BOOT** bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself. If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When **BOOT** bit is set to '1' the content of internal flash is copied

inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

**Table 22. High-pass filter mode configuration**

| HPM1 | HPM0 | High-pass filter mode                       |
|------|------|---|
| 0    | 0    | Normal mode (reset reading HP_RESET_FILTER) |
| 0    | 1    | Reference signal for filtering              |
| 1    | 0    | Normal mode (reset reading HP_RESET_FILTER) |

**HPCF[1:0]**. These bits are used to configure high-pass filter cut-off frequency  $f_t$  which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPC}\right) \cdot \frac{f_s}{2\pi}$$

The equation can be simplified to the following approximated equation:

$$f_t = \frac{f_s}{6 \cdot HPC}$$

**Table 23. High-pass filter cut-off frequency configuration**

| HPcoeff2,1 | $f_t$ [Hz]<br>Data rate = 50 Hz | $f_t$ [Hz]<br>Data rate = 100 Hz | $f_t$ [Hz]<br>Data rate = 400 Hz | $f_t$ [Hz]<br>Data rate = 1000 Hz |
|------------|---------------------------------|----------------------------------|----------------------------------|-----------------------------------|
| 00         | 1                               | 2                                | 8                                | 20                                |
| 01         | 0.5                             | 1                                | 4                                | 10                                |
| 10         | 0.25                            | 0.5                              | 2                                | 5                                 |
| 11         | 0.125                           | 0.25                             | 1                                | 2.5                               |

### 7.3 CTRL\_REG3 [Interrupt CTRL register] (22h)

**Table 24. CTRL\_REG3 register**

|     |       |      |         |         |      |         |         |
|-----|-------|------|---------|---------|------|---------|---------|
| IHL | PP_OD | LIR2 | I2_CFG1 | I2_CFG0 | LIR1 | I1_CFG1 | I1_CFG0 |
|-----|-------|------|---------|---------|------|---------|---------|

**Table 25. CTRL\_REG3 description**

|       |  |
|-------|--|
| IHL   | Interrupt active high, low. Default value: 0<br>(0: active high; 1: active low)                    |
| PP_OD | Push-pull/Open drain selection on interrupt pad. Default value 0.<br>(0: push-pull; 1: open drain) |

**Table 25. CTRL\_REG3 description (continued)**

|                     |  |
|---------------------|--|
| LIR2                | Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched)   |
| I2_CFG1,<br>I2_CFG0 | Data signal on INT 2 pad control bits. Default value: 00.<br>(see table below)   |
| LIR1                | Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC register. Default value: 0.<br>(0: interrupt request not latched; 1: interrupt request latched) |
| I1_CFG1,<br>I1_CFG0 | Data signal on INT 1 pad control bits. Default value: 00.<br>(see table below)   |

**Table 26. Data signal on INT 1 and INT 2 pad**

| I1(2)_CFG1 | I1(2)_CFG0 | INT 1(2) Pad                             |
|------------|------------|--|
| 0          | 0          | Interrupt 1 (2) source                   |
| 0          | 1          | Interrupt 1 source OR interrupt 2 source |
| 1          | 0          | Data ready                               |
| 1          | 1          | Boot running                             |

## 7.4 CTRL\_REG4 (23h)

**Table 27. CTRL\_REG4 register**

|     |     |     |     |        |   |    |     |
|-----|-----|-----|-----|--------|---|----|-----|
| BDU | BLE | FS1 | FS0 | STsign | 0 | ST | SIM |
|-----|-----|-----|-----|--------|---|----|-----|

**Table 28. CTRL\_REG4 description**

|          |  |
|----------|--|
| BDU      | Block data update. Default value: 0<br>(0: continuous update; 1: output registers not updated between MSB and LSB reading) |
| BLE      | Big/little endian data selection. Default value 0.<br>(0: data LSB @ lower address; 1: data MSB @ lower address)           |
| FS1, FS0 | Full-scale selection. Default value: 00.<br>(00: $\pm 6 g$ ; 01: $\pm 12 g$ ; 11: $\pm 24 g$ )                             |
| STsign   | Self-test sign. Default value: 00.<br>(0: self-test plus; 1 self-test minus)   |
| ST       | Self-test enable. Default value: 0.<br>(0: self-test disabled; 1: self-test enabled)                                       |
| SIM      | SPI serial interface mode selection. Default value: 0.<br>(0: 4-wire interface; 1: 3-wire interface)                       |

**BDU** bit is used to inhibit output registers update between the reading of upper and lower register parts. In default mode (BDU = '0') the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too. This feature avoids reading LSB and MSB related to different samples.

## 7.5 CTRL\_REG5 (24h)

**Table 29. CTRL\_REG5 register**

|   |   |   |   |   |   |         |         |
|---|---|---|---|---|---|---------|---------|
| 0 | 0 | 0 | 0 | 0 | 0 | TurnOn1 | TurnOn0 |
|---|---|---|---|---|---|---------|---------|

**Table 30. CTRL\_REG5 description**

|                     |   |
|---------------------|---|
| TurnOn1,<br>TurnOn0 | Turn-on mode selection for sleep to wake function. Default value: 00. |
|---------------------|---|

**TurnOn** bits are used for turning on the **sleep to wake** function.

**Table 31. Sleep to wake configuration**

| TurnOn1 | TurnOn0 | Sleep to wake status   |
|---------|---------|--|
| 0       | 0       | Sleep to wake function is disabled                                       |
| 1       | 1       | Turned on: The device is in low power mode (ODR is defined in CTRL_REG1) |

Setting TurnOn[1:0] bits to 11 the “sleep to wake” function is enabled. When an interrupt event occurs the device is turned to normal mode increasing the ODR to the value defined in CTRL\_REG1. Although the device is in normal mode, CTRL\_REG1 content is not automatically changed to “normal mode” configuration.

## 7.6 HP\_FILTER\_RESET (25h)

Dummy register. Reading at this address zeroes instantaneously the content of the internal high pass-filter. If the high pass filter is enabled all three axes are instantaneously set to 0g. This allows to overcome the settling time of the high pass filter.

## 7.7 REFERENCE (26h)

**Table 32. REFERENCE register**

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| Ref7 | Ref6 | Ref5 | Ref4 | Ref3 | Ref2 | Ref1 | Ref0 |
|------|------|------|------|------|------|------|------|

**Table 33. REFERENCE description**

|             |   |
|-------------|---|
| Ref7 - Ref0 | Reference value for high-pass filter. Default value: 00h. |
|-------------|---|

This register sets the acceleration value taken as a reference for the high-pass filter output. When filter is turned on (at least one of FDS, HPen2, or HPen1 bit is equal to '1') and HPM bits are set to "01", filter out is generated taking this value as a reference.

## 7.8 STATUS\_REG (27h)

**Table 34. STATUS\_REG register**

|       |     |     |     |       |     |     |     |
|-------|-----|-----|-----|-------|-----|-----|-----|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |
|-------|-----|-----|-----|-------|-----|-----|-----|

**Table 35. STATUS\_REG description**

|       |  |
|-------|--|
| ZYXOR | X, Y and Z axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: new data has overwritten the previous one before it was read) |
| ZOR   | Z axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the Z-axis has overwritten the previous one)            |
| YOR   | Y axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the Y-axis has overwritten the previous one)            |
| XOR   | X axis data overrun. Default value: 0<br>(0: no overrun has occurred;<br>1: a new data for the X-axis has overwritten the previous one)            |
| ZYXDA | X, Y and Z axis new data available. Default value: 0<br>(0: a new set of data is not yet available; 1: a new set of data is available)             |
| ZDA   | Z axis new data available. Default value: 0<br>(0: a new data for the Z-axis is not yet available;<br>1: a new data for the Z-axis is available)   |
| YDA   | Y axis new data available. Default value: 0<br>(0: a new data for the Y-axis is not yet available;<br>1: a new data for the Y-axis is available)   |
| XDA   | X axis new data available. Default value: 0<br>(0: a new data for the X-axis is not yet available;<br>1: a new data for the X-axis is available)   |

## 7.9 OUT\_X\_L (28h), OUT\_X\_H (29)

X-axis acceleration data. The value is expressed as two's complement.

**7.10 OUT\_Y\_L (2Ah), OUT\_Y\_H (2Bh)**

Y-axis acceleration data. The value is expressed as two's complement.

**7.11 OUT\_Z\_L (2Ch), OUT\_Z\_H (2Dh)**

Z-axis acceleration data. The value is expressed as two's complement.

**7.12 INT1\_CFG (30h)****Table 36. INT1\_CFG register**

|     |    |      |      |      |      |      |      |
|-----|----|------|------|------|------|------|------|
| AOI | 6D | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |
|-----|----|------|------|------|------|------|------|

**Table 37. INT1\_CFG description**

|      |   |
|------|---|
| AOI  | AND/OR combination of Interrupt events. Default value: 0.<br>(See <a href="#">Table 38</a> )  |
| 6D   | 6 direction detection function enable. Default value: 0.<br>(See <a href="#">Table 38</a> )   |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)   |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)   |
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)   |

Configuration register for Interrupt 1 source.

**Table 38. Interrupt 1 source configurations**

| AOI | 6D | Interrupt mode                      |
|-----|----|-------------------------------------|
| 0   | 0  | OR combination of interrupt events  |
| 0   | 1  | 6 direction movement recognition    |
| 1   | 0  | AND combination of interrupt events |
| 1   | 1  | 6 direction position recognition    |

## 7.13 INT1\_SRC (31h)

**Table 39. INT1\_SRC register**

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |
|---|----|----|----|----|----|----|----|

**Table 40. INT1\_SRC description**

|    |   |
|----|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z High event has occurred)   |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z Low event has occurred)   |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y High event has occurred)   |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y Low event has occurred)   |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X High event has occurred)   |
| XL | X low. Default value: 0<br>(0: no interrupt, 1: X Low event has occurred)   |

Interrupt 1 source register. Read only register.

Reading at this address clears INT1\_SRC IA bit (and the interrupt signal on INT 1 pin) and allows the refreshment of data in the INT1\_SRC register if the latched option was chosen.

## 7.14 INT1\_THS (32h)

**Table 41. INT1\_THS register**

|   |      |      |      |      |      |      |      |
|---|------|------|------|------|------|------|------|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |
|---|------|------|------|------|------|------|------|

**Table 42. INT1\_THS description**

|             |  |
|-------------|--|
| THS6 - THS0 | Interrupt 1 threshold. Default value: 000 0000 |
|-------------|--|

## 7.15 INT1\_DURATION (33h)

**Table 43. INT1\_DURATION register**

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|----|----|----|----|----|----|----|

**Table 44. INT2\_DURATION description**

|         |   |
|---------|---|
| D6 - D0 | Duration value. Default value: 000 0000 |
|---------|---|

**D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

## 7.16 INT2\_CFG (34h)

**Table 45. INT2\_CFG register**

|     |    |      |      |      |      |      |      |
|-----|----|------|------|------|------|------|------|
| AOI | 6D | ZHIE | ZLIE | YHIE | YLIE | XHIE | XLIE |
|-----|----|------|------|------|------|------|------|

**Table 46. INT2\_CFG description**

|      |   |
|------|---|
| AOI  | AND/OR combination of interrupt events. Default value: 0.<br>(See table below)  |
| 6D   | 6 direction detection function enable. Default value: 0.<br>(See table below)   |
| ZHIE | Enable interrupt generation on Z high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| ZLIE | Enable interrupt generation on Z low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)   |
| YHIE | Enable interrupt generation on Y high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| YLIE | Enable interrupt generation on Y low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)   |



**Table 46. INT2\_CFG description**

|      |   |
|------|---|
| XHIE | Enable interrupt generation on X high event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value higher than preset threshold) |
| XLIE | Enable interrupt generation on X low event. Default value: 0<br>(0: disable interrupt request;<br>1: enable interrupt request on measured accel. value lower than preset threshold)   |

Configuration register for Interrupt 2 source.

**Table 47. Interrupt mode configuration**

| AOI | 6D | Interrupt mode                      |
|-----|----|-------------------------------------|
| 0   | 0  | OR combination of interrupt events  |
| 0   | 1  | 6 direction movement recognition    |
| 1   | 0  | AND combination of interrupt events |
| 1   | 1  | 6 direction position recognition    |

## 7.17 INT2\_SRC (35h)

**Table 48. INT2\_SRC register**

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| 0 | IA | ZH | ZL | YH | YL | XH | XL |
|---|----|----|----|----|----|----|----|

**Table 49. INT2\_SRC description**

|    |   |
|----|---|
| IA | Interrupt active. Default value: 0<br>(0: no interrupt has been generated; 1: one or more interrupts have been generated) |
| ZH | Z high. Default value: 0<br>(0: no interrupt, 1: Z high event has occurred)   |
| ZL | Z low. Default value: 0<br>(0: no interrupt; 1: Z low event has occurred)   |
| YH | Y high. Default value: 0<br>(0: no interrupt, 1: Y high event has occurred)   |
| YL | Y low. Default value: 0<br>(0: no interrupt, 1: Y low event has occurred)   |
| XH | X high. Default value: 0<br>(0: no interrupt, 1: X high event has occurred)   |
| XL | X Low. Default value: 0<br>(0: no interrupt, 1: X low event has occurred)   |

Interrupt 2 source register. Read only register.

Reading at this address clears INT2\_SRC IA bit (and the interrupt signal on INT 2 pin) and allows the refreshment of data in the INT2\_SRC register if the latched option was chosen.

## 7.18 INT2\_THS (36h)

**Table 50. INT2\_THS register**

|   |      |      |      |      |      |      |      |
|---|------|------|------|------|------|------|------|
| 0 | THS6 | THS5 | THS4 | THS3 | THS2 | THS1 | THS0 |
|---|------|------|------|------|------|------|------|

**Table 51. INT2\_THS description**

|             |  |
|-------------|--|
| THS6 - THS0 | Interrupt 1 threshold. Default value: 000 0000 |
|-------------|--|

## 7.19 INT2\_DURATION (37h)

**Table 52. INT2\_DURATION register**

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| 0 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|----|----|----|----|----|----|----|

**Table 53. INT2\_DURATION description**

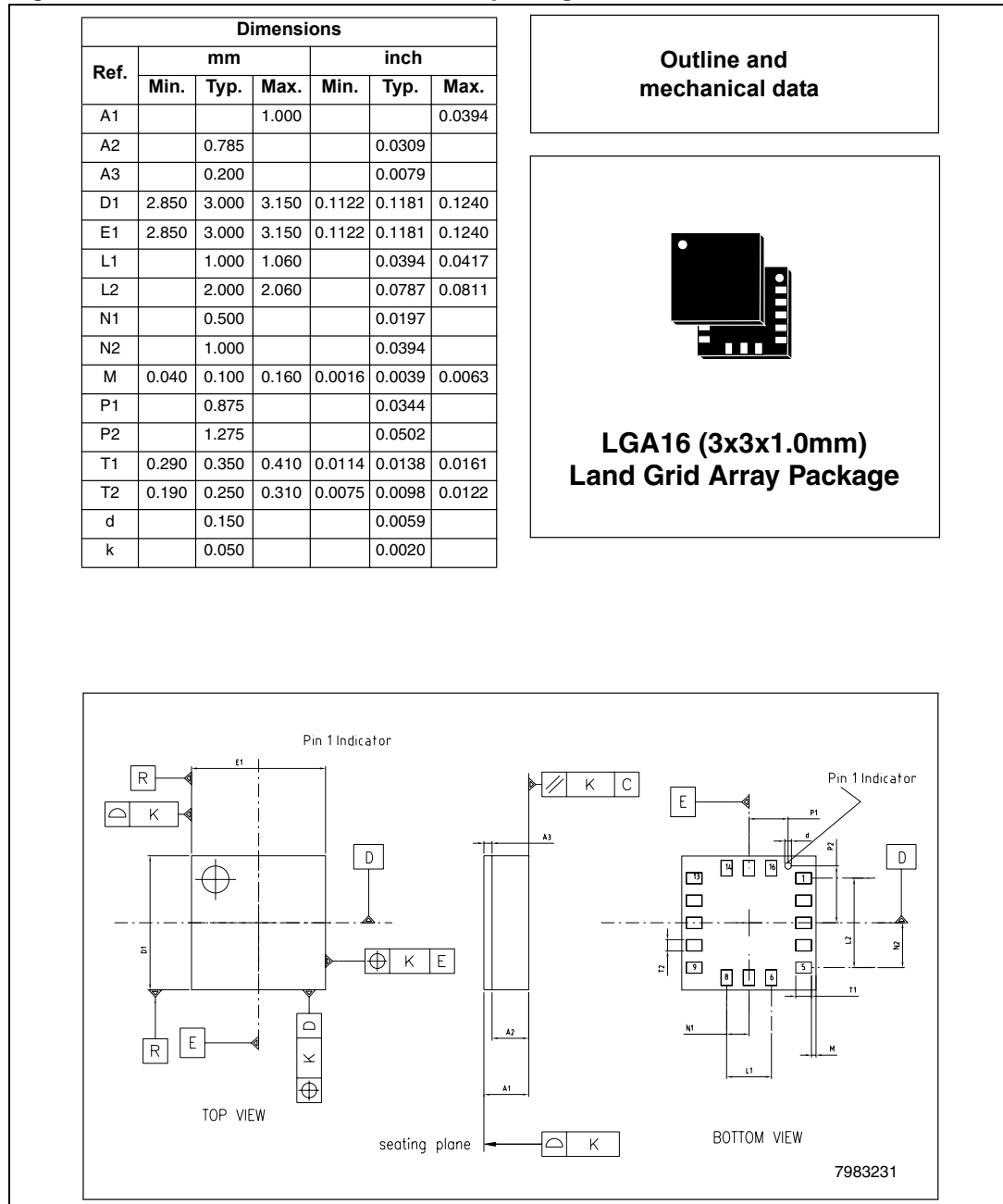
|         |   |
|---------|---|
| D6 - D0 | Duration value. Default value: 000 0000 |
|---------|---|

**D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

# 8 Package information

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**Figure 12. LGA16: Mechanical data and package dimensions**



## 9 Revision history

**Table 54. Document revision history**

| Date        | Revision | Changes         |
|-------------|----------|-----------------|
| 05-Oct-2009 | 1        | Initial release |

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