

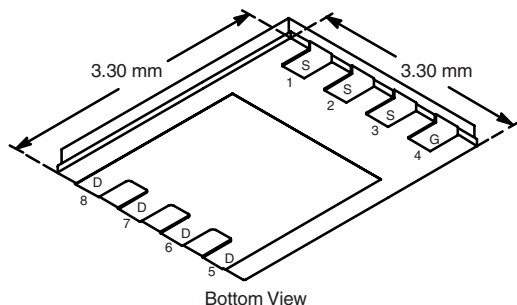


P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)
- 30	0.021 at V _{GS} = - 10 V	- 24 ^e	15 nC
	0.034 at V _{GS} = - 4.5 V	- 18.7	

PowerPAK® 1212-8



Ordering Information: Si7619DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

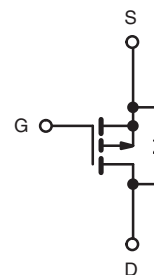
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC


RoHS
 COMPLIANT
 HALOGEN
FREE

APPLICATIONS

- Notebook PC
- Load Switch
- Battery Switch
- Adaptor Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 30	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	A
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Pulsed Drain Current	I _{DM}	- 50	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	
Avalanche Current	I _{AS}	- 20	mJ
Single-Pulse Avalanche Energy	E _{AS}	20	
Maximum Power Dissipation	P _D	T _C = 25 °C	W
		T _C = 70 °C	
		T _A = 25 °C	
		T _A = 70 °C	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{f, g}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	R _{thJA}	29	36	°C/W
Maximum Junction-to-Case	R _{thJC}	3.6	4.5	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. Maximum under Steady State conditions is 81 °C/W.

d. Based on T_C = 25 °C.

e. Package Limited.

 f. See Solder Profile (www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

g. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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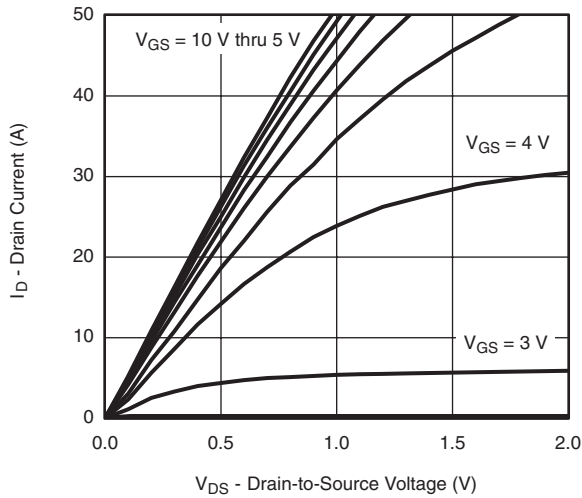
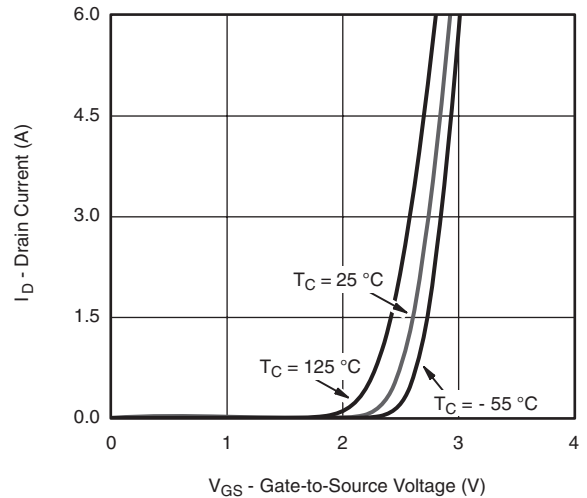
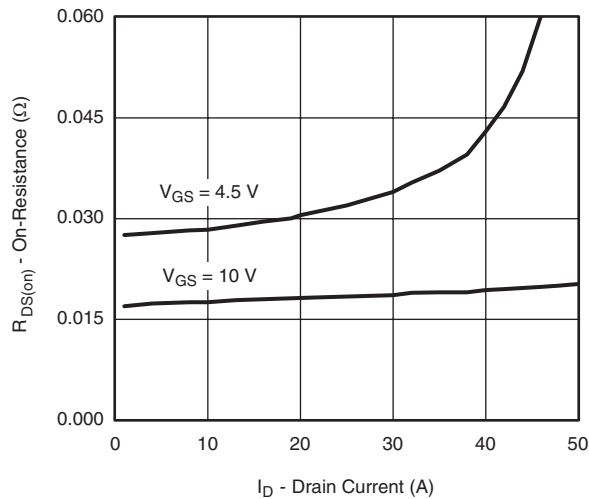
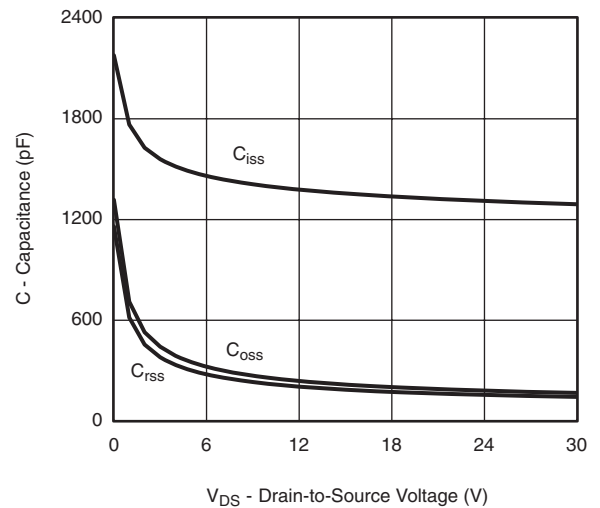
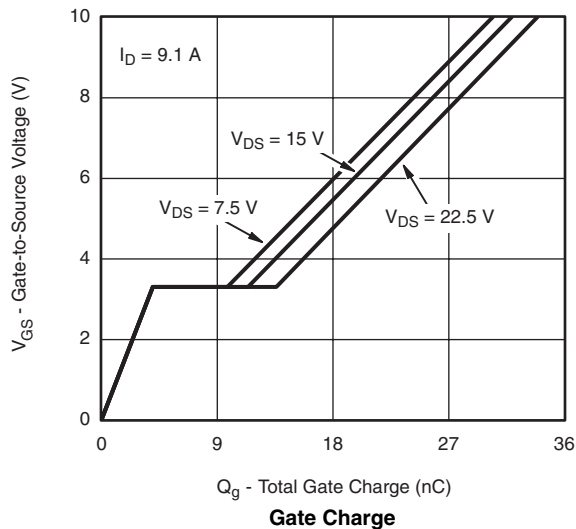
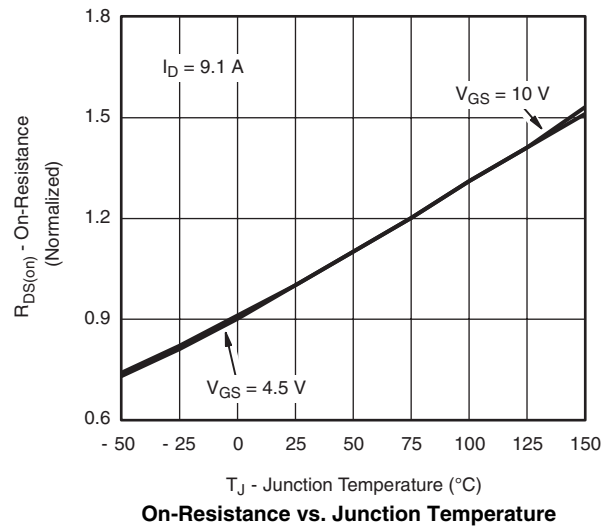
SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 31		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			4.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1.0		- 3.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 30 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 30 V, V _{GS} = 0 V, T _J = 55 °C			- 5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ - 10 V, V _{GS} = - 10 V	- 30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 10.5 A		0.0175	0.021	Ω
		V _{GS} = - 4.5 V, I _D = - 8.3 A		0.0283	0.034	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 10.5 A		23		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		1350		pF
Output Capacitance	C _{oss}			215		
Reverse Transfer Capacitance	C _{rss}			185		
Total Gate Charge	Q _g	V _{DS} = - 15 V, V _{GS} = - 10 V, I _D = - 10.5 A		32	50	nC
		V _{DS} = - 15 V, V _{GS} = - 4.5 V, I _D = - 10.5 A		15	25	
Q _{gs}			4			
Q _{gd}			7.5			
Gate Resistance	R _g	f = 1 MHz	1.2	5.8	11.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.8 Ω I _D ≡ - 8.4 A, V _{GEN} = - 10 V, R _g = 1 Ω		10	15	ns
Rise Time	t _r			8	15	
Turn-Off DelayTime	t _{d(off)}			45	70	
Fall Time	t _f			12	25	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 15 V, R _L = 1.8 Ω I _D ≡ - 8.4 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		42	70	
Rise Time	t _r			35	60	
Turn-Off DelayTime	t _{d(off)}			40	70	
Fall Time	t _f			16	30	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			- 23.2	A
Pulse Diode Forward Current	I _{SM}				- 50	
Body Diode Voltage	V _{SD}	I _S = - 8.4 A, V _{GS} = 0 V		- 0.85	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 8.4 A, dI/dt = 100 A/μs, T _J = 25 °C		34	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			22	40	nC
Reverse Recovery Fall Time	t _a			11		ns
Reverse Recovery Rise Time	t _b			23		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

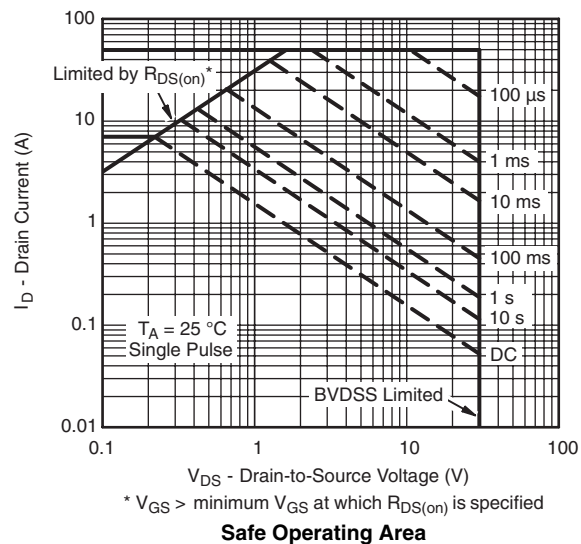
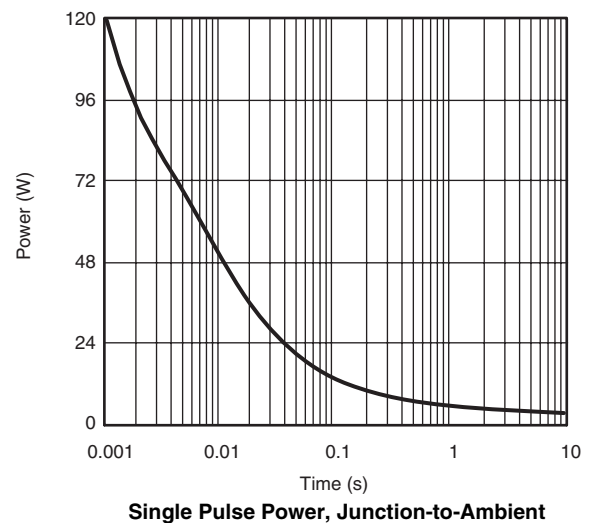
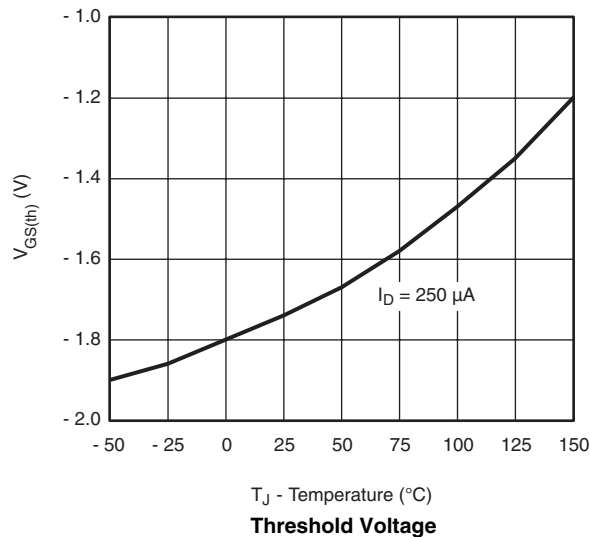
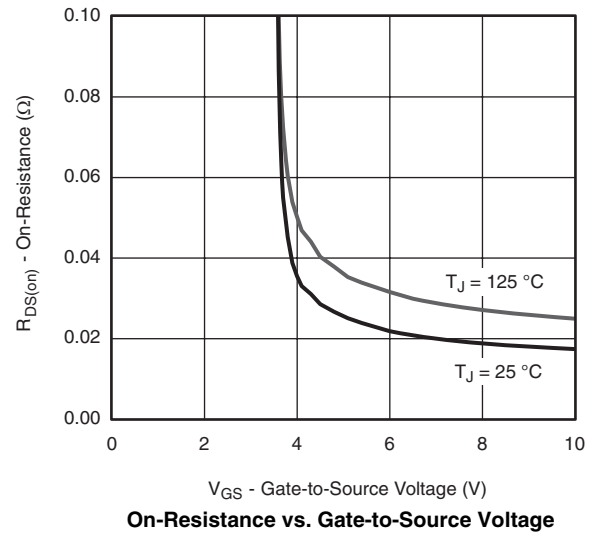
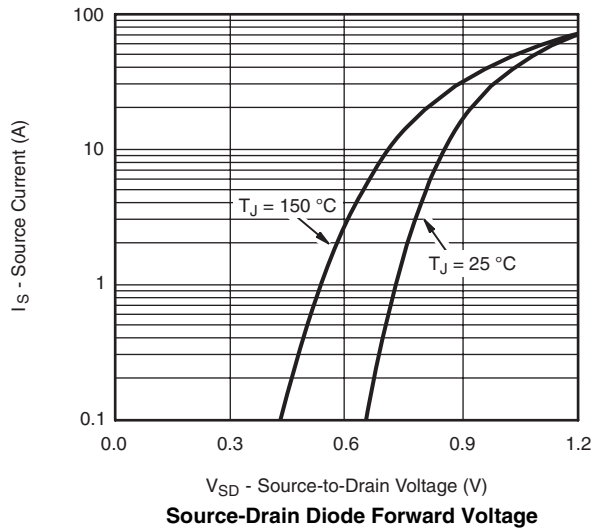
b. Guaranteed by design, not subject to production testing.

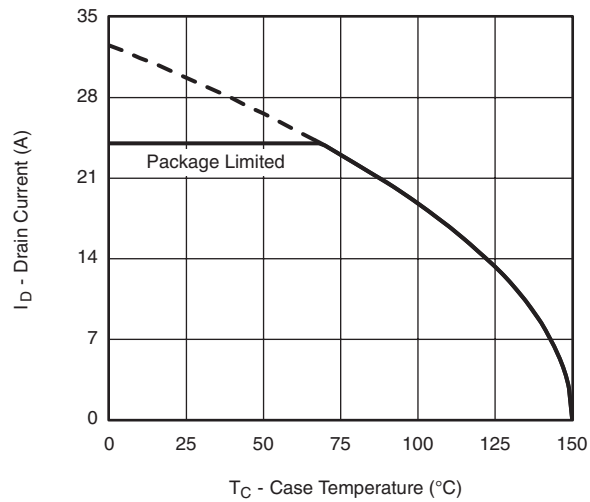
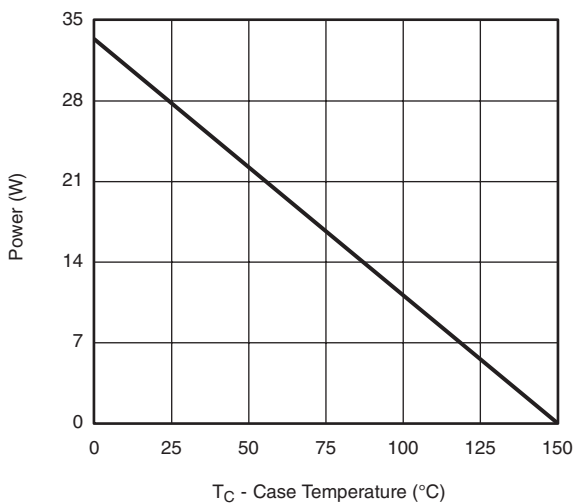
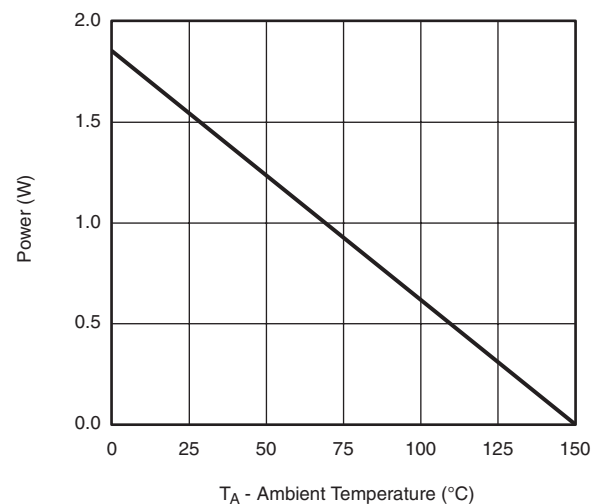
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

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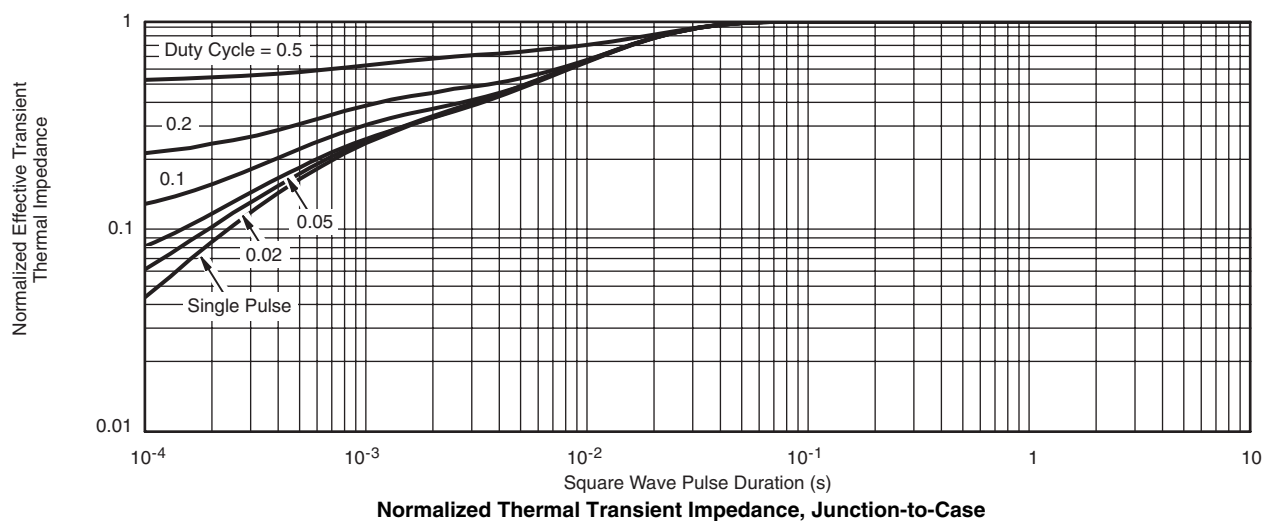
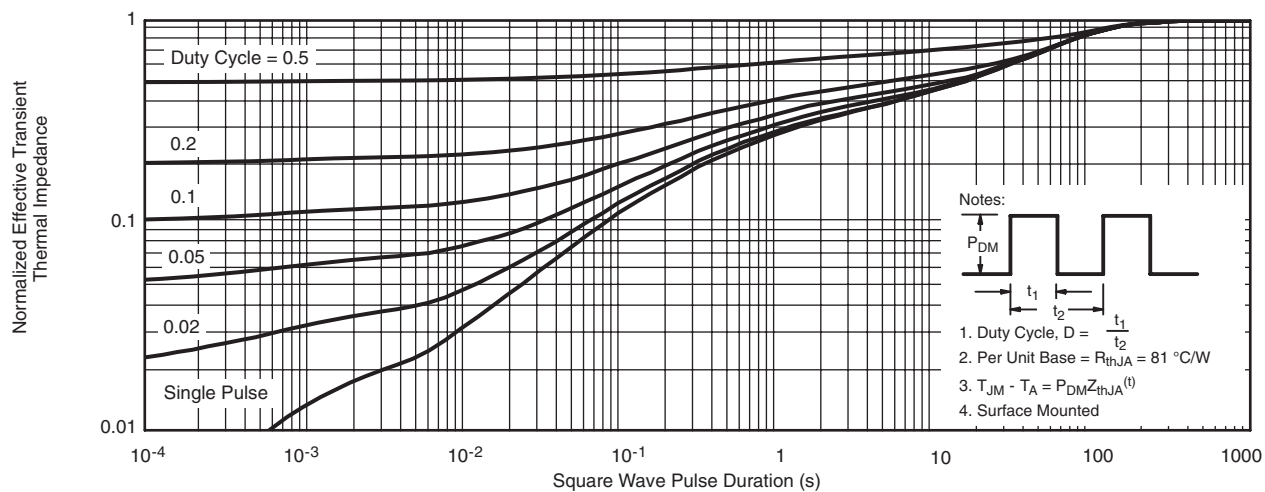
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Current Derating*

Power, Junction-to-Case

Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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