May 2014

FAN3240 / FAN3241
Smart Dual-Coil Relay Drivers

Features

- 8-V to 60-V Operation Range for use with 12-V, 24-V or 48-V Relays
- Strong DC Current to Break through Welded Contacts without using External Switches
- Integrated Linear Regulator for Isolated or Non-Isolated Meter Power Designs
- Accurate Input Filter Time and XOR input protection
- Accurate maximum output pulse width
- Two output operating modes – follows input width or maximum value
- 3.3-V or 5-V Square-Wave Logic Input Signals
- Enable Pin for Operational Flexibility
- Internal Thermal Shutdown Protection
- Rated from –40°C to +105°C Ambient

Applications

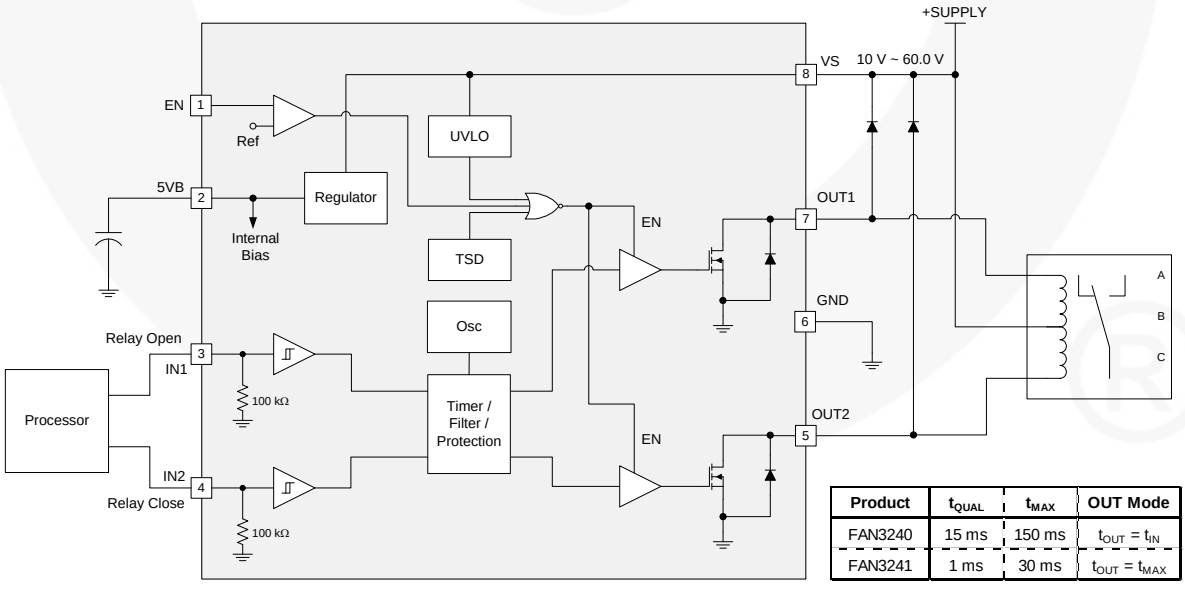
- Smart E-Meters, Energy Generation & Distribution, Building and Home Control, Industrial dual-coil relay Driving Applications

Description

The FAN324x family includes dual high-current relay drivers designed to drive dual-coil polarized latching relays that connect and disconnect power in smart electronic meters and solar inverter applications.

The output of the FAN324x is rated for operation with supply voltage range from 8 V to 60 V. The filter / timer block prevents inadvertent switching from noisy input signals by providing input-pulse qualification (t_{QUAL}) and maximum output pulse width limit (t_{MAX}). The output can operate in follow-input mode or maximum width mode. These parameters are factory adjustable and additional configurations are available. XOR input protection is also provided so that both outputs are prevented from being on at the same time. Under-Voltage Lockout (UVLO) function disables the outputs until the supply voltage is within the operating range.

The FAN324x has two separate driver channels with non-inverting logic. One enable / disable pin allows shutdown of both channels, independent of the input signals. Internal thermal shutdown function is provided for thermal protection. The FAN324x is available in an Lead (Pb)-Free 8-lead SOIC package.



Product	t_{QUAL}	t_{MAX}	OUT Mode
FAN3240	15 ms	150 ms	$t_{OUT} = t_{IN}$
FAN3241	1 ms	30 ms	$t_{OUT} = t_{MAX}$

Figure 1. Typical Application Diagram

Ordering Information

Part Number	Minimum Input Time	Maximum Pulse Width	Package	Packing Method	Reel Quantity
FAN3240TMX	15 ms	150 ms	SOIC-8	Tape & Reel	2,500
FAN3241TMX	1 ms	30 ms	SOIC-8	Tape & Reel	2,500

All standard Fairchild Semiconductor products are RoHS compliant and many are also “GREEN” or going green. *For Fairchild’s definition of “green” please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*

Package Outline

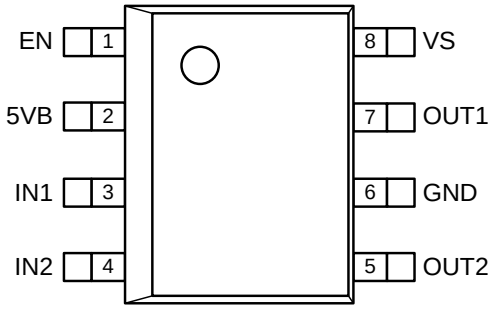


Figure 2. SOIC-8 (Top View)

Thermal Characteristics(1)

Package	Θ_{JL}(2)	Θ_{JT}(3)	Θ_{JA}(4)	Ψ_{JB}(5)	Ψ_{JT}(6)	Unit
8-Pin, Small-Outline Integrated Circuit (SOIC)	40	31	89	43	3.0	°C/W

Notes:

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the MLP-8 package, the board reference is defined as the PCB copper connected to the thermal pad and protruding from either end of the package. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

Block Diagram

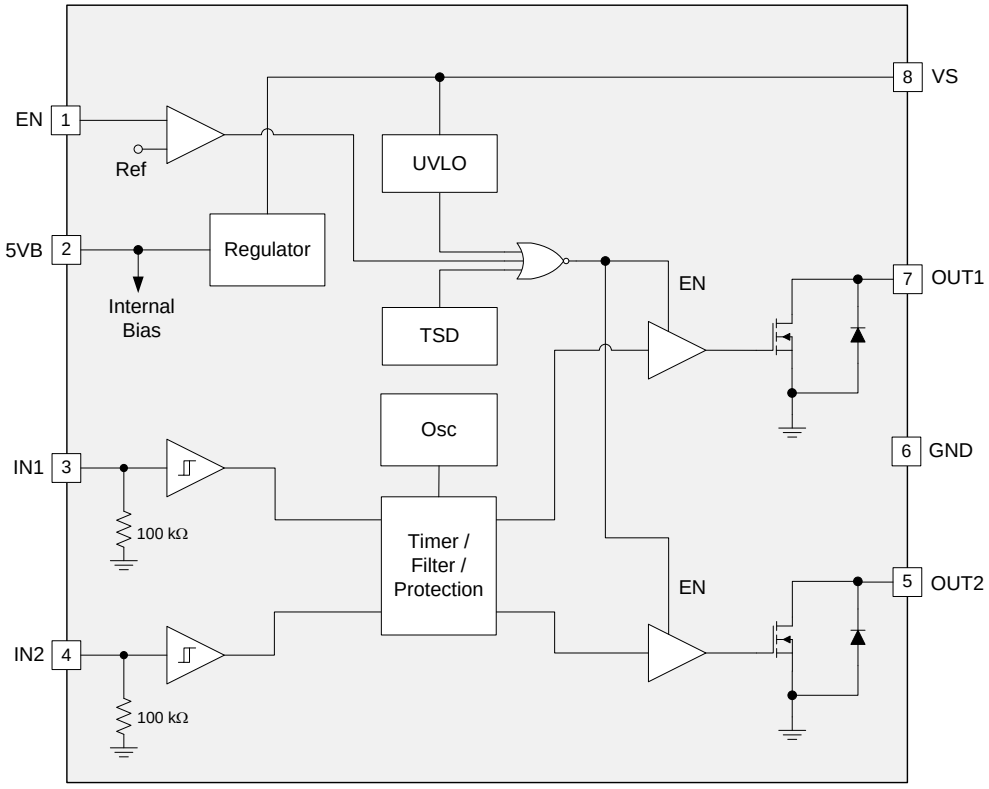


Figure 3. Block Diagram

Pin Definitions

Pin	Name	Pin Description
1	EN	**Enable input for both channels**. Pull pin LOW to inhibit operation of the drivers. This input has a precision threshold and comparator input stage.
2	5VB	**5 V bypass** pin for the internal 5 V regulator that provides power to the IC control circuitry.
3	IN1	**Input to driver Channel 1**. This input has TTL thresholds.
4	IN2	**Input to driver Channel 2**. This input has TTL thresholds.
5	OUT2	**Relay drive output 2**: Open-drain output. HIGH impedance unless required active input(s) are present and V_S is above UVLO threshold.
6	GND	**Ground**. Common ground reference for input and output circuits.
7	OUT1	**Relay drive output 1**: Open-drain output. HIGH impedance unless required active input(s) are present and V_S is above UVLO threshold.
8	VS	**Supply voltage**. Provides power to the device. Usually connected to the bias voltage of the relay being driven by the device.

Configurations

The FAN324x products are set at the factory with the following configurations.

	t_{QUAL}	t_{MAX}	OUT Mode
FAN3240	15 ms	150 ms	$t_{OUT} = t_{IN}$
FAN3241	1 ms	30 ms	$t_{OUT} = t_{MAX}$

Contact your Fairchild sales representatives for additional configurations. The parameter t_{QUAL} can be configured between 128 µs and 20 ms and t_{MAX} can be programmed between 1 ms and 350 ms.

where:

t_{QUAL}: Qualification Time. The minimum input pulse width duration recognized as a valid input command.

t_{MAX}: Maximum Output Pulse Width. Output pulses are terminated after this time interval even if the input pulse is longer or held in a HIGH state continuously.

OUT Mode: Output Mode. TheFAN324x offers two fundamentally different output pulse generation methods:

$t_{OUT} = t_{IN} < t_{MAX}$. In this mode, the output pulse duration (t_{OUT}) replicates the length of the input pulse (t_{IN}) up to $t_{MAX.}$

$t_{OUT} = t_{MAX}$. The output is on for a fixed time interval of t_{MAX}, regardless of the input pulse width.

The mode of operation has no impact on the qualification requirements or on the maximum output pulse width limiting. In both output operating modes, the qualification requirement must be met ($t_{IN} > t_{QUAL}$) to produce an output pulse.

Output Logic(7)

EN	IN1	IN2	OUT1	OUT2
0	0	0	H	H
0	0	1	H	H
0	1	0	H	H
0	1	1	H	H
1	0	0	H	H
1	0	1	H	L
1	1	0	L	H
1	1	1	H	H

Note:

7. Inputs and EN are defined as logic signals (positive logic; 1 is active), outputs are defined as HIGH or LOW impedance due to the open-drain output structures. Low output impedance is needed to energize the relay coil.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_S	VS to GND	-0.3	70.0	V
V_{5VB}	5VB to GND	-0.3	6.0	V
V_{EN}	EN to GND	GND - 0.3	6.0	V
V_{IN}	IN1 and IN2 to GND	GND - 0.3	6.0	V
V_{OUT}	OUT1 and OUT2 to GND	GND - 0.3	V_S + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	ºC
T_J	Junction Temperature	-55	+125	ºC
T_{STG}	Storage Temperature	-65	+150	ºC

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Output Supply Voltage Range	8		60	V
V_{EN}	Enable Voltage EN	0	3.3 to 5.0	5.5	V
V_{IN}	Input Voltage IN1, IN2	0	3.3 to 5.0	5.5	V
C_{VS}	Bypass Capacitor at VS Pin		1		µF
C_{5VB}	Bypass Capacitor at 5VB Pin	100	220		nF
T_A	Operating Ambient Temperature	-40		+105	ºC

Electrical Characteristics

Unless otherwise noted, V_S = 40 V, C_{5VB} = 0.22 µF, and T_J = -40°C to +105°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply (VS)						
I_{STDBY}	Standby Current	INx = 0 V, EN = 0 V		350	550	µA
I_{SUPPLY}	Operating Current	IN1 or IN2 = 5 V, EN = 5 V		400	600	µA
V_{ON}	Turn-On Voltage	IN1 = IN2 = EN = 5 V	6.9	7.9	8.9	V
V_{OFF}	Turn-Off Voltage	IN1 = IN2 = EN = 5 V	5.7	6.7	7.7	V
V_{HYS}	Turn-On Hysteresis		0.5	1.2		V
Inputs (IN1, IN2)(9)						
V_{INL}	INx Logic Low Threshold		0.8	1.1		V
V_{INH}	INx Logic High Threshold			1.6	2.0	V
V_{IN_HYS}	INx Logic Input Hysteresis			0.5		V
I_{IN}	Input Current	INx = 5 V		55	80	µA
t_{QUAL}	Valid Input Qualification Time(11)	FAN3240	13.5	15.0	16.5	ms
		FAN3241	0.9	1.0	1.1	ms
ENABLE (EN)						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	1.25	1.30	1.35	V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V	1.35	1.40	1.45	V
V_{HYS_T}	Enable Logic Input Hysteresis			0.1		V
t_{DEL}	EN to Output Propagation Delay(11)	EN from 5 V to 0 V, Logic Signal		5	9	µs
Internal Regulator (5VB)						
V_{5VB}	5VB Output Voltage	T_A = 25°C	4.9	5.0	5.1	V
		Total Variation Over Line (1 0V to 60 V), Load (0 mA to 5 mA), and Temperature(10)	4.8		5.2	V
		Line Regulation, 10 V to 60 V	-1%		1%	
		Load Regulation, 0 mA to 5 mA	-2%		2%	
I_{OUT}	Output Current		5.0			mA
Protection						
TSD	Thermal Shutdown Threshold(10)			150		°C
TSD_{HYS}	Thermal Shutdown Threshold Hysteresis(10)			25		°C

Continued on the following page…

Electrical Characteristics (Continued)

Unless otherwise noted, V_S = 40 V, C_{5VB} = 0.22 µF, and T_J = -40°C to +105°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Outputs (OUT1, OUT2)						
$R_{DS(ON)}$	On Resistance (OUT1, OUT2)	I_{SINK} = 500 mA, –40°C[10]	0.4	0.7	1.0	Ω
		I_{SINK} = 500 mA, 25°C[10]	0.7	1.0	1.3	
		I_{SINK} = 500 mA, 105°C[10]	1.2	1.6	2.0	
t_{RISE}	Output Rise Time[10,11]	$R_{PULL-UP}$ = 36 kΩ		7		µs
I_{MAX}	Maximum Current Driving Capability	t_{MAX} = 30 ms, 25°C	1.5			A
t_{FALL}	Output Fall Time[10,11]	$R_{PULL-UP}$ = 36 kΩ		7	20	ns
t_{MAX}	Maximum Pulse Width	FAN3240	135	150	165	ms
		FAN3241	27	30	33	
I_{RVS}	Output Reverse Current Withstand[10]			500		mA

Notes:

8. Lower supply current due to inactive TTL circuitry.
9. EN inputs have TTL thresholds; *refer to the ENABLE section.*
10. Not tested in production.
11. *See Timing Diagram of Figure 4.*

Timing Diagrams

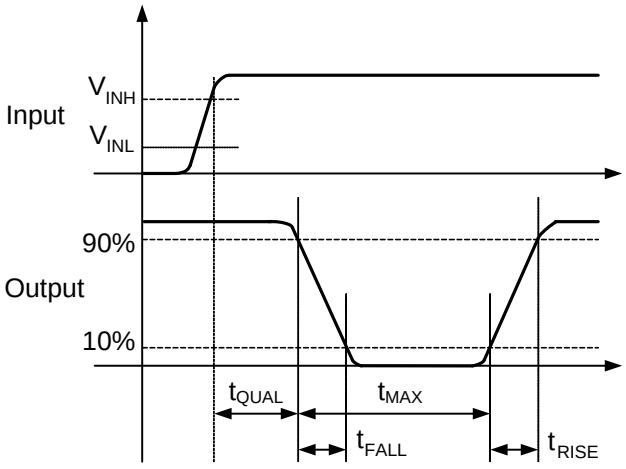


Figure 4. Timing (with EN HIGH)

Typical Performance Characteristics

Typical characteristics are provided at T_A = 25°C and V_S = 40 V unless otherwise noted.

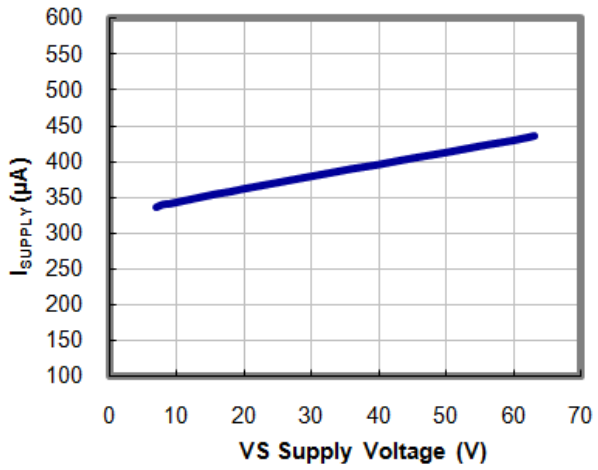


Figure 5. Supply Current vs. Supply Voltage

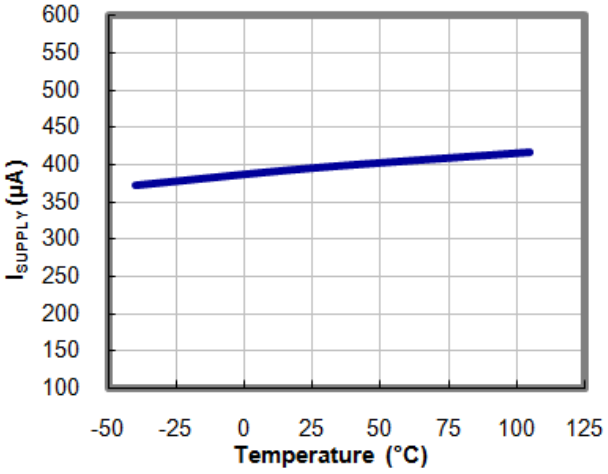


Figure 6. Supply Current vs. Temperature

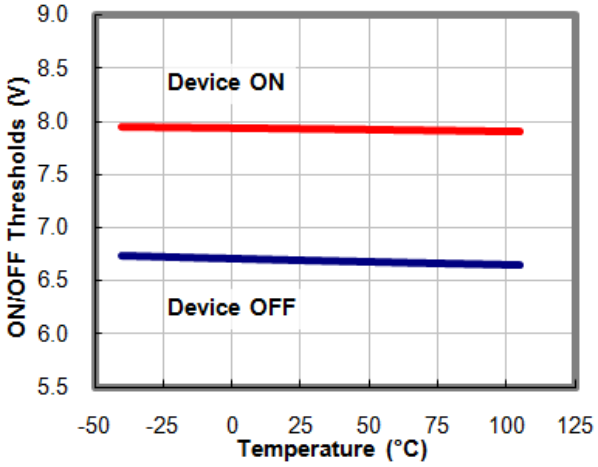


Figure 7. ON / OFF Thresholds vs. Temperature

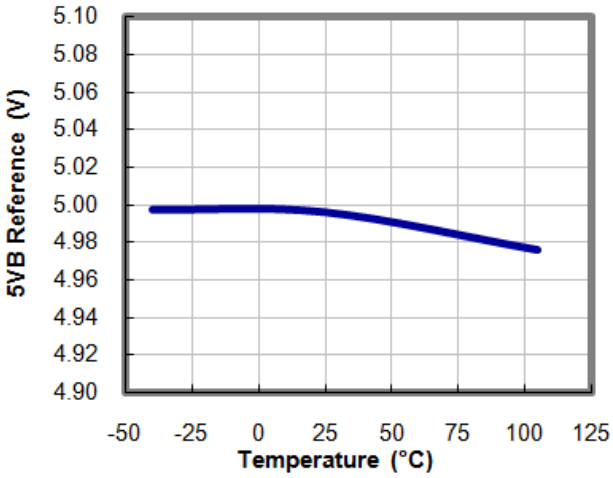


Figure 8. 5VB Reference vs. Temperature

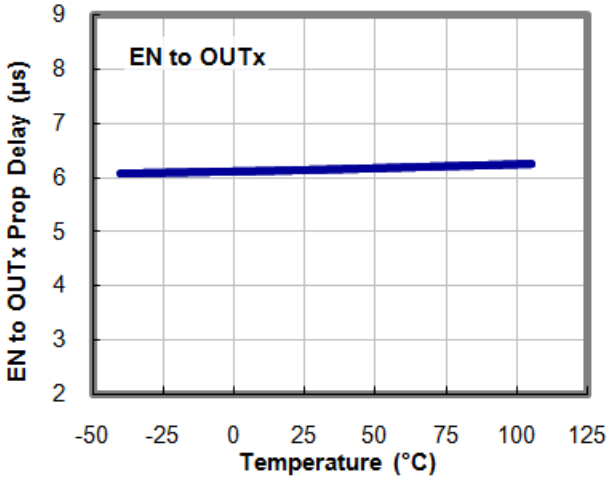


Figure 9. EN to OUTx Delay vs. Temperature

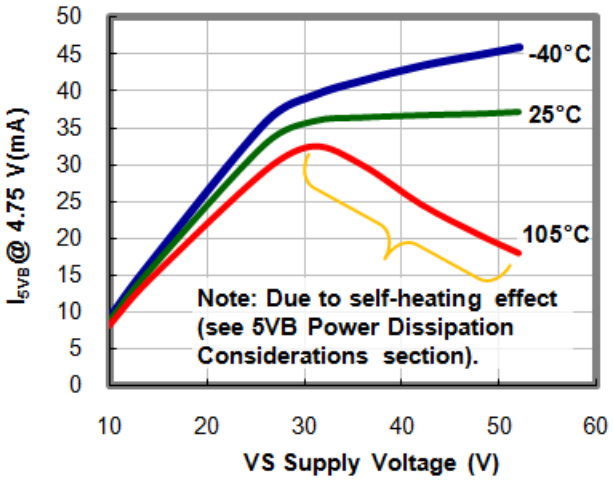


Figure 10. 5VB Current Capability at 4.75 V Output vs. Supply Voltage and Temperature

Typical Performance Characteristics

Typical characteristics are provided at T_A = 25°C and V_S = 40 V unless otherwise noted.

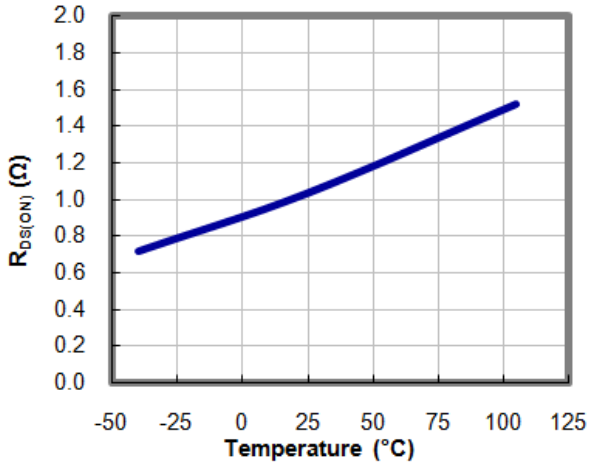


Figure 11. $R_{DS(ON)}$ vs. Temperature

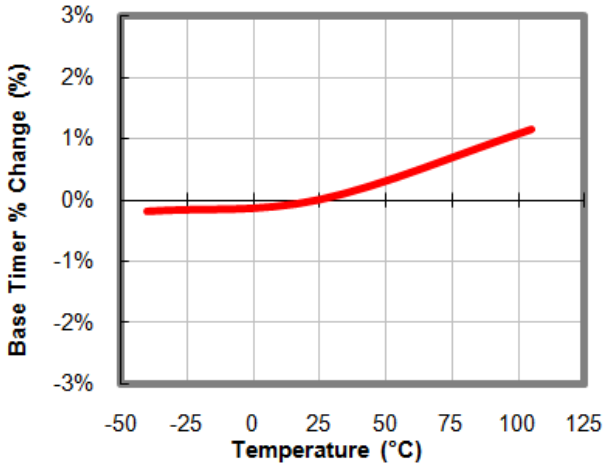


Figure 12. Base Timer % Change vs. Temperature

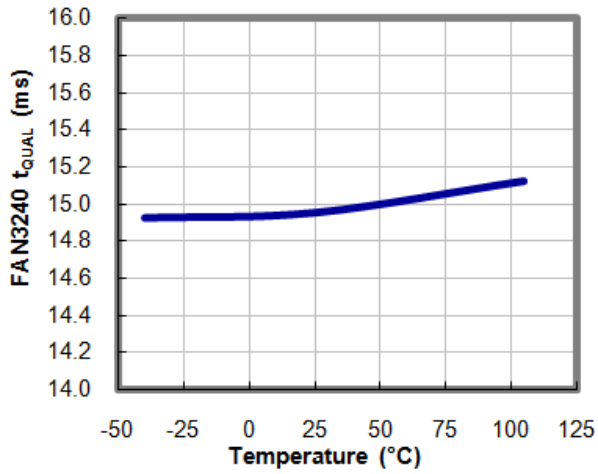


Figure 13. FAN3240 Qualification Time vs. Temperature

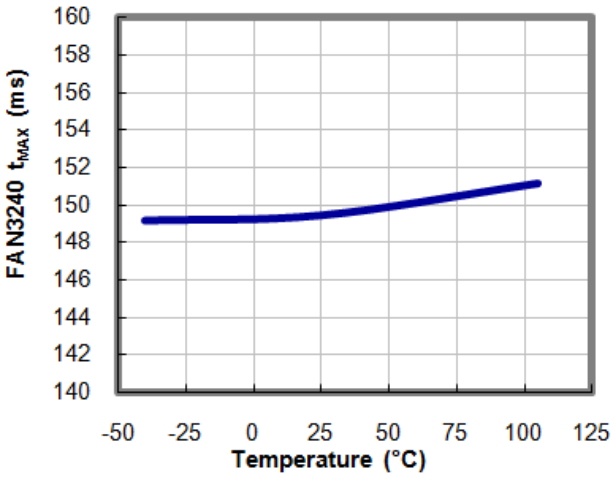


Figure 14. FAN3240 Max. Pulse vs. Temperature

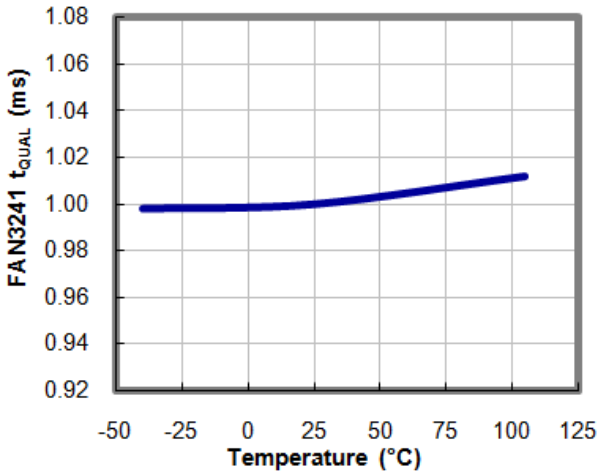


Figure 15. FAN3241 Qualification Time vs. Temperature

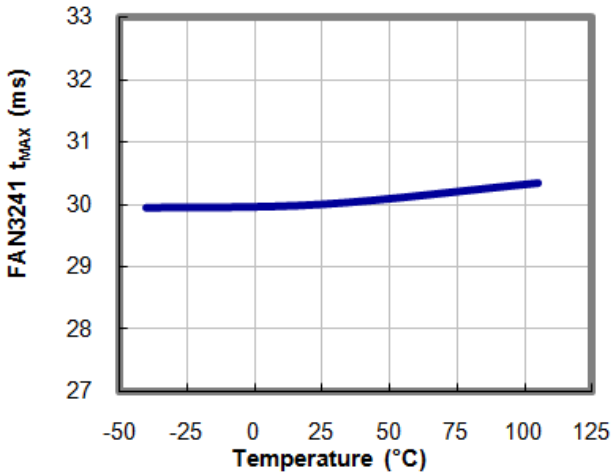


Figure 16. FAN3241 Max. Pulse vs. Temperature

Theory of Operation

Polarized, bi-stabile, latching relays are utilized in many kinds of electronic equipment and diverse applications. These relays usually employ two coils; one to move the relay contact(s) from open to closed position and another coil to move the contact(s) from closed to open position. To facilitate the mechanical movement, the relay coils need to be energized for a specific time interval. Once the contact(s) have changed position, the voltage should be removed from the winding of the relay. A simplified, typical circuit diagram is shown in Figure 17 with example waveforms.

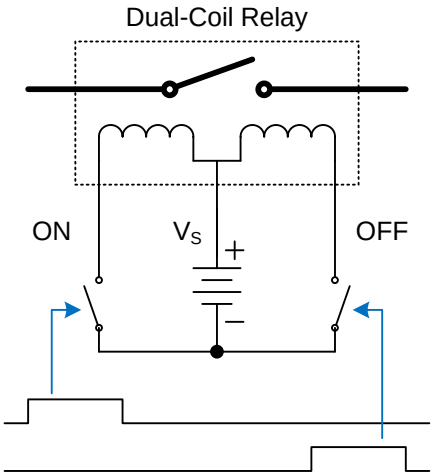


Figure 17. Simplified Diagram of a Relay Drive

As Figure 17 shows, a dual-coil relay is connected to its supply rail at the center point of the two relay windings. Each winding can be energized by the switches connected to the relay coils. The two switches must not be on at the same time because that would cause excessive currents drawn from the supply rail, V_S. Furthermore, to accommodate the relatively long time required for the relay contact to travel between its stationary positions (ON and OFF positions), the pulse must be longer than the minimum duration specified in the relay datasheet. It is also desirable to limit the maximum length of the drive pulse to prevent potential saturation of the relay winding and to avoid over heating the coils and drive electronics. The relay specification also defines the minimum and maximum operating voltages for reliable operation of the contact(s).

The FAN324x family of relay drivers is designed to minimize component count and board space, while increasing the reliability of the system and the noise immunity of the circuitry driving the coils of the relay. The integrated solution provides input signal qualification for the control signals, protection against simultaneous activation of the two relay coils, a maximum drive pulse duration limit, and many basic functions; such as monitoring the relay bias voltage (V_S) for sufficient voltage level, driver enable input, and thermal protection for the IC.

Functional Description

1. Powering the Device (VS Pin)

The FAN324x device is powered through its VS pin by a single voltage source, which should be the same source powering the relay. In general, the VS pin should be connected to the highest potential in the system because the voltage stresses on all other pins shall not exceed the VS pin voltage by more than the forward-voltage drop of a P-N junction, as indicated in the Absolute Maximum Ratings table.

During power-up, the FAN324x receives its bias voltage from the VS pin. As the voltage rises at the VS pin, the 5 V output internal bias regulator starts working. The voltage of the 5VB pin starts rising simultaneously with the bias voltage at the VS pin. Once the V_S voltage is sufficiently high (as described below), the on-board linear regulator enters regulation and provides bias for the FAN324x internal circuitry.

Due to the low power consumption of the internal control circuits; the on-board, low drop-out linear regulator is fully functional and in regulation from approximately 5.5 V on the VS pin. At this point, the FAN324x is still in under-voltage lockout (UVLO); i.e. the relay drive outputs are disabled and exhibit high impedance regardless of the status of the input and enable pins. The device becomes fully functional when the V_S voltage exceeds the UVLO turn-on threshold and stays operational until the V_S voltage falls below the UVLO turn-off threshold. The nominal UVLO hysteresis is about 1 V to prevent turning on and off the device due to noise when the V_S voltage is near the UVLO threshold. The startup behavior is shown in Figure 18.

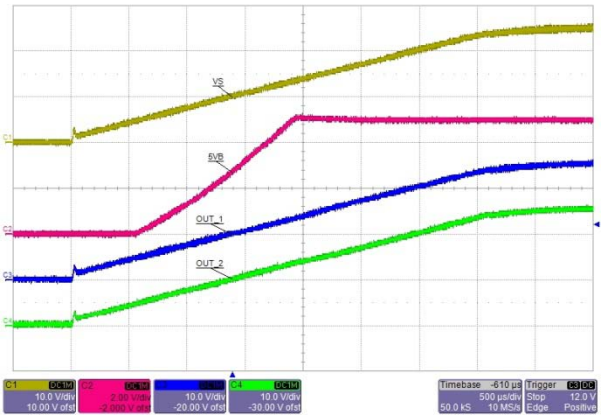


Figure 18. Startup Waveforms

As Figure 18 demonstrates, the startup behavior of the FAN324x devices are well controlled, the bias generator enters regulation smoothly without overshoot or oscillation, and the outputs remain high impedance during the entire startup interval.

2. Internal Bias Regulator (5VB Pin)

The FAN324x's internal bias generator is a low dropout linear regulator with a 5 V output. The regulator is designed to operate with minimum overhead; it is able to regulate its output with very low voltage drop across its bypass element.

The 5 V output of the regulator can be used to power external circuitry as well. In addition to the internal power consumption of the FAN324x, the regulator can deliver at least 5 mA additional current for an external load connected to the 5VB pin of the device.

Similar to other linear regulator circuits, the on-board regulator needs to be bypassed externally for stabile operation. It is recommended that the output of the regulator is bypassed by at least a 100 nF, good-quality, high-frequency, ceramic capacitor placed in close proximity to the 5VB and GND pins.

3. Enable Operation (EN Pin)

The enable (EN) input is a level-sensitive input and it is the most dominant input of the FAN324x during normal operation. The enable pin must be above the input threshold to generate an output pulse and energize the relay coil. The input circuit of the enable input is comprised of a comparator circuit with a precise voltage source connected to the inverting input of the comparator and the EN pin connected to the non-inverting input. To avoid erroneous operation due to potential noise superimposed on the incoming control signal, the enable signal goes through a low-pass filter before it connects to the non-inverting input of the comparator. The filter is designed with a large time-constant; thus the enable input has an approximately 5 µs delay before it can act on the received command level. Once the EN pin is pulled LOW and the signal propagates through the filter, the relay drive outputs become high impedance and the internal control circuit returns to its initial inactive state.

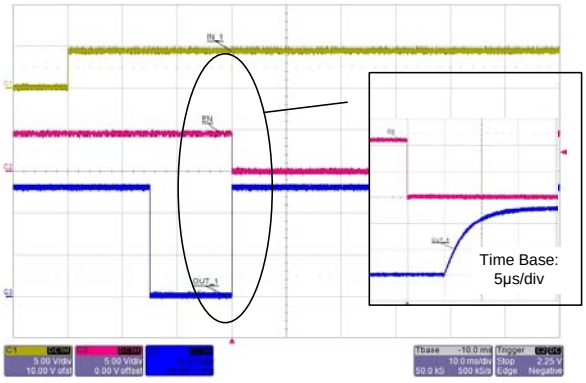


Figure 19. Enable Operating Waveforms

Due to the precise thresholds, the EN input can also be used as a voltage monitoring input that enables or disables the relay drive based on the monitored voltage level.

This functionality can be used to monitor other vital voltage levels in the system, such as the supply voltage for the logic generating the control signals for the FAN324x or the power rail of the relay being driven by the device. An example implementation of this monitoring functionality is shown in Figure 20.

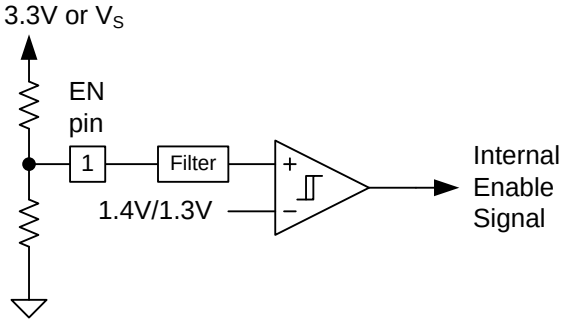


Figure 20. Voltage Monitoring Example Using the EN Input Circuit

As Figure 20 indicates, the input comparator is implemented with a fixed internal hysteresis of approximately 100 mV. The incoming low-pass filter and the built-in hysteresis of the comparator provide enough noise immunity to prevent inadvertent toggling of the internal enable signal. Additional filtering can be added by connecting an additional high-frequency capacitor between the EN pin and GND (pin 6).

Since the input threshold of the comparator is compatible with TTL logic signal levels, the EN input can also be driven directly from a logic source, such as a microcontroller or other similar digital circuits. When the EN pin is driven by a logic signal, the resistors shown in Figure 20 are not needed and additional filtering is not required because of the fast rise and fall times of such digital signals.

It is important to note that while the EN input is the most dominant input during normal operation, the Under-Voltage Lockout (UVLO) and Thermal Shutdown protection (TSD) override the enable input and can disable the operation of the device.

4. Input Signal Processing (IN1 and IN2 Pins)

The FAN324x features two drive channels, one to energize the relay coil to close the relay contact(s) and another one to open it. The channels utilize their respective inputs (IN1 and IN2 pins) and outputs (OUT1 and OUT2 pins). Since the circuitry comprising the two driver channels inside the FAN324x are identical in implementation and in operation, they can be assigned to perform either the opening or closing functions.

The voltage thresholds of the FAN324x inputs meet industry-standard TTL-logic levels independent of the supply voltage, V_S. Therefore, the input pins can be driven from a range of logic signal levels for which a voltage over 2 V is considered logic HIGH (active).

The inputs of the FAN324x are edge-sensitive inputs, which means that an input command is not recognized by the input being HIGH, but rather it is acknowledged when a LOW-to-HIGH transition is sensed at the input pin (IN1 or IN2). This is imperative to avoid erroneous output pulse generation in case an input would be permanently connected to a voltage above the TTL input threshold level. Such a scenario is plausible in case of a manufacturing mistake or if the signal source driving the INx pin stops working and stays permanently in HIGH state.

a) Input Qualification

One of the fundamental functions of the FAN324x is to qualify the incoming logic signals and differentiate between a valid command and noise at its inputs. For reliable operation, all input pulses shorter than the qualification time (t_{QUAL}) of the device are ignored. That means that only qualified input pulses produce an energizing pulse for the relay at output of the device. An input signal becomes qualified if it stays continuously in the HIGH state for a time interval longer than the qualification time.

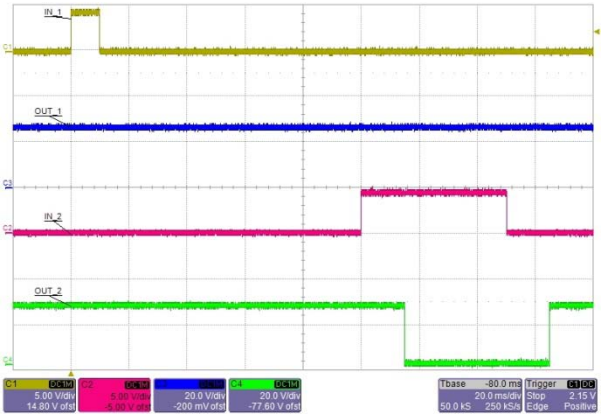


Figure 21. Input Qualification Waveforms

The waveforms shown in Figure 21 were taken with a FAN3240 device. The qualification time of this particular IC is 15 ms. The IN1 pulse width shown in Figure 21 is 10 ms long and it is ignored because it is shorter than t_{QUAL}. The IN2 input receives a 50 ms wide pulse, which is longer than t_{QUAL}; therefore, it qualifies as a valid command. Once the input signal stays continuously HIGH for longer than the qualification time, the relay drive output turns on (OUT2 waveform). In the FAN3240 device, the output pulse width equals the duration of the input signal, as shown in Figure 21.

The length of the output pulse width (an exact copy of the incoming pulse width, as shown, or always the maximum limit), as well as the duration of the qualification time and the maximum allowable length of the output pulse, are factory-adjustable parameters and can be fine tuned to application requirements. These options and the adjustment range of these parameters are described in Section 6 of this Functional Description.

The input qualification circuit provides additional protection against erroneous input pulses and noise at the input terminals. Figure 22 shows the presence of an erroneous input pulse at the IN2 input while the IN1 pulse is being qualified.

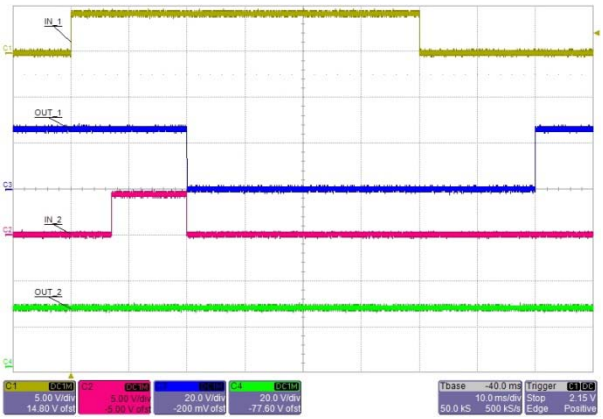


Figure 22. Pending Qualification Waveform

Before IN1 is fully qualified, an erroneous signal appears at the IN2 input. In this case, the qualification of IN1 continues, but the result is pending. If IN2 stays HIGH for longer than t_{QUAL}, both inputs are valid. That scenario falls under XOR protection, which is discussed in the next section. In the example shown in Figure 22, IN2 is shorter than the qualification time and is ignored. At the time when IN2 goes LOW, the IN1 signal is already HIGH for longer than t_{QUAL}. Therefore, IN1 is a valid command and is executed as demonstrated by the waveforms in Figure 22.

b) Additional Input Protection Functions

It is also possible that activating one of the inputs and its corresponding output signal will create noise in the system which will show up at the inactive input.

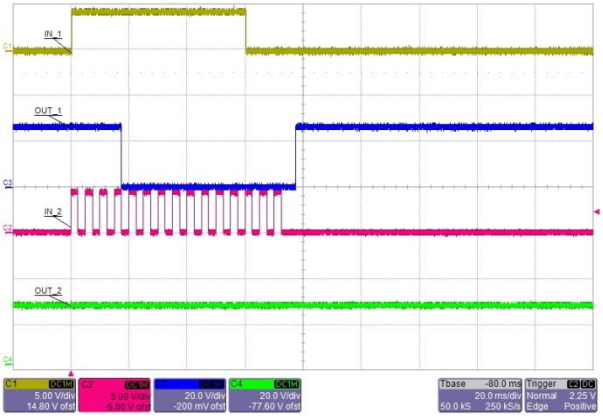


Figure 23. Noise at the Inactive Input

As Figure 23 shows, noise on the inactive input pin is suppressed and ignored. The FAN324x family of relay drivers can handle excessive noise signatures reliably.

Another aspect of protecting the integrity of the system is to ensure that a new command cannot be received and executed until the previous command execution is finished.

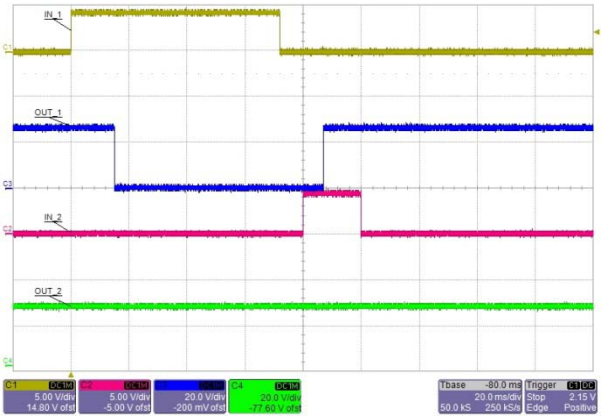


Figure 24. Exclusion of Overlapping Commands

Figure 24 illustrates the operation of the FAN324x with overlapping commands. The IN2 input signal is being received while the previous command on channel one is still being executed. It is signified by the fact that OUT1 is still LOW when the rising edge of the IN2 signal arrives. Because the previous command is still active, the IN2 signal is discarded by the input protection logic of the FAN324x. That means that once the FAN324x is committed to an output pulse, it ignores the other input (except the EN input, which is the most dominant input of the device).

c) XOR Input Protection

The XOR protection implemented in the FAN324x devices prohibits output pulses when two qualified input signals have been received at the same time. The XOR protection works when both inputs are asserted together or a second qualified input is received while the first one is being qualified. The two cases of the XOR protection are illustrated in Figure 25 and Figure 26.

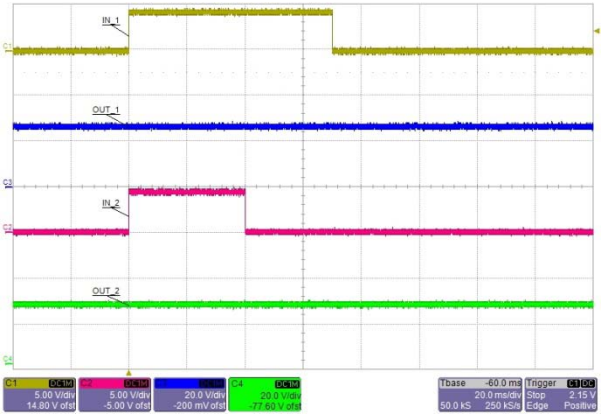


Figure 25. Simultaneous Insertion of Two Qualified Inputs

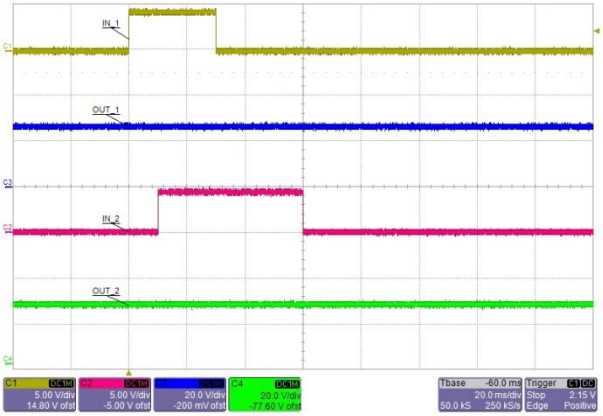


Figure 26. Overlapping Qualified Inputs Case

The XOR protection prevents simultaneous drive signals being delivered to the two coils of the relay and is an important feature of the device.

5. Relay Drive Outputs (OUT1 and OUT2 Pins)

The actual relay is driven through the dedicated drive outputs of the FAN324x. These outputs utilize monolithic MOSFET power devices, in an open-drain configuration, which are capable of handling the voltage level and drive current required to energize the relay coils. The typical R_{DSON} resistance of these devices is 0.9 Ω and they are designed for approximately 1 A output currents. Carrying the rated output current continuously through the relay coil and the output transistors of the FAN324x would cause excessive power dissipation in the relay coil as well as in the driver. It is therefore necessary to prevent the outputs to be on continuously.

The maximum on-time of the FAN324x outputs is limited by the protection logic circuit. Under no circumstances should the outputs be on longer than the duration specified by the t_{MAX} parameter. Figure 27 demonstrates operation of the output pulse width limiter of the device.

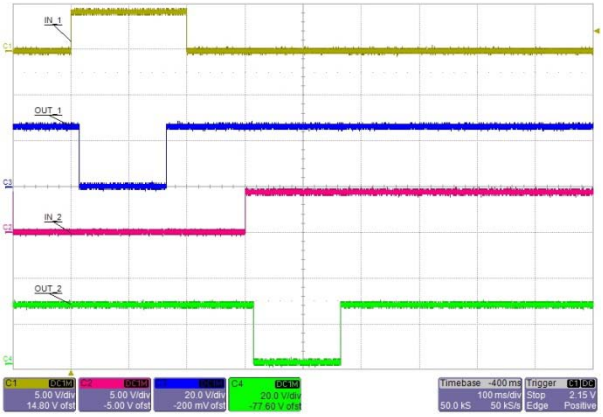


Figure 27. Maximum Output Pulse Width Limiting

If the input pulse is longer than the maximum on-time listed in the datasheet, the duration of the output pulse width is equal to t_{MAX}.

This protection feature works for any event that would produce a longer-than-allowed input command. Figure 27 shows typical cases of receiving a long input signal.

In the case of IN1, the input signal is a square wave, but its HIGH state is longer than t_{MAX}. The corresponding OUT1 output is terminated 150 ms after its start time, which is the exact maximum on-time of the FAN3240 device used in the measurement.

Figure 27 shows the IN2 input staying HIGH permanently. Similar behavior to the long square wave input case can be observed on the OUT2 output. The drive signal is terminated when the pulse width reaches the t_{MAX} limit.

6. Operating Modes

Some aspects of the FAN324x family of relay drivers' operation can be adjusted through the below factory-configurable parameters:

1. t_{QUAL}: Qualification Time. This is the minimum input pulse width duration recognized as a valid input command.
2. t_{MAX}: Maximum Output Pulse Width. Output pulses are terminated after this time interval even if the input pulse is longer or held in a HIGH state continuously.
3. Output Mode: The FAN324x offers two output pulse generation methods:

   $t_{OUT} = t_{IN} < t_{MAX}$. In this mode, the output pulse duration (t_{OUT}) replicates the length of the input pulse (t_{IN}) up to t_{MAX}.

   $t_{OUT} = t_{MAX}$. The output is on for a fixed time interval of t_{MAX}, regardless of the input pulse width.

   The mode of operation has no impact on the qualification requirements or on the maximum output pulse width limiting. In both output operating modes, the qualification requirement must be met ($t_{IN} > t_{QUAL}$) to produce an output pulse.

Table 1. **Factory Set Configurations**

Product	t_{QUAL}	t_{MAX}	OUT Mode
FAN3240	15 ms	150 ms	$t_{OUT} = t_{IN}$
FAN3241	1 ms	30 ms	$t_{OUT} = t_{MAX}$

Contact a Fairchild sales representatives for additional configurations. The parameter t_{QUAL} can be configured between 128 µs and 20 ms. Parameter t_{MAX} can be programmed between 1 ms and 350 ms.

The Figure 28 and Figure 29 scope pictures clarify the operation of the FAN3240 device. The configuration options are listed in Table 1.

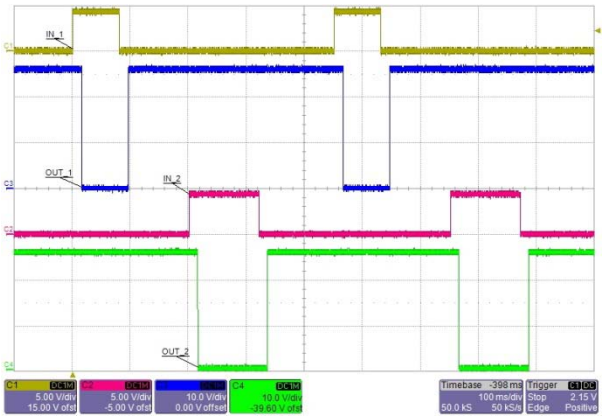


Figure 28. FAN3240 Operation

The FAN3240 is configured to produce an output pulse that equals the length of the incoming control signal. As Figure 28 indicates, the incoming signals might not be the same length. They are accurately reproduced at the respective outputs of the device. The delay between the input and output pulses is the qualification time. Further detail of the timing relationship between the input and output pulses are illustrated in Figure 29.

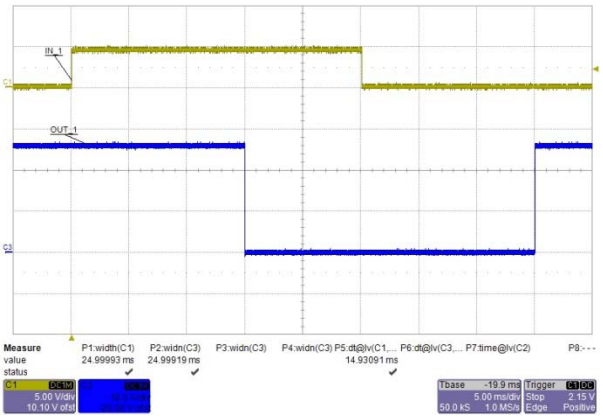


Figure 29. Timing Details of FAN3240 Operation

The input pulse width received at IN1 is measured by the oscilloscope and can be found under the label P1. The measurement P2 is the length of the output pulse generated by the FAN3240. Note the extremely accurate reproduction of the input pulse duration at the output of the device. The third measurement, labeled P5, is the time between the rising edge of IN_1 and the falling edge of OUT_1 traces. It is the qualification time measured by the oscilloscope.

Similar measurements demonstrating the operation of the FAN3241 are shown in Figure 30 and Figure 31.

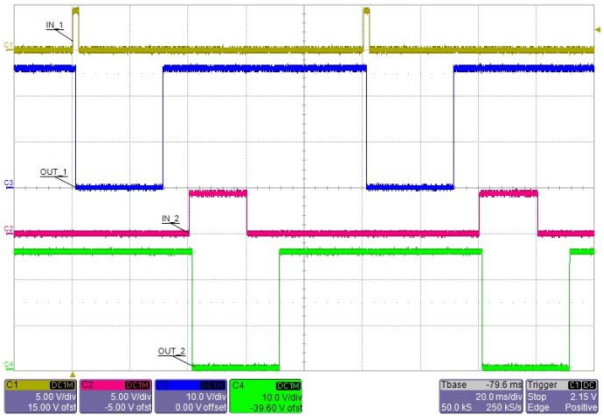


Figure 30. Operating Waveforms

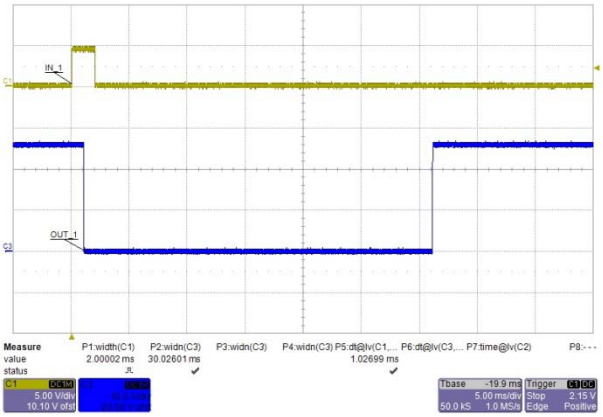


Figure 31. Timing Waveforms of the FAN3241

The FAN3241 produces fixed length output pulses as long as the incoming pulse width meets the qualification requirements. The timing details are shown in Figure 31.

Similar to the previous example, the P1 measurement of the oscilloscope shows the length of the input command, IN_1. The t_{MAX} duration is shown under the label P2 and t_{QUAL} is measured under P5. The results show accurate timing performance for both factory programmable parameters.

Applications Information

The FAN324x significantly improves reliability and offers many protection functions that would be impractical to implement using discrete circuit components. In addition, it also greatly reduces component count and simplifies the relay drive circuit. A typical relay drive application is depicted in Figure 32.

Input Connections

The inputs of the relay driver can be directly driven from any appropriate signal source producing a TTL-compatible logic signal. The IN1 and IN2 inputs have 100 kΩ internal pull-down resistors, ensuring the off-state of the drive outputs during the high-impedance state of the source. This could happen during startup when a microcontroller is used to control the system.

Enable Connection

The enable (EN) pin of the device must be connected to the 5VB pin if it is not used. There is no pull-up or pull-down termination at this pin because any internal impedance might impact the accuracy of the comparator circuit when this pin is used for voltage monitoring.

5VB Bypass Recommendations

The 5VB pin is the output of the internal bias regulator of the FAN324x. For stability of the negative feedback loop of the linear regulator and for noise filtering, a good quality high-frequency capacitor must be connected between this pin and the ground (GND) pin of the device. The recommended minimum capacitance is 100 nF. The capacitor should be placed near the 5VB and GND pins for best result.

The output voltage of the on-board linear regulator is 5 V. This 5 V output can be used to power external circuitry. An example is shown in the application schematic of Figure 34 for isolated designs. The maximum guaranteed output current that can be used by external circuits is 5 mA; the regulator can deliver at least 5 mA to the external load and still meet all specifications listed in the parametric tables.

5VB Power Dissipation Considerations

The output current of the 5VB bias regulator is supplied from the VS pin. While the recommended output current is 5 mA or less, the regulator is capable of sourcing significantly more current before its current limit is activated. Figure 10 of the typical performance characteristics curves shows the maximum current capability of the on-board linear regulator as a function of the input voltage and ambient temperature.

If FAN324x is within recommended operating conditions (I_{5VB} < 5 mA), the power dissipation of the regulator remains below 275 mW even at the highest operating voltage (60 V). However, at higher current levels, the power dissipation of the regulator and the thermal capabilities of the SOIC-8 package must be considered.

At high input voltage levels (V_S > 25 V) and currents over the guaranteed 5 mA level, the power loss of the on-board regulator might be high enough to elevate the junction temperature to the thermal protection shutdown threshold. If this occurs, the device shuts down to protect itself and functionality is lost until the junction temperature falls approximately 25°C (the thermal shutdown hysteresis).

To preserve full functionality and reliable operation, it is recommended to check the output current rating of the linear regulator and to always calculate the power dissipation and the maximum temperature rise due to self heating.

VS Pin Bypass Guidelines

Good-quality, high-frequency, ceramic capacitors should be placed in close proximity to the VS and GND pins for local bypass for the IC. A recommended value is 1 µF. This capacitor serves as separate energy storage for the FAN324x. As it is shown in Figure 32, a low value (~10 Ω) resistor could be used to form a filter with the VS pin bypass capacitor and prevent large noise spikes propagating from the relay power supply to the bias voltage of the device.

If deep discharge of the relay bypass capacitor is anticipated during the switching of the relay, an optional small-signal diode in series with the filter resistor is recommended. The diode can avert the discharge of the local VS pin bypass capacitor even if the relay supply voltage would fall during switching. This technique can prevent accidental activation of the under-voltage lockout mechanism.

Output Connections

The FAN324x devices feature an open-drain MOSFET output structure which is designed to carry the required current to energize the relay coils. The relay coils can be considered as a series combination of an inductor and a resistor. Like in many other applications where substantial inductive load current is being interrupted, switching spikes can present excessive voltage stresses on the output devices. Therefore, it is necessary to use two clamp diodes to protect each output of the FAN324x against the inductive spikes. It is important to emphasize that the clamp diodes sole responsibility is to protect the switches. Thus their location on the printed circuit board layout is very important.

It is recommended that the clamp diodes are placed near the OUT1 and OUT2 pins and the VS pin as shown in Figure 32.

If using the small blocking diode, the inductive energy is fully absorbed by the VS pin bypass capacitor. This might require increasing the size of the local bypass capacitor to effectively clamp the voltage at the VS pin. Consider that the quiescent current consumption of the FAN324x is the only load on the VS bypass capacitor. Rapid repetitive switching action might increase the voltage across the capacitor. To address this concern, Figure 33 (shows an alternative termination of the clamp diodes, back to the center point of the relay, directly to the relay power supply output, which has a much higher capacitance.

Typical Configurations

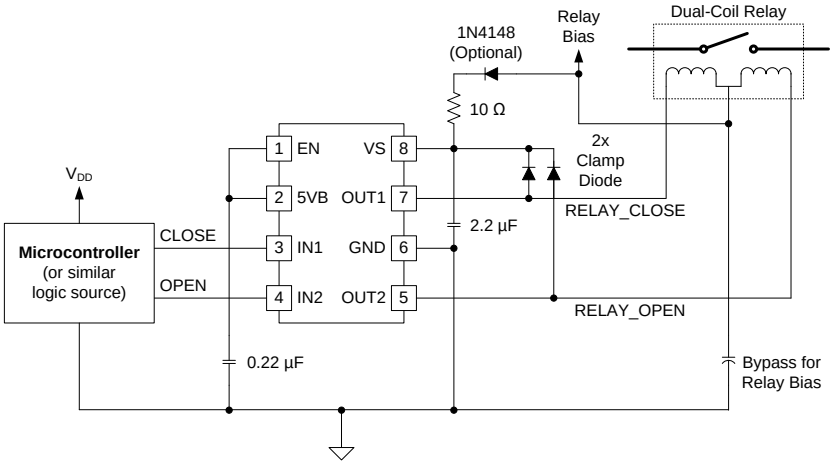


Figure 32. Typical Application Schematic

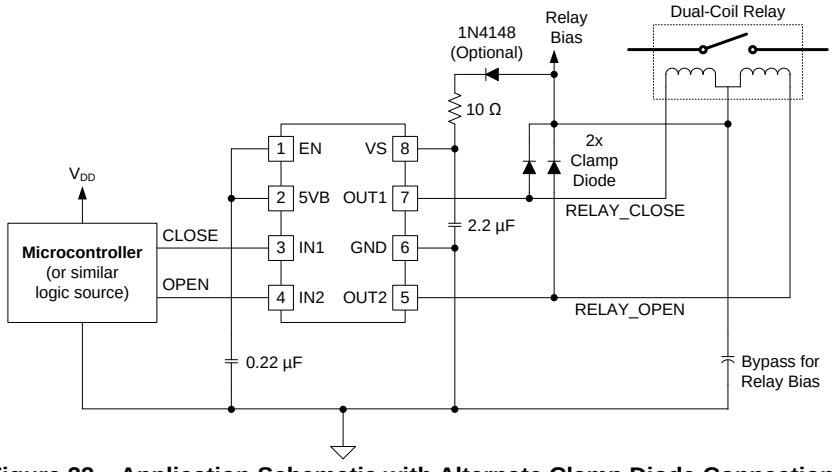


Figure 33. Application Schematic with Alternate Clamp Diode Connections

Isolated Applications

In some cases, it might be desirable to completely separate the power system of the actual relay drive from the supply voltages of the control electronics. The FAN324x relay drivers can facilitate an isolated relay drive implementation, as shown in the Figure 34 schematic. The solution can be as simple as inserting the opto-couplers in the command signal path. As indicated in Figure 34, the opto-couplers need a pull-up resistor to a positive voltage rail, which is available at the 5VB pin. Having the internal 5 V bias voltage accessible externally eliminates the need to generate an additional low voltage on the isolated side just for the pull-up resistors of the opto-couplers.

Note that the opto-couplers might also invert the control signals as they transmit them through the isolation boundary. The circuit in Figure 34 is an inverting opto-coupler implementation. When the logic signal goes HIGH at the microcontroller output, the input connection to the FAN324x is pulled LOW. This is the exact opposite of the required control sequence. The solution is to use negative logic at the output of the microcontroller in anticipation of the inversion at the opto-coupler output. The other option is to connect the anodes of the opto diodes to the bias supply of the digital logic (V_{DD}) and exert the control from the microcontroller at the cathode of the opto-coupler.

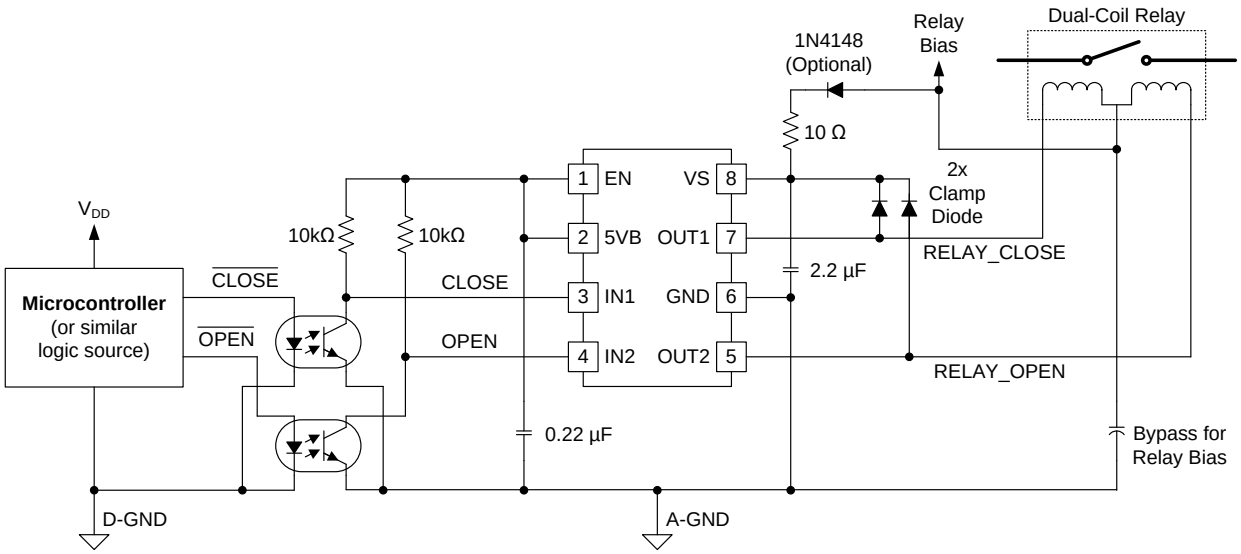


Figure 34. Application Schematic for Isolated Designs

Layout and Connection Guidelines

The FAN324x relay drivers incorporate fast input circuits and powerful output stages capable of delivering high current peaks. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate from the logic and enable input signals and signal ground paths.
- Keep the driver as close to the load as possible to minimize the length of high-current traces.
- Minimize the relay current loop. Keep in mind that the current of the relay coil flows through the relay bias power supply's output capacitor, the coils themselves, the integrated output switches of the FAN324x and the GND connections.

Physical Dimensions

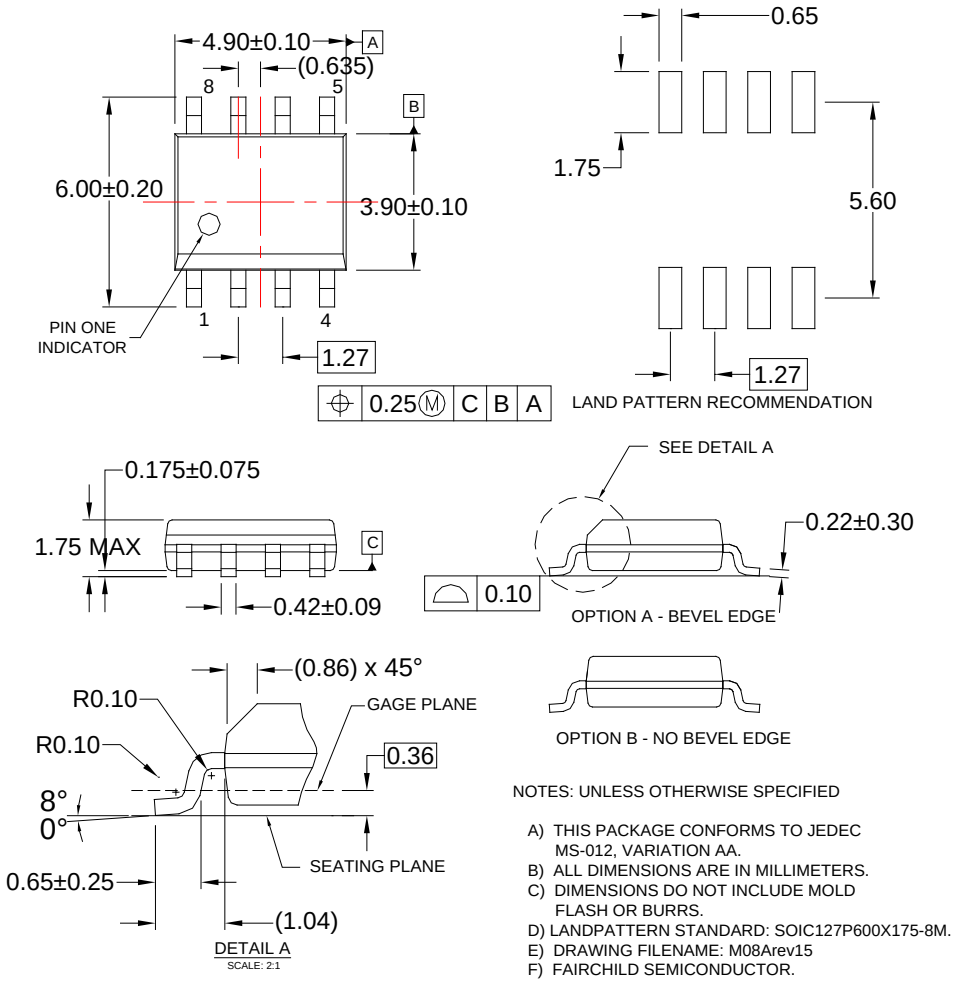


Figure 35. 8-Lead, Small-Outline Integrated Curcuit (SOIC)

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