## **Power MOSFET**

## 60 V, 27.5 m $\Omega$ , 21 A, Single N–Channel

#### Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low R<sub>DS(on)</sub> to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- NVMFS5C680NLWF Wettable Flanks Product
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### **MAXIMUM RATINGS** (T<sub>J</sub> = $25^{\circ}$ C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	60	V
Gate-to-Source Voltage			V <sub>GS</sub>	±20	V
Continuous Drain		$T_{C} = 25^{\circ}C$	Ι <sub>D</sub>	21	А
Current $R_{\theta JC}$ (Notes 1, 2, 3, 4)	Steady	T <sub>C</sub> = 100°C		15	
Power Dissipation	State	T <sub>C</sub> = 25°C	PD	24	W
$R_{\theta JC}$ (Notes 1, 2, 3)		T <sub>C</sub> = 100°C		12	
Continuous Drain	Steady State	$T_A = 25^{\circ}C$	Ι <sub>D</sub>	8.1	А
Current R <sub>0JA</sub> (Notes 1 & 3, 4)		T <sub>A</sub> = 100°C		5.7	
Power Dissipation		T <sub>A</sub> = 25°C	PD	3.4	W
$R_{\theta JA}$ (Notes 1, 3)		$T_A = 100^{\circ}C$		1.7	
Pulsed Drain Current	$T_{A} = 25$	°C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	87	А
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Source Current (Body Diode)			۱ <sub>S</sub>	20	А
Single Pulse Drain–to–Source Avalanche Energy ( $I_{L(pk)} = 1.5 \text{ A}$ )			E <sub>AS</sub>	44.6	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			ΤL	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### THERMAL RESISTANCE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 3)	$R_{\thetaJC}$	6.3	°C/W
Junction-to-Ambient - Steady State (Note 3)	$R_{\thetaJA}$	44	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

2. Psi ( $\Psi$ ) is used as required per JESD51–12 for packages in which substantially less than 100% of the heat flows to single case surface.

3. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.

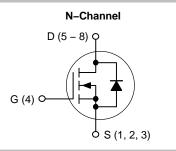
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



### **ON Semiconductor®**

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V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> MAX	I <sub>D</sub> MAX
60 V	27.5 mΩ @ 10 V	21 A
60 V	43.0 mΩ @ 4.5 V	217





ZZ = Lot Traceability

#### ORDERING INFORMATION

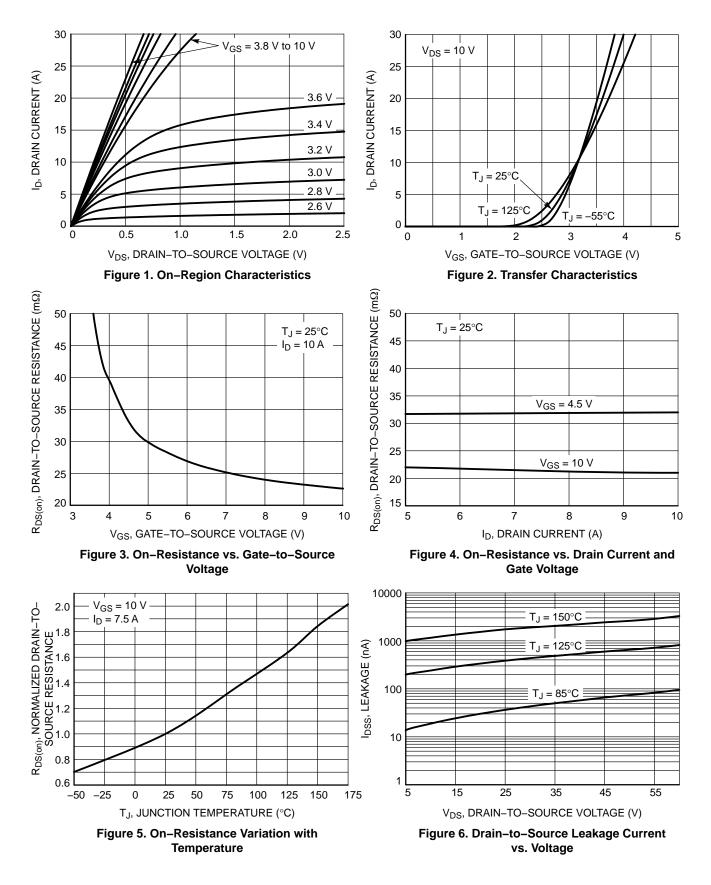
See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

#### ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

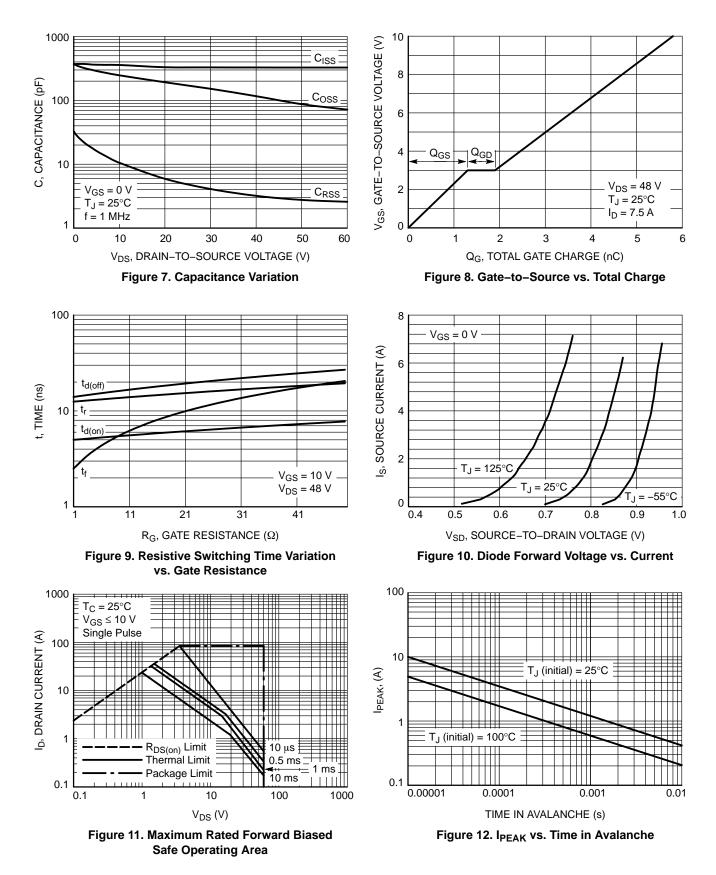
Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS}$ = 0 V, $I_D$ = 250 $\mu$ A		60			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	$T_J = 25^{\circ}C$			10	μΑ
			T <sub>J</sub> = 125°C			250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V				100	nA
ON CHARACTERISTICS (Note 5)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{DS}$	<sub>0</sub> = 13 μA	1.2		2.2	V
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$			22.9	27.5	mΩ
					35.8	43.0	
Forward Transconductance	9fs	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A			20		S
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V			330		pF
Output Capacitance	C <sub>oss</sub>				172		-
Reverse Transfer Capacitance	C <sub>rss</sub>				5		
Total Gate Charge	Q <sub>G(TOT)</sub>	$V_{GS} = 10 \text{ V}, \text{ V}_{DS} = 48 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}, \text{ V}_{DS} = 48 \text{ V}, \text{ I}_{D} = 7.5 \text{ A}$			5.8		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>				0.8		nC
Gate-to-Source Charge	Q <sub>GS</sub>				1.3		
Gate-to-Drain Charge	Q <sub>GD</sub>				0.6		
Total Gate Charge	Q <sub>G(TOT)</sub>				2.7		nC
SWITCHING CHARACTERISTICS (No	te 6)		-				
Turn-On Delay Time	t <sub>d(on)</sub>				5		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = 10 V, V <sub>L</sub>	<sub>0S</sub> = 48 V,		12.5		1
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}$ = 10 V, $V_{DS}$ = 48 V, I <sub>D</sub> = 7.5 A, R <sub>G</sub> = 1.0 Ω			14		
Fall Time	t <sub>f</sub>				2.5		
DRAIN-SOURCE DIODE CHARACTER	ISTICS						
Forward Diode Voltage	V <sub>SD</sub>	$V_{GS} = 0 V,$ $I_{S} = 7.5 A$	$T_J = 25^{\circ}C$		0.87	1.2	V
			T <sub>J</sub> = 125°C		0.76		
Reverse Recovery Time	t <sub>RR</sub>	$V_{GS} = 0 V$ , $dI_S/dt = 100 A/\mu s$ , $I_S = 7.5 A$			18		ns
Charge Time	ta				8.3		
Discharge Time	t <sub>b</sub>				9.7		
Reverse Recovery Charge	Q <sub>RR</sub>				7.5		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

#### **TYPICAL CHARACTERISTICS**



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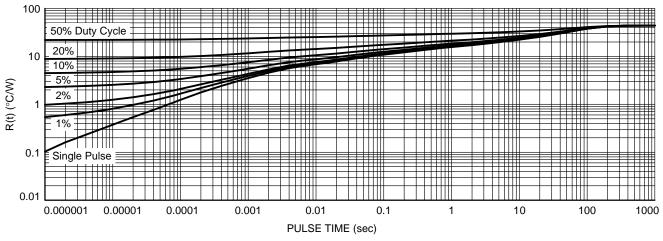


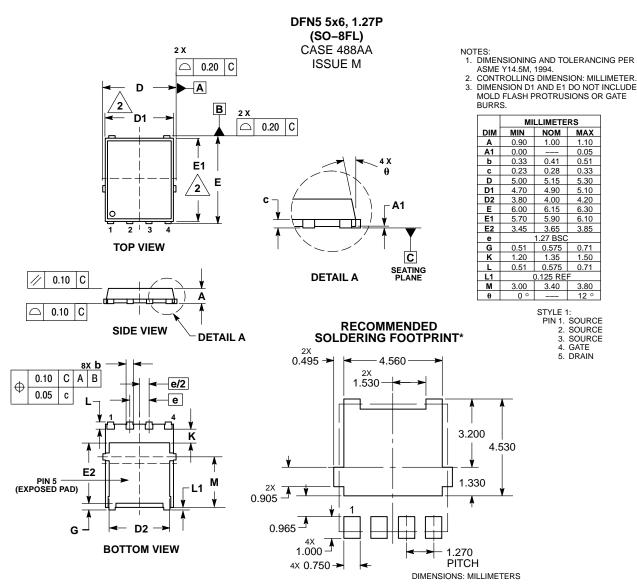
Figure 13. Thermal Characteristics

#### **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NVMFS5C680NLT1G	5C680L	DFN5 (Pb–Free)	1500 / Tape & Reel
NVMFS5C680NLWFT1G	680LWF	DFN5 (Pb–Free)	1500 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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#### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT

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