FEATURES
Dual 14-bit SAR ADC
Simultaneous sampling
Throughput rate: 4.2 MSPS per channel
Specified for a $V_{DD}$ of 2.5 V
Power dissipation: 36 mW at 4.2 MSPS
On-chip reference: 2.048 V ± 0.25%, 6 ppm/°C
Dual conversion with read
High speed serial interface
SPI-/QSPI-/MICROWIRE-/DSP-compatible
−40°C to +125°C operation
16-lead TSSOP package
Qualified for automotive applications

APPLICATIONS
Automotive radar
Data acquisition systems
Motion control
I and Q demodulation
RFID readers

GENERAL DESCRIPTION
The AD7357\(^1\) is a dual, 14-bit, high speed, low power, successive approximation analog-to-digital converter (ADC) that operates from a single 2.5 V power supply and features throughput rates up to 4.2 MSPS. The part contains two ADCs, each preceded by a low noise, wide bandwidth track-and-hold circuit that can handle input frequencies in excess of 110 MHz.

The conversion process and data acquisition use standard control inputs allowing for easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of CS; a conversion is also initiated at this point. The conversion time is determined by the SCLK frequency.

The AD7357 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With a 2.5 V supply and a 4.2 MSPS throughput rate, the part consumes 14 mA typically. The part also offers flexible power/throughput rate management options.

The analog input range for the part is the differential common mode ±$V_{REF}$/2. The AD7357 has an on-chip 2.048 V reference that can be overdriven when an external reference is preferred.

The AD7357 is available in a 16-lead thin shrink small outline package (TSSOP).

PRODUCT HIGHLIGHTS
1. Two Complete ADC Functions.
   These functions allow simultaneous sampling and conversion of two channels. The conversion result of both channels is simultaneously available on separate data lines or in succession on one data line if only one serial port is available.

2. High Throughput with Low Power Consumption.
   The AD7357 offers a 4.2 MSPS throughput rate with 36 mW power consumption.

3. Simultaneous Sampling.
   The part features two standard successive approximation ADCs with accurate control of the sampling instant via a CS input and once-off conversion control.

Table 1. Related Devices

<table>
<thead>
<tr>
<th>Generic</th>
<th>Resolution</th>
<th>Throughput</th>
<th>Analog Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD7356</td>
<td>12-bit</td>
<td>5 MSPS</td>
<td>Differential</td>
</tr>
<tr>
<td>AD7352</td>
<td>12-bit</td>
<td>3 MSPS</td>
<td>Differential</td>
</tr>
<tr>
<td>AD7266</td>
<td>12-bit</td>
<td>2 MSPS</td>
<td>Differential/single-ended</td>
</tr>
<tr>
<td>AD7866</td>
<td>12-bit</td>
<td>1 MSPS</td>
<td>Single-ended</td>
</tr>
<tr>
<td>AD7366</td>
<td>12-bit</td>
<td>1 MSPS</td>
<td>Single-ended bipolar</td>
</tr>
<tr>
<td>AD7367</td>
<td>14-bit</td>
<td>1 MSPS</td>
<td>Single-ended bipolar</td>
</tr>
</tbody>
</table>

\(^1\) Protected by U.S. Patent No. 6,681,332.
IMPORTANT LINKS for the AD7357*

Last content update 12/15/2013 08:15 pm

SIMILAR PRODUCTS & PARAMETRIC SELECTION TABLES
Find Similar Products By Operating Parameters

DOCUMENTATION
CN-0061: DC-Coupled, Single-Ended-to-Differential Conversion Using the AD8138 Low Distortion Differential ADC Driver and AD7357 Dual, 4.2 MSPS, 14-Bit SAR ADC
MS-2210: Designing Power Supplies for High Speed ADC

PRODUCT RECOMMENDATIONS & REFERENCE DESIGNS
CN-0061: DC-Coupled, Single-Ended-to-Differential Conversion Using the AD8138 Low Distortion Differential ADC Driver and AD7357 Dual, 4.2 MSPS, 14-Bit SAR ADC

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India: 1800-419-0108
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Quality and Reliability
Lead(Pb)-Free Data

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- Request Evaluation Board
- Request Samples
- Check Inventory & Purchase

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* This page was dynamically generated by Analog Devices, Inc. and inserted into this data sheet.
Note: Dynamic changes to the content on this page (labeled 'Important Links') does not constitute a change to the revision number of the product data sheet. This content may be frequently modified.
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REVISION HISTORY

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4/09—Revision 0: Initial Version
**SPECIFICATIONS**

\( V_{DD} = 2.5 \pm 10\% \ V, \ V_{DRIVE} = 2.25 \ V \) to \( 3.6 \ V, \) internal reference = \( 2.048 \ V, \ f_{SCLK} = 80 \ MHz, \ f_{SAMPLE} = 4.2 \ MSPS; \ T_A = T_{MIN} \) to \( T_{MAX}, \) unless otherwise noted.

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>AD7357B/AD7357Y</th>
<th></th>
<th>AD7357WY</th>
<th></th>
<th>Test Conditions/ Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal-to-Noise Ratio (SNR)</td>
<td>74.5</td>
<td>76.5</td>
<td>74.5</td>
<td>76.5</td>
<td>dB ( f_{IN} = 500 \ kHz ) sine wave</td>
</tr>
<tr>
<td>Signal-to-Noise and Distortion (SINAD)(^2)</td>
<td>74</td>
<td>76</td>
<td>74</td>
<td>76</td>
<td>dB ( T_A = T_{MIN} ) to ( T_{MAX}, ) −40°C to +25°C only</td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)(^2)</td>
<td>−83 3</td>
<td>−80</td>
<td>−83</td>
<td>−80</td>
<td>dB ( T_A = T_{MIN} ) to ( T_{MAX}, ) −40°C to +25°C only</td>
</tr>
<tr>
<td>Spurious Free Dynamic Range (SFDR)</td>
<td>−85 3</td>
<td>−82</td>
<td>−85</td>
<td>−82</td>
<td>dB ( T_A = T_{MIN} ) to ( T_{MAX}, ) −40°C to +25°C only</td>
</tr>
<tr>
<td>Intermodulation Distortion (IMD)(^2)</td>
<td>−86</td>
<td>−86</td>
<td>−86</td>
<td>−86</td>
<td>dB ( f_a = 1 \ MHz ) + 50 kHz, ( f_b = 1 \ MHz ) − 50 kHz</td>
</tr>
<tr>
<td>Second-Order Terms</td>
<td>−86</td>
<td></td>
<td>−86</td>
<td></td>
<td>dB ( f_{NOISE} = 100 \ kHz ) to 2.5 MHz</td>
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<tr>
<td>Third-Order Terms</td>
<td>−79</td>
<td></td>
<td>−79</td>
<td></td>
<td>dB ( f_{NOISE} = 100 \ kHz ) to 2.5 MHz</td>
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<tr>
<td>ADC-to-ADC Isolation(^2)</td>
<td>−100</td>
<td></td>
<td>−100</td>
<td></td>
<td>dB ( f_{NOISE} = 100 \ kHz ) to 2.5 MHz</td>
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<tr>
<td><strong>SAMPLE-AND-HOLD</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Aperture Delay</td>
<td>3.5</td>
<td></td>
<td>3.5</td>
<td></td>
<td>ns ( f_{IN} = 1 \ MHz )</td>
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<tr>
<td>Aperture Delay Match</td>
<td>40</td>
<td></td>
<td>40</td>
<td></td>
<td>ps ( f_{NOISE} = 100 \ kHz ) to 2.5 MHz</td>
</tr>
<tr>
<td>Aperture Jitter</td>
<td>16</td>
<td></td>
<td>16</td>
<td></td>
<td>ps ( f_{IN} = 1 \ MHz )</td>
</tr>
<tr>
<td>Full Power Bandwidth</td>
<td>110</td>
<td></td>
<td>110</td>
<td></td>
<td>MHz ( f_{NOISE} = 100 \ kHz ) to 2.5 MHz</td>
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<tr>
<td>@ 3 dB</td>
<td>77</td>
<td></td>
<td>77</td>
<td></td>
<td>@ 0.1 dB</td>
</tr>
<tr>
<td>@ 0.1 dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DC ACCURACY</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>14</td>
<td></td>
<td>14</td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Integral Nonlinearity (INL)(^2)</td>
<td>±2</td>
<td>±3</td>
<td>±2</td>
<td>±3</td>
<td>LSB Guaranteed no missed codes to 14 bits</td>
</tr>
<tr>
<td>Differential Nonlinearity (DNL)(^2)</td>
<td>±0.5</td>
<td>±0.99</td>
<td>±0.5</td>
<td>±0.99</td>
<td>LSB Guaranteed no missed codes to 14 bits</td>
</tr>
<tr>
<td>Positive Full-Scale Error(^2)</td>
<td>±20</td>
<td></td>
<td>±20</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Positive Full-Scale Error Match(^2)</td>
<td>±20</td>
<td></td>
<td>±20</td>
<td></td>
<td>LSB</td>
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<tr>
<td>Midscale Error(^2)</td>
<td>0/35</td>
<td></td>
<td>0/35</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Midscale Error Match(^2)</td>
<td>±12</td>
<td></td>
<td>±15</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Negative Full-Scale Error(^2)</td>
<td>±20</td>
<td></td>
<td>±20</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Negative Full-Scale Error Match(^2)</td>
<td>±20</td>
<td></td>
<td>±20</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td><strong>ANALOG INPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fully Differential Input Range (( V_{IN+} ) and ( V_{IN-} ))</td>
<td>( V_{CM} \pm V_{REF}/2 )</td>
<td>( V_{CM} \pm V_{REF}/2 )</td>
<td>( V_{CM} \pm V_{REF}/2 )</td>
<td>( V_{CM} \pm V_{REF}/2 )</td>
<td>( V_{CM} \pm V_{REF}/2 )</td>
</tr>
<tr>
<td>Common-Mode Voltage Range</td>
<td>0.5</td>
<td>1.6</td>
<td>0.5</td>
<td>1.6</td>
<td>V The voltage around which ( V_{IN+} ) and ( V_{IN-} ) are centered</td>
</tr>
<tr>
<td>DC Leakage Current</td>
<td>±0.5</td>
<td>±5</td>
<td>±0.5</td>
<td>±5</td>
<td>µA When in track mode</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>32</td>
<td></td>
<td>32</td>
<td></td>
<td>pF When in hold mode</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td></td>
<td>8</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>
## AD7357

### Parameter | AD7357B/AD7357Y | AD7357WY | Unit | Test Conditions/Comments
--- | --- | --- | --- | ---
**REFERENCE INPUT/OUTPUT**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Input Voltage Range</td>
<td>2.048 + 0.1</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>2.048 + 0.1</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>V</td>
<td>mA</td>
<td>When in reference overdrive mode</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Input Current</td>
<td>0.3</td>
<td>0.45</td>
<td>0.3</td>
<td>0.45</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Output Voltage</td>
<td>2.038</td>
<td>2.058</td>
<td>2.038</td>
<td>2.058</td>
<td>V</td>
<td>±2.048 V ± 0.5% max @ V&lt;sub&gt;DD&lt;/sub&gt; = 2.5 V ± 5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Temperature Coefficient</td>
<td>6</td>
<td>20</td>
<td>6</td>
<td>20</td>
<td>ppm/°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Long Term Stability</td>
<td>100</td>
<td>100</td>
<td>ppm</td>
<td>For 1000 hours</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Thermal Hysteresis</td>
<td>50</td>
<td>50</td>
<td>ppm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Noise</td>
<td>60</td>
<td>60</td>
<td>µV rms</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>V&lt;sub&gt;REF&lt;/sub&gt; Output Impedance</td>
<td>1</td>
<td>1</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
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</table>

**LOGIC INPUTS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage, V&lt;sub&gt;INH&lt;/sub&gt;</td>
<td>0.6 × V&lt;sub&gt;DRIVE&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage, V&lt;sub&gt;INL&lt;/sub&gt;</td>
<td>0.3 × V&lt;sub&gt;DRIVE&lt;/sub&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current, I&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>±1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance, C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>3</td>
<td>3</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
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</table>

**LOGIC OUTPUTS**

<table>
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<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage, V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>V&lt;sub&gt;DRIVE&lt;/sub&gt; − 0.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Output Low Voltage, V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>0.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Floating-State Leakage Current</td>
<td>±1</td>
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<td>Floating-State Output Capacitance</td>
<td>5.5</td>
<td>5.5</td>
<td>pF</td>
<td></td>
<td></td>
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<tr>
<td>Output Coding</td>
<td>Straight binary</td>
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**CONVERSION RATE**

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<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Time</td>
<td>t&lt;sub&gt;2&lt;/sub&gt; + 15.5 × t&lt;sub&gt;SCLK&lt;/sub&gt;</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Track-and-Hold Acquisition Time&lt;sup&gt;2&lt;/sup&gt;</td>
<td>33</td>
<td>33</td>
<td>ns</td>
<td>Full-scale step input</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Throughput Rate</td>
<td>4.2</td>
<td>4.2</td>
<td>MSPS</td>
<td></td>
<td></td>
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</table>

**POWER REQUIREMENTS**

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<tr>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>2.25</td>
<td>2.75</td>
<td>2.25</td>
<td>2.75</td>
<td>V</td>
<td></td>
<td>Nominal V&lt;sub&gt;DD&lt;/sub&gt; = 2.5 V</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DRIVE&lt;/sub&gt;</td>
<td>2.25</td>
<td>3.6</td>
<td>2.25</td>
<td>3.6</td>
<td>V</td>
<td>Digital inputs = 0 V or V&lt;sub&gt;DRIVE&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I&lt;sub&gt;TOTAL&lt;/sub&gt;&lt;sup&gt;4&lt;/sup&gt;</td>
<td>14</td>
<td>20</td>
<td>14</td>
<td>20</td>
<td>mA</td>
<td>Normal Mode (Operational)</td>
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</tr>
<tr>
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<td>6</td>
<td>7.6</td>
<td>6</td>
<td>7.6</td>
<td>mA</td>
<td>Partial Power-Down Mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3.5</td>
<td>4.5</td>
<td>3.5</td>
<td>4.5</td>
<td>mA</td>
<td>Full Power-Down Mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>5</td>
<td>40</td>
<td>5</td>
<td>40</td>
<td>µW</td>
<td>Power Dissipation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normal Mode (Operational)</td>
<td>36</td>
<td>59</td>
<td>36</td>
<td>59</td>
<td>mW</td>
<td>Normal Mode (Operational)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Normal Mode (Static)</td>
<td>16</td>
<td>21</td>
<td>16</td>
<td>21</td>
<td>mW</td>
<td>Normal Mode (Static)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Partial Power-Down Mode</td>
<td>9.5</td>
<td>11.5</td>
<td>9.5</td>
<td>11.5</td>
<td>mW</td>
<td>Partial Power-Down Mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full Power-Down Mode</td>
<td>16</td>
<td>110</td>
<td>16</td>
<td>110</td>
<td>µW</td>
<td>Full Power-Down Mode</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

<sup>1</sup> Temperature ranges are as follows: AD7357Y: −40°C to +125°C, AD7357B: −40°C to +85°C, AD7357WY: −40°C to +125°C.

<sup>2</sup> See the Terminology section.

<sup>3</sup> The interface is functional with V<sub>DRIVE</sub> voltages down to 1.8 V. In this condition, the SCLK speed may need to be slowed down. See the access and hold times in the Timing Specifications section.

<sup>4</sup> I<sub>TOTAL</sub> is the total current flowing in V<sub>DD</sub> and V<sub>DRIVE</sub>. 

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TIMING SPECIFICATIONS

$V_{DD} = 2.5 \, V \pm 10\%, \, V_{\text{drive}} = 2.25 \, V \text{ to } 3.6 \, V, \text{ internal reference} = 2.048 \, V, \, T_A = T_{\text{MAX}} \text{ to } T_{\text{MIN}}^1$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit at $T_{\text{MIN}}, T_{\text{MAX}}$</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{SCLK}}$</td>
<td>500</td>
<td>kHz min</td>
<td></td>
</tr>
<tr>
<td></td>
<td>80</td>
<td>MHz max</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{CONVERT}}$</td>
<td>$t_2 + 15.5 \times t_{\text{SCLK}}$</td>
<td>ns min</td>
<td>$t_{\text{SCLK}} = 1/f_{\text{SCLK}}$</td>
</tr>
<tr>
<td>$t_{\text{QUIET}}$</td>
<td>5</td>
<td>ns min</td>
<td>Minimum time between end of serial read and next falling edge of $\overline{CS}$</td>
</tr>
<tr>
<td>$t_2$</td>
<td>5</td>
<td>ns min</td>
<td>$\overline{CS}$ to SCLK setup time</td>
</tr>
<tr>
<td>$t_2^2$</td>
<td>6</td>
<td>ns max</td>
<td>Delay from $\overline{CS}$ until SDATAA and SDATAa are three-state disabled</td>
</tr>
<tr>
<td>$t_{42}$</td>
<td>12.5</td>
<td>ns max</td>
<td>Data access time after SCLK falling edge</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>ns max</td>
<td>$1.8 , V \leq V_{\text{drive}} &lt; 2.25 , V$</td>
</tr>
<tr>
<td></td>
<td>9.5</td>
<td>ns max</td>
<td>$2.25 , V \leq V_{\text{drive}} &lt; 2.75 , V$</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>ns max</td>
<td>$2.75 , V \leq V_{\text{drive}} &lt; 3.3 , V$</td>
</tr>
<tr>
<td></td>
<td>3.5</td>
<td>ns max</td>
<td>$3.3 , V \leq V_{\text{drive}} \leq 3.6 , V$</td>
</tr>
<tr>
<td>$t_5$</td>
<td>5</td>
<td>ns min</td>
<td>SCLK low pulse width</td>
</tr>
<tr>
<td>$t_6$</td>
<td>5</td>
<td>ns min</td>
<td>SCLK high pulse width</td>
</tr>
<tr>
<td>$t_2^3$</td>
<td>3.5</td>
<td>ns min</td>
<td>SCLK to data valid hold time</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>ns min</td>
<td>$1.8 , V \leq V_{\text{drive}} &lt; 2.75 , V$</td>
</tr>
<tr>
<td></td>
<td>9.5</td>
<td>ns max</td>
<td>$2.75 , V \leq V_{\text{drive}} \leq 3.6 , V$</td>
</tr>
<tr>
<td>$t_8$</td>
<td>9.5</td>
<td>ns max</td>
<td>$\overline{CS}$ rising edge to SDATAA, SDATAa, high impedance</td>
</tr>
<tr>
<td>$t_9$</td>
<td>5</td>
<td>ns min</td>
<td>$\overline{CS}$ rising edge to falling edge pulse width</td>
</tr>
<tr>
<td>$t_{10}^2$</td>
<td>4.5</td>
<td>ns min</td>
<td>SCLK falling edge to SDATAA, SDATAa, high impedance</td>
</tr>
<tr>
<td></td>
<td>9.5</td>
<td>ns max</td>
<td>SCLK falling edge to SDATAA, SDATAa, high impedance</td>
</tr>
</tbody>
</table>

Latency | 1 conversion latency |

$^1$ Temperature ranges are as follows: AD7357Y: $-40^\circ\text{C to } +125^\circ\text{C}$, AD7357B: $-40^\circ\text{C to } +85^\circ\text{C}$, AD7357WY: $-40^\circ\text{C to } +125^\circ\text{C}$.

$^2$ Specified with a load capacitance of 10 pF on SDATAA and SDATAa.

$^3$ The time required for the output to cross 0.4 V or 2.4 V.
ABSOLUTE MAXIMUM RATINGS

Table 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ to AGND, DGND, REFGND</td>
<td>$-0.3,\text{V to } +3,\text{V}$</td>
</tr>
<tr>
<td>$V_{\text{DRIVE}}$ to AGND, DGND, REFGND</td>
<td>$-0.3,\text{V to } +5,\text{V}$</td>
</tr>
<tr>
<td>$V_{DD}$ to $V_{\text{DRIVE}}$</td>
<td>$-5,\text{V to } +3,\text{V}$</td>
</tr>
<tr>
<td>AGND to DGND to REFGND</td>
<td>$-0.3,\text{V to } +0.3,\text{V}$</td>
</tr>
<tr>
<td>Analog Input Voltages$^1$ to AGND</td>
<td>$-0.3,\text{V to } V_{DD} + 0.3,\text{V}$</td>
</tr>
<tr>
<td>Digital Input Voltages$^2$ to DGND</td>
<td>$-0.3,\text{V to } V_{\text{DRIVE}} + 0.3,\text{V}$</td>
</tr>
<tr>
<td>Digital Output Voltages$^3$ to DGND</td>
<td>$-0.3,\text{V to } V_{\text{DRIVE}} + 0.3,\text{V}$</td>
</tr>
<tr>
<td>Input Current to Any Pin Except Supplies$^4$</td>
<td>$\pm 10,\text{mA}$</td>
</tr>
</tbody>
</table>

Operating Temperature Range
- AD7357Y: $-40\,\text{°C to } +125\,\text{°C}$
- AD7357B: $-40\,\text{°C to } +85\,\text{°C}$
- AD7357WY: $-40\,\text{°C to } +125\,\text{°C}$

Storage Temperature Range $-65\,\text{°C to } +150\,\text{°C}$

Junction Temperature $150\,\text{°C}$

TSSOP Package
- $\theta_{JA}$ Thermal Impedance: $143\,\text{°C/W}$
- $\theta_{JC}$ Thermal Impedance: $45\,\text{°C/W}$

Lead Temperature, Soldering
- Reflow Temperature (10 sec to 30 sec): $255\,\text{°C}$
- ESD: $2\,\text{kV}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

1 Analog input voltages are $V_{\text{INA+}}, V_{\text{INA−}}, V_{\text{INB+}}, V_{\text{INB−}}, V_{\text{REFA}},$ and $V_{\text{REFB}}$.
2 Digital input voltages are $\text{CS}$ and $\text{SCLK}$.
3 Digital output voltages are $\text{SDATAA}$ and $\text{SDATAB}$.
4 Transient currents of up to $100\,\text{mA}$ do not cause SCR latch-up.
## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

![AD7357 Pin Diagram](top_view_not_to_scale.png)

Figure 2. Pin Configuration

### Table 5. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>VINA+, VINA-</td>
<td>Analog Inputs of ADC A. These analog inputs form a fully differential pair.</td>
</tr>
<tr>
<td>3, 6</td>
<td>REF_A, REF_B</td>
<td>Reference Decoupling Capacitor Pins. Decoupling capacitors are connected between these pins and the REFGND pin to decouple the reference buffer for each respective ADC. It is recommended to decouple each reference pin with a 10 µF capacitor. Provided that the output is buffered, the on-chip reference can be taken from these pins and applied externally to the rest of the system. The nominal internal reference voltage is 2.048 V and appears at these pins. These pins can also be overdriven by an external reference. The input voltage range for the external reference is 2.048 V + 100 mV to VDD.</td>
</tr>
<tr>
<td>4</td>
<td>REFGND</td>
<td>Reference Ground. This is the ground reference point for the reference circuitry on the AD7357. Any external reference signal should be referred to this REFGND voltage. Decoupling capacitors must be placed between this pin and the REF_A and REF_B pins.</td>
</tr>
<tr>
<td>5, 11</td>
<td>AGND</td>
<td>Analog Ground. This is the ground reference point for all analog circuitry on the AD7357. All analog input signals should be referred to this AGND voltage. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.</td>
</tr>
<tr>
<td>7, 8</td>
<td>VINB-, VINB+</td>
<td>Analog Inputs of ADC B. These analog inputs form a fully differential pair.</td>
</tr>
<tr>
<td>9</td>
<td>VDD</td>
<td>Power Supply Input. The VDD range for the AD7357 is 2.5 V ± 10%. The supply should be decoupled to AGND with a 0.1 µF capacitor and a 10 µF tantalum capacitor.</td>
</tr>
<tr>
<td>10</td>
<td>CS</td>
<td>Chip Select. Active low, logic input. This input provides the dual function of initiating conversions on the AD7357 and framing the serial data transfer.</td>
</tr>
<tr>
<td>12</td>
<td>DGND</td>
<td>Digital Ground. This is the ground reference point for all digital circuitry on the AD7357. This pin should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.</td>
</tr>
<tr>
<td>13, 14</td>
<td>SDATA_B, SDATA_A</td>
<td>Serial Data Outputs. The data output is supplied to each pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. 16 SCLK falling edges are required to access the 14 bits of data from the AD7357. The data simultaneously appears on both data output pins from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros, followed by the 14 bits of conversion data. The data is provided MSB first. If CS is held low for 18 SCLK cycles rather than 16, then two trailing zeros appear after the 14 bits of data. If CS is held low for an additional 18 SCLK cycles on either SDATA_A or SDATA_B, the data from the other ADC follows on the SDATA pins. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either SDATA_A or SDATA_B.</td>
</tr>
<tr>
<td>15</td>
<td>SCLK</td>
<td>Serial Clock. Logic input. A serial clock input provides the SCLK for accessing the data from the AD7357. This clock is also used as the clock source for the conversion process.</td>
</tr>
<tr>
<td>16</td>
<td>VDRIVE</td>
<td>Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different to that at VDD.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

![Figure 3. Typical FFT](image1)

-140 -120 -100 -80 -60 -40 -20 0 250 500 750 1000 1250 1500 1750 2000

FREQUENCY (kHz)  dB

0 250 500 750 1000 1250 1500 1750 2000

Figure 3. Typical FFT

![Figure 4. Typical DNL](image2)

-1.0 -0.8 -0.6 -0.4 -0.2 0 0.2 0.4 0.6 0.8 1.0

CODE 07757-004

Figure 4. Typical DNL

![Figure 5. Typical INL](image3)

-1.5 -1.0 -0.5 0 0.5 1.0 1.5

CODE 07757-005

Figure 5. Typical INL

![Figure 6. Histogram of Codes](image4)

0 5 10 15 20 25

SUPPLY RIPPLE FREQUENCY (MHz)  PSRR (dB)

0 5 10 15 20 25

Figure 8. PSRR vs. Supply Ripple with No Supply Decoupling

0 10 20 30 40 50

ANALOG INPUT FREQUENCY (MHz)  SNR (dB)

0 10 20 30 40 50

Figure 7. SNR vs. Analog Input Frequency

0 5 10 15 20 25

SUPPLY RIPPLE FREQUENCY (MHz)  PSRR (dB)

0 5 10 15 20 25

Figure 8. PSRR vs. Supply Ripple with No Supply Decoupling

0 20000 15000 10000 5000 0

NUMBER OF OCCURRENCES

0 250 500 750 1000 1250 1500 1750 2000

FREQUENCY (kHz)  dB

0 250 500 750 1000 1250 1500 1750 2000

Figure 3. Typical FFT

16,384 POINT FFT

fSAMPLE = 4.2MSPS

fIN = 1MHz

SINAD = 76.8dB

THD = –84.5dB

Figure 3. Typical FFT

1.0 0.8 0.6 0.4 0.2 0.0

SNR (dB)

Figure 7. SNR vs. Analog Input Frequency

1.5 1.0 0.5 0.0

INL ERROR (LSB)

Figure 5. Typical INL

0 5 10 15 20 25

SUPPLY RIPPLE FREQUENCY (MHz)  PSRR (dB)

0 5 10 15 20 25

Figure 8. PSRR vs. Supply Ripple with No Supply Decoupling

0 4000 8000 12,000 16,000

DNL ERROR (LSB)

Figure 4. Typical DNL

0 4000 8000 12,000 16,000

INL ERROR (LSB)

Figure 5. Typical INL

0 4000 8000 12,000 16,000

INL ERROR (LSB)

Figure 5. Typical INL

32 HITS

8188 8189 8190 8191 8192 8193 8194 8195

CODE

Figure 6. Histogram of Codes

32 HITS

8188 8189 8190 8191 8192 8193 8194 8195

CODE

Figure 6. Histogram of Codes
Figure 9. $V_{REF}$ vs. Reference Output Current Drive

Figure 10. Linearity Error vs. SCLK Frequency

Figure 11. Linearity Error vs. External $V_{REF}$

Figure 12. Access Time vs. $V_{DRIVE}$

Figure 13. Hold Time vs. $V_{DRIVE}$
TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (1 LSB below the first code transition) and full scale (1 LSB above the last code transition).

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Negative Full-Scale Error
Negative full-scale error is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal (that is, \(-V_{\text{REF}} + 0.5 \text{ LSB}\)) after the midscale error has been adjusted out.

Negative Full-Scale Error Match
Negative full-scale error match is the difference in negative full-scale error between the two ADCs.

Midscale Error
Midscale error is the deviation of the midscale code transition (011 ... 111) to (100 ... 000) from the ideal (that is, 0 V).

Midscale Error Match
Midscale error match is the difference in midscale error between the two ADCs.

Positive Full-Scale Error
Positive full-scale error is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, \(V_{\text{REF}} - 1.5 \text{ LSB}\)) after the midscale error has been adjusted out.

Positive Full-Scale Error Match
Positive full-scale error match is the difference in positive full-scale error between the two ADCs.

ADC-to-ADC Isolation
ADC-to-ADC isolation is a measure of the level of crosstalk between ADC A and ADC B. It is measured by applying a full-scale 1 MHz sine wave signal to one of the two ADCs and applying a full-scale signal of variable frequency to the other ADC. The ADC-to-ADC isolation is defined as the ratio of the power of the 1 MHz signal on the converted ADC to the power of the noise signal on the other ADC that appears in the FFT. The noise frequency on the unselected channel varies from 100 kHz to 2.5 MHz.

Power Supply Rejection Ratio (PSRR)
PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, \(f\), to the power of a 100 mV p-p sine wave applied to the common-mode voltage of \(V_{\text{IN+}} \) and \(V_{\text{IN-}}\) of frequency, \(f_s\), as follows:

\[
\text{PSRR (dB)} = 10 \log(\frac{P_f}{P_{fs}})
\]

where:
- \(P_f\) is the power at frequency, \(f\), in the ADC output.
- \(P_{fs}\) is the power at frequency, \(f_s\), in the ADC output.

Common-Mode Rejection Ratio (CMRR)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, \(f\), to the power of a 100 mV p-p sine wave applied to the common-mode voltage of \(V_{\text{IN+}} \) and \(V_{\text{IN-}}\) of frequency, \(f_s\), as follows:

\[
\text{CMRR (dB)} = 10 \log(\frac{P_f}{P_{fs}})
\]

where:
- \(P_f\) is the power at frequency, \(f\), in the ADC output.
- \(P_{fs}\) is the power at frequency, \(f_s\), in the ADC output.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of a conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of conversion.

Signal-to-(Noise + Distortion) Ratio (SINAD)
SINAD is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency (\(f_s/2\), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical SINAD for an ideal N-bit converter with a sine wave input is given by

\[
\text{SINAD (dB)} = (6.02 N + 1.76) \text{ dB}
\]

Thus, for a 12-bit converter, SINAD is 74 dB and for a 14-bit converter, SINAD is 86 dB.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7357, it is defined as

\[
\text{THD (dB)} = -20 \log \left( \frac{\sqrt{V_1^2 + V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1} \right)
\]

where:
- \(V_1\) is the rms amplitude of the fundamental.
- \(V_2, V_3, V_4, V_5, \) and \(V_6\) are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to \(f_s/2\) and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.
Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, \( f_a \) and \( f_b \), any active device with nonlinearities creates distortion products at sum and difference frequencies of \( m f_a \pm n f_b \) where \( m, n = 0, 1, 2, 3, \) and so on. Intermodulation distortion terms are those for which neither \( m \) nor \( n \) are equal to zero. For example, the second-order terms include \((f_a + f_b)\) and \((f_a - f_b)\), while the third-order terms include \((2f_a + f_b)\), \((2f_a - f_b)\), \((f_a + 2f_b)\), and \((f_a - 2f_b)\).

The AD7357 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification (see Table 2), where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

Thermal Hysteresis
Thermal hysteresis is defined as the absolute maximum change of the reference output voltage after the device is cycled through temperature from either

\[
T_{\text{HYS}+} = 25^\circ\text{C} \text{ to } T_{\text{MAX}} \text{ to } 25^\circ\text{C} \\
T_{\text{HYS}–} = 25^\circ\text{C} \text{ to } T_{\text{MIN}} \text{ to } 25^\circ\text{C}
\]

It is expressed in ppm using the following equation:

\[
V_{\text{HYS}} \text{ (ppm)} = \left| \frac{V_{\text{REF}} (25^\circ\text{C}) - V_{\text{REF}} (T_{\text{HYS}})}{V_{\text{REF}} (25^\circ\text{C})} \right| \times 10^6
\]

where:

- \( V_{\text{REF}} (25^\circ\text{C}) \) is \( V_{\text{REF}} \) at 25\(^\circ\text{C}\).
- \( V_{\text{REF}} (T_{\text{HYS}}) \) is the maximum change of \( V_{\text{REF}} \) at \( T_{\text{HYS}+} \) or \( T_{\text{HYS}–} \).
THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7357 is a high speed, dual, 14-bit, single-supply, successive approximation analog-to-digital converter. The part operates from a 2.5 V power supply and features throughput rates up to 4.2 MSPS.

The AD7357 contains two on-chip differential track-and-hold amplifiers, two successive approximation analog-to-digital converters, and a serial interface with two separate data output pins. The part is housed in a 16-lead TSSOP package, offering the user considerable space-saving advantages over alternative solutions.

The serial clock input accesses data from the part, but also provides the clock source for each successive approximation ADC. The AD7357 has an on-chip 2.048 V reference. If an external reference is desired the internal reference can be overdriven with a reference value ranging from (2.048 V + 100 mV) to VDD. If the internal reference is to be used elsewhere in the system, the reference output needs to be buffered first. The differential analog input range for the AD7357 is VCM ± VREF/2.

The AD7357 features power-down options to allow power saving between conversions. The power-down feature is implemented via the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7357 has two successive approximation ADCs, each based around two capacitive DACs. Figure 14 and Figure 15 show simplified schematics of one of these ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, a SAR, and two capacitive DACs. In Figure 14 (the acquisition phase), SW3 is closed, SW1 and SW2 are in Position A, the comparator is held in a balanced condition, and the sampling capacitor arrays may acquire the differential signal on the input.

When the ADC starts a conversion (see Figure 15), SW3 opens and SW1 and SW2 move to Position B, causing the comparator to become unbalanced. Both inputs are disconnected when the conversion begins. The control logic and charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the VIN+ and VIN− pins must be matched; otherwise, the two inputs have different settling times, resulting in errors.

ANALOG INPUT STRUCTURE

Figure 16 shows the equivalent circuit of the analog input structure of the AD7357. The four diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

The C1 capacitors in Figure 16 are typically 8 pF and can primarily be attributed to pin capacitance. The R1 resistors are lumped components made up of the on resistance of the switches. The value of these resistors is typically about 30 Ω. The C2 capacitors are the ADC’s sampling capacitors with a capacitance of 32 pF typically.
For ac applications, it is recommended to remove high frequency components from the analog input signal by the use of an RC low-pass filter on the analog input pins. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and may necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated. The THD increases as the source impedance increases and performance degrades. Figure 17 shows a graph of the THD vs. the analog input signal frequency for various source impedances.

The amplitude of the differential signal is the difference between the signals applied to the VIN+ and VIN− pins in each differential pair (VIN+ − VIN−). VIN+ and VIN− should be simultaneously driven by two signals each of amplitude VREF that are 180° out of phase. This amplitude of the differential signal is, therefore, −VREF to +VREF peak-to-peak regardless of the common mode (CM).

CM is the average of the two signals and is, therefore, the voltage on which the two inputs are centered.

\[ CM = \frac{(VIN+ + VIN−)}{2} \]

This results in the span of each input being CM ± VREF/2. This voltage has to be set up externally. When setting up the CM, ensure that that VIN+ and VIN− remain within GND/VDD. When a conversion takes place, CM is rejected, resulting in a virtually noise free signal of amplitude −VREF to +VREF corresponding to the digital codes of 0 to 16,383.

**ANALOG INPUTS**

Differential signals have some benefits over single-ended signals, including noise immunity based on the device’s common-mode rejection and improvements in distortion performance. Figure 19 defines the fully differential input of the AD7357.

The amplitude of the differential signal is the difference between the signals applied to the VIN+ and VIN− pins in each differential pair (VIN+ ~ VIN−). VIN+ and VIN− should be simultaneously driven by two signals each of amplitude VREF that are 180° out of phase. This amplitude of the differential signal is, therefore, −VREF to +VREF peak-to-peak regardless of the common mode (CM).

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**DRIVING DIFFERENTIAL INPUTS**

Differential operation requires VIN+ and VIN− to be driven simultaneously with two equal signals that are 180° out of phase. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion.

**Differential Amplifier**

An ideal method of applying differential drive to the AD7357 is to use a differential amplifier such as the AD8138. This part can be used as a single-ended-to-differential amplifier or as a differential-to-differential amplifier. The AD8138 also provides common-mode level shifting. Figure 20 shows how the AD8138 can be used as a single-ended-to-differential amplifier. The positive and negative outputs of the AD8138 are connected to the respective inputs on the ADC via a pair of series resistors to minimize the effects of switched capacitance on the front end of the ADC. The architecture of the AD8138 results in outputs that are very highly balanced over a wide frequency range without requiring tightly matched external components.
If the analog inputs source being used has zero impedance, all four resistors (R₁, R₂, R₃, and R₄) should be the same. If the source has a 50 Ω impedance and a 50 Ω termination, for example, the value of R₂ should be increased by 25 Ω to balance this parallel impedance on the input and thus ensure that both the positive and negative analog inputs have the same gain. The outputs of the amplifier are perfectly matched balanced differential outputs of identical amplitude and are exactly 180° out of phase.

Figure 20. Using the AD8138 as a Single-Ended-to-Differential Amplifier

Op Amp Pair

An op amp pair can be used to directly couple a differential signal to one of the analog input pairs of the AD7357. The circuit configurations shown in Figure 21 and Figure 22 show how an op amp pair can be used to convert a single-ended signal into a differential signal for a bipolar and unipolar input signal, respectively. The voltage applied to Point A sets up the common-mode voltage. In both diagrams, Point A is connected in some way to the reference. The AD8022 is a suitable dual op amp that can be used in this configuration to provide differential drive to the AD7357.

Figure 21. Dual Op Amp Circuit to Convert a Single-Ended Unipolar Signal into a Differential Signal

VOLTAGE REFERENCE

The AD7357 allows the choice of a very low temperature drift internal voltage reference or an external reference. The internal 2.048 V reference of the AD7357 provides excellent performance and can be used in almost all applications. When the internal reference is used, the reference voltage is present on the REFA and REFB pins. These pins should be decoupled to REFGND with 10 μF capacitors. The internal reference voltage can be used elsewhere in the system, provided it is buffered externally.

The REFA and REFB pins can also be overdriven with an external voltage reference if desired. The applied reference voltage can range from 2.048 V + 100 mV to VDD. A common choice would be to use an external 2.5 V reference such as the ADR441 or ADR431.

ADC TRANSFER FUNCTION

The output coding for the AD7357 is straight binary. The designed code transitions occur at successive LSB values (such as, 1 LSB, 2 LSBs). The LSB size is (2 × VREF)/16,384. The ideal transfer characteristic of the AD7357 is shown in Figure 23.
MODES OF OPERATION

The AD7357 mode of operation is selected by controlling the logic state of the CS signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. After a conversion has been initiated, the point at which CS is pulled high determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, CS can control whether the device returns to normal operation or remains in a power-down mode. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for the differing application requirements.

NORMAL MODE

Normal mode is intended for applications needing the fastest throughput rates. The user does not have to worry about any power-up times because the AD7357 remains fully powered at all times. Figure 24 shows the general diagram of the operation of the AD7357 in this mode.

When a data transfer is complete and SDATAA and SDATAB have returned to three-state, another conversion can be initiated after the quiet time, \( t_{\text{QUIET}} \), has elapsed by bringing CS low again (assuming the required acquisition time has been allowed).

PARTIAL POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions can be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7357 is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffers.

To enter partial power-down mode, the conversion process must be interrupted by bringing CS high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 25. When CS is brought high in this window of SCLKs, the part enters partial power-down mode, the conversion that was initiated by the falling edge of CS is terminated, and SDATAA and SDATAB go back into three-state. If CS is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the CS line.

To exit this mode of operation and to power up the AD7357 again, perform a dummy conversion. On the falling of CS, the device begins to power up and continues to power up as long as CS is held low until after the falling edge of the 10th SCLK. The device is fully powered up after approximately 200 ns elapses (or one full conversion), and valid data results from the next conversion, as shown in Figure 26. If CS is brought high before the second SCLK falling edge, the AD7357 again goes into partial power-down mode. This avoids accidental power-up due to glitches on the CS line. Although the device may begin to power up on the falling edge of CS, it powers down again on the rising edge of CS. If the AD7357 is already in partial power-down mode and CS is brought high between the second and 10th falling edges of SCLK, the device enters full power-down mode.
**FULL POWER-DOWN MODE**

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from a partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and, thus, power-down. When the AD7357 is in full power-down, all analog circuitry is powered down. Full power-down is entered in a way that is similar to partial power-down, except that the timing sequence shown in Figure 25 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing CS high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK. The device enters partial power-down mode at this point.

To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure 27. When CS has been brought high in this window of SCLKs, the part completely powers down.

Note that it is not necessary to complete the 16 SCLKs once CS has been brought high to enter a power-down mode.

To exit full power-down mode and power up the AD7357, perform a dummy conversion, such as powering up from partial power-down. On the falling edge of CS, the device begins to power up, as long as CS is held low until after the falling edge of the 10th SCLK. The required power-up time must elapse before a conversion can be initiated, as shown in Figure 28.
POWER-UP TIMES
The AD7357 has two power-down modes: partial power-down and full power-down. There are described in detail in the Partial Power-Down Mode and Full Power-Down Mode sections. This section deals with the power-up time required when coming out of either of these modes. It should be noted that the power-up times apply with the recommended decoupling capacitors in place on the REFa and REFb pins.

To power up from partial power-down mode, one dummy cycle is required. The device is fully powered up after approximately 200 ns from the falling edge of CS has elapsed. Once the partial power-up time has elapsed, the ADC is fully powered up and the input signal is acquired properly. The quiet time, tQUIET, must still be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of CS.

To power up from full power-down, approximately 6 ms should be allowed from the falling edge of CS, shown in Figure 28 as tPOWER-UP.

Note that during power-up from partial power-down mode, the track-and-hold, which is in hold mode while the part is powered down, returns to track mode after the first SCLK edge that the part receives after the falling edge of CS.

When power supplies are first applied to the AD7357, the ADC can power up in either of the power-down modes or in normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if the part is to be kept in partial power-down mode immediately after the supplies are applied, then two dummy cycles must be initiated. The first dummy cycle must hold CS low until after the 10th SCLK falling edge; in the second cycle, CS must be brought high between the second and 10th SCLK falling edges (see Figure 25).

Alternatively, if the part is to be placed into full power-down mode when the supplies are applied, three dummy cycles must be initiated. The first dummy cycle must hold CS low until after the 10th SCLK falling edge; the second and third dummy cycles place the part into full power-down mode (see Figure 27 and the Modes of Operation section).

POWER vs. THROUGHPUT RATE
The power consumption of the AD7357 varies with the throughput rate. When using very slow throughput rates and as fast an SCLK frequency as possible, the various power-down options can be used to make significant power savings. However, the AD7357 quiescent current is low enough that even without using the power-down options, there is a noticeable variation in power consumption with sampling rate. This is true whether a fixed SCLK value is used or if it is scaled with the sampling rate. Figure 29 shows a plot of power vs. throughput rate when operating in normal mode for a fixed maximum SCLK frequency and an SCLK frequency that scales with the sampling rate. The internal reference was used for Figure 29.

![Figure 29. Power vs. Throughput Rate](image-url)
SERIAL INTERFACE

Figure 30 shows the detailed timing diagram for serial interfacing to the AD7357. The serial clock provides the conversion clock and controls the transfer of information from the AD7357 during conversion. There is a single sample delay in the result that is clocked out from the AD7357.

The \( \text{CS} \) signal initiates the data transfer and conversion process. The falling edge of \( \text{CS} \) puts the track-and-hold into hold mode at which point the analog input is sampled and the bus is taken out of three-state. The conversion is also initiated at this point and requires a minimum of 16 SCLKs to complete. When 16 SCLK falling edges have elapsed, the track-and-hold goes back into track on the next SCLK rising edge, as shown in Figure 30 at Point B. On the rising edge of \( \text{CS} \), the conversion is terminated and SDATA\(_A\) and SDATA\(_B\) go back into three-state. If \( \text{CS} \) is not brought high but is, instead, held low for an additional 16 SCLK cycles on SDATA\(_A\), the data from the conversion on ADC B is output on SDATA\(_A\).

Likewise, if \( \overline{\text{CS}} \) is held low for an additional 16 SCLK cycles on SDATA\(_A\), the data from the conversion on ADC A is output on SDATA\(_B\) (see Figure 31). In this case, the SDATA line in use goes back into three-state on the 32\(^{nd}\) SCLK falling edge or the rising edge of \( \overline{\text{CS}} \), whichever occurs first.

A minimum of 16 serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the AD7357. Note that the data that is accessed on SDATA\(_A\) and SDATA\(_B\) is the result of the previous conversion. \( \overline{\text{CS}} \) going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second leading zero. Thus, the first falling clock edge on the serial clock has the leading zero provided and also clocks out the second leading zero. The 14-bit result then follows with the final bit in the data transfer valid on the 16\(^{th}\) falling edge, having been clocked out on the previous (15\(^{th}\)) falling edge. In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge depending on the SCLK frequency. The first rising edge of SCLK after the \( \overline{\text{CS}} \) falling edge has the second leading zero provided, and the 15\(^{th}\) rising SCLK edge has DB0 provided.

![Figure 30. Serial Interface Timing Diagram](image)

![Figure 31. Reading Data from Both ADCs on One SDATA Line with 32 SCLKs](image)
APPLICATION HINTS

GROUNDING AND LAYOUT

The analog and digital supplies to the AD7357 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The printed circuit board (PCB) that houses the AD7357 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This design facilitates the use of ground planes that can be easily separated.

To provide optimum shielding for ground planes, a minimum etch technique is generally best. The two AGND pins of the AD7357 should be sunk in the AGND plane. Digital and analog ground plans should be joined in only one place. If the AD7357 is in a system where multiple devices require an AGND and DGND connection, the connection should still be made at one point only. A star ground point should be established as close as possible to the ground pins on the AD7357.

Avoid running digital lines under the device because this couples noise onto the die. The analog ground planes should be allowed to run under the AD7357 to avoid noise coupling. The power supply lines to the AD7357 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

To avoid radiating noise to other sections of the board, fast switching signals such as clocks should be shielded with digital ground, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. To reduce the effects of feedthrough within the board, traces on opposite sides of the board should run at right angles to each other. A microstrip technique is the best method, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is important; all supplies should be decoupled with 10 μF tantalum capacitors in parallel with 0.1 μF capacitors to GND. To achieve the best results from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1 μF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types or surface-mount types. These low ESR and ESI capacitors provide a low impedance path to ground at high frequencies to handle transient currents due to logic switching.

EVALUATING THE AD7357 PERFORMANCE

The recommended layout for the AD7357 is outlined in evaluation board documentation. The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the converter evaluation and development board (CED). The CED can be used in conjunction with the AD7357 evaluation board (as well as many other evaluation boards ending in the ED designator from Analog Devices, Inc.) to demonstrate/evaluate the ac and dc performance of the AD7357.

The software allows the user to perform ac (fast Fourier transform) and dc (linearity) tests on the AD7357. The software and documentation are on a CD that is shipped with the evaluation board.
OUTLINE DIMENSIONS

![Diagram of 16-Lead Thin Shrink Small Outline Package (TSSOP) RU-16]

Dimensions shown in millimeters

Figure 32. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

ORDERING GUIDE

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<td>EVAL-CED1Z</td>
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</tbody>
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1 Z = RoHS Compliant Part.
2 W = Qualified for Automotive Applications
3 The EVAL-AD7357EDZ can be used as a standalone evaluation board or in conjunction with the EVAL-CED1Z board for evaluation/demonstration purposes.
4 The EVAL-CED1Z is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the ED designator.

AUTOMOTIVE PRODUCTS

The AD7357W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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