MP2229

High Efficiency 21V, 6A Synchronous Step-Down Converter with External Sync, Low-Power Mode, and External Soft-Start

DESCRIPTION

The MP2229 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution to achieve a 6A continuous output current over a wide input-supply range with excellent load and line regulation. The MP2229 has synchronous-mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include over-current protection (OCP) and thermal shutdown (TSD).

The MP2229 requires a minimal number of readily available, standard, external components and is available in a space-saving 3mm x 3mm 14-pin QFN package.

FEATURES

- Wide 4.5V to 21V Operating Input Range
- 6A Output Current
- Low 40mΩ/18mΩ $R_{DS(ON)}$ of Internal Power MOSFETs
- Programmable Switching Frequency
- Frequency SYNC from 300KHz to 2MHz External Clock
- Low-Power Mode Selectable by an External Signal
- External Soft-Start
- Pre-Bias Start-Up
- OCP with Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.6V
- Available in a QFN-14 (3mmx3mm) Package

APPLICATIONS

- DSL Modems
- Cable Modems
- Set -Top Boxes
- Telecom
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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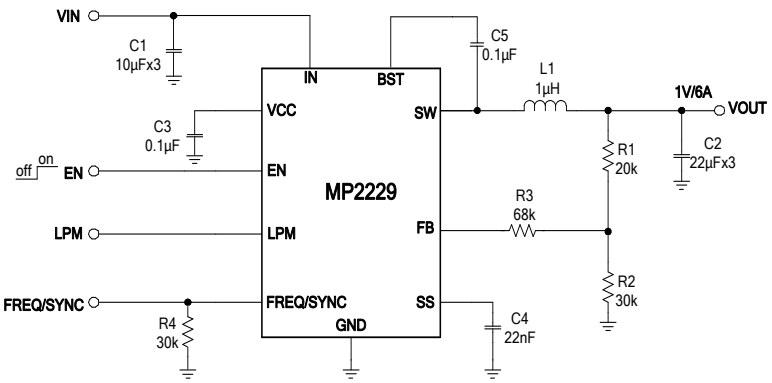
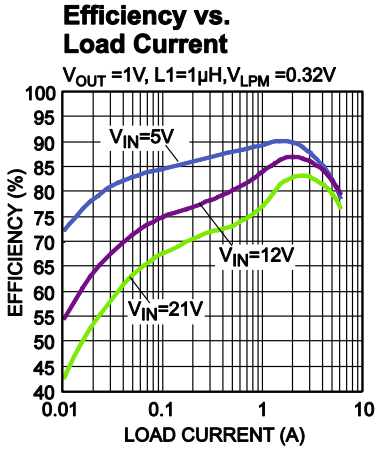
TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number	Package	Top Marking
MP2229GQ*	QFN-14 (3mm×3mm)	*See Below*

* For Tape & Reel, add suffix –Z (eg. MP2229GQ–Z);

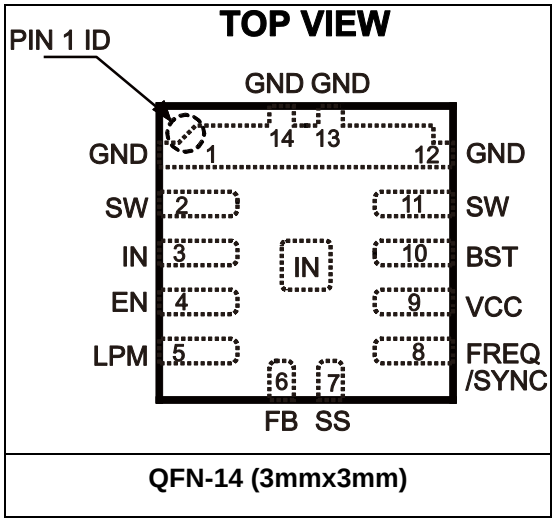
TOP MARKING

AGQY

LLL

AGQ: product code of MP2229GQ;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



QFN-14 (3mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to 24V
V_{SW} .....
-0.3V (-5V for <10ns) to 24V (28V for <10ns)
V_{BST} .....V_{SW} + 5.5V
All Other Pins.....-0.3V to 5.5V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
.....2.1W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature……-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN}..... 4.5V to 21V
Output Voltage V_{OUT}..... 0.6V to V_{IN} x D_{MAX}
Operating Junction Temp. (T_J) -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}
QFN-14 (3mmx3mm)	60	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Please refer to the “Enable Control” section on page 12 for the absolute maximum rating of EN.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C to +125°C(6), typical value is tested at T_J=+25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_S	V_{EN} = 0V,T_J=25°C		8.5	12	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.7V		400	500	μA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		40		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC}=5V		18		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 12V, T_J=25°C			1	μA
Current Limit(7)	I_{LIMIT}	Duty=40%	7.5	10.5		A
Oscillator Frequency	f_{SW}	R_{SET}=30k	380	500	610	kHz
		R_{SET}=51k	200	300	380	kHz
		R_{SET}=6.7k	1400	1800	2100	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 500mV	90	95		%
Minimum On Time(8)	T_{ON}			50		ns
Sync Frequency Range	f_{SYNC}		0.3		2	MHz
Foldback Frequency	f_{FOLD}	V_{FB} = 100mV		0.5		f_{SW}
Feedback Voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J=-40°C to +125°C	591	600	609	mV
Feedback Current	I_{FB}	V_{FB} = 650mV			50	nA
EN Falling Threshold	$V_{EN-Falling}$		0.98	1.2	1.34	V
EN Rising Threshold	$V_{EN-Rising}$		1.28	1.46	1.65	V
EN Pull-Up Current	I_{EN}		1	2.3	3.6	μA
V_{IN} Under-Voltage Lockout Threshold Rising	$INUV_{Vth}$		3.85	4.1	4.35	V
V_{IN} Under-Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			600		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		1		%
Soft-Start Current	I_{SS}		7	10	13	μA
Thermal Shutdown(8)	T_{SD}			150		°C
Thermal Shutdown Hysteresis(8)	T_{SD-HYS}			30		°C

Note:
6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.
8) Guaranteed by design.

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PIN FUNCTIONS

Package Pin #	Name	Description
1, 12, 13, 14	GND	Ground. Connect GND pins with larger copper areas to the negative terminals of the input and output capacitors.
2, 11	SW	Switch Output. Use wide PCB traces to make the connection.
3, Exposed Pad	IN	Supply Voltage Input. The MP2229 operates from a 4.5V to 21V input rail. Requires a low ESR and a low-inductance capacitor to decouple the input rail. Place the input capacitor very close to IN and connect it with wide PCB traces and multiple vias.
4	EN	Enable. EN high enables the MP2229. EN sources 2.3μA. Float EN to enable the MP2229 automatically.
5	LPM	Low-Power Mode Input. An active-high signal enables low-power mode operation. Connect LPM to GND to disable the converter and make the converter operate constantly in CCM.
6	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage.
7	SS	Soft-Start. Connect an external capacitor to program the soft-start time for the switch-mode regulator.
8	FREQ/ SYNC	Switching Frequency Program Input. Connect a resistor from FREQ/SYNC to GND to set the switching frequency. Also, FREQ/SYNC serves as a frequency-synchronous clock input.
9	VCC	Internal Bias Supply. Internal 5V LDO output. Decouple with 0.1μF capacitor. The decouple capacitor must be close enough to VCC to increase noise immunity.
10	BST	Bootstrap. Requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver. A 10Ω resistor placed between SW and the BST cap is recommended strongly to reduce the SW spike voltage.

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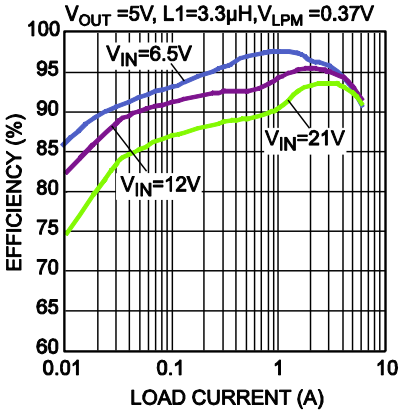
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are captured from the evaluation board discussed in the Design Example section. V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, F_S=500kHz, T_A = +25°C, unless otherwise noted.

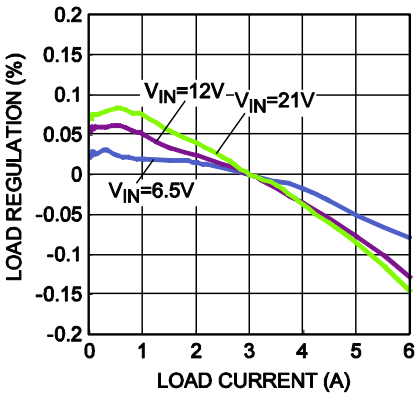
Efficiency vs. Load Current

V_{OUT} =5V, L1=3.3µH,V_{LPM} =0.37V



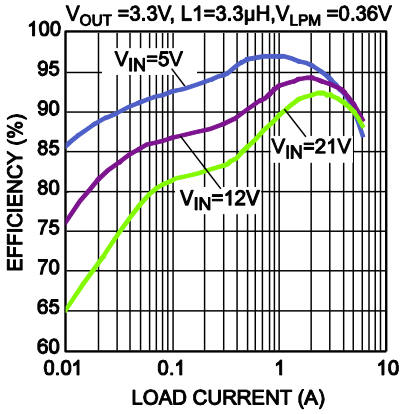
Load Regulation

V_{OUT} =5V, L1=3.3µH,V_{LPM} =0.37V



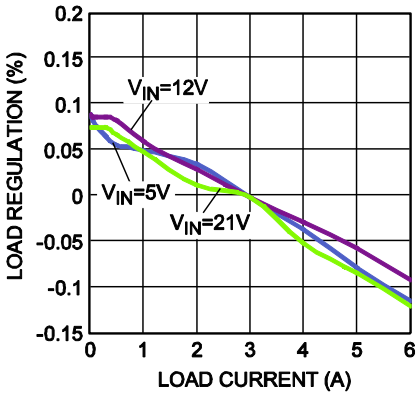
Efficiency vs. Load Current

V_{OUT} =3.3V, L1=3.3µH,V_{LPM} =0.36V



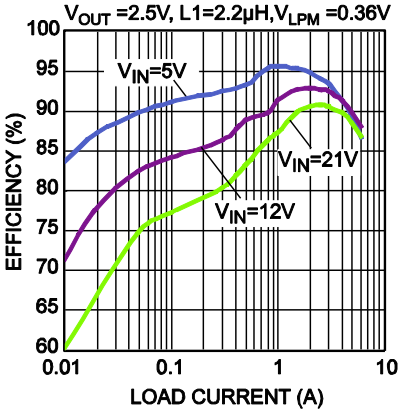
Load Regulation

V_{OUT} =3.3V, L1=3.3µH,V_{LPM} =0.36V



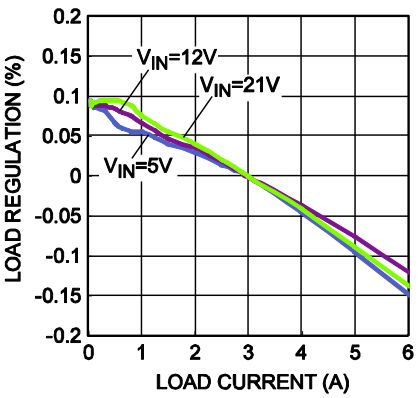
Efficiency vs. Load Current

V_{OUT} =2.5V, L1=2.2µH,V_{LPM} =0.36V



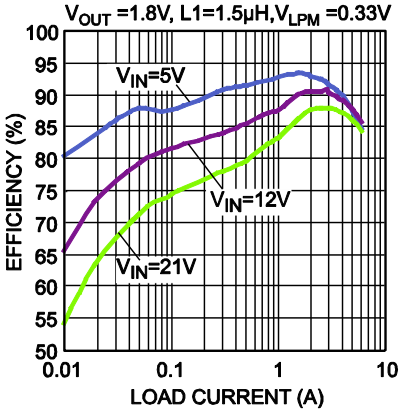
Load Regulation

V_{OUT} =2.5V, L1=2.2µH,V_{LPM} =0.36V



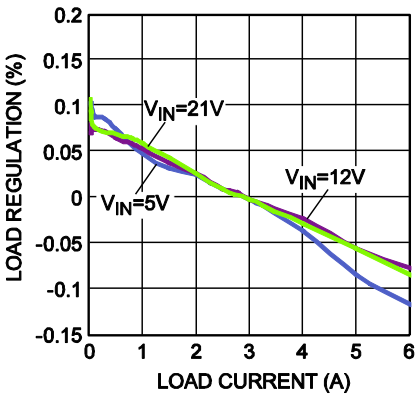
Efficiency vs. Load Current

V_{OUT} =1.8V, L1=1.5µH,V_{LPM} =0.33V



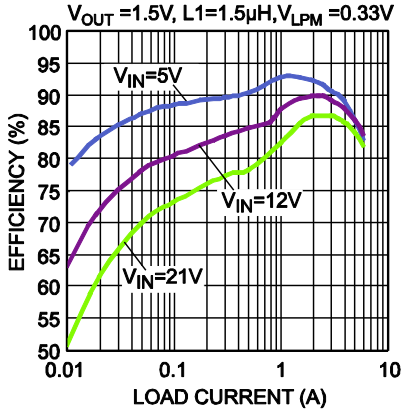
Load Regulation

V_{OUT} =1.8V, L1=1.5µH,V_{LPM} =0.33V



Efficiency vs. Load Current

V_{OUT} =1.5V, L1=1.5µH,V_{LPM} =0.33V



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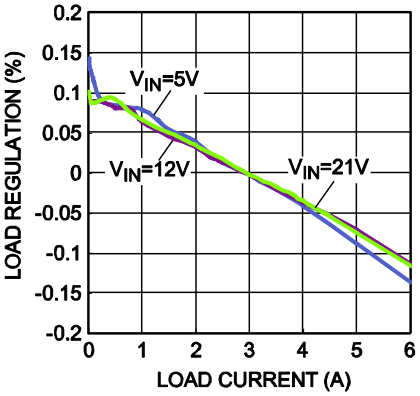
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section. V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, F_S=500kHz, T_A = +25°C, unless otherwise noted.

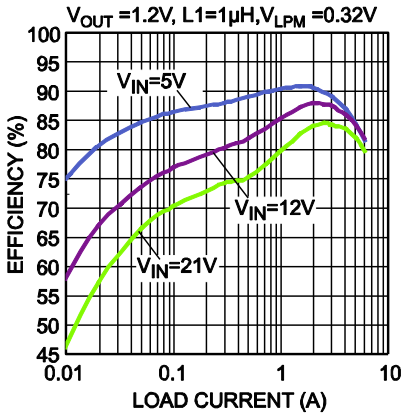
Load Regulation

V_{OUT} =1.5V, L1=1.5µH,V_{LPM} =0.33V



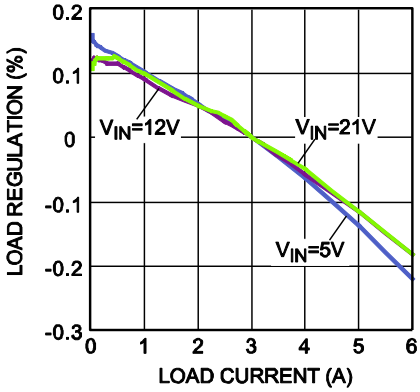
Efficiency vs. Load Current

V_{OUT} =1.2V, L1=1µH,V_{LPM} =0.32V



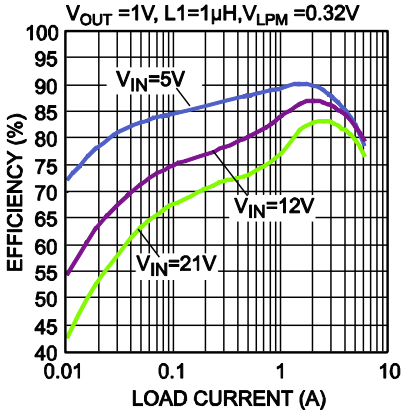
Load Regulation

V_{OUT} =1.2V, L1=1µH,V_{LPM} =0.32V



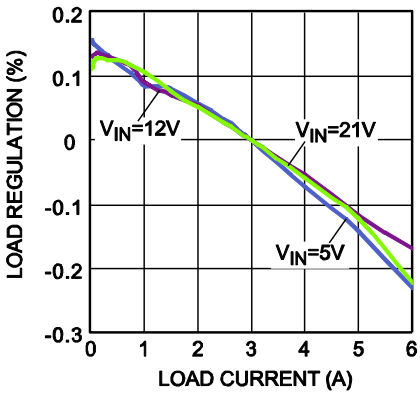
Efficiency vs. Load Current

V_{OUT} =1V, L1=1µH,V_{LPM} =0.32V



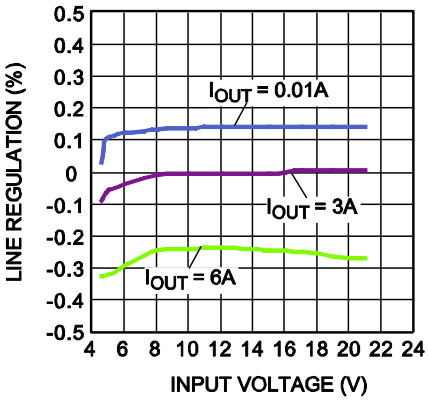
Load Regulation

V_{OUT} =1V, L1=1µH,V_{LPM} =0.32V

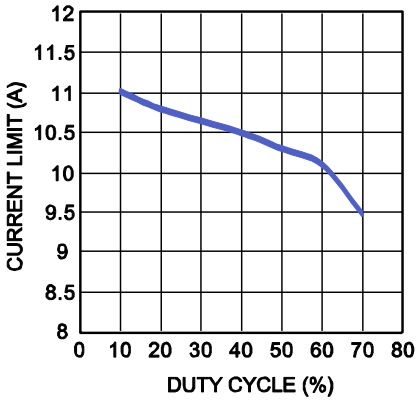


Line Regulation

V_{OUT} =1V, L1=1µH,V_{LPM} =0.32V

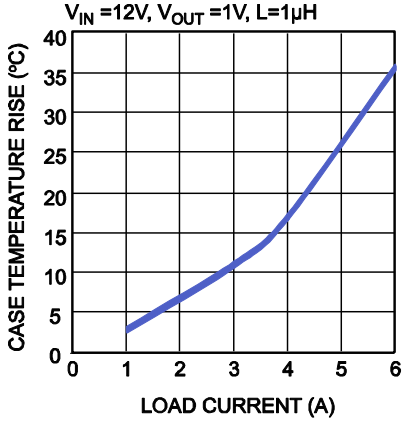


Inductor Peak-Current Limit vs. Duty Cycle



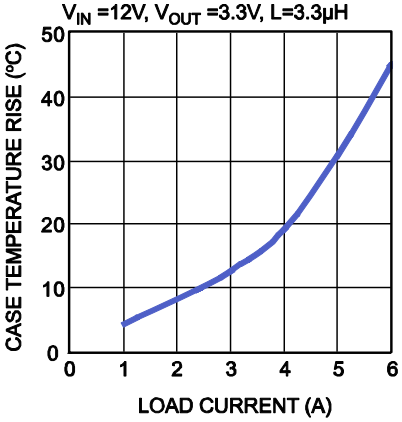
Case Temperature Rise vs. Load Current

V_{IN} =12V, V_{OUT} =1V, L=1µH



Case Temperature Rise vs. Load Current

V_{IN} =12V, V_{OUT} =3.3V, L=3.3µH



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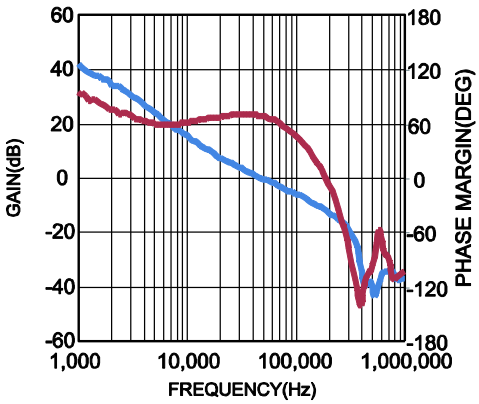
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section. V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, F_S=500kHz, T_A = +25°C, unless otherwise noted.

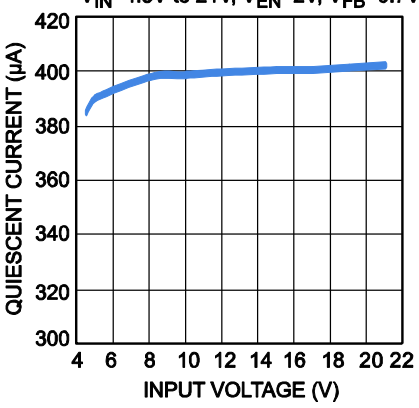
Bode Plot

I_{OUT} =6A



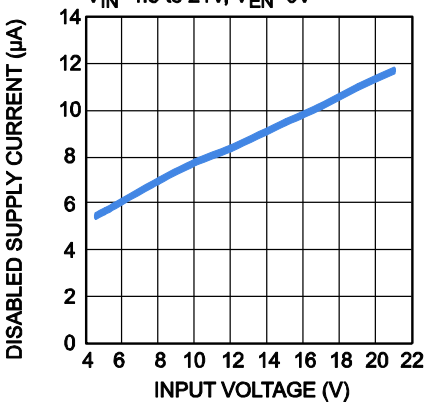
Quiescent Current vs. Input Voltage

V_{IN}=4.5V to 21V, V_{EN}=2V, V_{FB}=0.7V

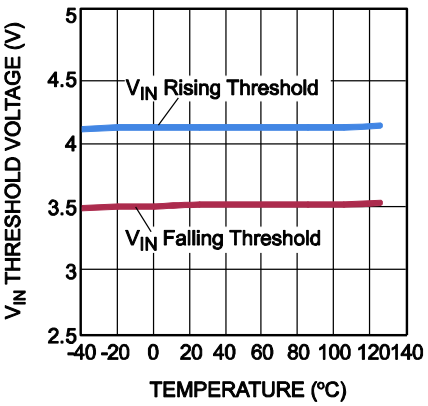


Disabled Supply Current vs. Input Voltage

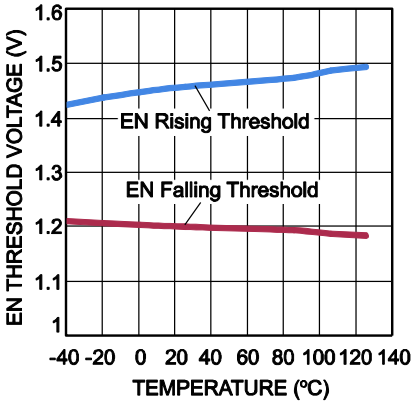
V_{IN}=4.5 to 21V, V_{EN}=0V



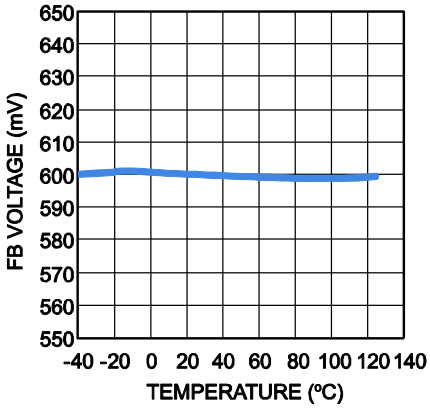
V_{IN} Threshold vs. Temperature



EN Threshold vs. Temperature



FB Voltage vs. Temperature



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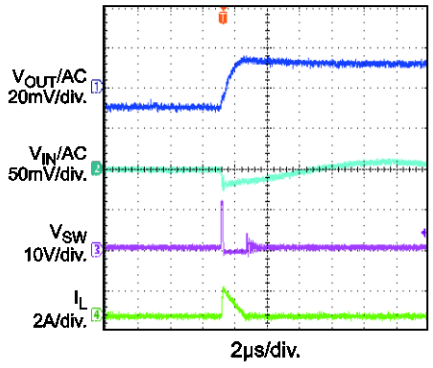
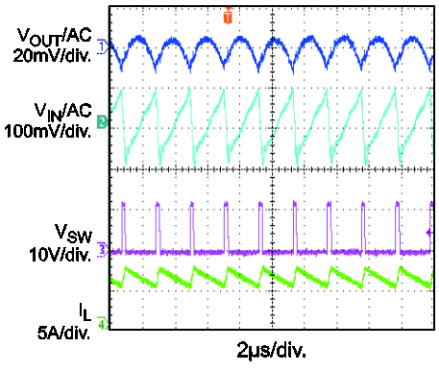
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section. V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, F_S=500kHz, T_A = +25°C, unless otherwise noted.

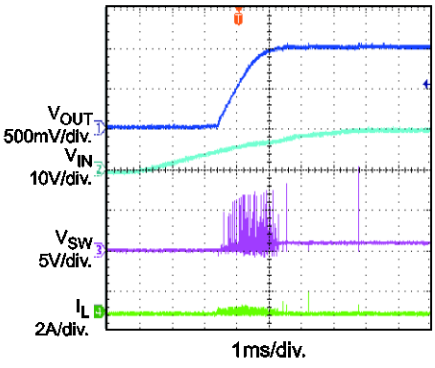
Input/Output Ripple
I_{OUT} = 0A



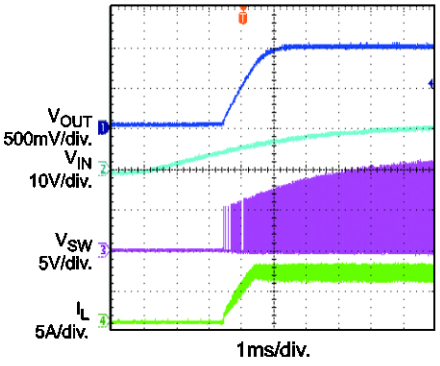
Input/Output Ripple
I_{OUT} = 6A



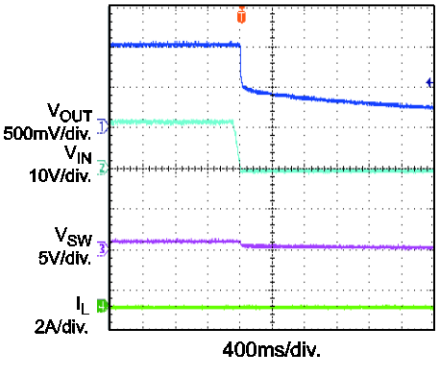
Start-Up Through Input Voltage
I_{OUT} = 0A



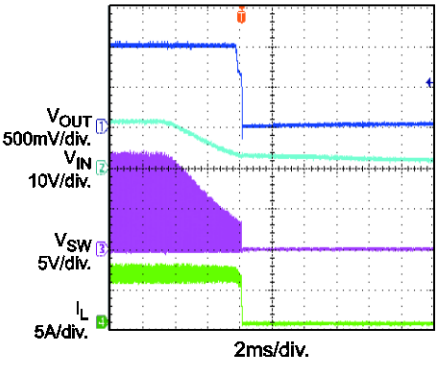
Start-Up through Input Voltage
I_{OUT} = 6A



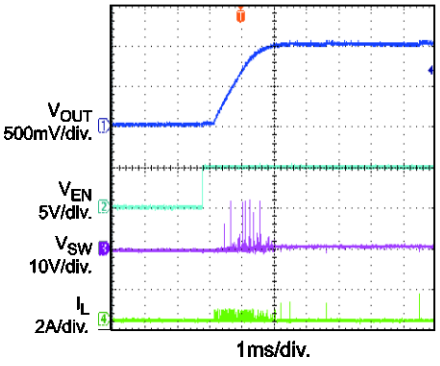
Shutdown through Input Voltage
I_{OUT} = 0A



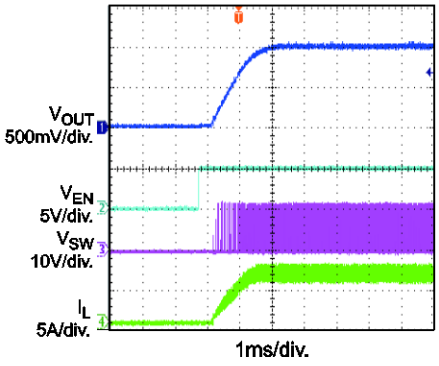
Shutdown through Input Voltage
I_{OUT} = 6A



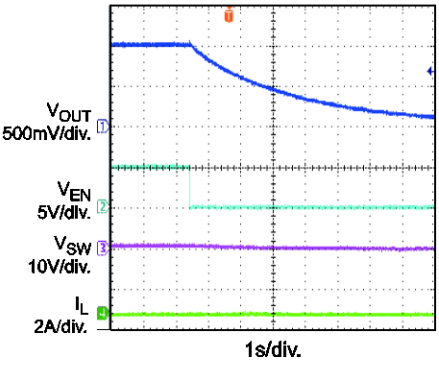
Start-Up through Enable
I_{OUT} = 0A



Start-Up through Enable
I_{OUT} = 6A



Shutdown through Enable
I_{OUT} = 0A



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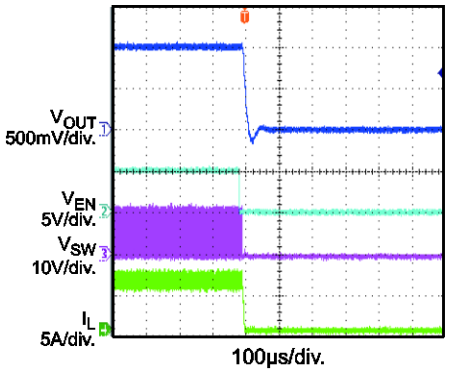
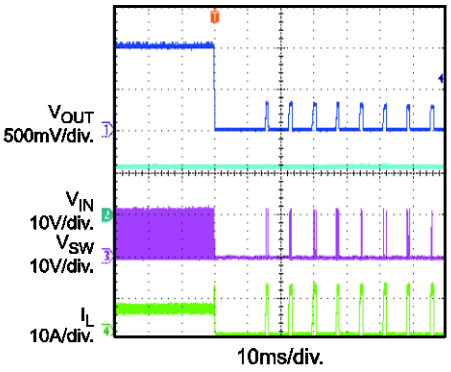
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are captured from the evaluation board discussed in the Design Example section. V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, F_S=500kHz, T_A = +25°C, unless otherwise noted.

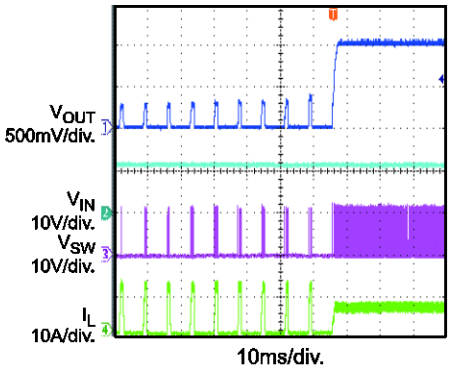
Shutdown through Enable
I_{OUT} = 6A



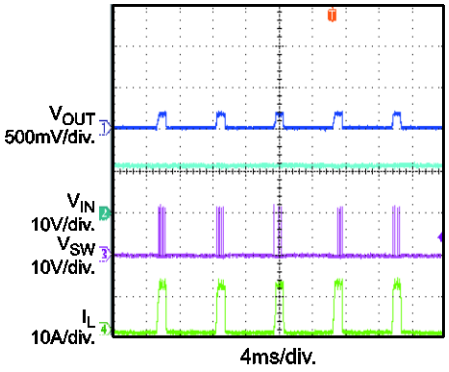
Short-Circuit Entry
I_{OUT} = 6A



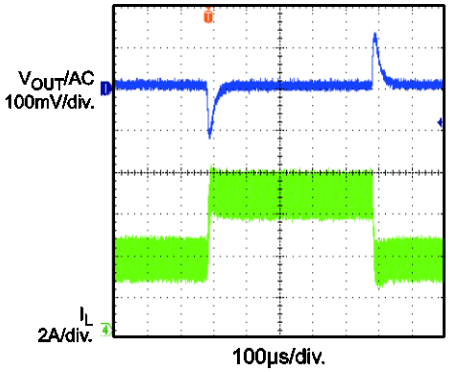
Short-Circuit Recovery
I_{OUT} = 6A



Short-Circuit Steady State



Load Transient
I_{OUT} = 3A to 6A



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FUNCTIONAL BLOCK DIAGRAM

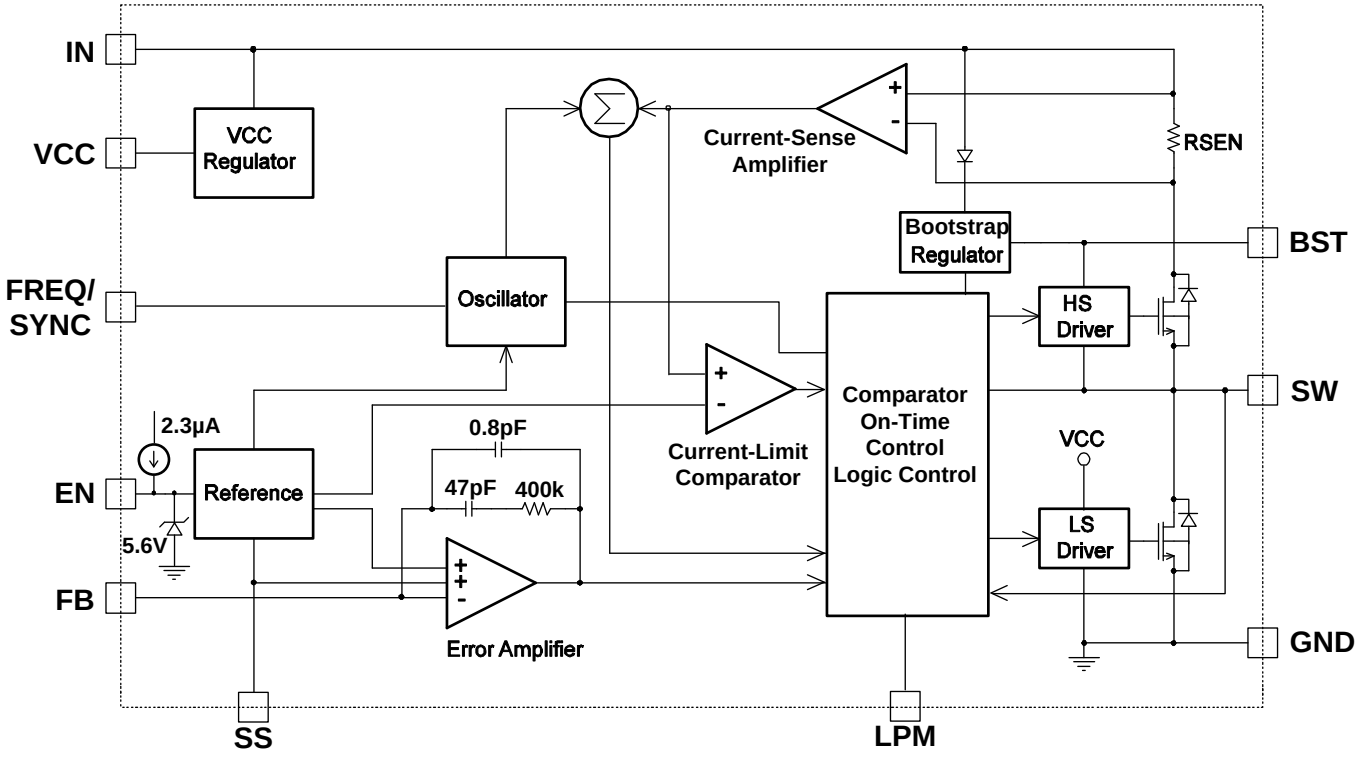

FIGURE 1. Functional Block Diagram

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OPERATION

The MP2229 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a compact solution to achieve a 6A continuous output current over a wide input-supply range with excellent load and line regulation.

When MP2229 works in fixed-frequency peak current-mode control to regulate the output voltage, the internal clock initiates the PWM cycle and turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the value set by the COMP value within 95% of one PWM period, then the HS-FET is forced off.

Error Amplifier (EA)

The error amplifier compares the FB voltage against the internal 0.6V reference (V_{REF}) and outputs a current proportional to the difference between the two. This output current charges or discharges the internal compensation network to form the COMP voltage, which controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies control loop design.

Internal Regulator

The 5V internal regulator powers most of the internal circuitries. The regulator takes the V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5V, the output of the regulator is in full regulation. If V_{IN} is less than 5V, the output decreases with V_{IN}. The part requires a 0.1µF ceramic decoupling capacitor.

Enable Control (EN)

The MP2229 has a dedicated enable control pin (EN). Pull EN high, or float, to enable the IC; pull EN low to disable the IC.

The EN voltage is clamped to around 5.6V by an internal Zener diode (see Figure 2). A pull-up resistor is not needed to pull up the EN voltage. If EN is connected to a voltage source higher than 5V, a resistor is needed from the voltage source to EN in order to limit the EN input current to less than 100µA. This helps prevent damage to the internal Zener diode.

For example, connecting 12V to EN through a pull-up resistor, $R_{PULLUP} \geq (12V - 5.6V)/100\mu A = 64k\Omega$.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to below 5V to prevent damage to the internal Zener diode.

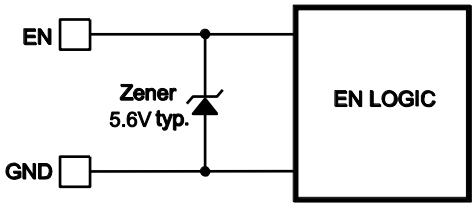

FIGURE 2. Zener Diode between EN and GND

Setting the Frequency and Synchronizing

Connect a resistor from FREQ/SYNC to ground to set the switching frequency. The value of the frequency can be calculated approximately from:

$$F_S(kHz) = \frac{16000}{R_{FREQ}(k\Omega) + 2.3}$$

The frequency vs. R_{FREQ} is shown in Figure 3.

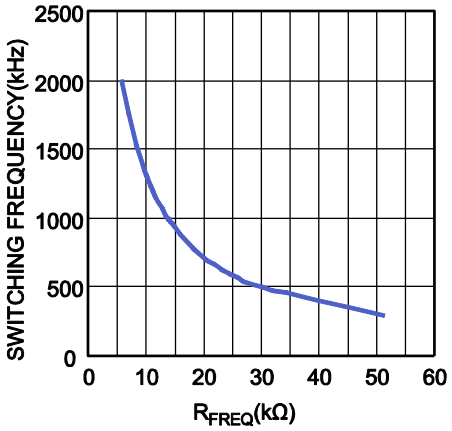

FIGURE 3. Switching Frequency vs R_{FREQ}

Also, the MP2229 can be synchronized to an external clock with a range from 300kHz to 2MHz through FREQ/SYNC. The

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internal clock rising edge is synchronized to the external clock rising edge.

Low-Power Mode (LPM)

The MP2229 has a low-power mode for light load. Under a heavy-load condition, V_{COMP} is higher than V_{LPM}. When the clock goes high, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock re-sets every time V_{COMP} is higher than V_{LPM}.

Under a light-load condition, the value of V_{COMP} becomes low. When V_{COMP} is less than V_{LPM}, and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{LPM}. During this time, the internal clock is blocked. Thus, the MP2229 skips pulses for pulse frequency modulation (PFM) mode, achieving the light-load power save (see Figure 4).

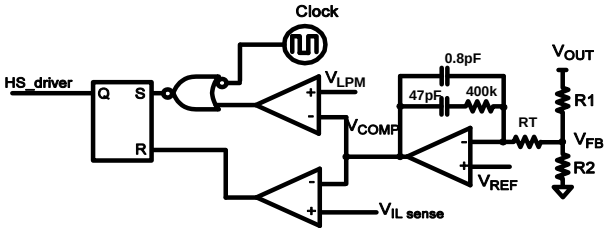

FIGURE 4. Simplified LPM Control Logic

To enable low-power mode, connect LPM to VCC or to a voltage divider from VCC. When the external V_{LPM} is higher than 1.2V, the MP2229 takes the internal V_{LPM}. To disable low-power mode, connect LPM to ground, and the converter operates constantly in fixed frequency CCM.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2229 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is 4.1V while its falling threshold is 3.5V.

External Soft-Start (SS)

Connect a capacitor from SS to ground to adjust the soft-start time. When the soft-start begins, an internal 10μA current source charges the external capacitor. The soft-start capacitor connects to the non-inverting input of the error amplifier. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the 0.6V reference. At this point, the reference voltage takes over at the non-inverting error-amplifier input. The soft-start time can be calculated as follows:

$$t_{SS}(ms) = \frac{0.6V \times C_{SS}(nF)}{10\mu A}$$

Pre-Bias Start-Up

The MP2229 has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is charged by V_{IN}. If BST voltage exceeds its rising threshold voltage, then the soft-start capacitor is charged. When the soft-start capacitor voltage exceeds the sensed output voltage at FB, the part starts to operate normally.

Over-Current Protection (OCP)

The MP2229 has a cycle-by-cycle over-current limit, which limits the inductor current in case of an output over load or short circuit. If the over load or short circuit lasts for an extended period, the FB voltage can drop below the under-voltage (UV) threshold (40% of the reference, typically). Once a UV is triggered, the MP2229 enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP2229 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature reaches 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold (120°C, typically), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.03V with a hysteresis of 200mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, R5, C5, L1, and C2 (see Figure 5). If (V_{IN}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C5. A 10Ω resistor

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placed between SW and the BST capacitor is recommended strongly to reduce the SW spike voltage and noise.

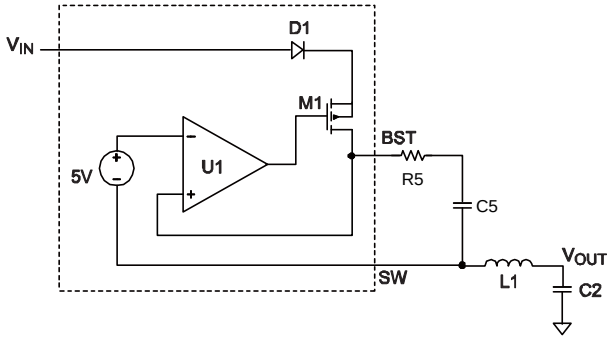

FIGURE 5. Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip is enabled. The reference block starts up first, generating a stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In shutdown, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down.

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APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (see "Typical Application" on page 1). Choose R1 around 20kΩ, then R2 is:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1}$$

The T-type network is recommended highly (see Figure 6).

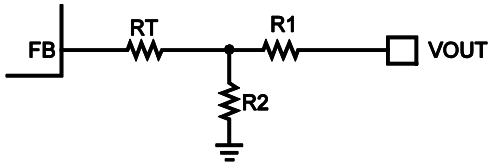

FIGURE 6. T-Type Network

Table 1 lists the recommended T-type resistor values for common output voltages.

TABLE1. Resistor Selection for Common Output Voltages(9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	RT (kΩ)
1.0	20	30	68
1.2	20	20	68
1.5	20	13.7	51
1.8	20	10	51
2.5	20	6.34	33
3.3	20	4.42	24
5	20	2.7	16

Notes:

9) The recommended parameters are based on a 500kHz switching frequency. A different input voltage, output inductors, and output capacitors may affect the recommended values of R1, R2, and RT. For additional component parameters, please refer to the "Typical Application Circuits" on pages 19-21.

Selecting the Inductor

For most applications, use a 1μH to 10μH inductor with a DC current rating at least 25% percent higher than the maximum load current. Select an inductor with a DC resistance less than 15mΩ for best efficiency. Use the following equation to derive the inductor value for most designs:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where, ΔI_L is the inductor-ripple current.

Choose the inductor-ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light-load conditions (below 100mA), use a larger inductor for improved efficiency.

Setting the Switching Frequency

An external resistor (R_{FREQ}) from FREQ/SYNC to GND sets the MP2229 oscillating frequency. The value of R_{FREQ} can be calculated approximately using the formula below:

$$R_{FREQ}(k\Omega) = \frac{16000}{f_S(kHz)} - 2.3$$

Setting the LPM Voltage

The LPM voltage is used to set the transition point from LPM to CCM. Choose a transition point that provides the best combination of efficiency, stability, ripple, and transient.

If the LPM voltage is set lower than the recommended value (see Figure 8), then stability and ripple improves but efficiency during LPM mode and transient degrades. Likewise, if the LPM voltage is set higher, then the efficiency during LPM and transient improves, but stability and ripple degrades. Calculate the optimal balance point of the LPM voltage for good efficiency, stability, and ripple.

The LPM voltage comes from the tap of a resistor divider from V_{CC} (5V) to GND (see Figure 7.

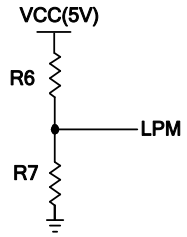

FIGURE 7. LPM Network

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Generally, choose R6 to be around 100kΩ, then R7 is:

$$R7 = \frac{V_{LPM} \times R6}{V_{CC} - V_{LPM}}$$

Refer to Figure 8 when setting the LPM voltage.

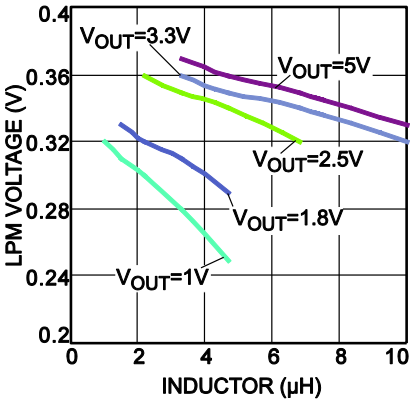

FIGURE 8. Recommended LPM Selection for Common Output Voltages (V_{IN}=12V, F_S=500kHz)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended highly because of their low ESR and small temperature coefficients. For most applications, a 22μF and a 10μF capacitor are sufficient.

Since the input capacitor (C1) absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1μF) as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input-voltage ripple caused by the capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. Use low ESR capacitors to limit the output-voltage ripple. Estimate the output-voltage ripple with:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output-voltage ripple is caused mainly by the capacitance. For simplification, the output-voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor affect the stability of the regulatory system. The MP2229 can be optimized for a wide range of capacitance and ESR values.

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External Bootstrap Diode

BST voltage may become insufficient at particular specs (see conditions below). In these cases an external bootstrap diode can enhance the efficiency of the regulator at heavy load and avoid BST voltage insufficiency during PFM operation at light load. Insufficient BST voltage is more likely to happen at either of the following conditions:

- V_{IN} is below 5V
- V_{OUT} is 5V or 3.3V; and the duty cycle is large: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases (if insufficient BST voltage occurs), the output-ripple voltage may become extremely high during a light-load condition. Add an external BST diode from VCC to BST (see Figure 9).

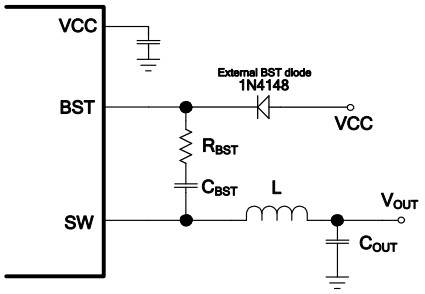


FIGURE 9. Optional Bootstrap Diode

The recommended external BST diode is IN4148, and the BST capacitor is 0.1μF to 1μF.

PCB Layout Guidelines(10)

Efficient PCB layout is critical to achieve stable operation. For best results, please refer to Figure 10 and follow the guidelines below:

1) Keep the connection of input ground and GND as short and wide as possible.

2) Keep the connection of the input capacitor and IN as short and wide as possible.

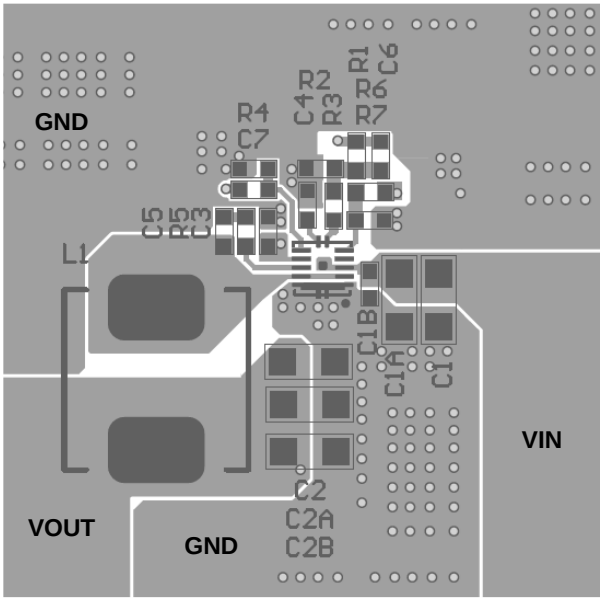
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) Route SW away from sensitive analog areas (such as FB).

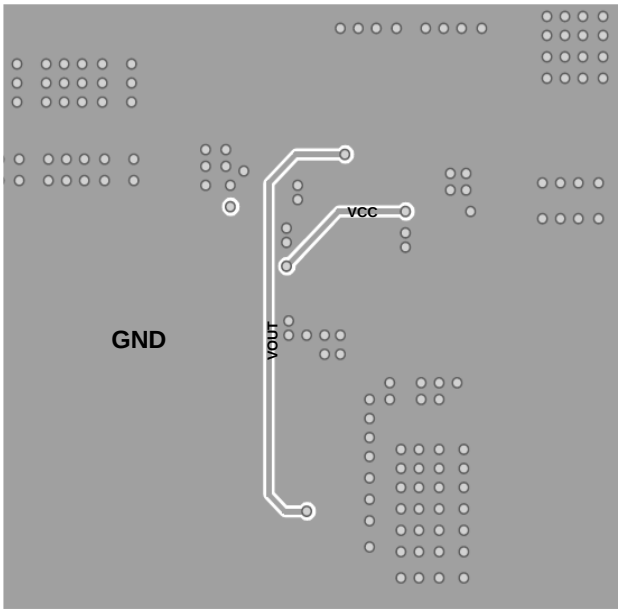
To improve performance, use a 4-layer board. Figure 10 shows the top and bottom layer of the PCB (inner 1 and inner 2 are all GND).

Notes:

10) The recommended layout is based on the Figure 11 "Typical Application Circuit" on Page19.



Top Layer



Bottom Layer

FIGURE 10. Recommended PCB Layout

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Design Example

Table 2 below is a design example following the application guidelines for the specifications:

TABLE 2. Design Example

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	6A
F_S	500kHz

The detailed application schematics are shown in Figure 11. The typical performance and circuit waveforms have been shown in the "Typical Performance Characteristics" section. For additional device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS(11)

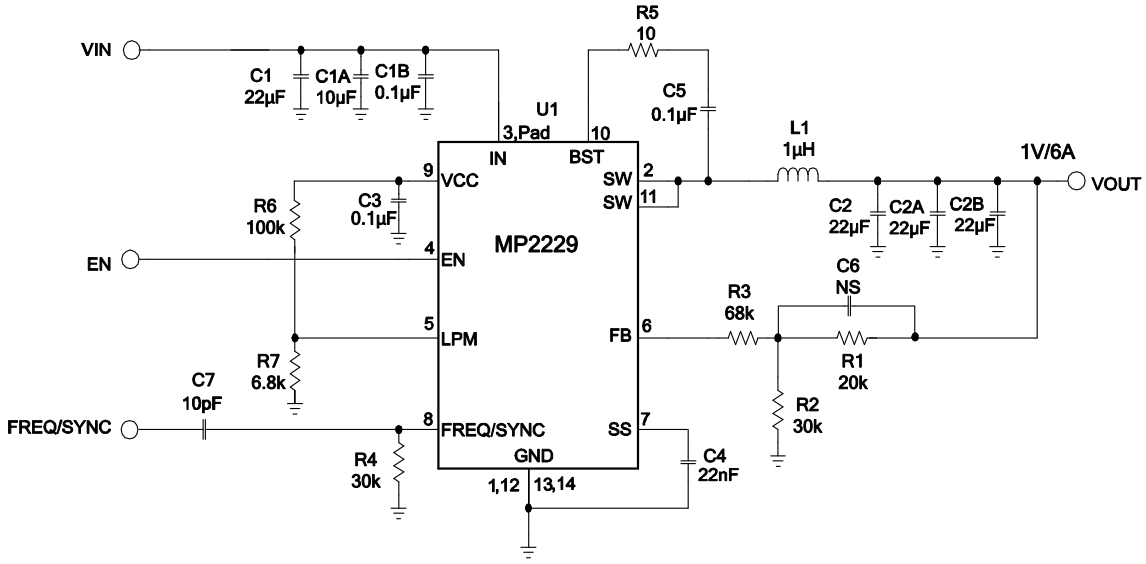

FIGURE 11. V_{IN}=12V, F_S=500kHz, V_{OUT}=1V,I_{OUT}=6A

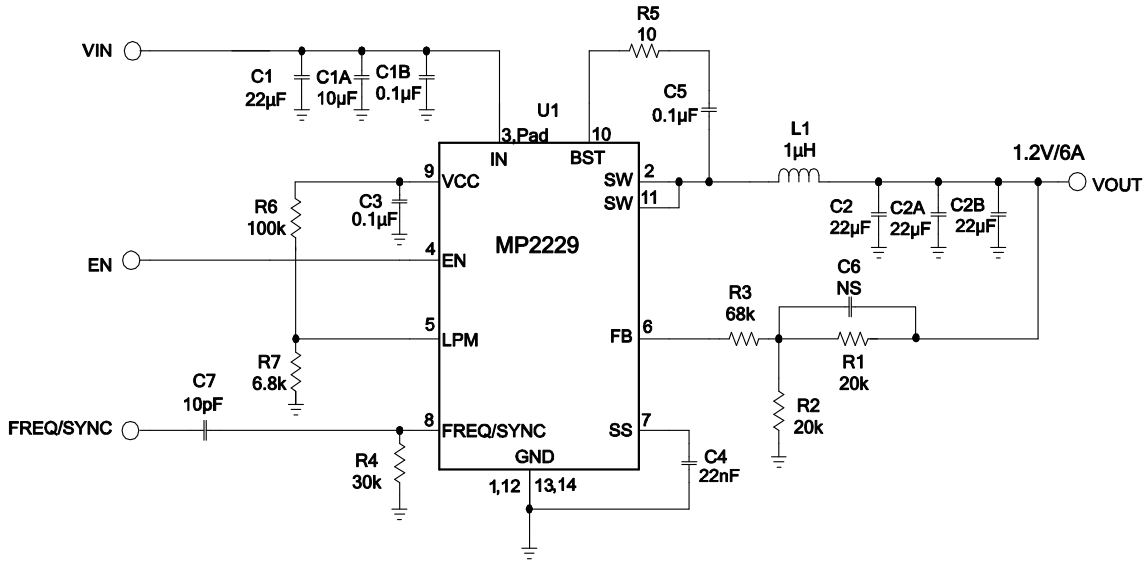

FIGURE 12. V_{IN}=12V, F_S=500kHz, V_{OUT}=1.2V, I_{OUT}=6A

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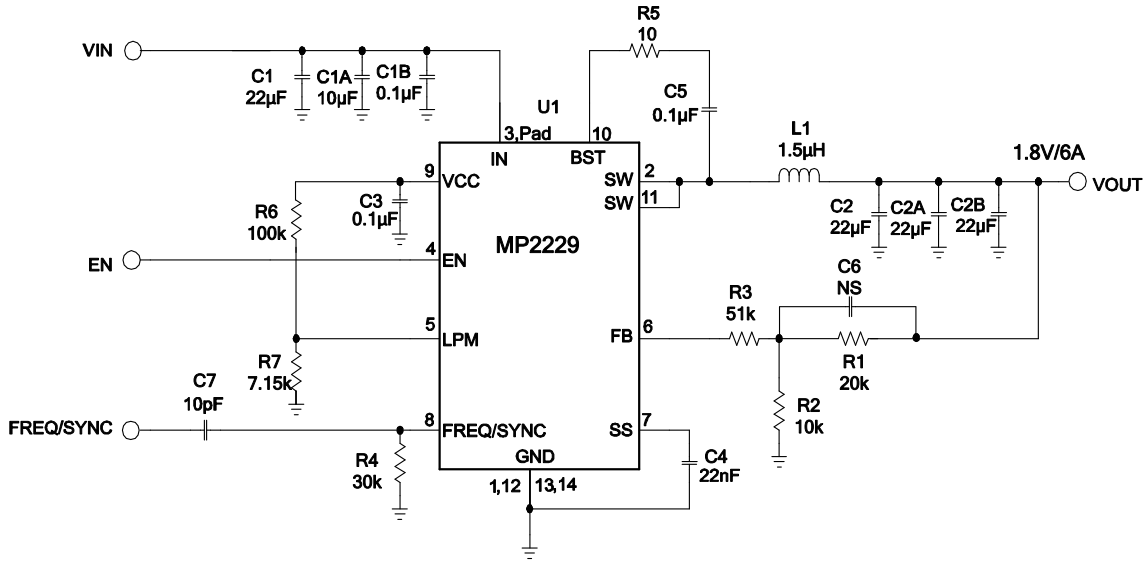

FIGURE 13. V_{IN}=12V, F_S=500kHz, V_{OUT}=1.8V, I_{OUT}=6A

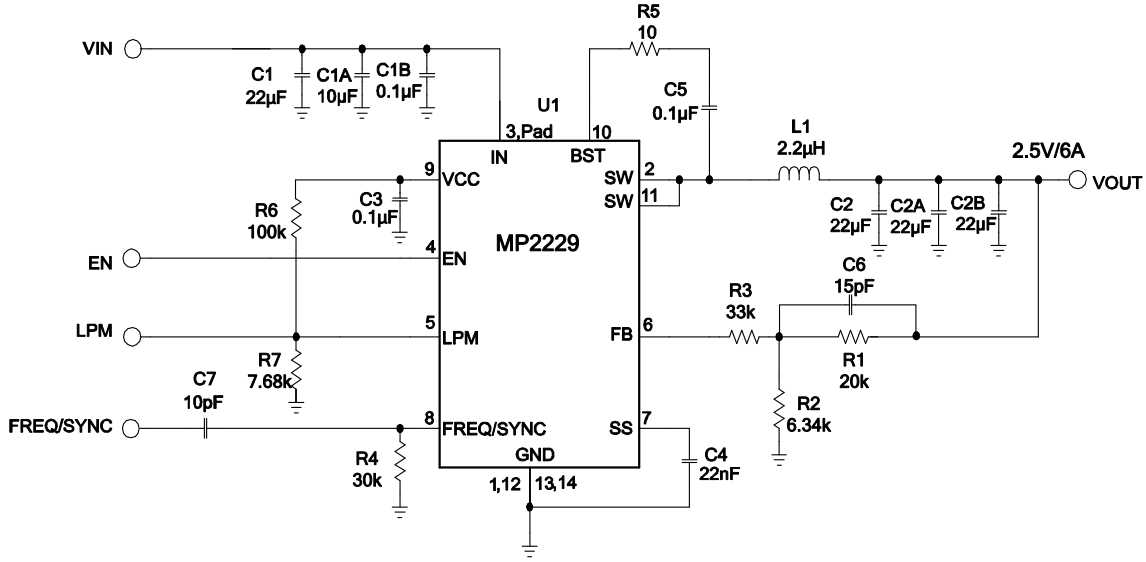

FIGURE 14. V_{IN}=12V, F_S=500kHz, V_{OUT}=2.5V, I_{OUT}=6A

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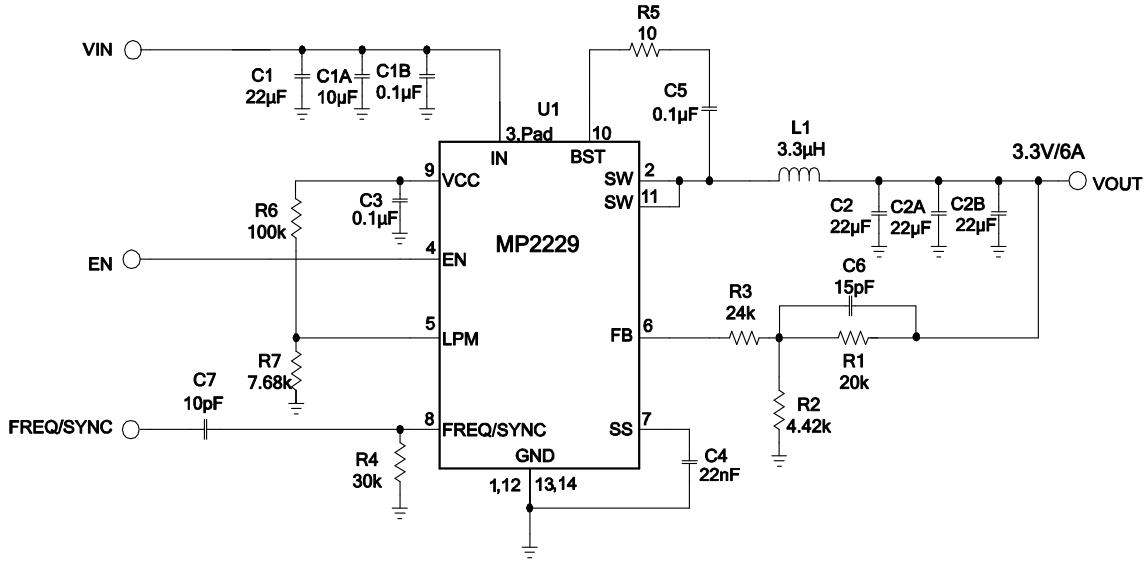

FIGURE 15. V_{IN}=12V, F_S=500kHz, V_{OUT}=3.3V, I_{OUT}=6A

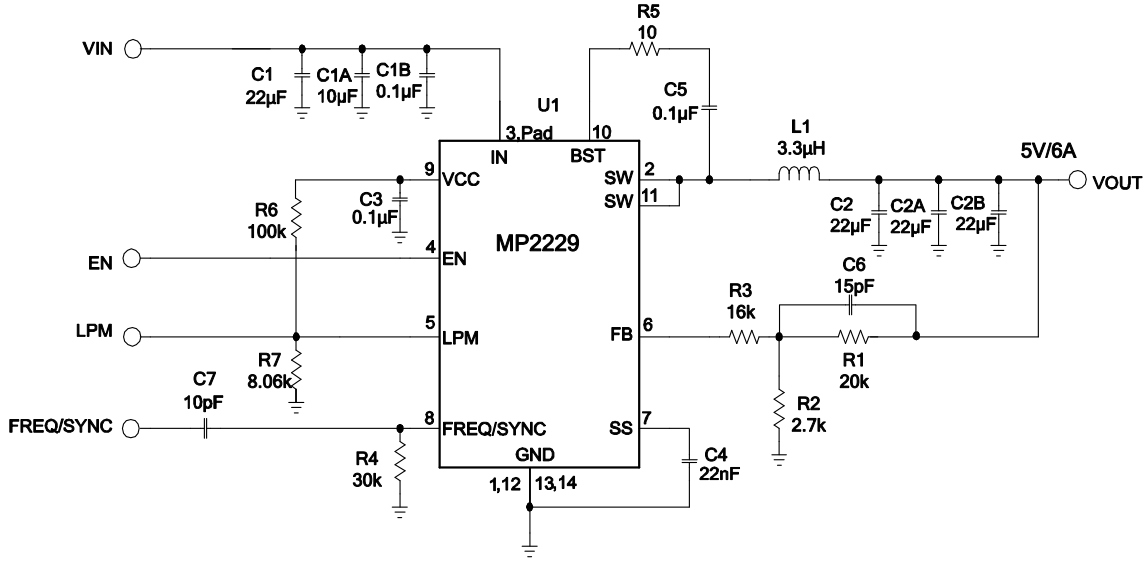

FIGURE 16. V_{IN}=12V, F_S=500kHz, V_{OUT}=5V, I_{OUT}=6A

Notes:

11) For V_{OUT}=3.3V application, when V_{IN} is lower than 5V and I_{OUT}>5A, an additional input capacitor may be needed to reduce the input-voltage ripple for better stability.
For V_{OUT}=5V application, when V_{IN} is lower than 7V and I_{OUT}>5A, an additional input capacitor may be needed to reduce the input-voltage ripple for better stability.

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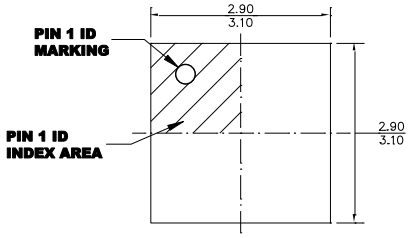
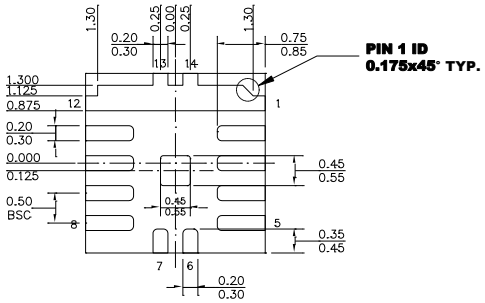
PACKAGE INFORMATION

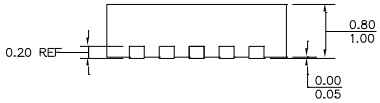
QFN-14 (3mmx3mm)



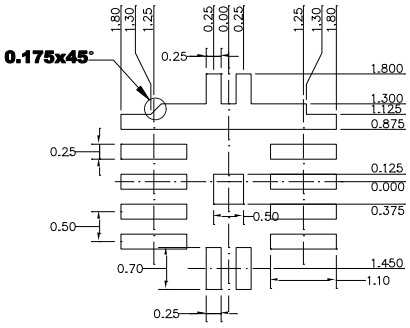
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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