Vishay Dale

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IHLP[®] Commercial Inductors, Low DCR Series



DESIGN SUPPORT TOOLS click logo to get started

3D Models I Available

Adels Design Tools Vailable Available

XÖ

L ₀ INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (μH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) ⁽¹⁾	SATURATION CURRENT DC TYP. (A) ⁽²⁾	SRF TYP. (MHz)
0.10	2.7	2.9	21.0	25.0	266
0.22	4.1	4.5	17.0	13.0	146
0.33	5.5	5.9	13.0	7.5	108
0.47	7.1	7.7	12.5	8.0	83
1.0	16.8	18.1	7.5	7.0	66
2.2	34.9	37.7	5.0	5.5	41
3.3	53.5	57.8	4.1	4.7	29
4.7	75.3	81.3	3.2	3.0	27
5.6	85.2	92.0	3.0	2.2	24
6.8	114.0	121.0	2.8	2.1	21
10.0	169.3	182.8	2.2	2.0	17

Notes

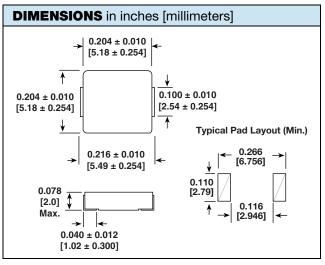
- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +125 °C
- The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application.
- Rated operating voltage (across inductor) = 40 V
- $^{(1)}$ DC current (A) that will cause an approximate ΔT of 40 $^{\circ}C$
- $^{(2)}\,$ DC current (A) that will cause L_0 to drop approximately 20 %

FEATURES

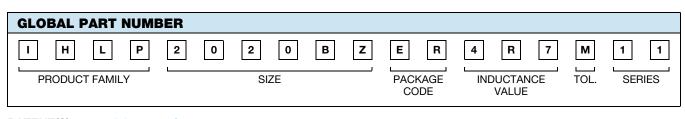
- Shielded construction
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
 COMPLIANT
- Ultra low buzz noise, due to composite HALOGEN
 construction
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up to SRF (see "Standard Electrical Specifications" table)
- IHLP design. PATENT(S): <u>www.vishay.com/patents</u>
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- PDA / notebook / desktop / server applications
- High current POL converters
- · Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for Field Programmable Gate Array (FPGA)



DESCRIPTION IHLP-2020BZ-11 4.7 μH ± 20 % ER e3 MODEL INDUCTANCE VALUE INDUCTANCE TOLERANCE PACKAGE CODE JEDEC[®] LEAD (Pb)-FREE STANDARD



PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.

Revision: 12-Oct-17

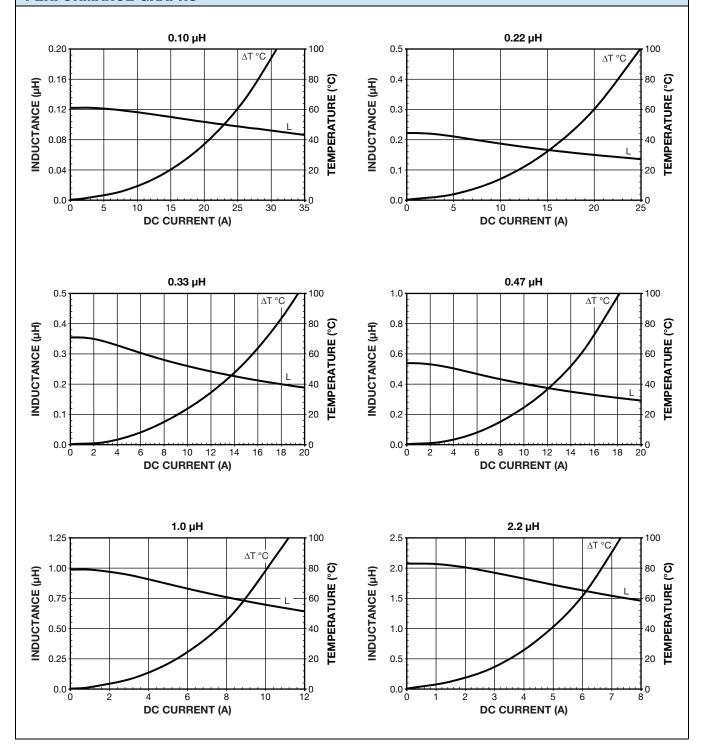
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Document Number: 34261



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PERFORMANCE GRAPHS

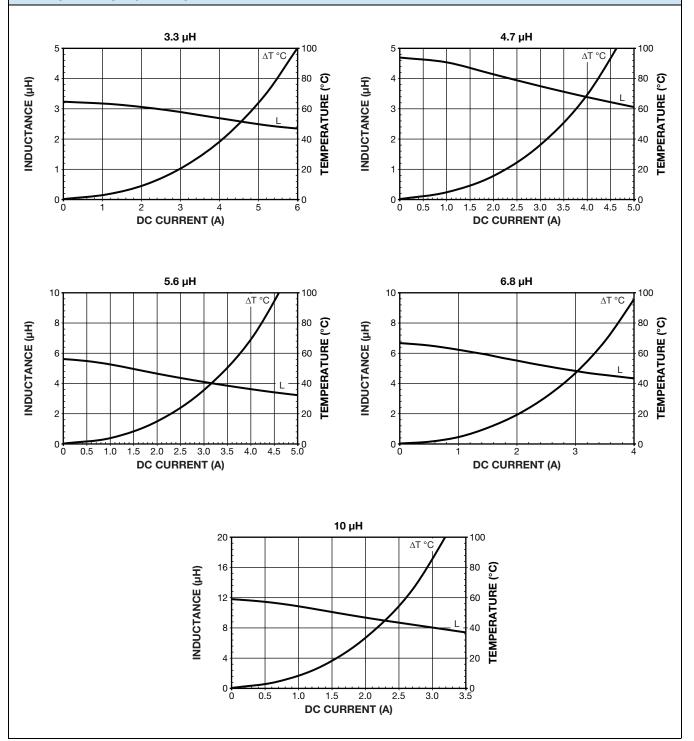


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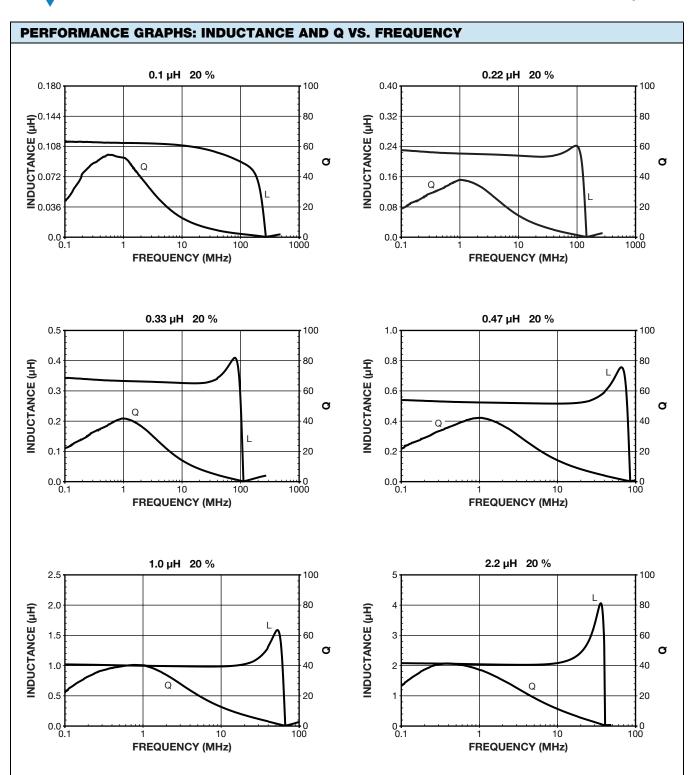
PERFORMANCE GRAPHS



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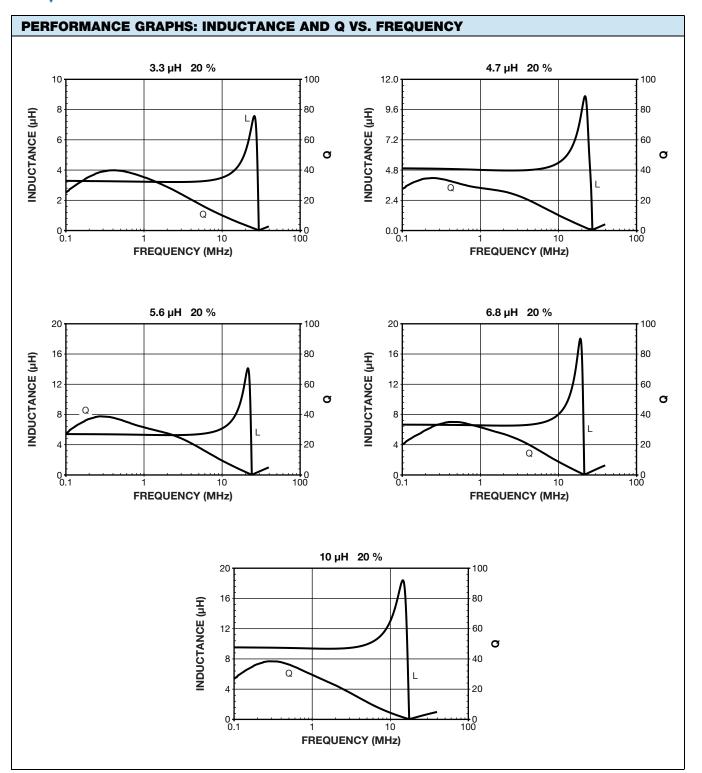
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