MIC23250

4 MHz Dual 400 mA Synchronous Buck Regulator with HyperLight Load™

Features

- Input Voltage: 2.7V to 5.5V
- Dual Output Current 400 mA/400 mA
- Up to 94% Peak Efficiency and 85% Efficiency at 1 mA
- 33 µA Dual Quiescent Current
- 1 µH Inductor with a 4.7 µF Capacitor
- 4 MHz in PWM Operation
- Ultra Fast Transient Response
- Low Voltage Output Ripple
- 20 mVpp in HyperLight Load™ Mode
- 3 mV Output Voltage Ripple in Full PWM Mode
- 0.01 µA Shutdown Current
- Fixed Output:10-lead 2 mm x 2 mm UDFN
- Adjustable Output:12-Lead 2.5 mm x 2.5 mm UDFN
- -40°C to +125°C Junction Temperature Range

Applications

- Mobile Handsets
- Portable Media Players
- Portable Navigation Devices (GPS)
- WiFi/WiMax/WiBro Modules
- Digital Cameras
- Wireless LAN Cards
- USB Powered Devices

General Description

The MIC23250 is a high efficiency 4 MHz dual 400 mA synchronous buck regulator with HyperLight Load™ mode. HyperLight Load™ provides very high efficiency at light loads and ultra-fast transient response, which is perfectly suited for supplying processor core voltages.

An additional benefit of this proprietary architecture is very low output ripple voltage throughout the entire load range with the use of small output capacitors. The fixed output MIC23250 has a tiny 2 mm x 2 mm UDFN package that saves precious board space by requiring only 6 additional external components to drive both outputs up to 400 mA each.

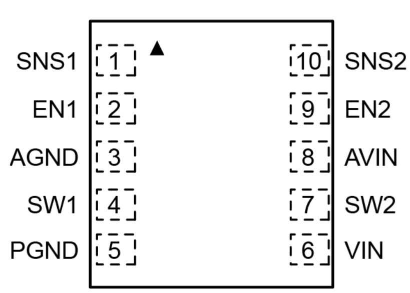
The device is designed for use with a 1 µH inductor and a 4.7 µF output capacitor that enables a sub-1 mm height.

The MIC23250 has a very low quiescent current of 33 µA with both outputs enabled and can achieve over 85% efficiency at 1 mA. At higher loads, the MIC23250 provides a constant switching frequency around 4 MHz, while providing peak efficiencies up to 94%.

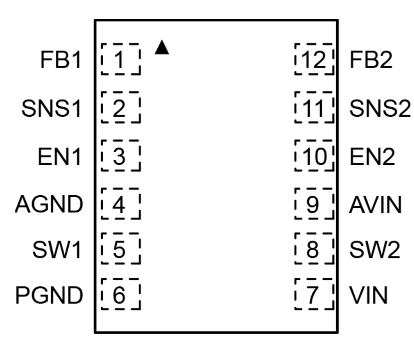
The MIC23250 fixed output voltage option is available in a 10-lead 2 mm x 2 mm UDFN. The adjustable output options are available in a 12-lead 2.5 mm x 2.5 mm UDFN. The MIC23250 is designed to operate over the junction operating range of -40°C to +125°C.

Package Types

MIC23250
10-Lead Fixed Output
(Top View)

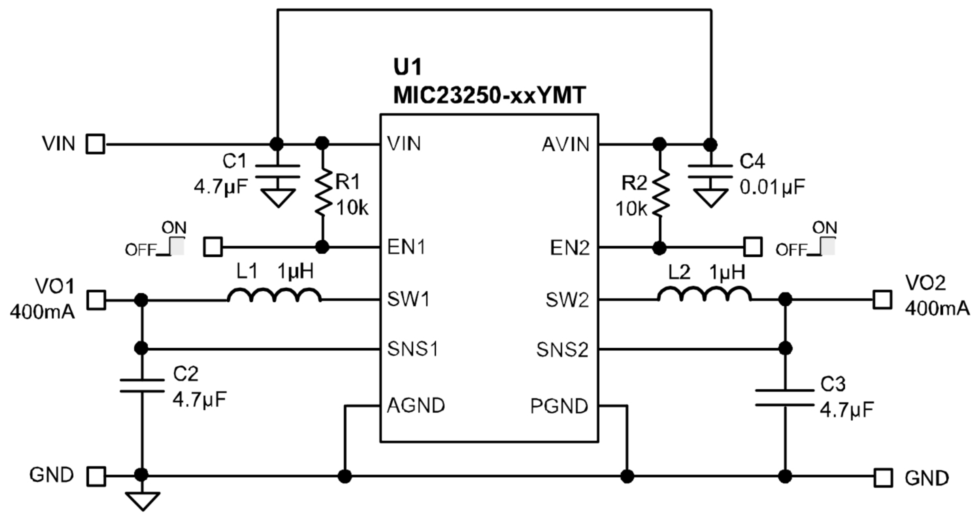


MIC23250
12-Lead Adjustable Output
(Top View)

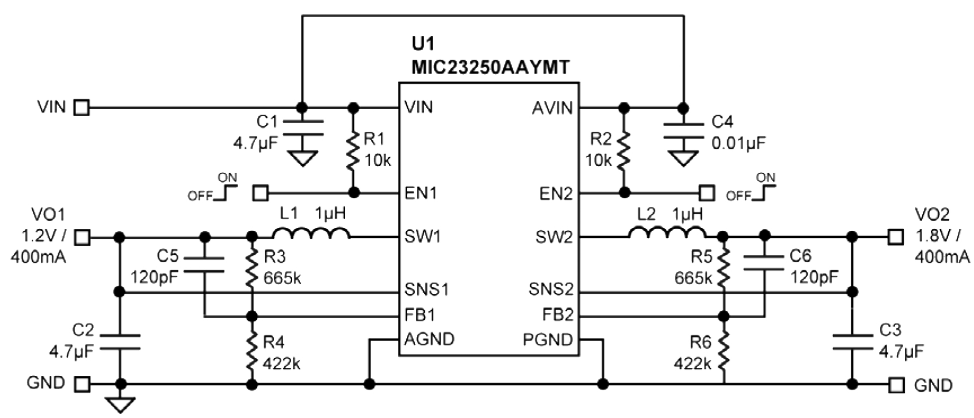


Typical Application Circuits

MIC23250 Typical Application Circuit
(Fixed Output)

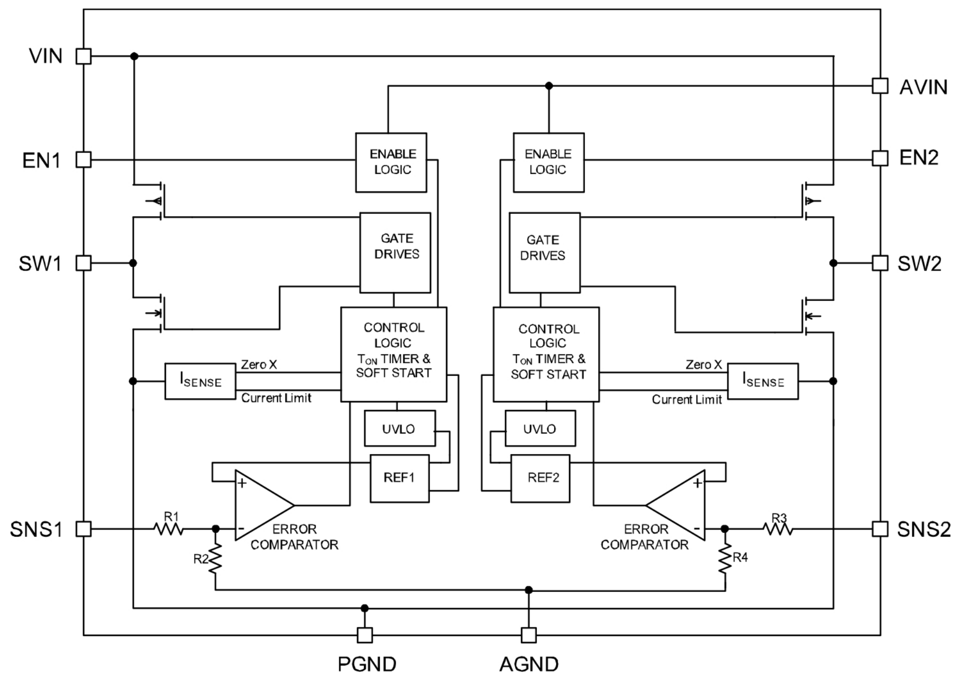


MIC23250 Typical Application Circuit
(Adjustable Output)

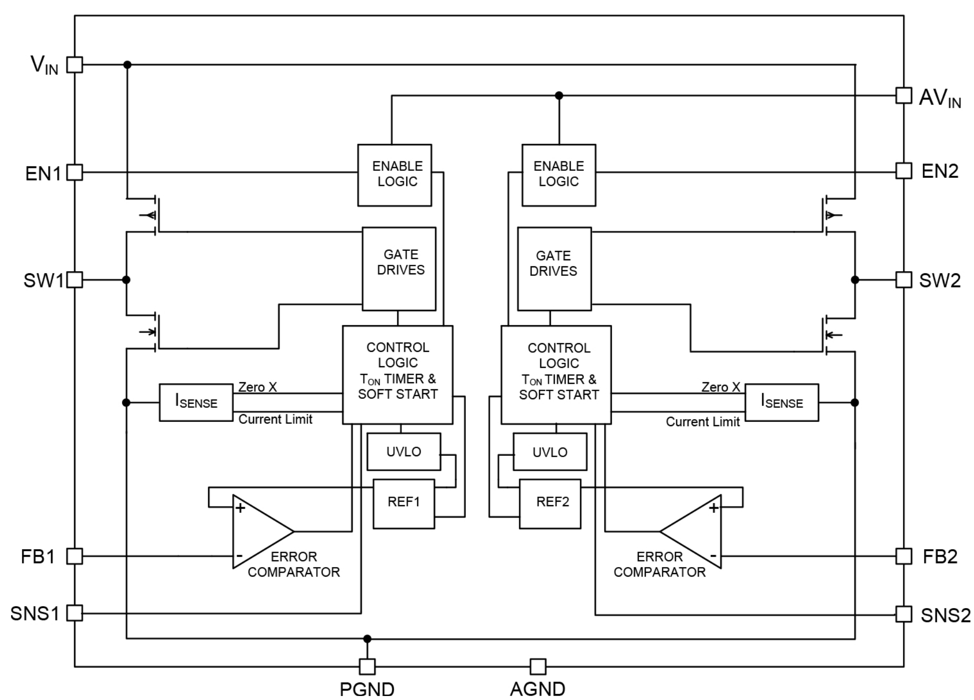


Functional Block Diagram

MIC23250 Simplified Fixed Output Block Diagram



MIC23250 Simplified Adjustable Output Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN})..6V
Output Switch Voltage (V_{SW})..6V
Logic Input Voltage (V_{EN1}, V_{EN2})..-0.3V to V_{IN}
ESD Rating (Note 1)..500V

Operating Ratings ‡

Supply Voltage (V_{IN})..2.7V to 5.5V
Logic Input Voltage (V_{EN1}, V_{EN2})..0V to V_{IN}

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note1: Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

T_A = 25°C with V_{IN} = V_{EN1} = V_{EN2} = 3.6V; L = 1 µH; C_{OUT} = 4.7 µF; I_{OUT} = 20 mA; only one channel power is enabled, unless otherwise specified. **Bold** values indicate -40°C < T_J < +125°C. (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Undervoltage Lockout Threshold	V_{UVLO_TH}	2.45	2.55	2.65	V	(Turn on)
UVLO Hysteresis	V_{UVLO_HYS}	—	60	—	mV	—
Quiescent Current	I_Q	—	33	50	µA	$V_{OUT1, 2}$ (both enabled), $I_{OUT1, 2}$ = 0 mA, $V_{SNS1, 2}$ > 1.2 * $V_{OUT1, 2}$ nominal
Shutdown Current	I_{SHDN}	—	0.01	**4**	µA	$V_{EN1, 2}$ = 0V; V_{IN} = 5.5V
Output Voltage Accuracy	ACC_OUT	**-2.5**	—	**+2.5**	%	V_{IN} = 3.6V if V_{OUTNOM} < 2.5V, I_{LOAD} = 20 mA
		-2.5	—	**+2.5**	%	V_{IN} = 4.5V if V_{OUTNOM} ≥ 2.5V, I_{LOAD} = 20 mA
Feedback Voltage (Adj only)	V_{FB}	—	0.720	—	V	—
Current Limit in PWM Mode	I_{LIM_PWM}	**0.410**	0.65	**1**	A	SNS = 0.9*V_{OUT} NOM
Output Voltage Line Regulation	LINE_REG	—	0.4	—	%/V	V_{IN} = 3.6V to 5.5V if V_{OUTNOM} < 2.5V, I_{LOAD} = 20 mA
		—	0.4	—	%/V	V_{IN} = 4.5V to 5.5V if V_{OUTNOM} ≥ 2.5V, I_{LOAD} = 20 mA
Output Voltage Load Regulation	LOAD_REG	—	0.5	—	%	20 mA < I_{LOAD} < 400 mA, V_{IN} = 3.6V if V_{OUTNOM} < 2.5V
		—	0.5	—	%	20 mA < I_{LOAD} < 400 mA, V_{IN} = 5.0V if V_{OUTNOM} ≥ 2.5V

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

T_A = 25°C with V_{IN} = V_{EN1} = V_{EN2} = 3.6V; L = 1 µH; C_{OUT} = 4.7 µF; I_{OUT} = 20 mA; only one channel power is enabled, unless otherwise specified. **Bold** values indicate -40°C < T_J < +125°C. (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PWM Switch ON-Resistance	$R_{DS(ON)}$	—	0.6	—	Ω	I_{SW} = 100 mA PMOS
		—	0.8	—	Ω	I_{SW} = -100 mA NMOS
Frequency	f_{SW}	—	4	—	MHz	I_{LOAD} = 120 mA
Soft Start Time	t_{SS}	—	260	—	µs	V_{OUT} = 90%
Enable Threshold	V_{EN}	**0.5**	0.8	**1.2**	V	—
Enable Input Current	I_{EN}	—	0.1	**2**	µA	—
Overtemperature Shutdown	T_{SHDN}	—	160	—	°C	—
Overtemperature Shutdown Hysteresis	T_{SHDN_HYS}	—	40	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Junction Temperature Range	T_J	-40	—	+125	°C	—
Storage Temperature Range	T_S	-65	—	+150	°C	—
Thermal Resistance						
2 mm x 2 mm UDFN	θ_{JA}	—	70	—	°C/W	—
2.5 mm x 2.5 mm UDFN	θ_{JA}	—	65	—	°C/W	—

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

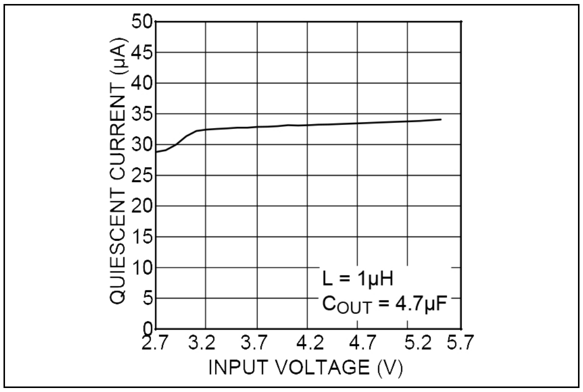


FIGURE 2-1: *Quiescent Current vs. Input Voltage.*

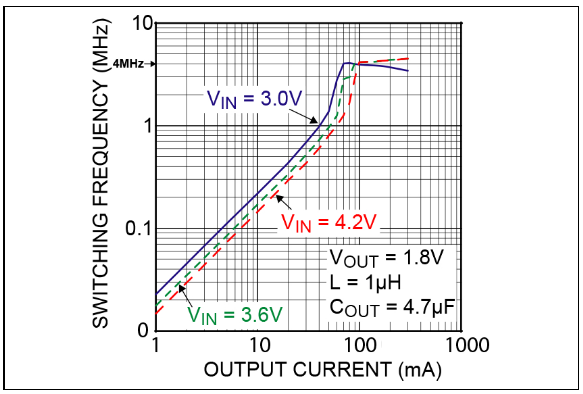


FIGURE 2-2: *Switching Frequency vs. Output Current.*

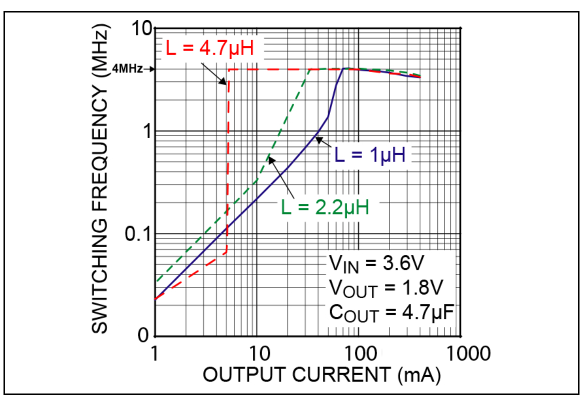


FIGURE 2-3: *Switching Frequency vs. Output Current.*

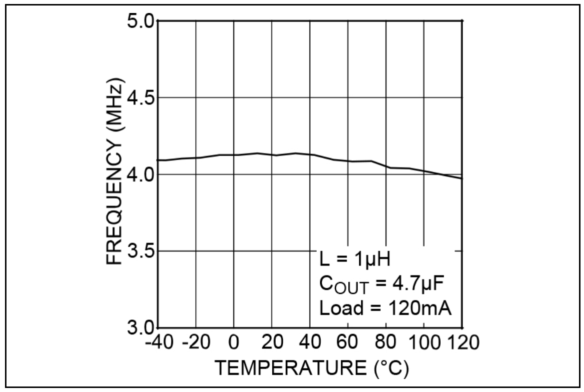


FIGURE 2-4: *Frequency vs. Temperature.*

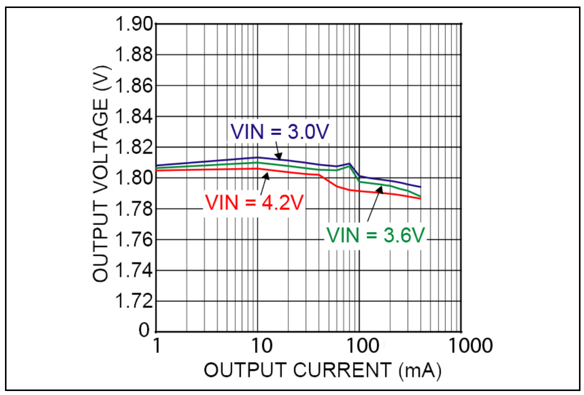


FIGURE 2-5: *Output Voltage vs. Output Current.*

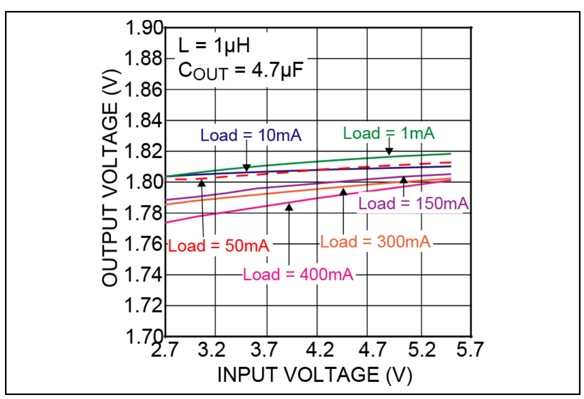


FIGURE 2-6: *Output Voltage vs. Input Voltage.*

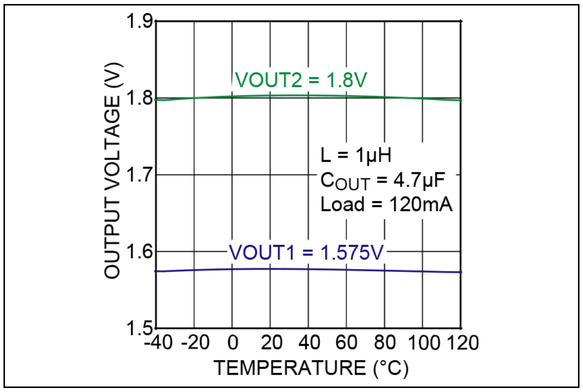


FIGURE 2-7: *Output Voltage vs. Temperature.*

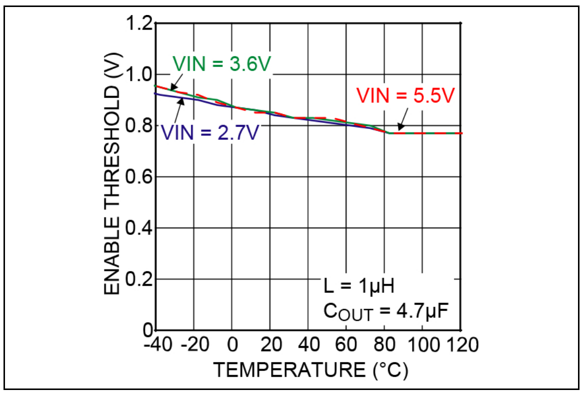


FIGURE 2-8: *Enable Threshold vs. Temperature.*

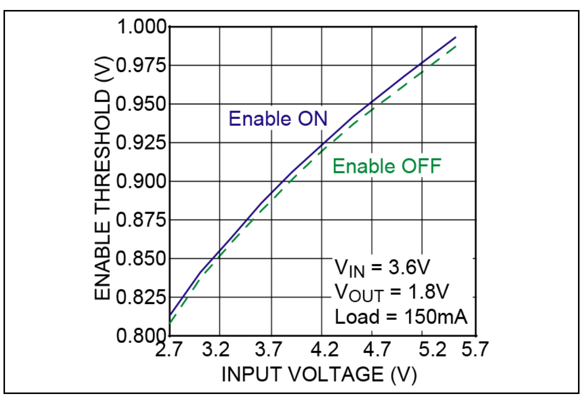


FIGURE 2-9: *Enable Threshold vs. Input Voltage.*

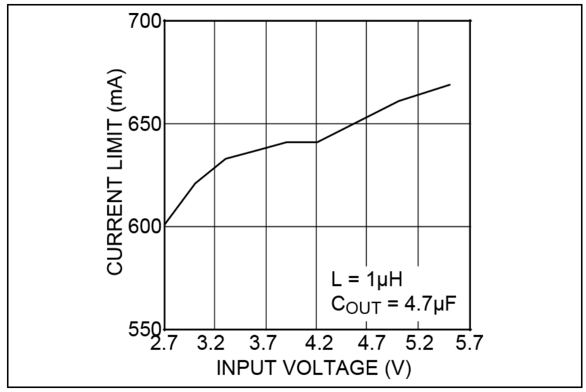


FIGURE 2-10: *Current Limit vs. Input Voltage.*

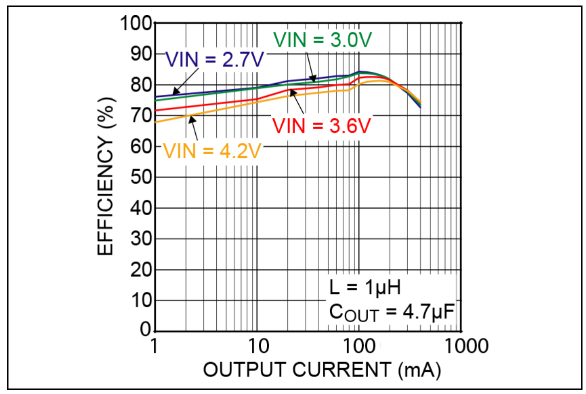


FIGURE 2-11: *Efficiency V_{OUT} = 1.2V.*

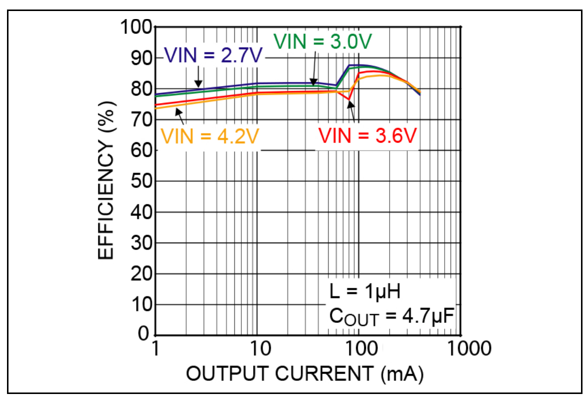


FIGURE 2-12: *Efficiency V_{OUT} = 1.575V.*

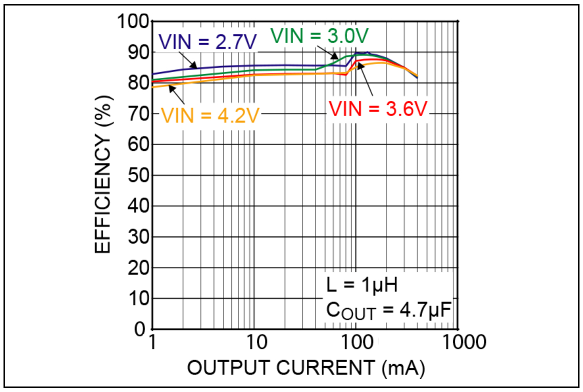


FIGURE 2-13: *Efficiency V_{OUT} = 1.8V.*

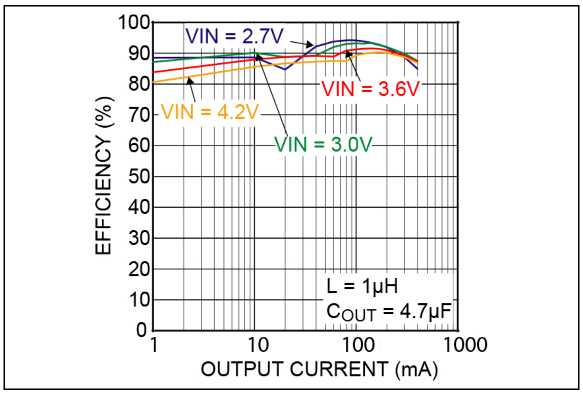


FIGURE 2-14: *Efficiency V_{OUT} = 2.5V.*

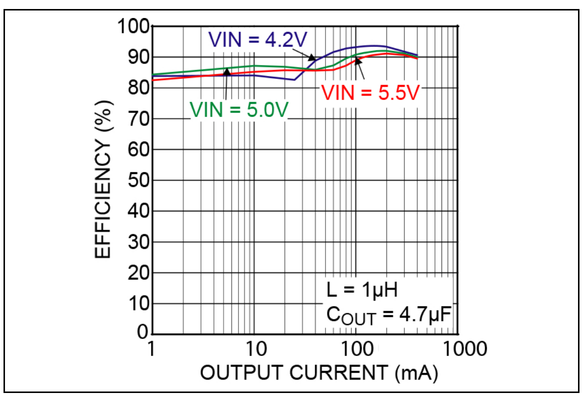


FIGURE 2-15: *Efficiency V_{OUT} = 3.3V.*

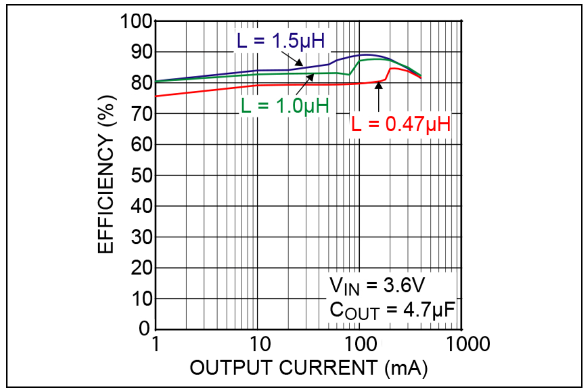


FIGURE 2-16: *Efficiency V_{OUT} = 1.8V with Various Indicators.*

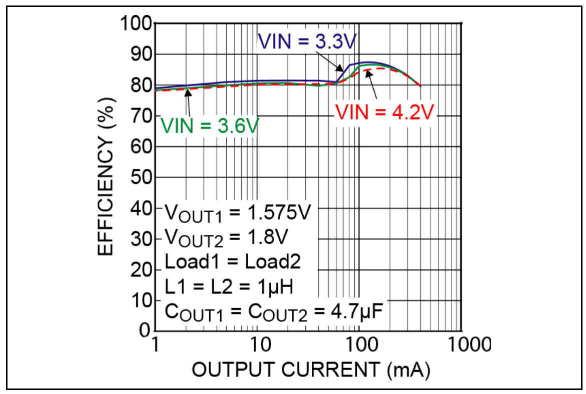


FIGURE 2-17: *Dual Output Efficiency.*

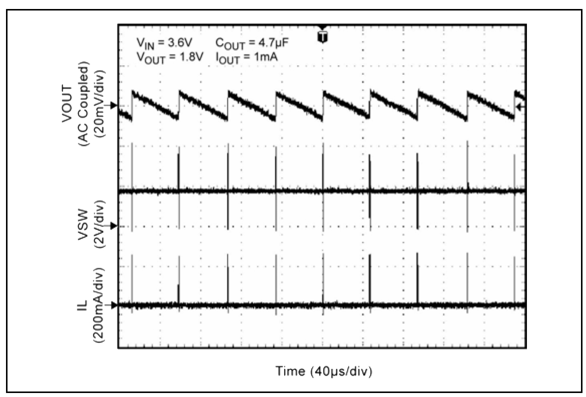


FIGURE 2-18: *Switching Waveform - Discontinuous Mode.*

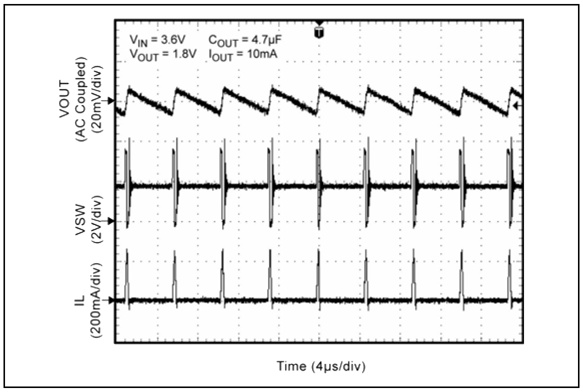


FIGURE 2-19: *Switching Waveform - Discontinuous Mode.*

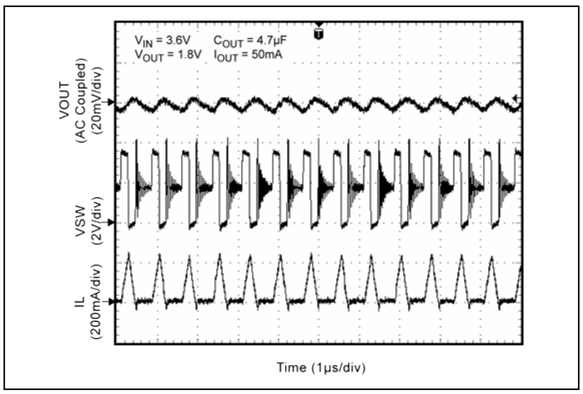


FIGURE 2-20: *Switching Waveform - Discontinuous Mode.*

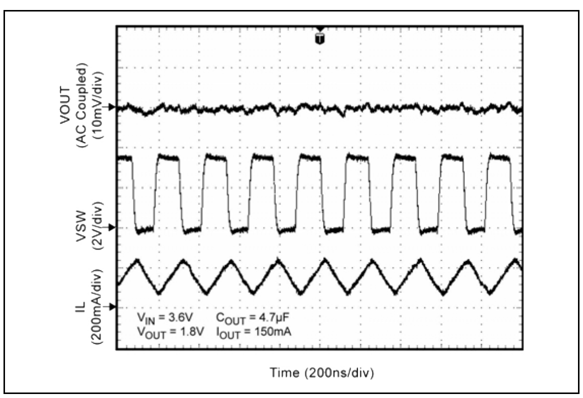


FIGURE 2-21: *Switching Waveform - Continuous Mode.*

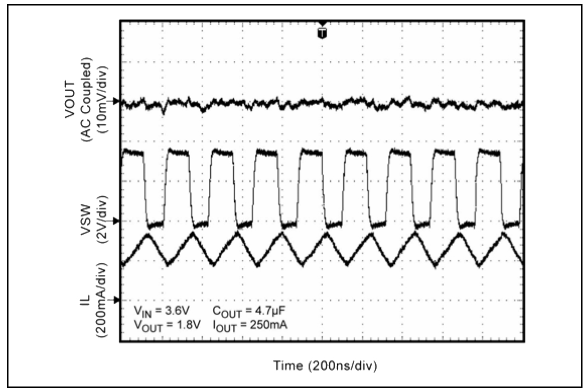


FIGURE 2-22: *Switching Waveform - Continuous Mode.*

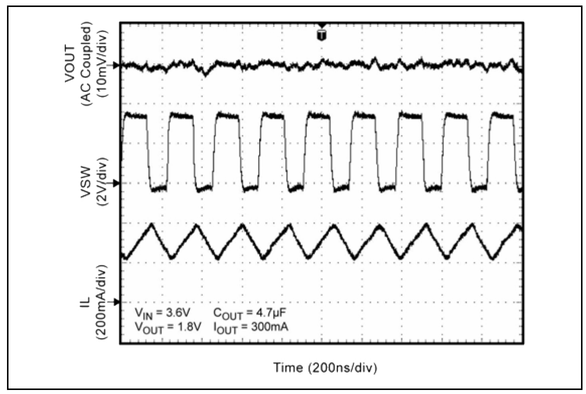


FIGURE 2-23: *Switching Waveform - Continuous Mode.*

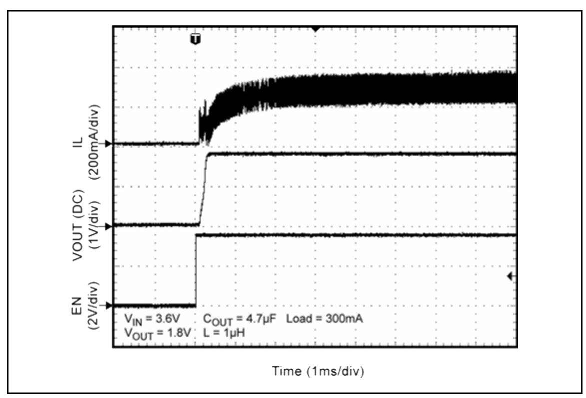


FIGURE 2-24: *Start-Up Waveform.*

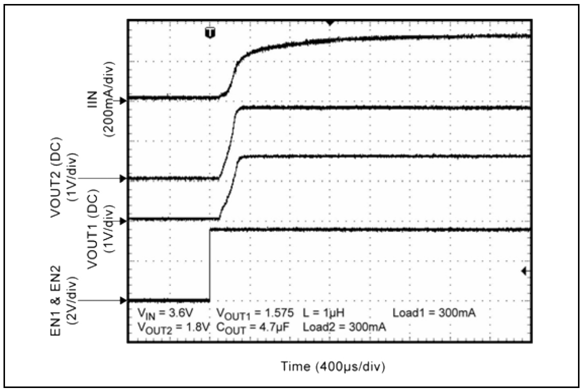


FIGURE 2-25: *Start-Up Waveform.*

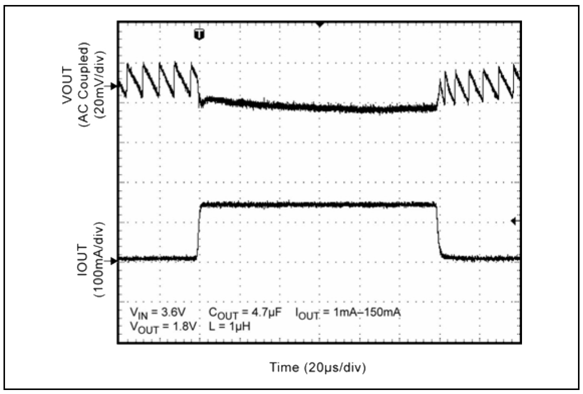


FIGURE 2-26: *Load Transient.*

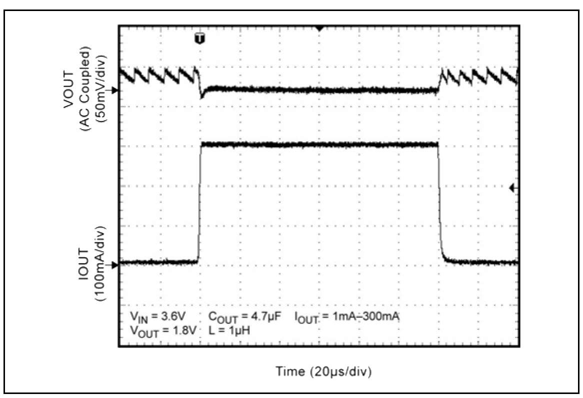


FIGURE 2-27: *Load Transient.*

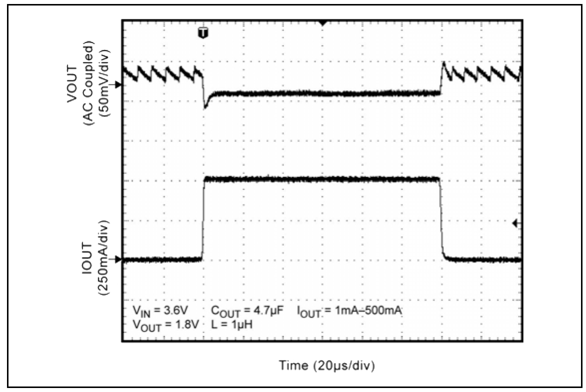


FIGURE 2-28: *Load Transient.*

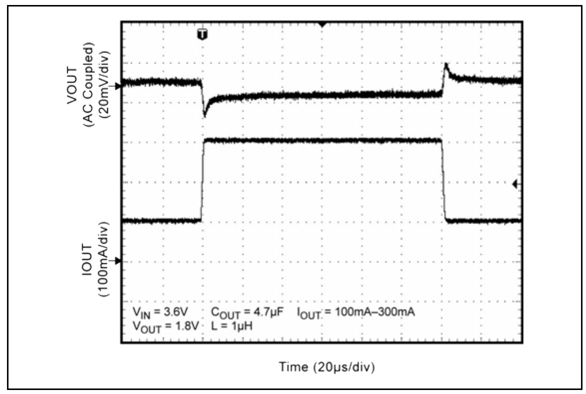


FIGURE 2-29: *Load Transient.*

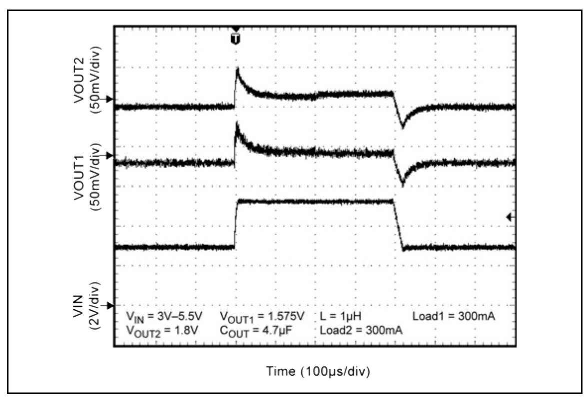


FIGURE 2-30: *Line Transient.*

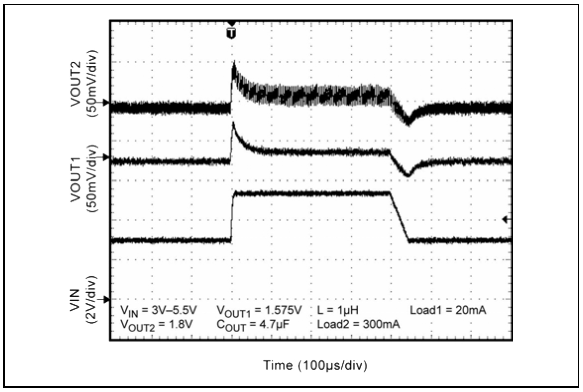


FIGURE 2-31: *Line Transient.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number (Fixed)	Pin Number (Adjustable)	Pin Name	Description
–	1	FB1	Feedback VOUT1 (input): Connect resistor divider at this node to set output 1 voltage. Resistors should be selected based on a nominal VFB of 0.72V.
1	2	SNS1	Sense 1 (input): Error amplifier input. Connect to output 1 voltage.
2	3	EN1	Enable 1 (input): Logic low will shut down output 1. Logic high powers up output 1. Do not leave unconnected.
3	4	AGND	Analog ground. Must be connected externally to PGND.
4	5	SW1	Switch node 1 (output): Internal power MOSFET output.
5	6	PGND	Power ground.
6	7	VIN	Supply voltage (power input): Requires close bypass capacitor to PGND.
7	8	SW2	Switch node 2 (output): Internal power MOSFET output.
8	9	AVIN	Supply voltage (power input): Analog control circuitry. Connect to VIN.
9	10	EN2	Enable 2 (input): Logic low will shut down output 2. Logic high powers up output 2. Do not leave unconnected.
10	11	SNS2	Sense 2 (input): Error amplifier input. Connect to output 2 voltage.
–	12	FB2	Feedback VOUT2 (input): Connect resistor divider at this node to set output 2 voltage. Resistors should be selected based on a nominal VFB of 0.72V.

4.0 FUNCTIONAL DESCRIPTION

Please refer to the PCB Layout Recommendations (Fixed Output) and PCB Layout Recommendations (Adjustable Output) for more details.

4.1 VIN

The VIN provides power to the internal MOSFETs for the switch-mode regulator, along with the current limit sensing. The VIN operating range is 2.7V to 5.5V, so an input capacitor with a minimum voltage rating of 6.3V is recommended.

Due to the high switching speed, a minimum of a 2.2 µF bypass capacitor placed close to the VIN and power ground (PGND) pins is required. Based upon size, performance, and cost, a TDK C1608X5R0J475K size 0603 4.7 µF ceramic capacitor is highly recommended for most applications.

4.2 AVIN

The analog VIN (AVIN) provides power to the analog supply circuitry. AVIN and VIN must be tied together. Careful layout should be considered to ensure high-frequency switching noise caused by VIN is reduced before reaching AVIN. A 0.01 µF bypass capacitor placed as close to AVIN as possible is recommended.

4.3 EN1/EN2

The enable pins (EN1 and EN2) control the on and off states of outputs 1 and 2, respectively. A logic high signal on the enable pin activates the output voltage of the device. A logic low signal on each enable pin deactivates the output. MIC23250 features built-in soft-start circuitry that reduces inrush current and prevents the output voltage from overshooting at start up.

4.4 SW1/SW2

The switching pin (SW1 or SW2) connects directly to one end of the inductor (L1 or L2) and provides the current path during switching cycles. The other end of the inductor is connected to the load and SNS pin. Due to the high-speed switching on this pin, the switch node should be routed away from sensitive nodes.

4.5 SNS1/SNS2

The SNS pin (SNS1 or SNS2) is connected to the output of the device to provide feedback to the control circuitry. A minimum of a 2.2 µF bypass capacitor should be connected in shunt with each output. Based upon size, performance, and cost, a TDK C1608X5R0J475K size 0603 4.7 µF ceramic capacitor is highly recommended for most applications.

In order to reduce parasitic inductance, it is good practice to place the output bypass capacitor as close to the inductor as possible. The SNS connection should be placed close to the output bypass capacitor.

4.6 PGND

The power ground (PGND) is the ground path for the high current in PWM mode. The current loop for the power ground should be as small as possible and separate from the analog ground (AGND) loop.

4.7 AGND

The signal ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the power ground (PGND) loop.

4.8 FB1/FB2 (Adjustable Output Only)

The feedback pins (FB1/FB2) are two extra pins that can only be found on the MIC23250-AAYMT devices. They allow the regulated output voltage to be set by applying an external resistor network. The internal reference voltage is 0.72V and the recommended value of RBOTTOM is within 10% of 442kΩ.

The RTOP resistor is the resistor from the FB pin to the output of the device and RBOTTOM is the resistor from the FB pin to ground. The output voltage is calculated from the equation below. See Section 5.4, Compensation for recommended feedback component values.

EQUATION 4-1:

$$V_{OUT} = 0.72V \times \left(\frac{R_{TOP}}{R_{BOTTOM}} + 1\right)$$

5.0 APPLICATION INFORMATION

The MIC23250 is designed for high performance with a small solution size. With dual 400 mA outputs in a tiny 2 mm x 2 mm UDFN package and requiring only six external components, the MIC23250 meets today's needs for miniature portable electronic devices. While small solution size is one of its advantages, the MIC23250 is big on performance.

Using the HyperLight Load™ switching scheme, the MIC23250 is able to maintain high efficiency throughout the entire load range while providing ultra-fast load transient response. Even with all the given benefits, the MIC23250 can be as easy to use as linear regulators. The following sections provide an overview of implementing the MIC23250 in related applications

5.1 Input Capacitor

A minimum of a 2.2 µF ceramic capacitor should be placed close to the VIN and PGND pins for bypassing. A TDK C1608X5R0J475K size 0603 4.7 µF ceramic capacitor is recommended based upon performance, size and cost. A X5R or X7R temperature rating is recommended for the input capacitor.

Y5V temperature rating capacitors, aside from losing most of their capacitance over temperature, can also become resistive at high frequencies. This reduces their ability to filter out high-frequency noise.

5.2 Output Capacitor

The MIC23250 was designed for use with a 2.2 µF or greater ceramic output capacitor. Increasing the output capacitance will lower output ripple and improve load transient response but could increase solution size or cost.

A low equivalent series resistance (ESR) ceramic output capacitor, such as the TDK C1608X5R0J475K size 0603 4.7 µF ceramic capacitor, is recommended based upon performance, size and cost.

Either the X7R or X5R temperature rating capacitors are recommended. The Y5V and Z5U temperature rating capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies.

5.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC23250 was designed for use with an 0.47 µH to 4.7 µH inductance range. Typically, a 1 µH inductor is recommended for a balance of transient response, efficiency, and output ripple. For faster transient response, a 0.47 µH inductor may be used. For lower output ripple, a 4.7 µH inductor is recommended.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or for a 10% to 20% loss in inductance.

Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin so that the peak current of the inductor does not cause it to saturate. Peak current can be calculated as follows:

EQUATION 5-1:

$$I_{PEAK} = \left[I_{OUT} + V_{OUT} \times \left(\frac{1 - V_{OUT}/V_{IN}}{2 \times f \times L}\right)\right]$$

As shown by Equation 5-1, the peak inductor current is inversely proportional to the switching frequency and the inductance; the lower the switching frequency or the inductance, the higher the peak current. As input voltage increases, the peak current also increases.

The size of the inductor depends on the requirements of the application. Refer to the Typical Application Circuits and Bill of Material for details.

DC resistance (DCR) is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to Section 5.5, Efficiency Considerations.

5.4 Compensation

The MIC23250 is designed to be stable with a 0.47 µH to 4.7 µH inductor with a minimum of 2.2 µF ceramic (X5R) output capacitor.

For the adjustable MIC23250, the total feedback resistance should be kept around 1 MΩ to reduce current loss down the feedback resistor network. This helps to improve efficiency. A feed-forward capacitor (CFF) of 120 pF must be used in conjunction with the external feedback resistors to reduce the effects of parasitic capacitance that is inherent in most circuit board layouts.

Figure 5-1 and Table 5-1 show the recommended feedback resistor values along with the recommended feed-forward capacitor values for the MIC23250 adjustable device.

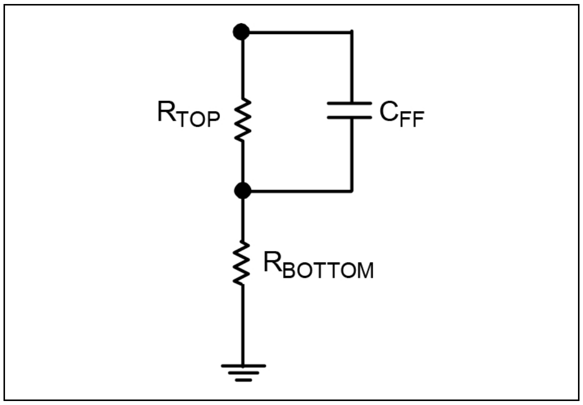


FIGURE 5-1: *Feedback Resistor Network.*

TABLE 5-1: RECOMMENDED FEEDBACK COMPONENT VALUES

V_{OUT} (V)	R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	CFF (pF)
0.8	49	442	120
0.9	111	442	120
1	172	442	120
1.1	233	442	120
1.2	295	442	120
1.3	356	442	120
1.4	417	442	120
1.5	479	442	120
1.6	540	442	120
1.7	602	442	120
1.8	663	442	120
1.9	724	442	120
2	786	442	120
2.1	847	442	120
2.2	909	442	120
2.3	970	442	120
2.4	1031	442	120
2.5	1093	442	120
2.6	1154	442	120
2.7	1216	442	120
2.8	1277	442	120
2.9	1338	442	120
3	1400	442	120
3.1	1461	442	120
3.2	1522	442	120
3.3	1584	442	120

5.5 Efficiency Considerations

Efficiency is defined as the amount of useful output power divided by the amount of power supplied.

EQUATION 5-2:

$$\text{Efficiency\%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}}\right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations, and it reduces current consumption for battery-powered applications. Reduced current draw from a battery increases the device's operating time and is critical in handheld devices.

There are two types of losses in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high-side MOSFET R_{DSON} multiplied by the switch current squared.

During the off cycle, the low-side N-channel MOSFET conducts and also dissipates power. The device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss. The current required to drive the gates on and off at a constant 4 MHz frequency, as well as the switching transitions, make up the switching losses.

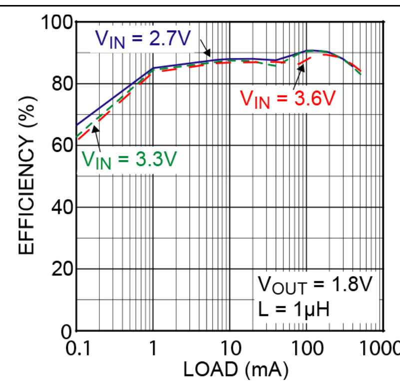


FIGURE 5-2: *Efficiency V_{OUT} = 1.8V.*

Figure 5-2 shows an efficiency curve. From no load to 100 mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By using the HyperLight Load™ mode, the MIC23250 is able to maintain high efficiency at low output currents. Over 100 mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses.

Higher input supply voltages will increase the gate-to-source voltage on the internal MOSFETs, thereby reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All losses except for the inductor losses are inherent to the device. Therefore, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

EQUATION 5-3:

$$\text{DCR Loss} = I_{OUT}^2 \times DCR$$

From this, the loss in efficiency due to inductor resistance can be calculated as follows:

EQUATION 5-4:

$$\text{Efficiency Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L\_P_D}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load increases. In this case, inductor selection becomes a trade-off between efficiency and size.

5.6 HyperLight Load Mode™

The MIC23250 uses a minimum on and off time proprietary control loop. When the output voltage falls below the regulation threshold, the error comparator begins a switching cycle that turns the PMOS on and keeps it on for the duration of the minimum-on-time. This increases the output voltage. If the output voltage is over the regulation threshold, then the error comparator turns the PMOS off for a minimum-off-time until the output drops below the threshold.

The NMOS acts as an ideal rectifier that conducts when the PMOS is off. Using a NMOS switch instead of a diode allows for lower voltage drop across the switching device when it is on.

The asynchronous switching combination between the PMOS and the NMOS allows the control loop to work in discontinuous mode for light load operations.

In discontinuous mode, the MIC23250 works in pulse frequency modulation (PFM) to regulate the output. As the output current increases, the off-time decreases, thus providing more energy to the output. This switching scheme improves the efficiency of the MIC23250 during light load currents by switching only when needed. As the load current increases, the MIC23250 enter Continuous Conduction mode (CCM) and switches at a frequency centered at 4 MHz.

The equation to calculate the load when the MIC23250 enters Continuous Conduction mode can be approximated by the following formula:

EQUATION 5-5:

$$I_{LOAD} > \left(\frac{(V_{IN} - V_{OUT}) \times D}{2L \times f}\right)$$

As shown in the previous equation, the load at which MIC23250 transitions from HyperLight Load™ mode to PWM mode is a function of the input voltage (V_{IN}), output voltage (V_{OUT}), duty cycle (D), inductance (L) and frequency (f). This is illustrated in the graph below.

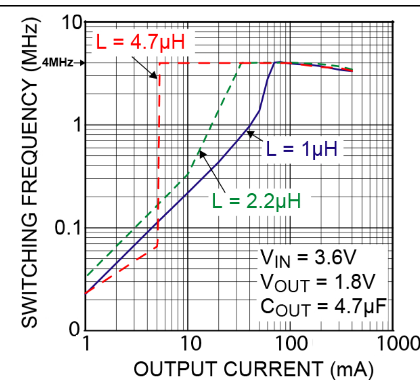


FIGURE 5-3: *Switching Frequency vs. Output Current.*

Since the inductance range of MIC23250 is from 0.47 µH to 4.7 µH, the device may then be tailored to enter HyperLight Load™ mode or PWM mode at a specific load current by selecting the appropriate inductance. For example, in the graph below, when the inductance is 4.7 µH the MIC23250 will transition into PWM mode at a load of approximately 5 mA. Under the same condition, when the inductance is 1 µH, the MIC23250 will transition into PWM mode at approximately 70 mA.

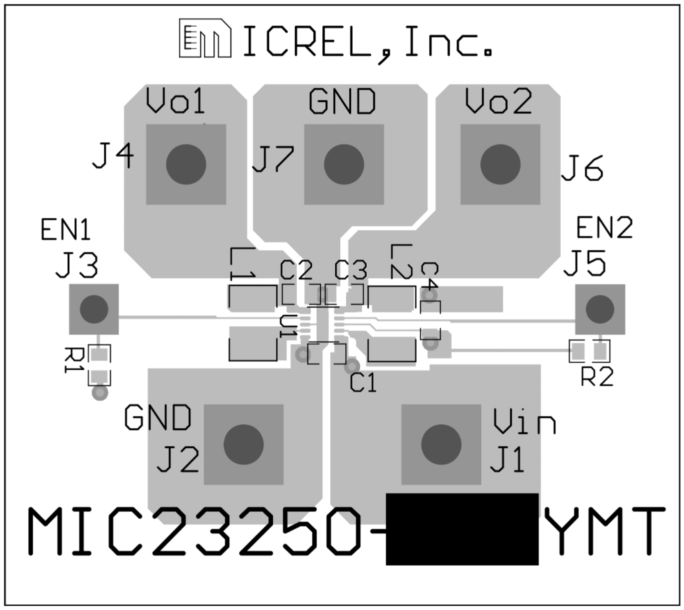
Bill of Material (Fixed Output)

Item	Part Number	Manufacturer	Description	Qty
C1, C2, C3	C1608X5R0J475K	TDK	4.7 µF Ceramic Capacitor, 6.3V, X5R, Size 0603	3
C4	VJ0603Y103KXXAT	Vishay®	0.01 µF Ceramic Capacitor, 25V, X7R, Size 0603	1
R1, R2	CRCW06031002FKEA	Vishay	10 kΩ, 1%, 1/16W, Size 0603	Optional
L1, L2	LQM21PN1R0MC0D	Murata®	1 µH, 0.8A, 190 mΩ, L2 mm × W1.25 mm × H0.5 mm	2
	LQH32CN1R0M33	Murata	1 µH, 1A, 60 mΩ, L3.2 mm x W2.5 mm x H2.0 mm	
	LQM31PN1R0M00	Murata	1 µH, 1.2A, 150 mΩ, L3.2 mm x W1.6 mm x H0.95 mm	
	LQM31PNR47M00	Murata	0.47 µH, 1.4A, 80 mΩ, L3.2 mm x W1.6 mm x H0.85 mm	
	MIPF2520D1R5	FDK	1.5 µH, 1.5A, 70 mΩ, L2.5 mm x W2 mm x H1.0 mm	
	EPL2010-102	Coilcraft	1.0 µH, 1.0A, 86 mΩ, L2.0 mm x W1.8 mm x H1.0 mm	
U1	MIC23250-xxYMT	Microchip	4 MHz Dual 400 mA Fixed Output Buck Regulator with HyperLight Load™ Mode	1

Bill of Material (Adjustable Output)

Item	Part Number	Manufacturer	Description	Qty
C1, C2, C3	C1608X5R0J475K	TDK	4.7 µF Ceramic Capacitor, 6.3V, X5R, Size 0603	3
C4	VJ0603Y103KXXAT	Vishay	0.01 µF Ceramic Capacitor, 25V, X7R, Size 0603	1
C5, C6	VJ0603Y121KXAAT	Vishay	120 pF Ceramic Capacitor, 50V, X7R, Size 0603	2
R1, R2	CRCW06031002FKEA	Vishay	10 kΩ, 1%, 1/16W, Size 0603	Optional
R3, R4	CRCW06036653FKEA	Vishay	665 kΩ, 1%, 1/16W, Size 0603	2
R5, R6	CRCW06034423FKEA	Vishay	442 kΩ, 1%, 1/16W, Size 0603	2
L1, L2	LQM21PN1R0MC0D	Murata	1 µH, 0.8A, 190 mΩ, L2.0 mm x W1.25 mm x H0.5 mm	2
	LQH32CN1R0M33	Murata	1 µH, 1A, 60 mΩ, L3.2 mm x W2.5 mm x H2.0 mm	
	LQM31PN1R0M00	Murata	1 µH, 1.2A, 150 mΩ, L3.2 mm x W1.6 mm x H0.95 mm	
	LQM31PNR47M00	Murata	0.47 µH, 1.4A, 80 mΩ, L3.2 mm x W1.6 mm x H0.85 mm	
	MIPF2520D1R5	FDK	1.5 µH, 1.5A, 70 mΩ, L2.5 mm x W2.0 mm x H1.0 mm	
	EPL2010-102	Coilcraft	1.0 µH, 1.0A, 86 mΩ, L2.0 mm x W1.8 mm x H1.0 mm	
U1	MIC23250-AAYMT	Microchip	4 MHz Dual 400 mA Adjustable Output Buck Regulator with HyperLight Load™ Mode	1

PCB LAYOUT RECOMMENDATIONS (FIXED OUTPUT)



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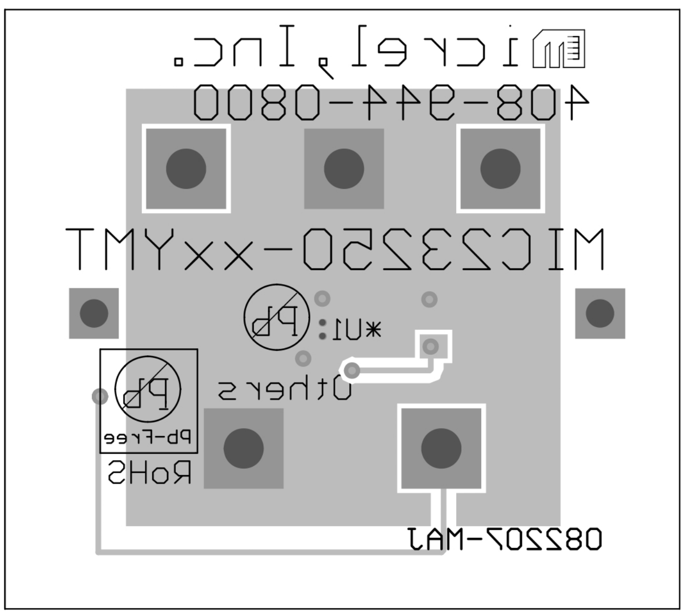

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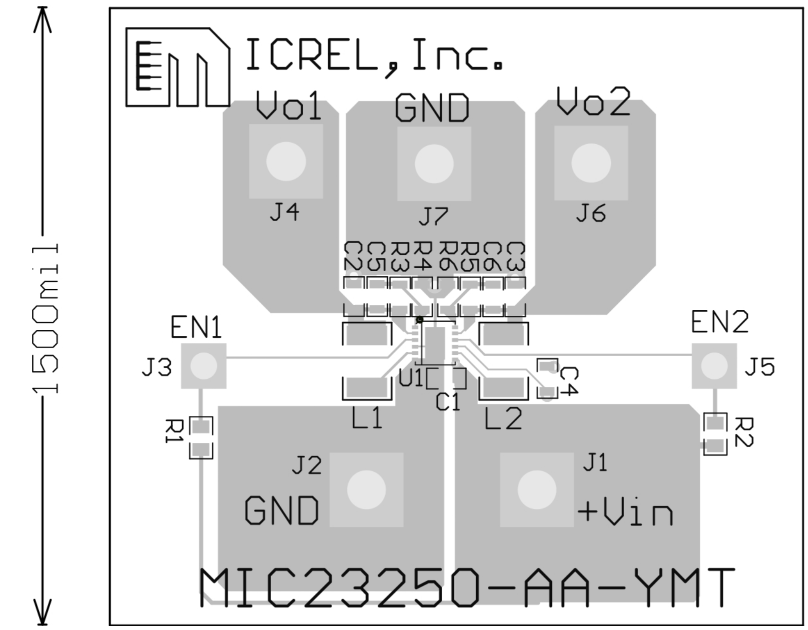
PCB LAYOUT RECOMMENDATIONS (ADJUSTABLE OUTPUT)



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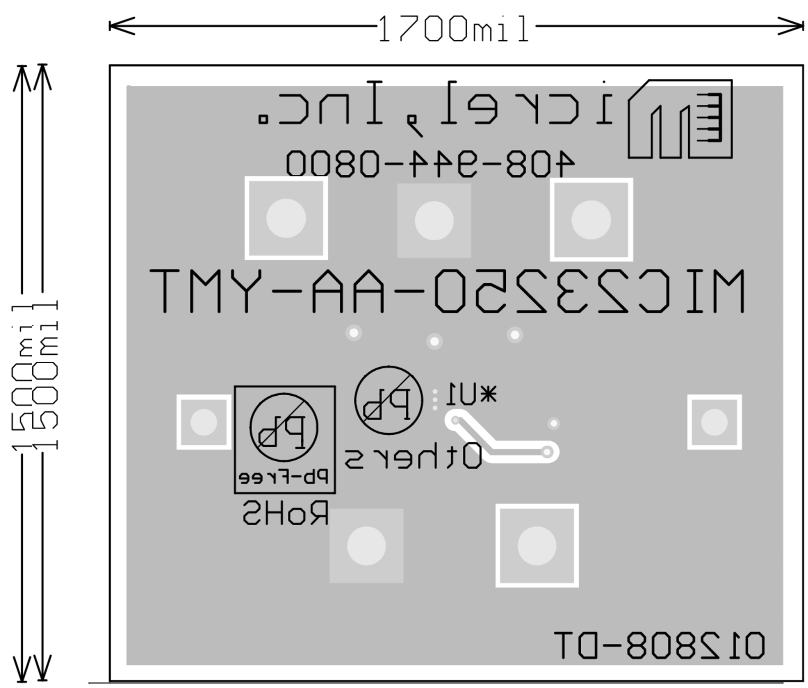

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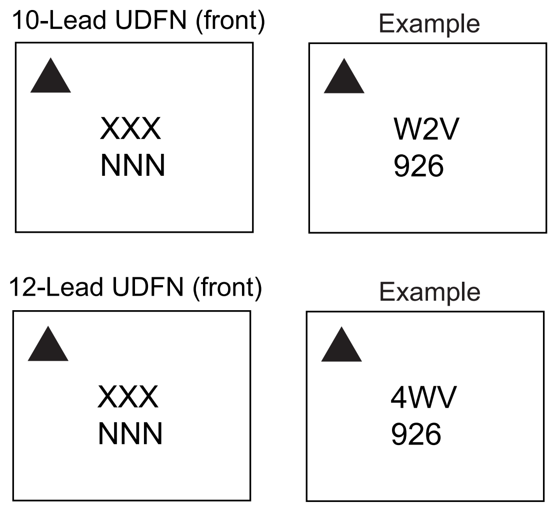
6.0 PACKAGING INFORMATION

6.1 Package Marking Information



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

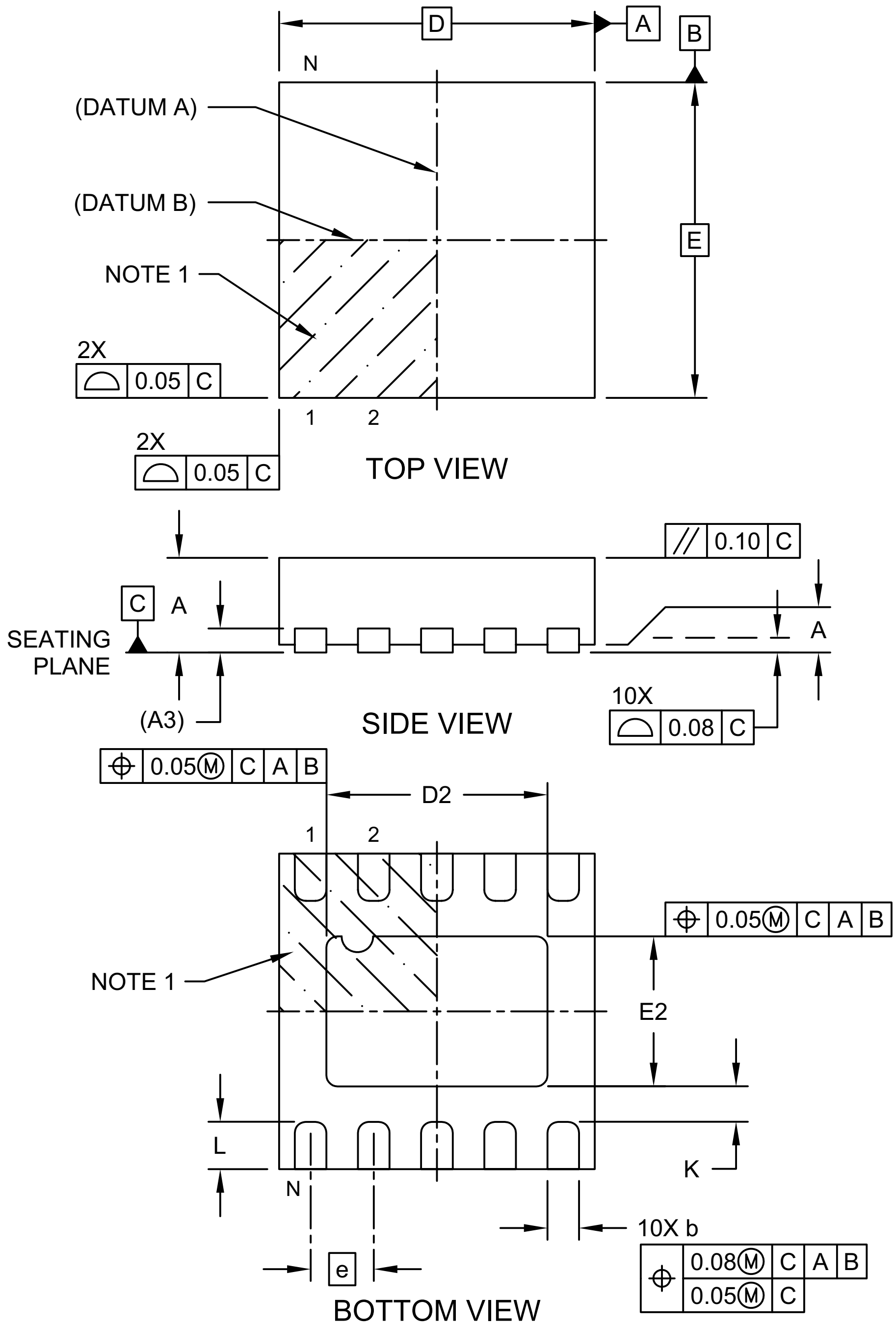
Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N.

MARKING CODES

Part Number	Marking Code	Nominal Output Voltage 1	Nominal Output Voltage 2	Package
MIC23250-W4YMT-TR	WV4	1.2V	1.6V	10-Lead 2.0 mm × 2.0 mm UDFN
MIC23250-G4YMT-TR	WV5	1.2V	1.8V	10-Lead 2.0 mm × 2.0 mm UDFN
MIC23250-S4YMT-TR	1WV	1.2V	3.3V	10-Lead 2.0 mm × 2.0 mm UDFN
MIC23250-SKYMT-TR	5WV	2.6V	3.3V	10-Lead 2.0 mm × 2.0 mm UDFN
MIC23250-AAYMT-TR	4WV	ADJ	ADJ	12-Lead 2.5 mm × 2.5 mm UDFN
MIC23250-M4YMT-TR	W2V	1.2V	2.8V	10-Lead 2.0 mm × 2.0 mm UDFN
MIC23250-F4YMT-TR	BWV	1.2V	1.5V	10-Lead 2.0 mm × 2.0 mm UDFN

10-Lead 2.0 mm × 2.0 mm UDFN Package Outline and Recommended Land Pattern

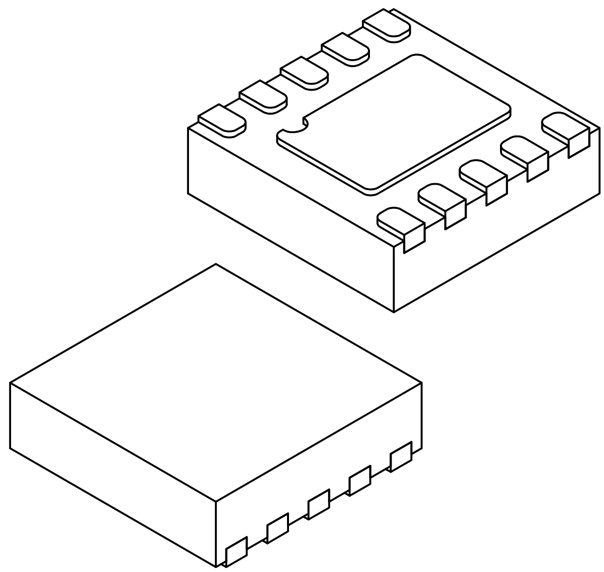
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1155 Rev A Sheet 1 of 2

10-Lead 2.0 mm × 2.0 mm UDFN Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.35	1.40	1.45
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.90	0.95	1.00
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	K	0.20	-	-

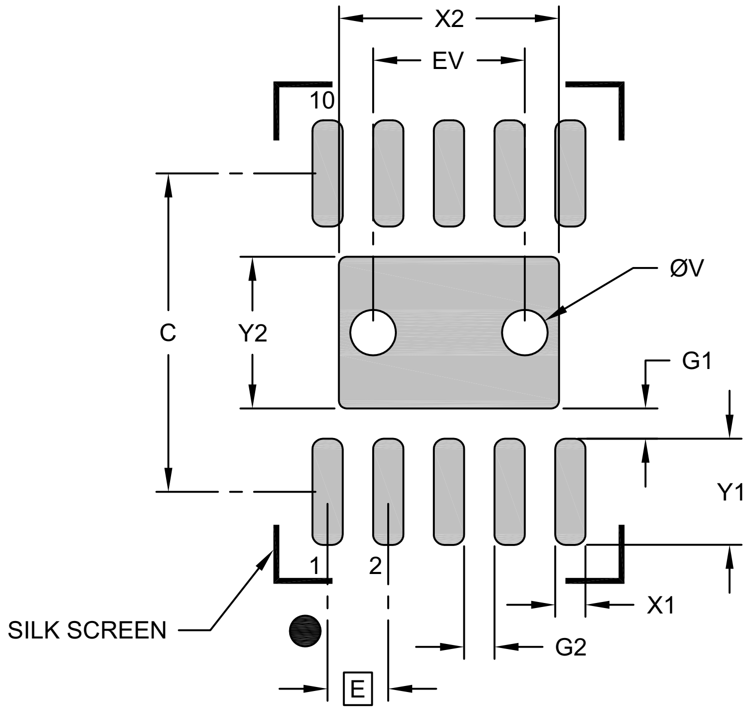
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1155 Rev A Sheet 2 of 2

10-Lead 2.0 mm × 2.0 mm UDFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Center Pad Width	X2			1.45
Center Pad Length	Y2			1.00
Contact Pad Spacing	C		2.10	
Contact Pad Width (X10)	X1			0.20
Contact Pad Length (X10)	Y1			0.70
Contact Pad to Center Pad (X10)	G1	0.20		
Contact Pad to Contact Pad (X8)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

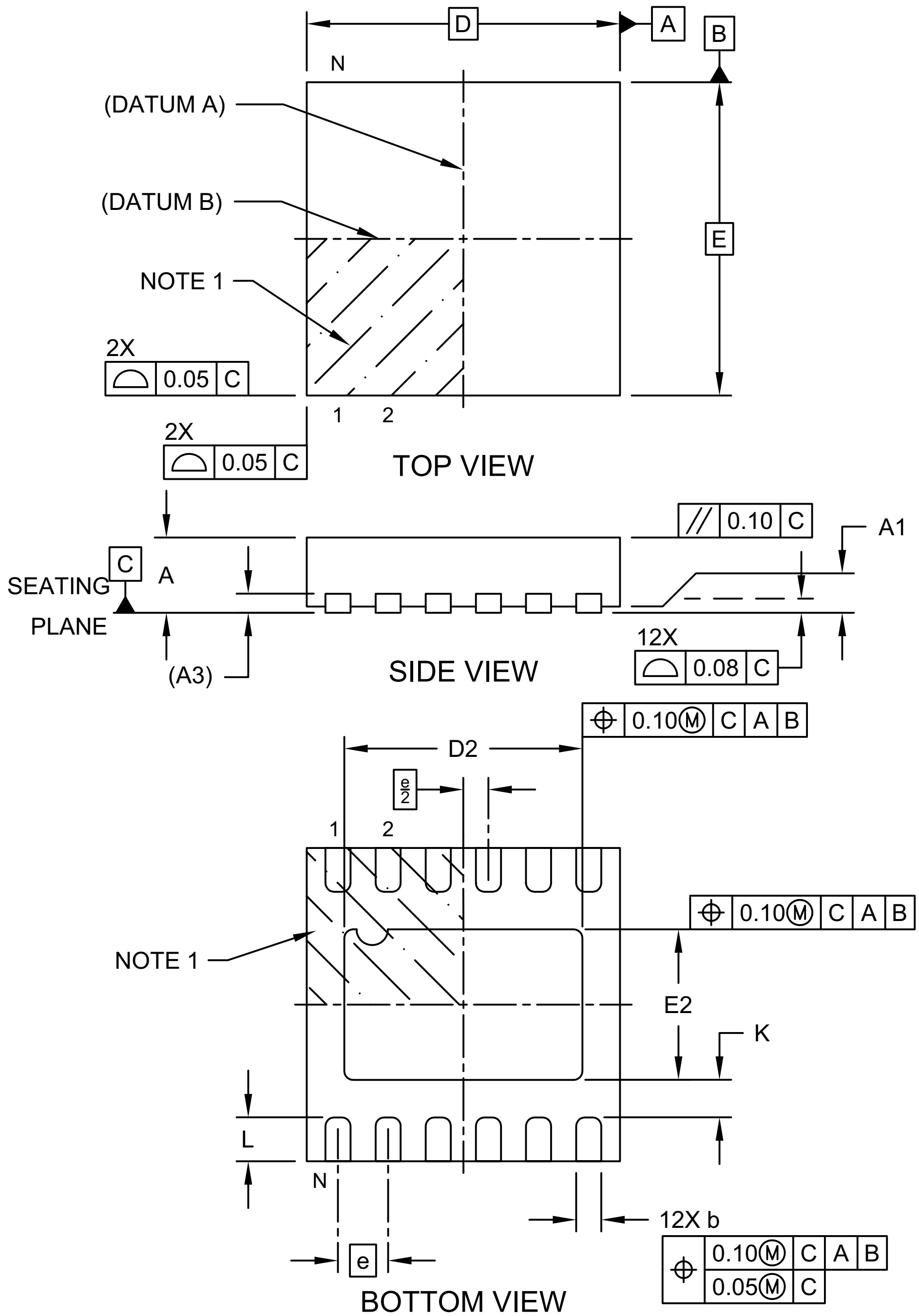
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3155 Rev A

12-Lead 2.5 mm × 2.5 mm UDFN Package Outline and Recommended Land Pattern

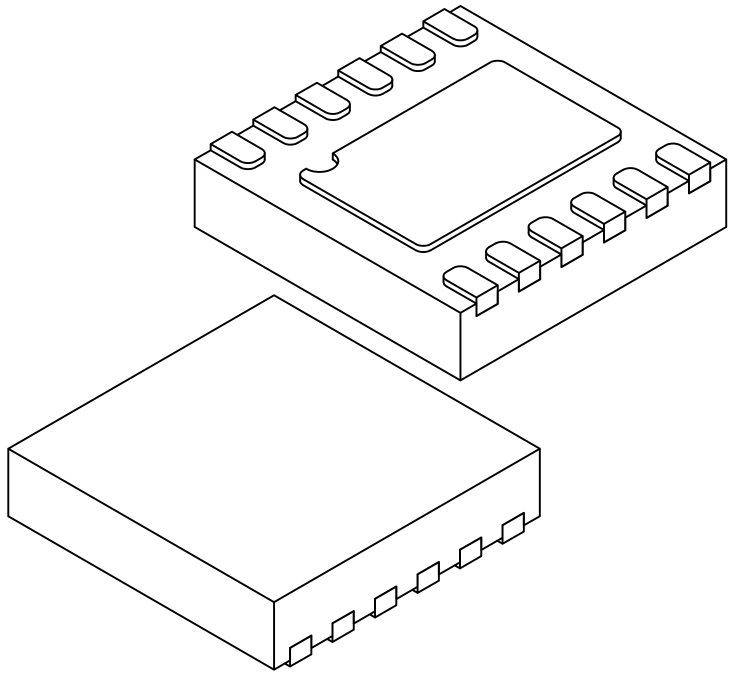
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1162 Rev A Sheet 1 of 2

12-Lead 2.5 mm × 2.5 mm UDFN Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		12	
Pitch	e		0.40 BSC	
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.152 REF	
Overall Length	D		2.50 BSC	
Exposed Pad Length	D2	1.85	1.90	1.95
Overall Width	E		2.50 BSC	
Exposed Pad Width	E2	1.15	1.20	1.25
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.30	0.35	0.40
Terminal-to-Exposed-Pad	K	0.20	-	-

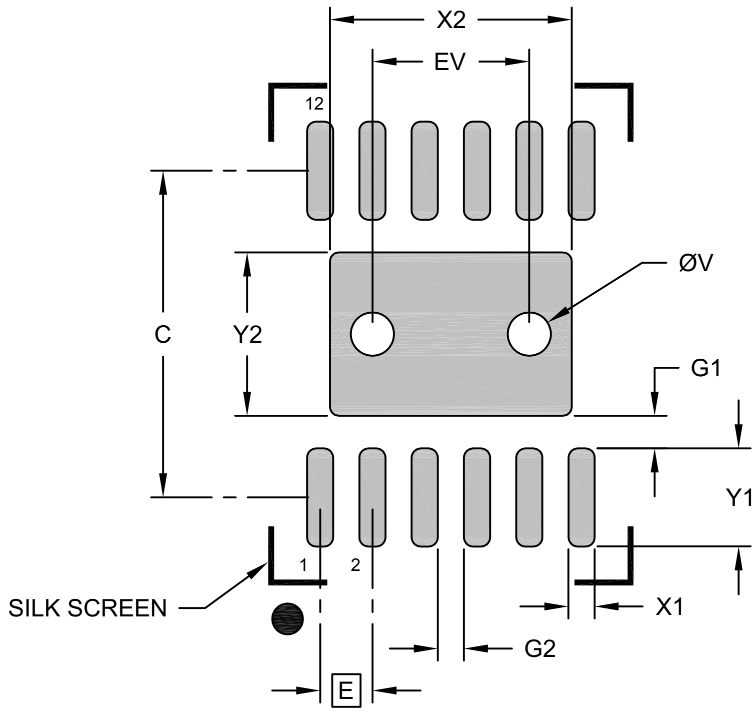
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1162 Rev A Sheet 1 of 2

12-Lead 2.5 mm × 2.5 mm UDFN Package Outline and Recommended Land Pattern

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			1.95
Optional Center Pad Length	Y2			1.25
Contact Pad Spacing	C		2.50	
Contact Pad Width (X12)	X1			0.20
Contact Pad Length (X12)	Y1			0.75
Contact Pad to Center Pad (X12)	G1	0.25		
Contact Pad to Contact Pad (X10)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3162 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (July 2025)

- Updated ESD Rating in Section , Absolute Maximum Ratings †.

Revision A (June 2025)

- Converted Micrel document MIC23250 to Microchip data sheet DS20006787A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part Number	-XX or -XXX	X	XX	-XX
Device	Output Voltage	Junction Temp. Range	Package	Media Type

Device: MIC23250: 4 MHz Dual 400 mA Synchronous Buck Regulator with HyperLight Load™

Output Voltage:
- -AA = Adjustable Nominal Output Voltage 1 and 2
- -SK = 2.6V/3.3V
- -G4 = 1.2V/1.8V
- -M4 = 1.2V/2.8V
- -W4 = 1.2V/1.6V
- -F4 = 1.2V/1.5V
- -S4 = 1.2V/3.3V

Junction Temperature Range: Y = –40°C to +125°C

Pack0age: MT = UDFN (12-Lead has adjustable dual output voltages; all others are 10-Lead)

Media Type: TR = 5000/Reel

Examples:

a) MIC23250-AAYMT-TR: MIC23250, Adjustable Output Voltage, -40°C to +125°C Temp. Range, 12-Lead UDFN, 5000/Reel

b) MIC23250-SKYMT-TR: MIC23250, 2.6V/3.3V Output Voltage, -40°C to +125°C Temp. Range, 12-Lead UDFN, 5000/Reel

c) MIC23250-W4YMT-TR: MIC23250, 1.2V/1.6V Output Voltage, -40°C to +125°C Temp. Range, 10-Lead UDFN, 5000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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