FAIRCHILD SEMICONDUCTOR®

Mar 2009

QFET™

# FQD20N06L / FQU20N06L

## 60V LOGIC N-Channel MOSFET

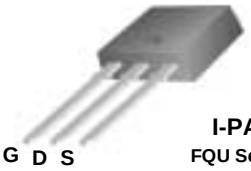
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

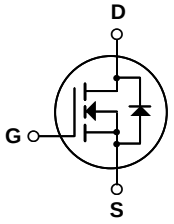
### Features

- 17.2A, 60V, $R_{DS(on)}$ = 0.06Ω @ $V_{GS}$ = 10V
- Low gate charge ( typical 9.5 nC)
- Low Crss ( typical 35 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 150°C maximum junction temperature rating
- Low level gate drive requirements allowing direct operation form logic drivers


D-PAK
FQD Series




I-PAK
FQU Series




## Absolute Maximum Ratings

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | | FQD20N06L / FQU20N06L | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 60 | V |
| $I_D$ | Drain Current - Continuous ($T_C$ = 25°C) | | 17.2 | A |
| | - Continuous ($T_C$ = 100°C) | | 10.9 | A |
| $I_{DM}$ | Drain Current - Pulsed | (Note 1) | 68.8 | A |
| $V_{GSS}$ | Gate-Source Voltage | | ± 20 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy | (Note 2) | 170 | mJ |
| $I_{AR}$ | Avalanche Current | (Note 1) | 17.2 | A |
| $E_{AR}$ | Repetitive Avalanche Energy | (Note 1) | 3.8 | mJ |
| dv/dt | Peak Diode Recovery dv/dt | (Note 3) | 7.0 | V/ns |
| $P_D$ | Power Dissipation ($T_A$ = 25°C) * | | 2.5 | W |
| | Power Dissipation ($T_C$ = 25°C) | | 38 | W |
| | - Derate above 25°C | | 0.30 | W/°C |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | -55 to +150 | °C |
| $T_L$ | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | °C |

## Thermal Characteristics

| Symbol | Parameter | Typ | Max | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | -- | 3.28 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient * | -- | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | -- | 110 | °C/W |

* When mounted on the minimum pad size recommended (PCB Mount)

## Electrical Characteristics

$T_C$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 60 | -- | -- | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | -- | 0.06 | -- | V/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | -- | -- | 1 | μA |
| | | $V_{DS}$ = 48 V, $T_C$ = 125°C | -- | -- | 10 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | -- | -- | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | -- | -- | -100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.0 | -- | 2.5 | V |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 8.6 A | -- | 0.046 | 0.06 | Ω |
| | | $V_{GS}$ = 5 V, $I_D$ = 8.6 A | -- | 0.057 | 0.075 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 25 V, $I_D$ = 8.6 A (Note 4) | -- | 11 | -- | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1.0 MHz | -- | 480 | 630 | pF |
| $C_{oss}$ | Output Capacitance | | -- | 175 | 230 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 35 | 45 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 10.5 A, $R_G$ = 25 Ω (Note 4, 5) | -- | 10 | 30 | ns |
| $t_r$ | Turn-On Rise Time | | -- | 165 | 340 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 35 | 80 | ns |
| $t_f$ | Turn-Off Fall Time | | -- | 70 | 150 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 48 V, $I_D$ = 21 A, $V_{GS}$ = 5 V (Note 4, 5) | -- | 9.5 | 13 | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 2.5 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 5.5 | -- | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | -- | -- | 17.2 | A |
| $I_{SM}$ | Maximum Pulsed Drain-Source Diode Forward Current | | -- | -- | 68.8 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 17.2 A | -- | -- | 1.5 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_F$ = 21 A, $dI_F$ / dt = 100 A/μs (Note 4) | -- | 54 | -- | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 75 | -- | nC |

**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 670μH, $I_{AS}$ = 17.2A, $V_{DD}$ = 25V, $R_G$ = 25 Ω, Starting $T_J$ = 25°C
3. $I_{SD}$ ≤ 21A, di/dt ≤ 300A/μs, $V_{DD}$ ≤ $BV_{DSS}$, Starting $T_J$ = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

## Typical Characteristics

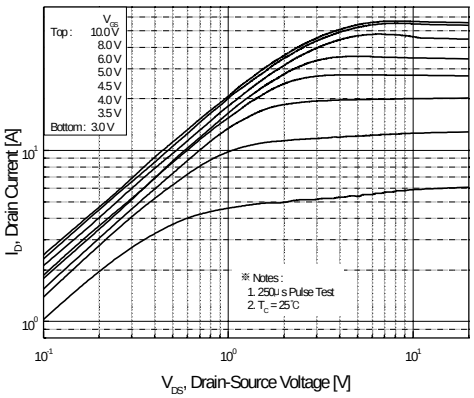



**Figure 1. On-Region Characteristics**

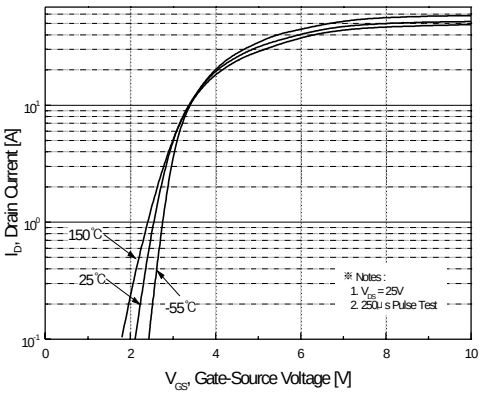



**Figure 2. Transfer Characteristics**

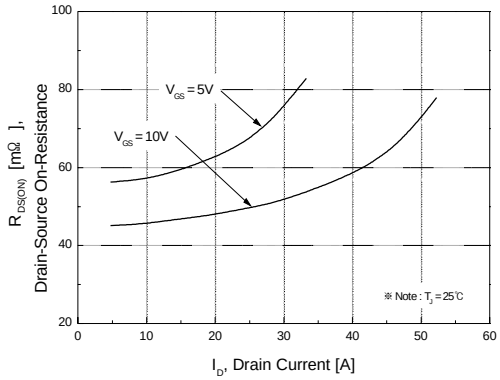



**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

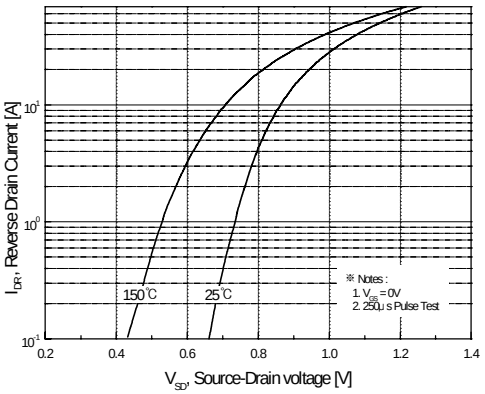



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

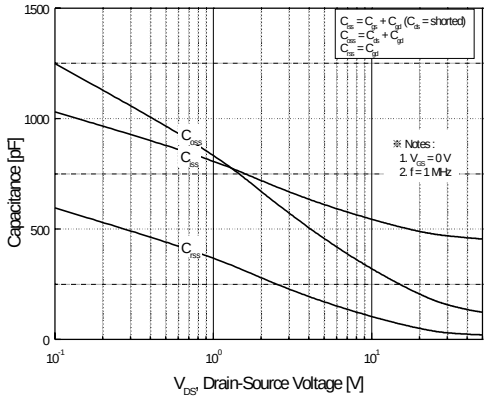



**Figure 5. Capacitance Characteristics**

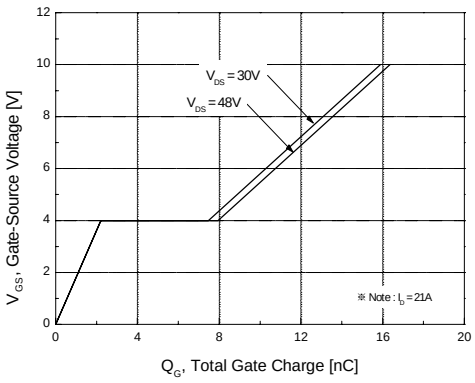



**Figure 6. Gate Charge Characteristics**

## Typical Characteristics (Continued)

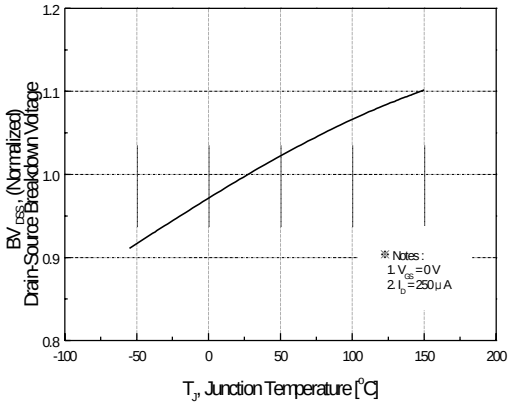



**Figure 7. Breakdown Voltage Variation vs. Temperature**

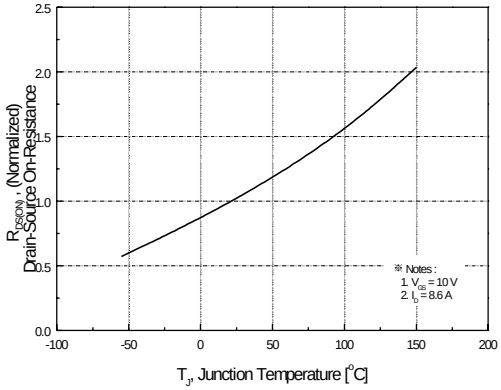



**Figure 8. On-Resistance Variation vs. Temperature**

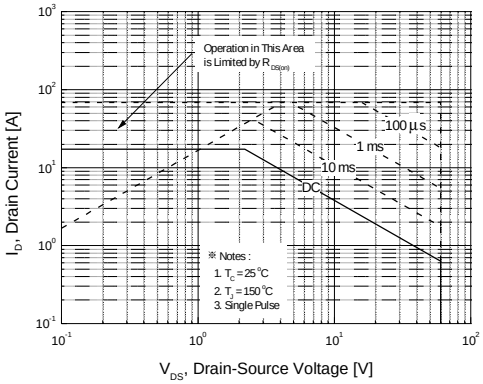



**Figure 9. Maximum Safe Operating Area**

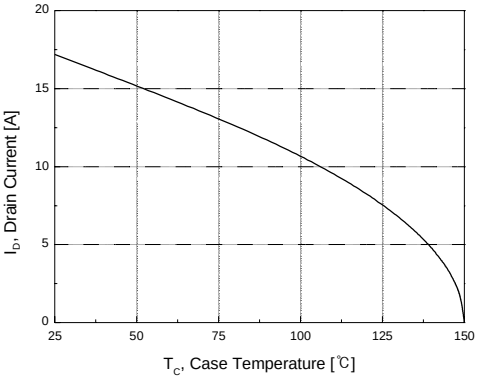



**Figure 10. Maximum Drain Current vs. Case Temperature**

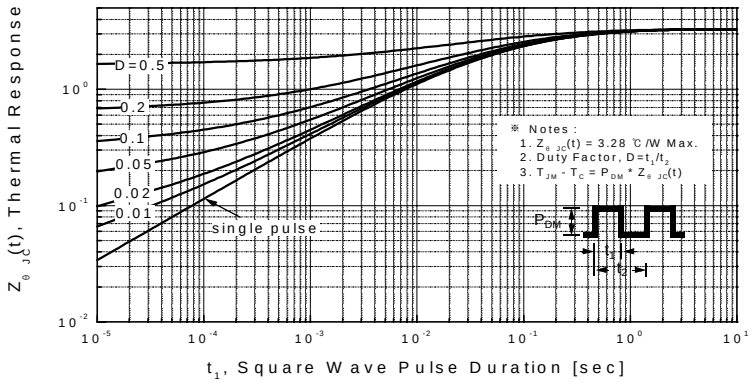
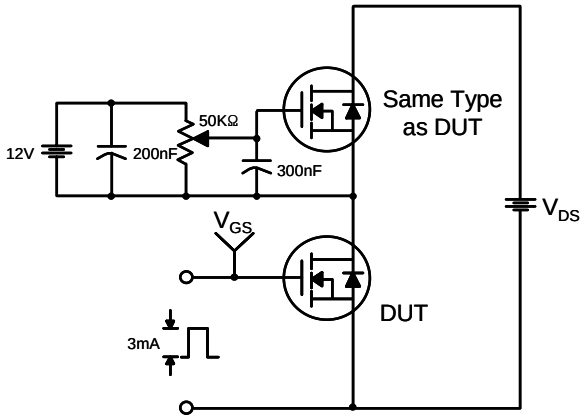
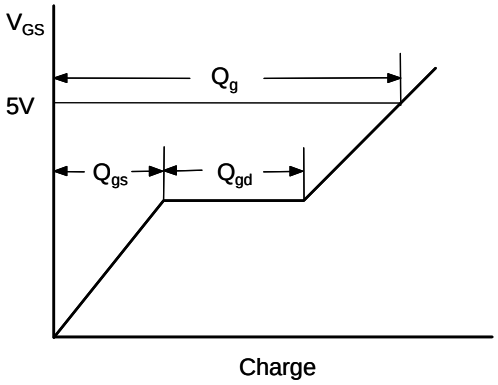


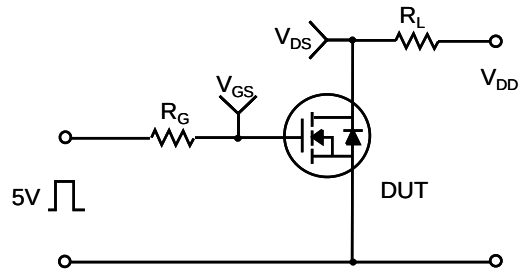

**Figure 11. Transient Thermal Response Curve**

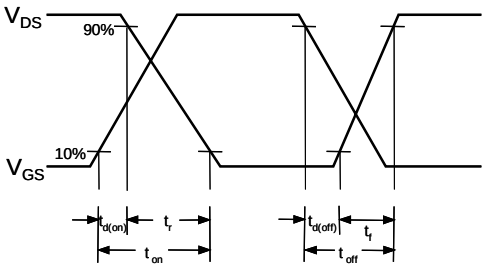
### Gate Charge Test Circuit & Waveform



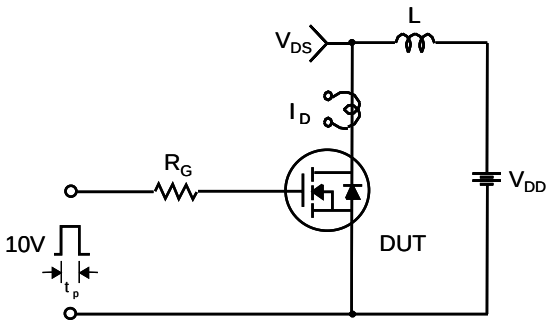




### Resistive Switching Test Circuit & Waveforms

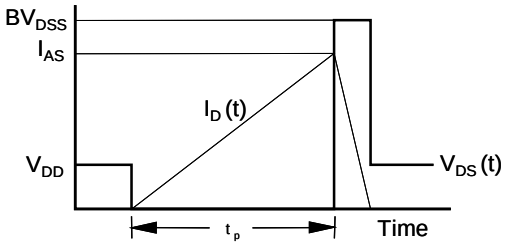


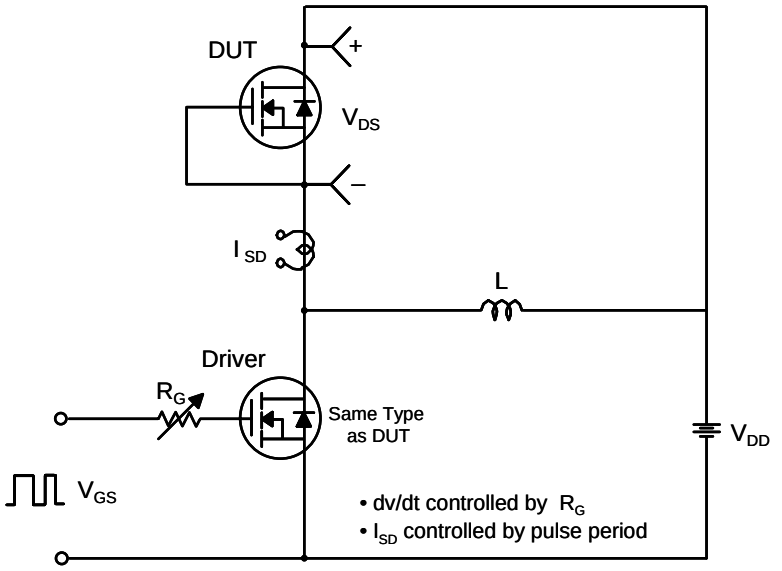

### Unclamped Inductive Switching Test Circuit & Waveforms

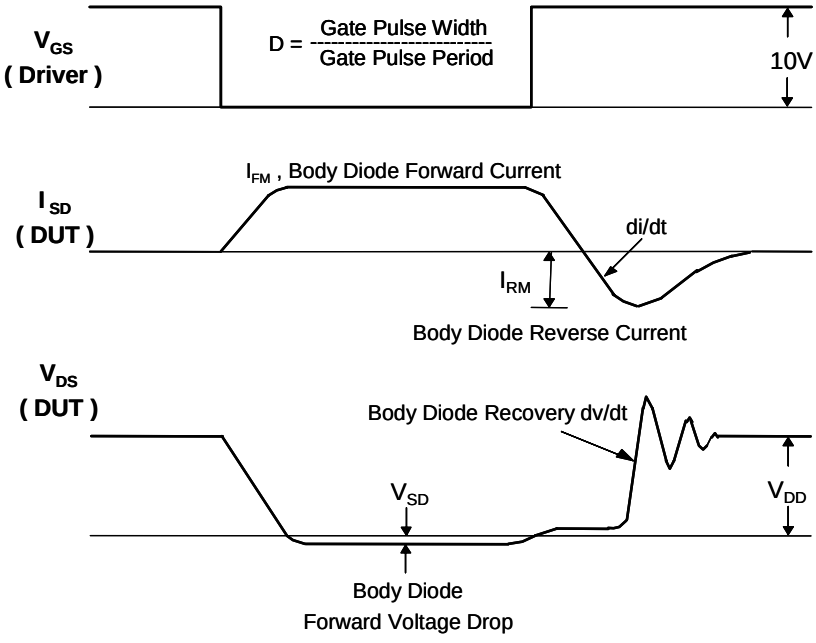



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



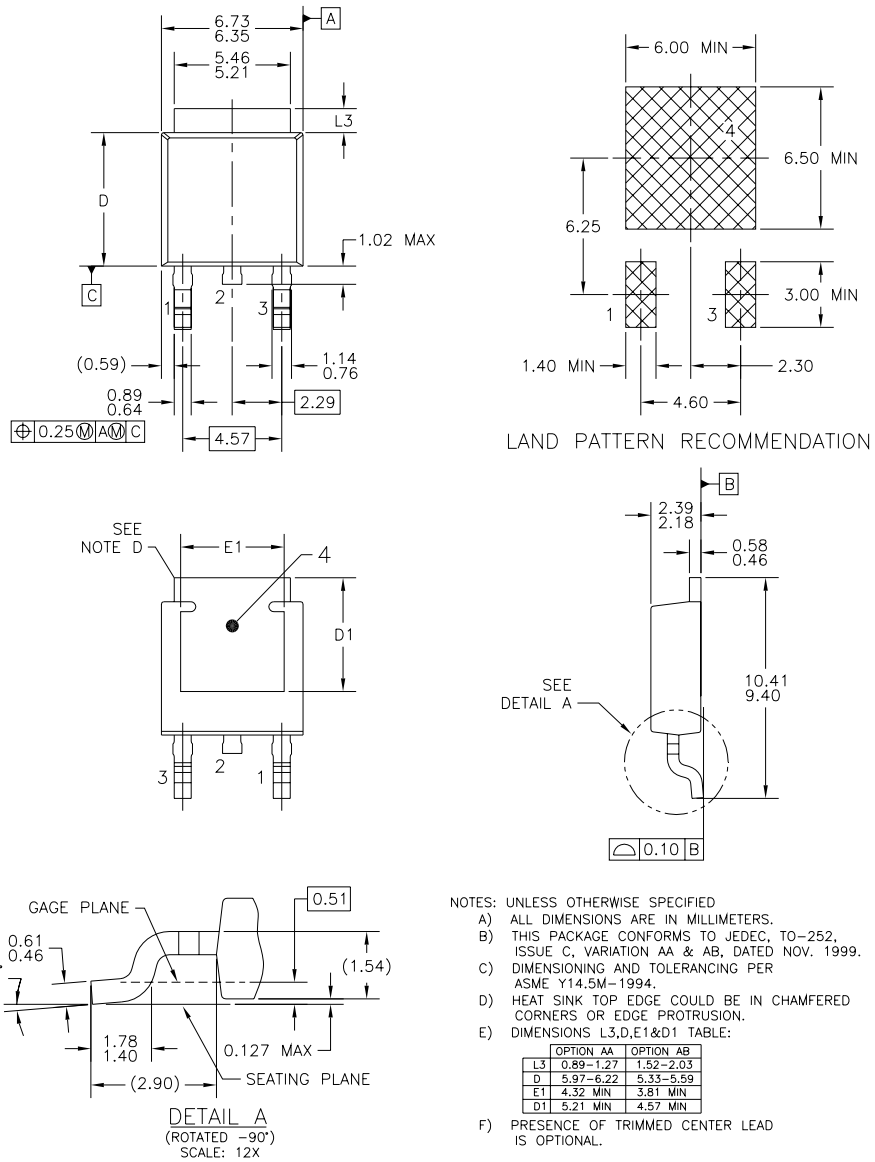
**Peak Diode Recovery dv/dt Test Circuit & Waveforms**



## Mechanical Dimensions

# D-PAK

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B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

E) DIMENSIONS L3,D,E1&D1 TABLE:

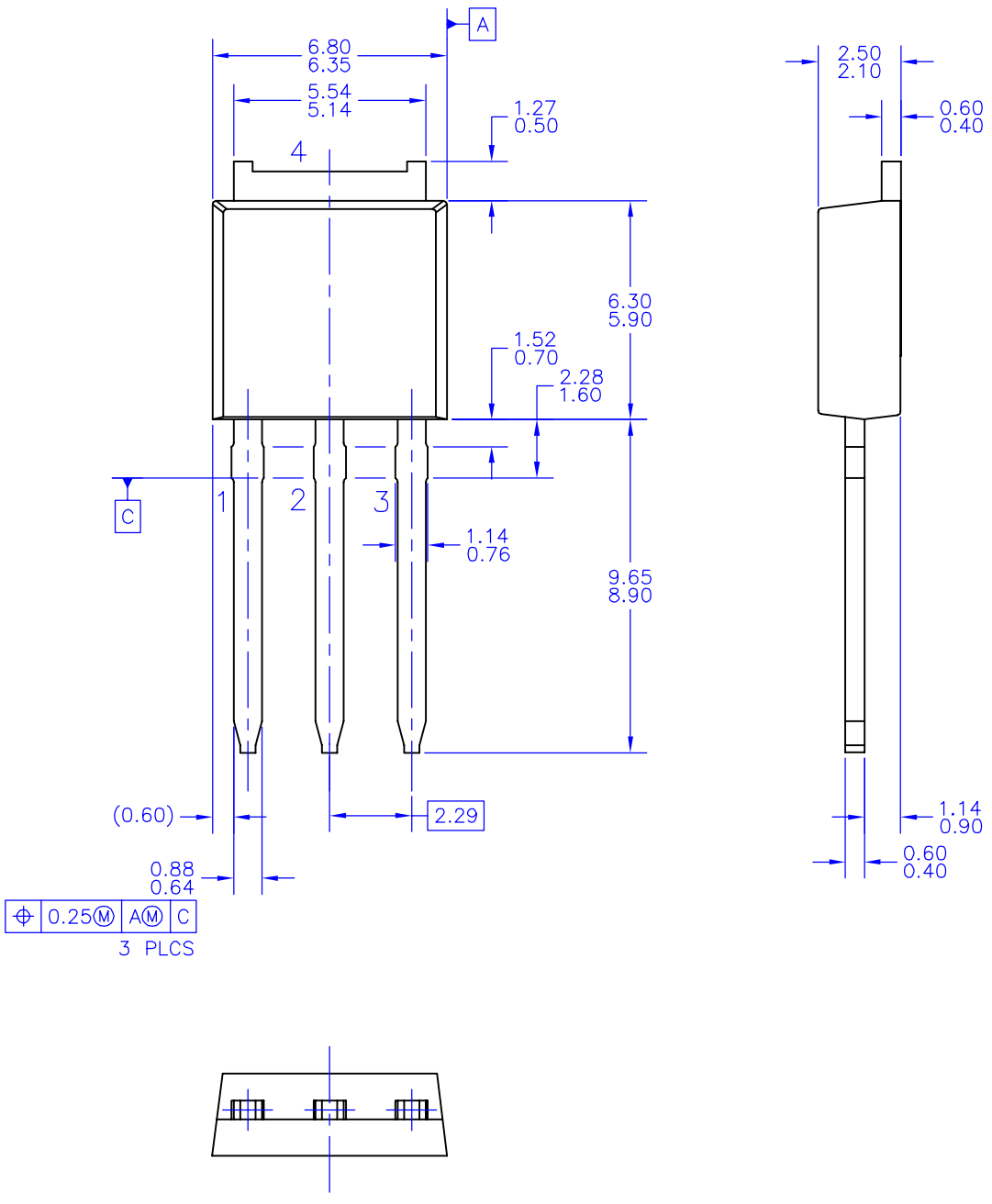
| | OPTION AA | OPTION AB |
|---|---|---|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN | 3.81 MIN |
| D1 | 5.21 MIN | 4.57 MIN |

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

## Package Dimensions (Continued)

# IPAK

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