X20DC4395

Data sheet
3.30 (October 2024)

Translation of the original documentation

Publishing information

B&R Industrial Automation GmbH

B&R Strasse 1

5142 Eggelsberg

Austria

Telephone: +43 7748 6586-0

Fax: +43 7748 6586-26

office@br-automation.com

Disclaimer

All information in this document is current as of its creation. The contents of this document are subject to change without notice. B&R Industrial Automation GmbH assumes unlimited liability in particular for technical or editorial errors in this document only (i) in the event of gross negligence or (ii) for culpably inflicted personal injury. Beyond that, liability is excluded to the extent permitted by law. Liability in cases in which the law stipulates mandatory unlimited liability (such as product liability) remains unaffected. Liability for indirect damage, consequential damage, business interruption, loss of profit or loss of information and data is excluded, in particular for damage that is directly or indirectly attributable to the delivery, performance and use of this material.

B&R Industrial Automation GmbH notes that the software and hardware designations and brand names of the respective companies used in this document are subject to general trademark, brand or patent protection.

Hardware and software from third-party suppliers referenced in this document is subject exclusively to the respective terms of use of these third-party providers. B&R Industrial Automation GmbH assumes no liability in this regard. Any recommendations made by B&R Industrial Automation GmbH are not contractual content, but merely non-binding information for which no liability is assumed. When using hardware and software from third-party suppliers, the relevant user documentation of these third-party suppliers must additionally be consulted and, in particular, the safety guidelines and technical specifications contained therein must be observed. The compatibility of the products from B&R Industrial Automation GmbH described in this document with hardware and software from third-party suppliers is not contractual content unless this has been separately agreed in individual cases; in this respect, warranty for such compatibility is excluded in any case, and it is the sole responsibility of the customer to verify this compatibility in advance.

Version history

B&R makes every effort to keep documents as current as possible. The most current versions are available for download on the B&R website (www.br-automation.com).

1 General information

1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual

1.2 Order data

Order number	Short description	Figure
	Counter functions	
X20DC4395	X20 digital counter module, 2 SSI absolute encoders, 24 V, 2 ABR incremental encoders, 24 V, 4 AB incremental encoders, 24 V, 8 event counters or 4 PWM, local time measurement functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20DC4395 - Order data

1.3 Module description

This module is a multifunctional counter module. It can be connected to two SSI encoders, two ABR encoders, four AB encoders or eight event counters. Four outputs are available for pulse width modulation. The functions can also be mixed.

Functions:

- Digital inputs and outputs
- Counters and encoders
- SSI encoder interface
- PWM - Pulse width modulation
- Time measurement function
- Controlling the LED status indicators
- Monitoring the encoder power supply

Digital inputs and outputs

This module is equipped with 8 digital channels. All channels are used as inputs, 4 channels are also configurable as outputs. The inputs can be compared with predefined states and used to generate events. In addition to being controlled from the application, the setting or clearing of outputs can also be controlled by events.

Counters and encoders

The module provides counter functions for each channel. These can be configured for different counter or encoder functions depending on the channel. These include:

- AB encoder
- ABR encoders
- Up/Down counter
- Event counters

SSI absolute encoder

The module provides 2 SSI absolute encoders that are directly supported by the hardware.

PWM - Pulse width modulation

The module provides 4 PWM functions that are directly supported by the hardware.

Time measurement function

The module has a time measurement function for each I/O channel. It can be configured separately for rising and falling edges on each channel.

Controlling LED status indicators

The module LED status indicators can be controlled by the application. This allows blink signals to be output or the states of physical inputs and outputs to be displayed.

Monitoring the supply voltage

The encoder power supply voltage is monitored.

2 Technical description

2.1 Technical data

Order number	X20DC4395
Short description	
I/O module	2 SSI absolute encoders 24 V, 2 ABR incremental encoders 24 V, 4 AB incremental encoders 24 V, 8x event counter or 4x pulse width modulation, time measurement, relative timestamp
General information	
Input voltage	24 VDC -15% / +20%
B&R ID code	0x1CC5
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Outputs	Yes, using LED status indicator and software (output state)
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by actuators (resistive) [W]	-
Type of signal lines	Shielded lines must be used for all signal lines.
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
CCS	Yes
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
KC	Yes
Incremental encoders	
Quantity	4
Encoder inputs	24 V, asymmetrical
Counter size	16/32-bit
Input frequency	Max. 100 kHz
Evaluation	4x
Encoder power supply	Module-internal, max. 600 mA
Overload characteristics of encoder power supply	Short-circuit proof, overload-proof
SSI absolute encoder	
Quantity	2
Encoder inputs	24 V, asymmetrical
Counter size	32-bit
Max. transfer rate	125 kbit/s
Encoder power supply	Module-internal, max. 600 mA
Coding	Gray/Binary
CLK: Output current	Max. 100 mA
Overload characteristics of encoder power supply	Short-circuit proof, overload-proof
Event counters	
Quantity	8
Nominal voltage	24 VDC
Signal form	Square wave pulse

Table 2: X20DC4395 - Technical data

Technical description

Order number	X20DC4395
Evaluation	Each edge, cyclic counter
Input frequency	Max. 100 kHz
Input current at 24 VDC	Approx. 1.3 mA
Input resistance	18.4 kΩ
Insulation voltage between channel and bus	500 V_{eff}
Counter frequency	200 kHz
Counter size	16/32-bit
Input filter	
Hardware	≤2 µs
Software	-
Switching threshold	
Low	<5 VDC
High	>15 VDC
Edge detection / Time measurement	
Possible measurements	Gate time, period duration, edge offset for various channels
Measurements per module	Up to 9
Measurements per channel	Up to 2
Signal form	Square wave pulse
Counter size	16-bit
Counter frequency	
Internal	8 MHz, 4 MHz, 2 MHz, 1 MHz, 500 kHz, 250 kHz, 125 kHz, 62.5 kHz
Measurement type	Continuous or triggered
Digital outputs	
Quantity	4
Variant	Push / Pull / Push-Pull
Nominal voltage	24 VDC
Switching voltage	24 VDC -15% / +20%
Nominal output current	0.1 A
Total nominal current	0.4 A
Output circuit	Sink or source
Output protection	Thermal shutdown in the event of overcurrent or short circuit, integrated protection for switching inductive loads
Pulse width modulation [1)]	
Period duration	41.6 µs to 1.36 s
Factor for period duration	n/48000 s, n = 2 to 65535
Pulse duration	0 to 100%
Resolution for pulse duration	0.1%
Actuator power supply	Module-internal, max. 600 mA
Diagnostic status	Output monitoring
Leakage current when the output is switched off	Max. 25 µA
Residual voltage	<0.9 V at 0.1 A nominal current
Peak short-circuit current	<10 A
Switch-on in the event of overload shutdown or short-circuit shutdown	Approx. 10 ms (depends on the module temperature)
Switching delay	
0 → 1	<2 µs
1 → 0	<2 µs
Switching frequency	
Resistive load	Max. 24 kHz
Inductive load	See section "Switching inductive loads".
Braking voltage when switching off inductive loads	Switching voltage + 0.6 VDC
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Bus isolated from encoder and output Output not isolated from output and encoder Encoder not isolated from encoder
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 2: X20DC4395 - Technical data

Order number	X20DC4395
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 2: X20DC4395 - Technical data

1) Dead time when switching between push and pull: Max. 1.5 µs.

2.2 LED status indicators

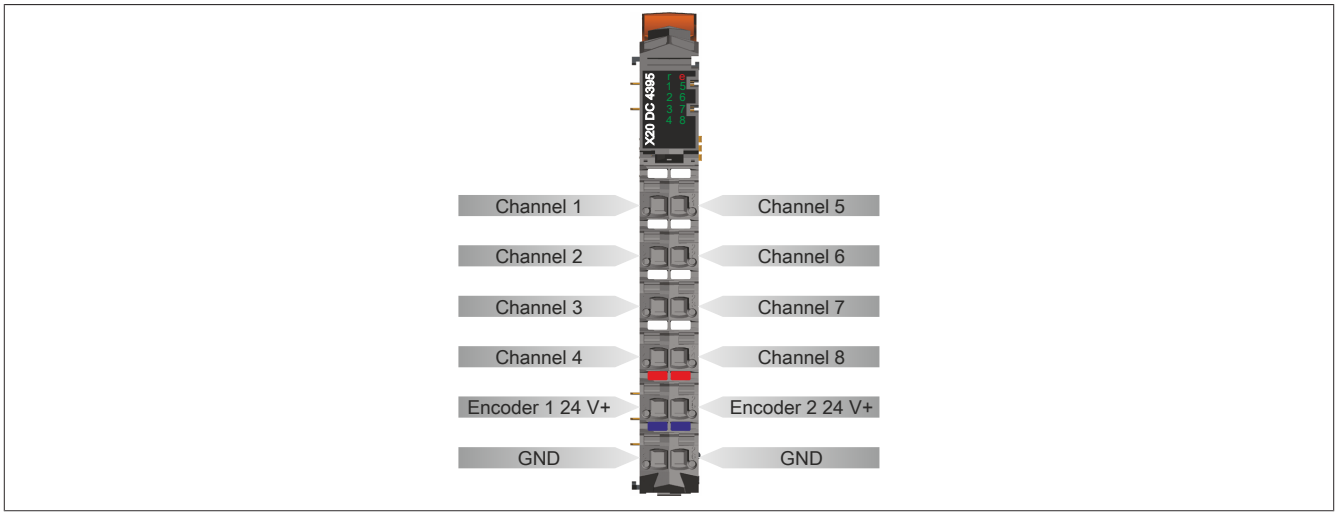
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green		Status of the corresponding digital signal

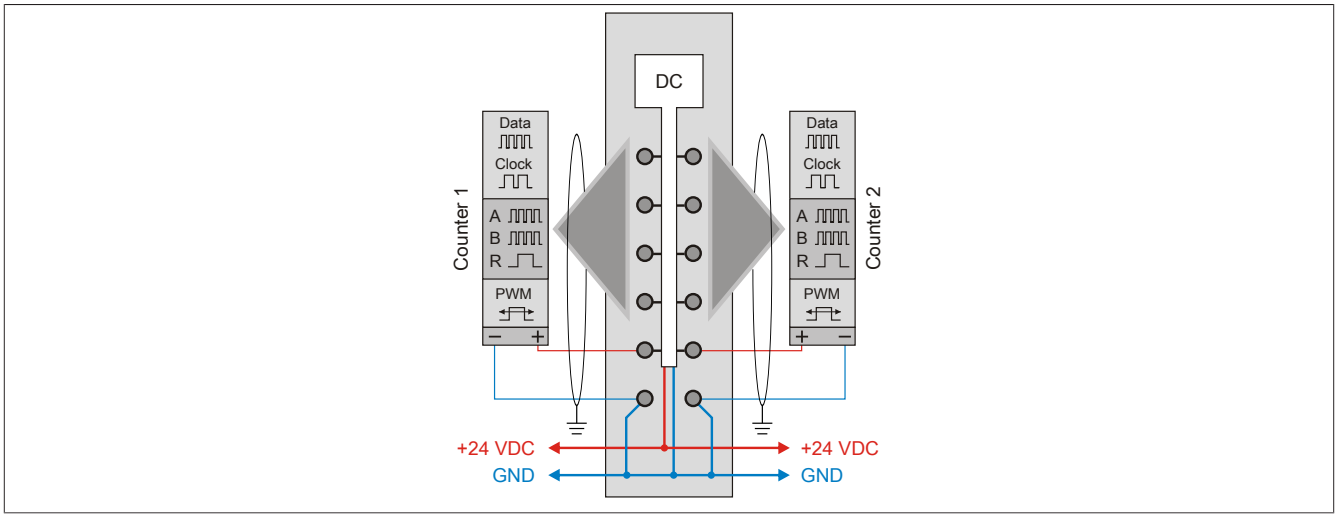
1) Depending on the configuration, a firmware update can take up to several minutes.

2.3 Pinout

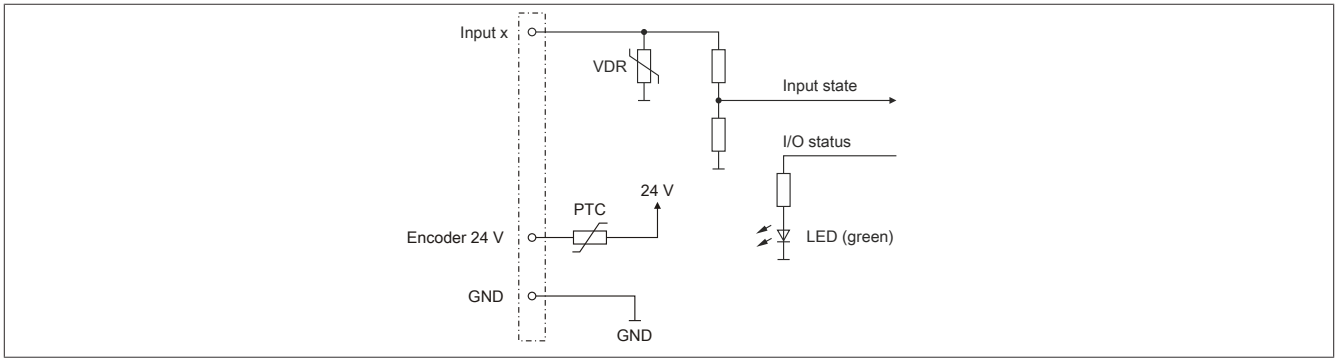
Shielded cables must be used for all signal lines.



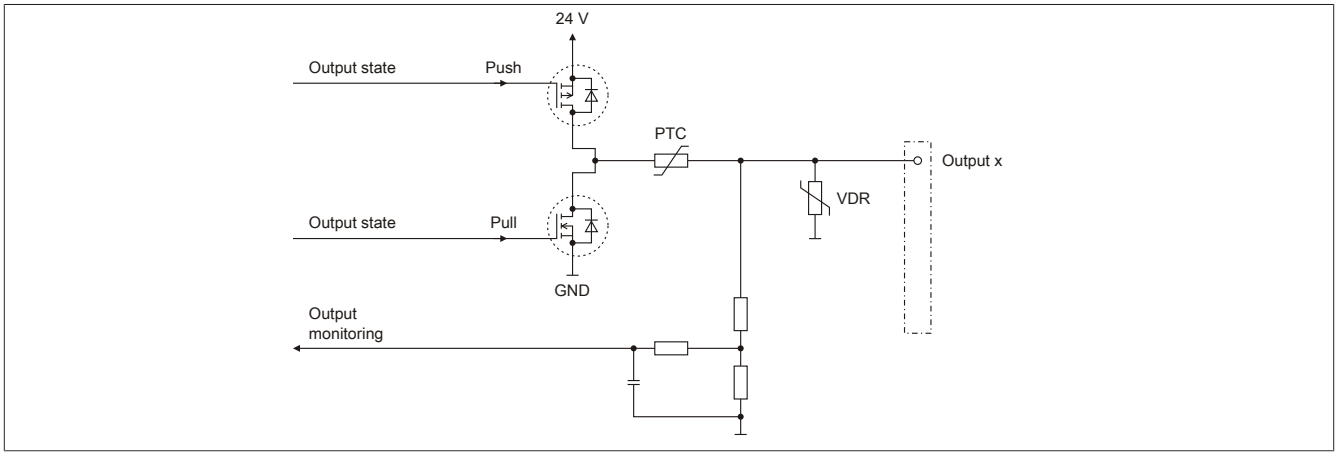
2.4 Connection example



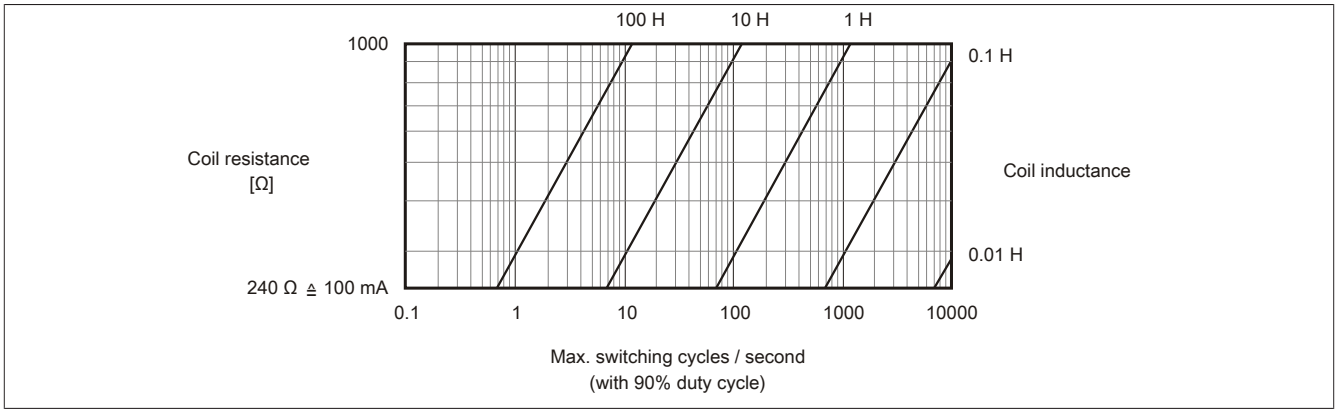
2.5 Input circuit diagram



2.6 Output circuit diagram



2.7 Switching inductive loads



3 Function description

3.1 Hardware channel functions

The following functions can be configured on the module. However, these cannot all be operated simultaneously due to the multiple use of the hardware channels and the cyclical data length limitation:

- 8 digital channels, 4 of which are configurable as outputs
- 8 event counters with adjustable counting direction and optional referencing via digital input
- 4 PWM outputs
- 4 up/down counters, each with optional latch inputs and comparator output
- 4 AB encoders, each with optional latch inputs and comparator output
- 2 ABR encoder with adjustable reference pulse edge and reference position, optional reference enable input, latch input and comparator output
- 2 SSI encoder, each with optional latch input and comparator output
- 2 Edge-triggered time measurement functions for each channel with selectable start edge regardless of the configuration setting

Information:

This module is a multifunctional module. Some bus controllers only support the default function model.

Default function model:

- **1x ABR incremental encoder (24 V)**
- **1x SSI absolute encoder (24 V)**
- **1x event counter (24 V)**
- **2x PWM output (24 V)**

3.1.1 Connecting options

Channels 1 to 8 can be connected as follows:

Channel	Function					
1	I	Event counter	A	A	SSI data	
2	I/O	Event counter	B	B	SSI cycle	PWM
3	I	Event counter	A	R		
4	I/O	Event counter	B	Enable reference		PWM
5	I	Event counter	A	A	SSI data	
6	I/O	Event counter	B	B	SSI cycle	PWM
7	I	Event counter	A	R		
8	I/O	Event counter	B	Enable reference		PWM

The functions can also be mixed. For example:

Example 1	
Channel	Function
1	SSI data
2	SSI cycle
3	Event counter
4	PWM
5	A
6	B
7	Event counter
8	PWM

Example 2	
Channel	Function
1	SSI data
2	SSI cycle
3	A
4	B
5	Event counter
6	Event counter
7	Event counter
8	Event counter

Example 3	
Channel	Function
1	Event counter
2	PWM
3	Event counter
4	PWM
5	SSI data
6	SSI cycle
7	A
8	B

Example 4	
Channel	Function
1	A
2	B
3	R
4	Enable reference
5	A
6	B
7	R
8	Enable reference

Example 5	
Channel	Function
1	A
2	B
3	Event counter
4	PWM
5	A
6	B
7	Event counter
8	Event counter

Example 6	
Channel	Function
1	Event counter
2	Event counter
3	Event counter
4	PWM
5	SSI data
6	SSI cycle
7	A
8	B

3.1.2 Description of channel assignments

The functions listed here are directly assigned to the respective hardware channels and cannot be changed.

Channel	Signal connections
1	• Digital input 1 • Event counter 1 • AB encoder 1 - signal line A • Up/down counter 1 - frequency • SSI encoder 1, data line • ABR encoder 1 - signal line A
2	• Digital input 2 • Digital output 2 • Event counter 2 • PWM output 2 • AB encoder 1 - signal line B • Up/down counter 1 - direction • SSI encoder 1, clock line • ABR encoder 1 - signal line B
3	• Digital input 3 • Event counter 3 • AB encoder 2 - signal line A • Up/down counter 2 - frequency • ABR encoder 1 - signal line R
4	• Digital input 4 • Digital output 4 • Event counter 4 • PWM output 4 • AB encoder 2 - signal line B • Up/down counter 2 - direction • ABR encoder 1 - reference enable input
5	• Digital input 5 • Event counter 5 • AB encoder 3 - signal line A • Up/down counter 3 - frequency • SSI encoder 2, data line • ABR encoder 2 - signal line A
6	• Digital input 6 • Digital output 6 • Event counter 6 • PWM output 6 • AB encoder 3 - signal line B • Up/down counter 3 - direction • SSI encoder 2, clock line • ABR encoder 2 - signal line B
7	• Digital input 7 • Event counter 7 • AB encoder 4 - signal line A • Up/down counter 4 - frequency • ABR encoder 2 - signal line R
8	• Digital input 8 • Digital output 8 • Event counter 8 • PWM output 8 • AB encoder 4 - signal line B • Up/down counter 4 - direction • ABR encoder 2 - reference enable input

Options available in addition to these basic functions, such as comparator outputs or latch inputs, can be configured freely to unused input/output channels.

3.2 Event functions

The module provides configurable event functions. An event function can be connected to physical I/O and the values derived from them (e.g. counters) or be purely used for internal processing.

Each event function has event inputs and outputs. Event functions can also only have event inputs or outputs. Each event output has a unique event ID. It is possible to configure when an event is generated on an event output. The effect of the arrival of an event is specified by the event function.

Event functions can also be linked to one another. The link takes place using the event input. Every event input has a 16-bit register to which the event number of the linked event output is written.

Information:

The module functions that can be configured in the Automation Studio I/O configuration are primarily based on these event functions and their links. Changes in the Automation Studio I/O configuration have multiple effects on event functions and their links.

The module functions cover the following areas:

- Edge events
- Direct input functions
- Direct output functions
- Counter event functions
- SSI event functions

3.2.1 List of event IDs

Various hardware and software functions send event IDs or require event IDs in order to start. The following table shows all of the IDs available to configure the module.

Event ID	Description	
Direct event inputs		
512	Comparator condition 1	FALSE
513		TRUE
544	Comparator condition 2	FALSE
545		TRUE
576	Comparator condition 3	FALSE
577		TRUE
608	Comparator condition 4	FALSE
609		TRUE
Counter event functions		
2,112	Counter function 1	Event function 1; FALSE
2,113		Event function 1; TRUE
2,144		Event function 2; FALSE
2,145		Event function 2; TRUE
2,368	Counter function 2	Event function 1; FALSE
2,369		Event function 1; TRUE
2,400		Event function 2; FALSE
2,401		Event function 2; TRUE
2,624	Counter function 3	Event function 1; FALSE
2,625		Event function 1; TRUE
2,656		Event function 2; FALSE
2,657		Event function 2; TRUE
2,880	Counter function 4	Event function 1; FALSE
2,881		Event function 1; TRUE
2,912		Event function 2; FALSE
2,913		Event function 2; TRUE
Edge events		
4,096	Falling edge on I/O channel	Channel 1
...		...
4,103		Channel 8
4,112	Rising edge on I/O channel	Channel 1
...		...
4,119		Channel 8
4,128	Rising or falling edge on I/O channel	Channel 1
...		...
4,135		Channel 8
SSI counter events		
7,168	SSI 1	SSI valid
7,169		SSI ready

Event ID	Description	
7,424	SSI 2	SSI valid
7,425		SSI ready
SSI comparator events		
7,232	SSI 1 comparator condition	FALSE
7,233		TRUE
7,488	SSI 2 comparator condition	FALSE
7,489		TRUE
Timerevents		
208	Timer1	50 µs
209	Timer2	100 µs
210	Timer3	200 µs
211	Timer4	400 µs
212	Timer5	800 µs
213	Timer6	1600 µs
214	Timer7	3200 µs
215	Timer8	3200 µs (time offset to timer 7)
Network functions		
224	SOAISOP (**S**ynchronous **O**ut **A**synchronous **I**n **S**tart **O**f **P**rotocol)	
225	AOSISOP (**A**synchronous **O**ut **S**ynchronous **I**n **S**tart **O**f **P**rotocol)	
226	SOAIEOP (**S**ynchronous **O**ut **A**synchronous **I**n **E**nd **O**f **P**rotocol)	
227	AOSIEOP (**A**synchronous **O**ut **S**ynchronous **I**n **E**nd **O**f **P**rotocol)	
Idle event		
192	No-load operation	

Timer

There are 8 timer events that the module can generate.

Information:

The timers have the highest event priority. All other system functions are interrupted when a timer event occurs, and jitter for the amount of time it takes to process the event.

Idle event

Idle time is the time that remains after the system has processed all higher priority events and operations. The module performs the following functions during idle time:

- Handling of the asynchronous protocol
- Mechanism for (re-)linking events
- Operation of LEDs
- Execution of event event functions linked to the idle function

3.3 Digital inputs and outputs

The module is equipped with 8 digital channels that can be configured as digital inputs or outputs.

Input channels

Each channel can be configured as an input channel. The input value is determined taking into account the polarity setting (normal/inverted) and is displayed under different names in the Automation Studio I/O mapping depending on the function used.

Output channels

Only channels 2, 4, 6 and 8 can be configured as output channels. The following steps must be carried out to configure a channel as an output:

- Enable bit 0 "Push" and/or bit 1 "Pull" in the channel configuration (register CfO_CFGchannel0x).
- Configure bits 4 to 7 in the channel configuration (register CfO_CFGchannel0x) to direct I/O.
- Set the set and reset mask for the affected channel to 0.

Set and reset masks of the outputs

The set and reset masks can be used to determine how the digital outputs can be switched.

- 0 enables manual setting and/or resetting of the digital outputs using registers DigitalOutput02 to 08.
- 1 prevents manual setting and/or resetting of the digital outputs using registers DigitalOutput02 to 08. This makes it possible to set or reset the outputs using the output event function.

Information:

The registers are described in "Digital inputs and outputs" on page 37.

3.3.1 Input states of the channels

The input states of the physical channels are determined taking into account the polarity settings (bit 2 in register CfO_CFGchannel). For a better overview, the bits determined are displayed under different names in the Automation Studio I/O mapping depending on the function used.

Physical input channel	Name in the Automation Studio I/O mapping
Channel 1	DigitalInput01
Channel 2	DigitalInput02 StatusDigitalOutput02 ComparatorActualValue02 ComparatorActualValue03
Channel 3	DigitalInput03
Channel 4	DigitalInput04 StatusDigitalOutput04 ReferenceEnableSwitch01 ComparatorActualValue01 ComparatorActualValue02 ComparatorActualValue03
Channel 5	DigitalInput05
Channel 6	DigitalInput06 StatusDigitalOutput06 ComparatorActualValue01
Channel 7	DigitalInput07
Channel 8	DigitalInput08 StatusDigitalOutput08 ReferenceEnableSwitch02 ComparatorActualValue01 ComparatorActualValue02 ComparatorActualValue03

Information:

The register is described in "Input states of the channels" on page 38.

3.3.2 Direct input functions

The module is equipped with 2 "direct input functions".

These event functions are based on the comparator functionality. All comparator functions can be operated in 4 different modes (see "Comparator modes" on page 21).

If the event configured for the input occurs, the event function compares the status of all direct I/O channels enabled in the comparison mask with the status specified in the comparison status. The event is generated according to the result of the comparison.

- If the corresponding bits are the same, it is event no. 512 or 545.
- If the corresponding bits are not the same, it is event no. 513 or 544.

Information:

The registers are described in "Direct input functions" on page 41.

3.3.3 Direct output functions

The module is equipped with 4 "direct output functions".

The effect of executing this event function is analogous to writing to register DigitalOutput02 to 08.

If the event configured for the output occurs, the changed output states are transferred directly to the hardware, but independently of the X2X cycle.

When using this event function, the set and reset masks of the corresponding outputs must be set to 1. Otherwise, the output state would constantly be overwritten by the values in register DigitalOutput02 to 08.

Information:

The registers are described in "Direct output functions" on page 43.

3.4 Edge events

3 event functions are available for each physical channel.

- Falling edge
- Rising edge
- Falling and rising edge

The respective event is triggered when an edge has been detected on the hardware input and the corresponding registers have been configured for the corresponding channel.

Edges are detected by the hardware and processed for each interrupt. The interrupt handler uses an event distributor, which requires a specific amount of time for each edge to operate the hardware and execute linked event functions. To reduce this time, edge detection can be enabled/disabled individually for each channel. To optimize system load and I/O jitter, it is important to only enable edge detection where it is actually needed.

Information:

Edge detection can also be used for channels that are configured to output.

Limiting the event frequency

To stabilize the system, there is a mechanism that limits the number of events created through edge recognition. After an edge event is processed, at least one idle event must occur before a new event is processed for the same edge.

This limit can be switched off per edge, in which case an event is generated from each edge. System overload can occur at high frequencies, however, which means that I/O operation can fail for up to 100 ms before the module enters the reset state.

Information:

The registers are described in "Edge events" on page 39.

3.5 Counters and encoders

The module is equipped with 4 internal counter functions with 2 counter registers each. Each of these 4 counters is permanently assigned to 2 physical inputs. This assignment cannot be changed.

Each of the 4 counter functions can be operated in 3 different modes. The counter channels and counter registers are assigned as follows:

	Counter function mode		
	Edge counter	AB encoder	Up/Down counter
Counter channel 1[1)]	Counting pulses of edge counter 1	A	Metering pulses
Counter channel 2[1)]	Counting pulses of edge counter 2	B	Counting direction (0 = Positive, 1 = Negative)
Counter register 1	Counter value 1	Position	Counter value
Counter register 2	Counter value 2		

1) Corresponds to the physical channels of the counter functions (see "Description of channel assignments" on page 12).

Names of the counter registers

The counter registers apply different functions depending on the selected linkage of the event functions. For reasons of clarity, different names are used in Automation Studio and in the register description.

Channel	Counter function	Counter register	Function	Name in Automation Studio
1	1	1	AB encoder ABR encoders Up/Down counter Event counters	ABEncoder01 ABREncoder01 Counter01 EventCounter01
2		2	Event counters	EventCounter02
3	2	1	AB encoder Up/Down counter Event counters	ABEncoder02 Counter02 EventCounter03
4		2	Event counters	EventCounter04
5	3	1	AB encoder ABR encoders Up/Down counter Event counters	ABEncoder03 ABREncoder02 Counter03 EventCounter05
6		2	Event counters	EventCounter06
7	4	1	AB encoder Up/Down counter Event counters	ABEncoder04 Counter04 EventCounter07
8		2	Event counters	EventCounter08

Information:

The registers are described in "Counters and encoders" on page 44.

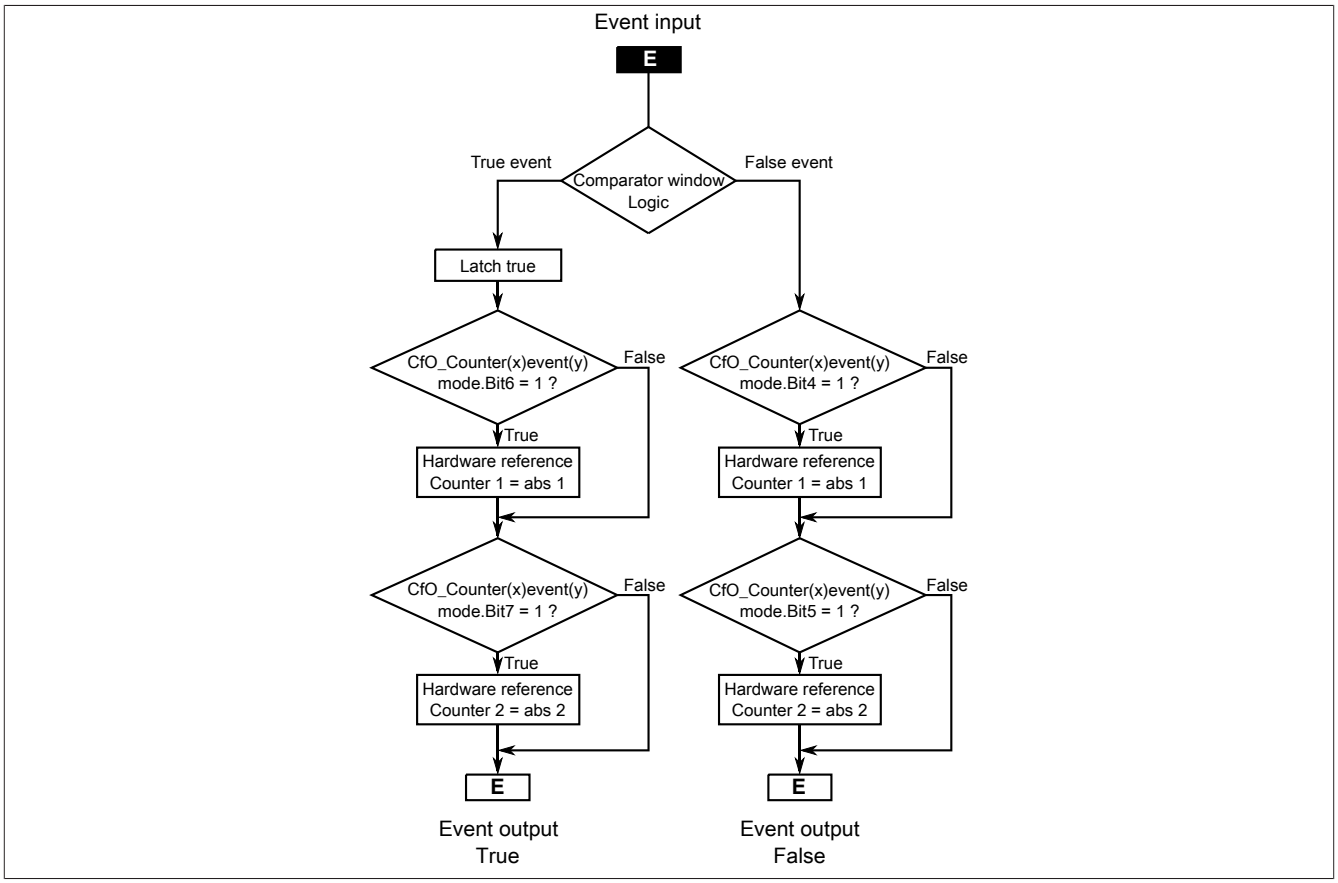
3.5.1 Counter event functions

Each of the 4 counter functions has 2 counter event functions. These consist of the following:

- Event ID that triggers the counter event function
- A window comparator
- Latch register for saving the counter value

After the counter event function has been completed, a combined event ID in the range from 2112 to 2913 (see "List of event IDs" on page 13) is transmitted.

Each counter event function also has the option to copy the current counter value to the "HW reference counter" when an event occurs (see "Counter value calculation" on page 19).



3.5.2 Counter value calculation

Selecting the counters

It is possible for each of the internal registers "counter1" and "counter2" to determine whether it is used for the counter calculation and whether the sign is taken into account.

Description	Value	Information
counterX - Use	0	0 is added instead of register "counterX".
	1	"counterX" is used for addition.
counterX - Sign	0	The sign of register "counterX" is not changed for addition.
	1	The sign of register "counterX" is reversed for addition.

Examples of calculation configurations

0b00000001	= 0x01	Only the "counter1 - use" bit is set, entering the contents of the "counter" (edge of counter event channel 1) directly in the counter register.
0b00000011	= 0x03	"counter 1 - use" and "counter1 - sign" bits are set. The sign is changed so that the counter register counts in the negative direction.
0b00001101	= 0x0d	Edges on counter input channel 1 increase the value in the counter register. Edges on counter input channel 2 decrease the value in the counter register. This value is the best setting for modes "AB counter" and "Up/Down counter".

Calculation procedure

The counter value for each counter function is calculated in 3 steps:

1. The 2 absolute value counters "abs1" and "abs2" are the basis for the counter value. These are only used within the module and cannot be read out. Depending on the mode, the physical input channels are mapped to these registers accordingly.

	Mode		
	Edge counters	**AB encoders**	**Up/Down counter**
abs1	Edges of counter channel 1	Increments in positive direction	Counter channel 2 = 0: Edges of counter channel 1 in up direction
abs2	Edges of counter channel 2	Increments in negative direction	Counter channel 2 = 1 Edges of counter channel 1 in down direction

2. 2 additional counters are formed from absolute value registers "abs1" and "abs2": "counter1" and "counter2". They are only used within the module and cannot be read out. The following values are used for the calculation:

- Absolute value registers "abs1" and "abs2"
- SW_reference_counter 1 and 2: This reference value can be specified by register CfO_CounterPreset-Value to enable referencing ≠ 0.
- HW_reference_counter 1 and 2: Register CfO_CounterEventMode can be used to configure whether latched values are copied to these registers when counter events occur.

counter1 = abs1 + SW_reference_counter1 - HW_reference_counter1
counter2 = abs2 + SW_reference_counter2 - HW_reference_counter2

3. The counter registers contain the sum of the two internal counters "counter 1" and "counter 2". In register CfO_CounterConfigReg, the sign can be defined for each "Counter" register and whether it is used.

Counter register = counter1 + counter2

3.5.3 Comparator functions

Comparator functions are available on the module for the ABR, AB and up/down counters. These consist of the following:

- Event ID that triggers the comparator function
- Window comparator
- Latch register for storing the counter position

After the comparator function has been completed, the corresponding event ID is transmitted (see "List of event IDs" on page 13).

These are comparators that are implemented in software. They do not work actively, but passively, i.e. the comparison is only carried out when an event is received. The received event is forwarded to the TRUE or FALSE branch depending on the state of the comparator condition.

Window comparator

All comparator functions can be operated in 4 different modes. For a description, see "Comparator modes" on page 21.

Value	Information
0	Off
1	Individual
2	State change
3	Continuous

Calculation of the comparator

It is possible for each of the internal registers "counter1" and "counter2" to determine whether it is used for the comparator calculation and whether the sign is taken into account.

Description	Value	Information
counterX - Use	0	0 is added instead of register "counterX".
	1	"counterX" is used for addition.
counterX - Sign	0	The sign of register "counterX" is not changed for addition.
	1	The sign of register "counterX" is reversed for addition.

The comparator is calculated in the same way as the counter registers. In addition, a mask value can be created with which an AND operator is carried out before the comparison. This makes it possible to generate a comparator pulse every 2^n increments.

Information:

The registers are described in "Comparator functions" on page 46.

3.5.3.1 Comparator modes

Comparator functions can be operated in 4 different modes.

- **Off**
  Events are ignored.
- **Individual**
  The event function is executed once and then disables itself automatically. To re-enable it, the "event function mode" must be changed, preferably to "off" and then to the desired mode. This setting allows a hardware latch to be simulated.
- **State change**
  The event function only responds when the comparator state changes, i.e. from FALSE to TRUE (or vice versa). Only the first event for each status is processed, e.g. the first TRUE of a sequence of events with the comparator condition TRUE. After the event function is enabled, the first incoming event is used to determine the starting state and therefore not forwarded. This setting allows a hardware comparator to be simulated.
- **Continuous**
  Each incoming event is forwarded on the TRUE or FALSE branch depending on the comparator condition. This setting can be used to create filters for events.

3.5.3.2 Latch function

If the comparator returns TRUE, then the current counter value is latched and copied to these registers. The calculation of the comparator value used for the latch can be configured in the calculation register (CfO_Counter[x]event[y]config).

The latch registers apply different functions depending on the selected linkage of the event functions. For reasons of clarity, different names are used in the register description.

Counter 1 - Latch 1		
Event function	**Function**	**Name**
1	**AB encoder**	Latch01AB01
	Up/Down counter	Latch01Counter01
2	**AB encoder**	Latch02AB01
	ABR encoders	Latch01ABR01
	Up/Down counter	Latch02Counter01

Counter 1 - Latch 2		
Event function	**Function**	**Name**
1	**AB encoder**	Latch01AB02
	Up/Down counter	Latch01Counter02
2	**AB encoder**	Latch02AB02
	Up/Down counter	Latch02Counter02

Counter 2 - Latch 1		
Event function	**Function**	**Name**
1	**AB encoder**	Latch01AB03
	Up/Down counter	Latch01Counter03
2	**AB encoder**	Latch02AB03
	ABR encoders	Latch01ABR02
	Up/Down counter	Latch02Counter03

Counter 2 - Latch 2		
Event function	**Function**	**Name**
1	**AB encoder**	Latch01AB04 Latch01ABConnector04
	Up/Down counter	Latch01Counter04
2	**AB encoder**	Latch02AB04 Latch02ABConnector04
	Up/Down counter	Latch02Counter04

Information:

The register is described in "Read latch position or counter value" on page 49.

3.6 SSI encoder interface

The module provides 2 SSI encoders that are directly supported by the hardware. 2 24 V output channels are permanently set for each SSI encoder and cannot be modified (see also "Description of channel assignments" on page 12).

When using the SSI encoder, the associated clock channel must be configured to "Channel-specific" and "Push/Pull" in the channel configuration (register CfO_CFGchannel0x).

Encoder	Data channel	Clock channel
SSI1	1	2
SSI2	5	6

Information:

The registers are described in "SSI encoder interface" on page 49.

3.6.1 SSI event functions

Each of the 2 SSI encoders consists of an event function and an event input. The SSI cycle is started when an event is received on this input.

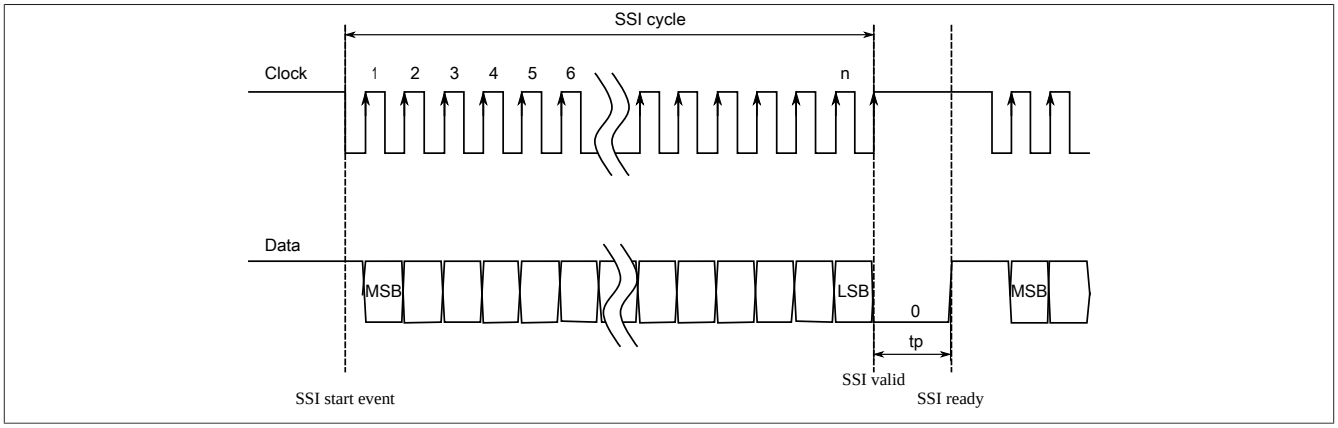
Information:

The SSI event function is not linked to an event by default, i.e. SSI functions are disabled.

2 events are transmitted from the SSI encoder interface.

- An "SSI valid" event is triggered immediately after the end of the SSI cycle if a new counter value is available.
- The "SSI ready" event then shows when the monoflop time has expired (tp in SSI encoder timing diagram). This is the earliest that the next SSI cycle can be started.

SSI encoder - Timing diagram



The SSI cycle is normally configured to network event 225 "AOSISOP". This ensures that the new encoder position is available for the next "I/O → Synchronous frame" transfer. It is important to note the SSI transfer time and the X2X cycle time since the SSI cycle must be completed within this time frame.

For a list of all possible event IDs, see "List of event IDs" on page 13.

3.6.2 SSI comparator condition

The module has an assigned comparator function for the SSI function. These consist of:

- Event ID that triggers the comparator function
- The window comparator
- Latch register for saving the counter value

After the comparator function has been completed, event ID 7232 to 7489 (see "List of event IDs" on page 13) is transmitted.

Window comparator

All comparator functions can be operated in 4 different modes. For a description, see "Comparator modes" on page 21.

Value	Information
0	Off
1	Individual
2	State change
3	Continuous

Performing the calculation

The position value used for the comparison is calculated as follows:

```
counter_window_value = ssi_counter & (2^ssi_data_bits - 1)
diff = counter_window_value - origin_comparator
if ((diff & (2^(comparator_mask)-1)) <= margin_comparator)
condition = True;
else
condition = False;
```

Latch function

If the comparison of the SSI window comparator returns "TRUE", the current SSI position is latched and saved.

3.7 PWM - Pulse width modulation

The module provides 4 PWM functions that are directly supported by the hardware. One 24 V output channel is permanently set for each PWM function and cannot be modified (see also "Description of channel assignments" on page 12).

When using the PWM function, the associated channel must be configured to "Channel-specific" in the channel configuration (register CfO_CFGchannel0x).

PWM function	Channel
PWM1	2
PWM2	4
PWM3	6
PWM4	8

Length of the PWM cycle

The basis for the length of the PWM cycle is a 48 MHz clock, which can be modified (divided). A PWM cycle consists of 1000 of these clock pulses resulting from the division. The period duration of the PWM cycle is therefore calculated as follows:

$$PWM\_Cycle = 1000 \frac{prescale}{48000000} [s]$$

Switch-on/Switch-off time

The PWM output can be switched to logical 1 in 1/10% steps of the PWM cycle. Logical 1 means that the PWM output is switched on.

Value	Information
0	PWM output always off
1 to 999	Switch-on time in 1/10% increments
1000	PWM output always on

Calculating the period duration

The period duration is calculated using the following formula:

$$Periodendauer = \frac{n}{48000} s$$

A value of 2 to 65535 can be defined for n.

n	Period duration	Frequency
2	416 µs	24 kHz
24000	500 ms	2 Hz
48000	1 s	1 Hz
65535	1.36 s	0.73 Hz

Information:

The registers are described in "PWM - Pulse width modulation" on page 52.

3.8 Time measurement function

The module has a time measurement function for each I/O channel. It can be configured separately for rising and falling edges on each channel.

A starting edge can be configured for each time measurement function. When a configured starting edge occurs, the value of the internal timer is saved in a FIFO buffer. This FIFO buffer holds up to 16 elements. When the actual trigger edge occurs, the difference in time between the starting edge and the triggered edge is copied to the respective register.

Bits 8 to 11 "Previous start edge" of registers CfO_EdgeTimeFallingMode and CfO_EdgeTimeRisingMode can be used to define which detected starting edge from the FIFO buffer should be used to calculate the difference. In addition, when the trigger edge occurs, the current counter value of the counter internally clocked by bits 12 to 15 "Resolution of time measurement" is copied to the timestamp register.

Information:

The time measurement function is an extension of edge detection, so all of the channels used must be configured there.

The following measurement functions are available:

- Detecting a falling or rising edge
  The falling or rising edge on the respective input can be detected.
- Displaying the first trigger edge
  The first falling or rising edge on the respective input since the associated bit was set can be recorded.
- Counting trigger edges
  Cyclic counters are incremented with each detected edge on the respective channel.
- Timestamp of the edge
  When an edge occurs on the respective channel, the current counter value of the module timer is saved.
- Time difference of the edge
  When an edge occurs on the respective channel, the time difference is saved.

Information:

The registers are described in "Time measurement function" on page 52.

3.9 Controlling the LED status indicators

The module LED status indicators can be controlled by the application. This allows blink signals to be output or the states of physical inputs and outputs to be displayed.

Possible modes:

Values	Information
0	LED blinking pattern
1	Inverted LED blinking pattern
2	Indicates the physical input state of a channel
3	Indicates the physical output state of a channel

States of the (inverted) LED indicators:

Values	Information
0	LED off
1	Blinking quickly
2	Blinking
3	Blinking slowly
4	Single flash
5	Double flash
6 to 15	Reserved

Information:

The register is described in "Configuring LED status indicators" on page 36.

3.10 Monitoring the encoder power supply

Monitoring the encoder power supply

The status of the integrated encoder power supply can be read.

Bit	Description
0	24 VDC encoder supply voltage OK
1	24 VDC encoder supply voltage faulty

Information:

The register is described in "Status of encoder power supply" on page 36.

4 Commissioning

4.1 Sample configurations

All configurations available in Automation Studio for AB encoders, ABR encoders, up/down counters and event counters are based on the 2 counter functions.
The following configuration examples show the values with which the module registers are initialized by Automation Studio to implement these functions.

4.1.1 I/O configuration - AB encoder

The following table shows how the module's various event functions can be linked in order to configure an AB encoder.

[x] stands for the counter function 1 to 4 used:

Register	Value	Comment
For the function		
CfO_Counter[x]config	0x01	Mode = Up/Down counter
CfO_Counter[x]configReg0	0x0D	Configures the calculation of internal registers "counter1" and "counter2" (see "Counter value calculation" on page 19)
For the latch		
CfO_Counter[x]event0config	0x000D	Configuration of the calculation of the first value used for the latch
CfO_Counter[x]event0mode	0x03	Mode of the first counter event function - Continuous
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger latch 1 ("Latch 01 - Channel" in the Automation Studio I/O configuration)
CfO_Counter[x]event1config	0x0D	Configuration of the calculation of the second value used for the latch
CfO_Counter[x]event1mode	0x03	Mode of the second counter event function - Continuous
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger latch 2
For the comparator		
CfO_Counter1event1IDwr CfO_Counter3event1IDwr	0x00D0	Event number of Timer 1 (50 µs) The latch and comparator must not have the same event number!
CfO_Counter1event1config CfO_Counter3event1config	0x900D or 0xA00D	Configuration of the comparator for the second counter event
CfO_Counter1event1mode CfO_Counter3event1mode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr CfO_DIREKTIOoutevent2IDwr	0x0861 0x0A61	TRUE event output of the respective counter for triggering the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0 CfO_DIREKTIOoutsetmask2	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be set if the comparator condition is TRUE
CfO_DIREKTIOoutevent1IDwr CfO_DIREKTIOoutevent3IDwr	0x0860 0x0A60	FALSE event output of the respective counter for triggering the direct output function (reset outputs).
CfO_DIREKTIOoutclearmask1 CfO_DIREKTIOoutclearmask3	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be reset if the comparator condition is FALSE

4.1.2 I/O configuration - ABR encoder

The following table shows how the module's various event functions can be linked in order to configure an ABR encoder.

Register	Value	Comment
For the function		
CfO_Counter1PresetValue1 CfO_Counter3PresetValue1	(any)	Desired offset value for referencing
CfO_Counter1event0IDwr CfO_Counter3event0IDwr	0x0201	Link to the first counter event with the "direct input" comparison condition TRUE
CfO_Counter1config CfO_Counter3config	0x01	Mode = AB encoder
CfO_Counter1configReg0 CfO_Counter3configReg0	0x0D	Configures the calculation of internal registers "counter1" and "counter2" (see "Counter value calculation" on page 19)
CfO_DIREKTIOevent0IDwr CfO_DIREKTIOevent1IDwr	0x1002 or 0x1012	Selection of the desired input edge as trigger for the ABR encoder function
CfO_Counter1event0config CfO_Counter3event0config	0x0000	Configuration of the first counter event (for referencing)
CfO_DIREKTIOevent0mode CfO_DIREKTIOevent1mode	0x03	Mode of the "direct input function" - Continuous
CfO_DIREKTIOevent0compState CfO_DIREKTIOevent1compState	0x00 or 0x08	Comparison status for the "direct input function"
CfO_Ev0CompMask CfO_Ev1CompMask	0x08	Comparison mask for the "direct input function"
For the latch		
CfO_Counter1event0config CfO_Counter3event1config	0x000D	Configuration of the calculation of the value used for the latch
CfO_Counter1event0mode CfO_Counter3event1mode	0x03	Mode of the first counter event function - Continuous
CfO_Counter1event0IDwr CfO_Counter3event1IDwr	(any)	Number of the event that should trigger the latch
For the comparator		
CfO_Counter1event1IDwr CfO_Counter3event1IDwr	0x00D0	Event number of Timer 1 (50 µs) The latch and comparator must not have the same event number!
CfO_Counter1event1config CfO_Counter3event1config	0x900D or 0xA00D	Configuration of the comparator for the second counter event
CfO_DIREKTIOoutevent0IDwr CfO_DIREKTIOoutevent2IDwr	0x0861 0x0A61	TRUE event output of the respective counter for triggering the direct output function (set outputs)
CfO_DIREKTIOoutsetmask0 CfO_DIREKTIOoutsetmask2	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be set if the comparator condition is TRUE
CfO_DIREKTIOoutevent1IDwr CfO_DIREKTIOoutevent3IDwr	0x0860 0x0A60	FALSE event output of the respective counter for triggering the direct output function (reset outputs)
CfO_DIREKTIOoutclearmask1 CfO_DIREKTIOoutclearmask3	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be reset if the comparator condition is FALSE

4.1.3 I/O configuration - Up/Down counter

The following table shows how the various event functions of the module can be linked to configure an up/down counter.

[x] stands for the counter function 1 to 4 used:

Register	Value	Comment
For the function		
CfO_Counter[x]config	0x03	Counter mode = Up/Down counter
CfO_Counter[x]configReg0	0x0D, 0x07	Configures the calculation of internal registers "counter1" and "counter2" (see "Counter value calculation" on page 19)
For the latch		
CfO_Counter[x]event0config	0x0D, 0x07	Configuration of the calculation of the first value used for the latch
CfO_Counter[x]event0mode	0x03	Mode of the first counter function - Continuous
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger latch 1
CfO_Counter[x]event1config	0x0D, 0x07	Configuration of the calculation of the second value used for the latch
CfO_Counter[x]event1mode	0x03	Mode of the second counter function - Continuous
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger latch 2
For the comparator		
CfO_Counter1event1IDwr CfO_Counter3event1IDwr	0x00D0	Event number of Timer 1 (50 µs)  The latch and comparator must not have the same event number!
CfO_Counter1event1config CfO_Counter3event1config	0x900D, 0xA00d or 0x9007, 0xA007	Configuration of the comparator for the second counter event
CfO_Counter1event1mode CfO_Counter3event1Imode	0x03	Mode of the second counter event function - Continuous
CfO_DIREKTIOoutevent0IDwr CfO_DIREKTIOoutevent2IDwr	0x0861	TRUE event output of the respective counter for triggering the direct output function (set outputs).
CfO_DIREKTIOoutsetmask0 CfO_DIREKTIOoutsetmask2	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be set if the comparator condition is TRUE
CfO_DIREKTIOoutevent1IDwr CfO_DIREKTIOoutevent3IDwr	0x0860 0x0A60	FALSE event output of the respective counter for triggering the direct output function (reset outputs)
CfO_DIREKTIOoutclearmask1 CfO_DIREKTIOoutclearmask3	0x08, 0x20, 0x80 0x02, 0x08, 0x80	Outputs that should be reset if the comparator condition is FALSE

4.1.4 I/O configuration - Event counter

The following table shows how the module's various event functions can be linked in order to configure an event counter.

[x] stands for the counter function 1 to 4 used:

Register	Value	Comment
For event counters on channels 1, 3, 5 and 7		
CfO_Counter[x]configReg0	0x01 or 0x03	Configures the calculation of internal registers "counter1" and "counter2" (see "Counter value calculation" on page 19)
CfO_Counter[x]event0mode	0x43	Mode of the first counter event function and referencing configuration
CfO_Counter[x]event0IDwr	(any)	Number of the event that should trigger referencing
For event counters on channels 2, 4, 6 and 8		
CfO_Counter[x]configReg1	0x04 or 0x08	Configures the calculation of internal registers "counter1" and "counter2" (see "Counter value calculation" on page 19)
CfO_Counter[x]event1mode	0x83	Mode of the second counter event function and referencing configuration
CfO_Counter[x]event1IDwr	(any)	Number of the event that should trigger referencing

4.2 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

4.2.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

5 Register description

5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

5.2 Function model 0 - Standard and Function model 1 - 32-bit counter

The following 2 models can be selected:

- 16-bit counter, Function model 0
- 32-bit counter - Function model 1
  Marked in the table by an additional "(D)" in the data type or "(_32Bit)" in the name.

The only difference between these two models is that they use either 16-bit or 32-bit registers for incremental counter functions. The following belong to this group:

- ABR encoders
- AB encoders
- Up/down counters
- Event counters

All other module functions e.g. SSI, PWM and time measurement, as well as their data types, are identical for the two models.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Module configuration - General						
(N-1) * 2	CfO_CFGchannel0N (Index N = 1 to 8)	USINT				•
64 + N * 2	CfO_LEDNsource (Index N = 0 to 7)	USINT				•
Configuration - Input for ABR encoders						
512	CfO_DIREKTIOevent0IDwr	UINT				•
544	CfO_DIREKTIOevent1IDwr	UINT				•
516	CfO_DIREKTIOevent0mode	USINT				•
548	CfO_DIREKTIOevent1mode	USINT				•
522	CfO_DIREKTIOevent0compState	UINT				•
544	CfO_DIREKTIOevent1compState	UINT				•
520	CfO_Ev0CompMask	USINT				•
552	CfO_Ev1CompMask	USINT				•
2064 + (N-1) * 256	CfO_CounterNPresetValue1(_32Bit) (Index N = 1 to 4)	U(D)INT				•
2068 + (N-1) * 256	CfO_CounterNPresetValue2(_32Bit) (Index N = 1 to 4)	U(D)INT				•
2048 + (N-1) * 256	CfO_CounterNconfig (Index N = 1 to 4)	USINT				•
2056 + (N-1) * 256	CfO_CounterNconfigReg0 (Index N = 1 to 4)	USINT				•
2058 + (N-1) * 256	CfO_CounterNconfigReg1 (Index N = 1 to 4)	USINT				•
2112 + (N-1) * 256	CfO_CounterNevent0IDwr (Index N = 1 to 4)	UDINT				•
2120 + (N-1) * 256	CfO_CounterNevent0config (Index N = 1 to 4)	UINT				•
2144 + (N-1) * 256	CfO_CounterNevent1IDwr (Index N = 1 to 4)	UINT				•
2152 + (N-1) * 256	CfO_CounterNevent1config (Index N = 1 to 4)	UINT				•
2148 + (N-1) * 256	CfO_CounterNevent1mode (Index N = 1 to 4)	USINT				•
Configuration - Inputs for AB, up/down and event counters						
2048 + (N-1) * 256	CfO_CounterNconfig (Index N = 1 to 4)	USINT				•
2056 + (N-1) * 256	CfO_CounterNconfigReg0 (Index N = 1 to 4)	USINT				•
2058 + (N-1) * 256	CfO_CounterNconfigReg1 (Index N = 1 to 4)	USINT				•
2112 + (N-1) * 256	CfO_CounterNevent0IDwr (Index N = 1 to 4)	UDINT				•
2120 + (N-1) * 256	CfO_CounterNevent0config (Index N = 1 to 4)	UINT				•
2116 + (N-1) * 256	CfO_CounterNevent0mode (Index N = 1 to 4)	USINT				•
2144 + (N-1) * 256	CfO_CounterNevent1IDwr (Index N = 1 to 4)	UINT				•
2152 + (N-1) * 256	CfO_CounterNevent1config (Index N = 1 to 4)	UINT				•
2148 + (N-1) * 256	CfO_CounterNevent1mode (Index N = 1 to 4)	USINT				•
Configuration - Inputs for SSI encoders						
7,176	CfO_SSI1cfg	UINT				•

Register description

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
7,432	CfO_SSI2cfg	UINT				•
7,180	CfO_SSI1control	USINT				•
7,436	CfO_SSI2control	USINT				•
7,168	CfO_SSI1eventIDwr	UINT				•
7,424	CfO_SSI2eventIDwr	UINT				•
7,232	CfO_SSI1event0IDwr	UINT				•
7,488	CfO_SSI2event0IDwr	UINT				•
7,240	CfO_SSI1event0config	UINT				•
7,496	CfO_SSI2event0config	UINT				•
7,236	CfO_SSI1event0mode	USINT				•
7,492	CfO_SSI2event0mode	USINT				•
7,172	ConfigAdvanced01	UDINT				•
7,428	ConfigAdvanced02	UDINT				•
Configuration - Comparator function for ABR, AB and SSI encoders as well as up/down counters						
256	CfO_OutClearMask	USINT				•
258	CfO_OutSetMask	USINT				•
1,024	CfO_DIREKTIOouteventOIDwr	UINT				•
1034 + N * 32	CfO_DIREKTIOoutsetmaskN (Index N = 0 to 3)	USINT				•
1032 + N * 32	CfO_DIREKTIOoutclearmaskN (Index N = 0 to 3)	USINT				•
1,066	CfO_DIREKTIOoutsetmask1	USINT				•
1,064	CfO_DIREKTIOoutclearmask1	USINT				•
1024 + N * 32	CfO_DIREKTIOouteventNIDwr (Index N = 0 to 3)	UINT				•
Configuration - Outputs for PWM (pulse width modulation)						
6144 + N * 16	CfO_PWMNprescaler (Index N = 0 to 3)	UINT				•
Module communication - General						
40	Status of encoder power supply	USINT	•			
	PowerSupply01	Bit 0				
Communication - Digital inputs						
264	Input states of the channels	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
Communication - Event counters						
2,080	EventCounter01	U(D)INT	•			
2,084	EventCounter02	U(D)INT	•			
2,336	EventCounter03	U(D)INT	•			
2,340	EventCounter04	U(D)INT	•			
2,592	EventCounter05	U(D)INT	•			
2,596	EventCounter06	U(D)INT	•			
2,848	EventCounter07	U(D)INT	•			
2,852	EventCounter08	U(D)INT	•			
Communication - Input for ABR encoders (optionally with comparator)						
2,080	ABREncoder01	(D)INT	•			
2,592	ABREncoder02	(D)INT	•			
2,116	ReferenceModeABR01	USINT			•	
2,628	ReferenceModeABR02	USINT			•	
2,160	OriginComparator01	(D)INT			•	
2,164	MarginComparator01	U(D)INT			•	
264	Input states of the channels	USINT	•			
	ComparatorActualValue02	Bit 1				
	ReferenceEnableSwitch01 (without comparator) ComparatorActualValue01 (with comparator) ComparatorActualValue02 (with comparator)	Bit3				
	ComparatorActualValue01	Bit 5				
	ReferenceEnableSwitch02 (without comparator) ComparatorActualValue01 (with comparator) ComparatorActualValue02 (with comparator)	Bit 7				
2,172	Latch01ABR01	(D)INT	•			
2,684	Latch01ABR02	(D)INT	•			
2,118	StatusABR01	USINT	•			
2,630	StatusABR02	USINT	•			
Communication - Input for AB						
2080 + (N-1) * 256	ABEncoder0N (Index N = 1 to 4)	(D)INT	•			
2,336	ABEncoder02	(D)INT	•			
2,160	OriginComparator01	(D)INT			•	
2,164	MarginComparator01	U(D)INT			•	
264	Input states of the channels	USINT	•			
	ComparatorActualValue03	Bit 1				
	ComparatorActualValue01 ComparatorActualValue03	Bit 3				
	ComparatorActualValue01	Bit 5				
	ComparatorActualValue01 ComparatorActualValue03	Bit 7				
2140 + (N-1) * 256	Latch01AB0N (Index N = 1 to 4)	(D)INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2172 + (N-1) * 256	Latch02AB0N (Index N = 1 to 4)	(D)INT	•			
Communication - Up/down counters						
2080 + (N-1) * 256	Counter0N (Index N = 1 to 4)	U(D)INT	•			
2,160	OriginComparator01	U(D)INT			•	
2,164	MarginComparator01	U(D)INT			•	
264	Input states of the channels	USINT	•			
	ComparatorActualValue03	Bit 1				
	ComparatorActualValue01 ComparatorActualValue03	Bit 3				
	ComparatorActualValue01	Bit 5				
	ComparatorActualValue01 ComparatorActualValue03	Bit 7				
2140 + (N-1) * 256	Latch01Counter0N (Index N = 1 to 4)	U(D)INT	•			
2172 + (N-1) * 256	Latch02Counter0N (Index N = 1 to 4)	U(D)INT	•			
Communication - Input for SSI encoders						
7,184	SSIEncoder01	UDINT	•			
7,440	SSIEncoder02	UDINT	•			
7,248	OriginComparator01	UDINT			•	
7,504	OriginComparator02	UDINT			•	
7,252	MarginComparator01	UDINT			•	
7,508	MarginComparator02	UDINT			•	
264	Input states of the channels	USINT	•			
	ComparatorActualValue02	Bit 1				
	ComparatorActualValue01 ComparatorActualValue02	Bit 3				
	ComparatorActualValue01	Bit 5				
	ComparatorActualValue01 ComparatorActualValue02	Bit 7				
7,260	Latch01SSI01	UDINT	•			
7,516	Latch01SSI02	UDINT	•			
Communication - Digital outputs						
260	Output states of the channels	USINT			•	
	DigitalOutput02	Bit 1				
	DigitalOutput04	Bit 3				
	DigitalOutput06	Bit 5				
	DigitalOutput08	Bit 7				
264	Input states of the channels	USINT	•			
	StatusDigitalOutput02	Bit 1				
	StatusDigitalOutput04	Bit 3				
	StatusDigitalOutput06	Bit 5				
	StatusDigitalOutput08	Bit 7				
Communication - Outputs for PWM (pulse width modulation)						
6130 + N * 8	PWMOutput0N (Index N = 2,4,6,8)	UINT			•	
Configuration - Edge detection						
4,104	CfO_EdgeDetectFalling	USINT				•
4,106	CfO_EdgeDetectRising	USINT				•
4,108	CfO_FallingDisProtection	USINT				•
4,110	CfO_RisingDisProtection	USINT				•
Configuration - Time measurement						
4,336	CfO_EdgeTimeglobalenable	USINT				•
4344 + N * 8	CfO_EdgeTimeFallingMode0N (Index N = 1 to 8)	UINT				•
4472 + N * 8	CfO_EdgeTimeRisingMode0N (Index N = 1 to 8)	UINT				•
Communication - Time measurement						
4,342	Trigger rising edge detection	USINT			•	
	TriggerRisingCH01	Bit 0				
	...	...				
	TriggerRisingCH08	Bit 7				
4,350	Show first rising trigger edge	USINT	•			
	BusyTriggerRisingCH01	Bit 0				
	...	...				
	BusyTriggerRisingCH08	Bit 7				
4,340	Trigger falling edge detection	USINT			•	
	TriggerFallingCH01	Bit 0				
	...	...				
	TriggerFallingCH08	Bit 7				
4,348	Show first falling trigger edge	USINT	•			
	BusyTriggerFallingCH01	Bit 0				
	...	...				
	BusyTriggerFallingCH08	Bit 7				
4474 + N * 8	CountRisingCH0N (Index N = 1 to 8)	USINT	•			
4476 + N * 8	TimeStampRisingCH0N (Index N = 1 to 8)	UINT	•			

Register description

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
4478 + N * 8	TimeDiffRisingCH0N (Index N = 1 to 8)	UINT	•			
4346 + N * 8	CountFallingCH0N (Index N = 1 to 8)	USINT	•			
4348 + N * 8	TimeStampFallingCH0N (Index N = 1 to 8)	UINT	•			
4350 + N * 8	TimeDiffFallingCH0N (Index N = 1 to 8)	UINT	•			

5.3 Function model 254 - Bus controller

Unlike the function models 0 and 1, this model only offers a selection of functions with a limited scope of configuration on the module.

The following functions are provided and can be run at the same time:

- SSI encoders
- ABR encoder with configurable reference pulse edge and reference position
- 1 event counter with configurable counting direction
- 2 PWM outputs

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Module configuration - General							
N * 2 - 2	-	CfO_CFGchannel0N (Index N = 1 to 8)	USINT				•
N * 2 + 64	-	CfO_LEDNsource (Index N = 0 to 7)	USINT				•
Configuration - ABR encoder							
512	-	CfO_DIREKTIOevent0IDwr	UINT				•
544	-	CfO_DIREKTIOevent1IDwr	UINT				•
2,560	-	CfO_Counter3config	USINT				•
2,568	-	CfO_Counter3configReg0	USINT				•
2,570	-	CfO_Counter3configReg1	USINT				•
2,576	-	CfO_Counter3PresetValue1	UINT				•
2,580		CfO_Counter3PresetValue2	UINT				•
2,624	-	CfO_Counter3event0IDwr	UINT				•
2,632	-	CfO_Counter3event0config	UINT				•
2,628	-	CfO_Counter3event0mode	USINT				•
2,656	-	CfO_Counter3event1IDwr	UINT				•
2,664	-	CfO_Counter3event1config	UINT				•
2,660	-	CfO_Counter3event1mode	USINT				•
4,104	-	CfO_EdgeDetectFalling	USINT				•
4,106	-	CfO_EdgeDetectRising	USINT				•
Configuration - Event counter							
2,304	-	CfO_Counter2config	USINT				•
2,312	-	CfO_Counter2configReg0	USINT				•
2,314	-	CfO_Counter2configReg1	USINT				•
2,368	-	CfO_Counter2event0IDwr	UINT				•
2,376	-	CfO_Counter2event0config	UINT				•
2,372	-	CfO_Counter2event0mode	USINT				•
2,400	-	CfO_Counter2event1IDwr	UINT				•
2,408	-	CfO_Counter2event1config	UINT				•
2,404	-	CfO_Counter2event1mode	USINT				•
Configuration - SSI encoder							
7,176	-	CfO_SSI1cfg	UINT				•
7,180	-	CfO_SSI1control	USINT				•
7,168	-	CfO_SSI1eventIDwr	UINT				•
7,232	-	CfO_SSI1event0IDwr	UINT				•
7,240	-	CfO_SSI1event0config	UINT				•
7,236	-	CfO_SSI1event0mode	USINT				•
7,172	-	ConfigAdvanced01	UDINT				•
Configuration - PWM (pulse width modulation)							
6,160	-	CfO_PWM1prescaler	UINT				•
6,192	-	CfO_PWM3prescaler	UINT				•
Module communication - General							
40	6	Status of encoder power supply	USINT	•			
		PowerSupply01	Bit 0				
Communication - Counters and encoders							
2,336	4	EventCounter03	UINT	•			
2,592	8	ABREncoder02	INT	•			
2,628	10	ReferenceModeABR02	USINT			•	
2,630	10	StatusABR02	USINT	•			
7,184	0	SSIEncoder01	UDINT	•			
Communication - PWM (pulse width modulation)							
6,162	0	PWMOutput04	UINT			•	
6,194	8	PWMOutput08	UINT			•	

1) The offset specifies the position of the register within the CAN object.

5.4 General module registers

5.4.1 Configuring LED status indicators

Name:
CfO_LED0source to CfO_LED7source

These registers can be used to determine the function of the module LED status indicators. This allows application-controlled blink signals to be output or the states of physical inputs and outputs to be displayed.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	CfO_LED0source = 0x20 ... CfO_LED7source = 0x27

Bit structure:

Bit	Description	Values	Information
0 - 3	MODE = 0	0	LED off
		1	Blinking quickly
		2	Blinking
		3	Blinking slowly
		4	Single flash
		5	Double flash
		6 to 15	Reserved
	MODE = 1 (inverted)	0	LED on
		1	Blinking quickly
		2	Blinking
		3	Blinking slowly
		4	Single flash
		5	Double flash
		6 to 15	Reserved
	MODE = 2	0 to 7	Number of the physical input channel (bus controller default setting)
		8 to 15	Reserved
	MODE = 3	0 to 7	Number of the physical output channel
		8 to 15	Reserved
4 - 7	Selection of the mode for the status LED	0	LED blinking pattern
		1	Inverted LED blinking pattern
		2	Indicates the physical input state of a channel (bus controller default setting)
		3	Indicates the physical output states of a channel
		4 to 15	Reserved

5.4.2 Status of encoder power supply

Name:
PowerSupply01

This register indicates the status of the integrated encoder power supply. A faulty encoder supply voltage is output as a warning.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	PowerSupply01	0	24 VDC encoder power supply OK
		1	24 VDC encoder power supply faulty
1 - 7	Reserved	-	

5.5 Digital inputs and outputs

5.5.1 Configuring physical channels

Name:
CfO_CFGchannel01 to CfO_CFGchannel08

This register can be used to configure physical I/O channels 1 to 8.

Information:

Except for bit 2 (inverted input), all other bits are only available for channels 2, 4, 6 and 8.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	CfO_CFGchannel01 = 0x00 CfO_CFGchannel02 = 0x73 CfO_CFGchannel03 = 0x00 CfO_CFGchannel04 = 0x63 CfO_CFGchannel05 to 07 = 0x00 CfO_CFGchannel08 = 0x63

Bit structure:

Bit	Description	Value	Information
0	Push[1)]	0	Disabled
		1	Enabled
1	Pull[1)]	0	Disabled
		1	Enabled
2	Inverted input	0	Disabled
		1	Enabled
3	Inverted output	0	Disabled
		1	Enabled
4 - 7	Output type	0	Direct I/O
		1 to 5	Reserved
		6	PWM (channel-specific)
		7	SSI clock (channel-specific)

1) To configure a channel as an output, Push and/or Pull must be enabled.

5.5.2 Reset mask of the digital channels

Name:
CfO_OutClearMask

The settings in this register only affect the values written to registers "DigitalOutput02 to 08" on page 39.

- 0 allows manual reset of digital outputs using registers DigitalOutput02 to 08
- 1 prevents manual reset of digital outputs using registers DigitalOutput02 to 08

When value "1" is used, the output event function can be used to reset the outputs.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0	Writing 0 to the DigitalOutput02 register resets the output
		1	Writing 0 to register DigitalOutput02 does not reset output.
2	Reserved	-	
3	DigitalOutput04	0	Writing 0 to the DigitalOutput04 register resets the output
		1	Writing 0 to register DigitalOutput04 does not reset output.
4	Reserved	-	
5	DigitalOutput06	0	Writing 0 to the DigitalOutput06 register resets the output
		1	Writing 0 to register DigitalOutput06 does not reset output.
6	Reserved	-	
7	DigitalOutput08	0	Writing 0 to the DigitalOutput08 register resets the output
		1	Writing 0 to register DigitalOutput08 does not reset output.

5.5.3 Set mask of the digital channels

Name:
CfO_OutSetMask

The settings in this register only affect the values written to registers "DigitalOutput02 to 08" on page 39.

- 0 allows manual setting of digital outputs using registers DigitalOutput02 to 08.
- 1 prevents manual setting of digital outputs using registers DigitalOutput02 to 08

When value "1" is used, the output event function can be used to set the outputs.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Values	Information
0	Reserved	-	
1	DigitalOutput02	0	Writing 1 to register DigitalOutput02 sets the output.
		1	Writing 1 to register DigitalOutput02 does not set the output.
2	Reserved	-	
3	DigitalOutput04	0	Writing 1 to register DigitalOutput04 sets the output.
		1	Writing 1 to register DigitalOutput04 does not set the output.
4	Reserved	-	
5	DigitalOutput06	0	Writing 1 to register DigitalOutput06 sets the output.
		1	Writing 1 to register DigitalOutput06 does not set the output.
6	Reserved	-	
7	DigitalOutput08	0	Writing 1 to register DigitalOutput08 sets the output.
		1	Writing 1 to register DigitalOutput08 does not set the output.

5.5.4 Input states of the channels

Name:
DigitalInput01 to DigitalInput08
StatusDigitalOutput02 to StatusDigitalOutput04
ReferenceEnableSwitch01 to ReferenceEnableSwitch02
ComparatorActualValue01 to ComparatorActualValue03

Depending on the function, different names are used for the bits of these registers (see "Input states of the channels" on page 15).

This register is used to read the input state of a physical channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Physical input channel	Value	Information
0	Channel 1	0 or 1	Input status of the physical channel
...		...	
7	Channel 8	0 or 1	Input status of the physical channel

5.5.5 Output states of the channels

Name:
DigitalOutput02 to DigitalOutput08

The output state of a physical channel can be written using this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	DigitalOutput02	0 or 1	Output status of channel 2
2	Reserved	-	
3	DigitalOutput04	0 or 1	Output status of channel 4
4	Reserved	-	
5	DigitalOutput06	0 or 1	Output status of channel 6
6	Reserved	-	
7	DigitalOutput08	0 or 1	Output status of channel 8

5.6 Edge events

3 event functions are available for each physical channel:

- Falling edge
- Rising edge
- Falling and rising edge

5.6.1 Generate event on falling edge

Name:
CfO_EdgeDetectFalling

This register defines whether an event is generated on a falling edge.

Data typ	Value	Bus controller default setting
USINT	See bit structure.	64

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	No event is generated on a falling edge (bus controller default setting).
		1	Events 4096 and 4128 are generated on falling edge.
...		...	
6	Channel 7	0	No event is generated on a falling edge.
		1	Events 4103 and 4135 are generated on a falling edge. (Bus controller default setting)
7	Channel 8	0	No event is generated on a falling edge. (Bus controller default setting)
		1	Events 4103 and 4135 are generated on a falling edge.

5.6.2 Generate event on rising edge

Name:
CfO_EdgeDetectRising

This register defines whether an event is generated on a rising edge.

Data typ	Value	Bus controller default setting
USINT	See bit structure.	64

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	No event is generated on a rising edge. (Bus controller default setting)
		1	Events 4112 and 4128 are generated on rising edge.
...		...	
6	Channel 7	0	No event is generated on a rising edge.
		1	Events 4119 and 4135 are generated on a rising edge. (Bus controller default setting)
7	Channel 8	0	No event is generated on a rising edge. (Bus controller default setting)
		1	Events 4119 and 4135 are generated on a rising edge.

5.6.3 Enable limit for falling edges

Name:
CfO_FallingDisProtection

This register can be used to enable or disable the event frequency limitation for falling edges of the corresponding channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
...		...	
7	Channel 7	0	Event frequency limit enabled.
		1	Event frequency limit disabled.

5.6.4 Enable limit for rising edges

Name:
CfO_RisingDisProtection

This register can be used to enable or disable the event frequency limitation for rising edges of the corresponding channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Event frequency limit enabled.
		1	Event frequency limit disabled.
...		...	
7	Channel 8	0	Event frequency limit enabled.
		1	Event frequency limit disabled.

5.7 Direct input functions

The module is equipped with 2 "direct input functions".

5.7.1 Configure event ID for input function

Name:
CfO_DIREKTIOevent0IDwr to CfO_DIREKTIOevent1IDwr

The event IDs that trigger the "direct input function" are written to these registers. For a list of all possible event IDs, see "List of event IDs" on page 13.

Data type	Value	Information
INT	192 to 7,289	ID of the event function Bus controller default setting: CfO_DIREKTIOevent0IDwr: 0 CfO_DIREKTIOevent1IDwr: 4102

5.7.2 Configure the mode of the input function

Name:
CfO_DIREKTIOevent0mode to CfO_DIREKTIOevent1mode

The mode in which the "direct input function" operates can be set in these registers.

All comparator functions can be operated in 4 different modes. For a description, see "Comparator modes" on page 21.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Individual
		2	State change
		3	Continuous
2 - 7	Reserved	-	

5.7.3 Comparator status for comparator mask

Name:
CfO_DIREKTIOevent0compState to CfO_DIREKTIOevent1compState

This register contains the status bits that are compared with the bits specified in the "CfO_Ev0CompMask" on page 42 register, which contain the I/O input status, when an event is received.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator status of channel 1	0 or 1	
...		...	
7	Comparator status of channel 8	0 or 1	

5.7.4 Configure the comparator mask for the input function

Name:
CfO_Ev0CompMask to CfO_Ev1CompMask

If a bit is set, then the input status of the respective channel is compared with that bit in the "CfO_DIREKTIOeventcompState" on page 41 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Do not compare bit
		1	Compare bit in register
...		...	
7	Channel 8	0	Do not compare bit
		1	Compare bit in register

5.8 Direct output functions

The module is equipped with 4 "direct output functions".

5.8.1 Configure event ID for output function

Name:
CfO_DIREKTIOevent0IDwr to CfO_DIREKTIOevent3IDwr

The event IDs that trigger the "direct output function" are written to these registers. For a list of all possible event IDs, see "List of event IDs" on page 13.

Data type	Value	Information
INT	192 to 7,489	ID of event function

5.8.2 Configure channels for resetting

Name:
CfO_DIREKTIOoutclearmask0 to CfO_DIREKTIOoutclearmask3

Writing "1" to the bit position that corresponds to a channel resets the output if the output event function is being executed. This corresponds to writing "0" in registers "DigitalOutput 02 to 08" on page 39.

The bit that corresponds to channels that should be reset should be set to "1" in the "CfO_OutClearMask" on page 37 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	Channel 2	0	Reset channel 2
		1	Do not reset channel 2
2	Reserved	-	
3	Channel 4	0	Reset channel 4
		1	Do not reset channel 4
4	Reserved	-	
5	Channel 6	0	Reset channel 6
		1	Do not reset channel 6
6	Reserved	-	
7	Channel 8	0	Reset channel 8
		1	Do not reset channel 8

5.8.3 Configure channels for setting

Name:
CfO_DIREKTIOoutsetmask0 to CfO_DIREKTIOoutsetmask3

Writing "1" to the bit position that corresponds to a channel sets the output if the output event function is being executed. This corresponds to writing "1" in registers "DigitalOutput 02 to 08" on page 39.

The bit that corresponds to channels that should be reset should be set to "1" in the "CfO_OutSetMask" on page 38 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Reserved	-	
1	Channel 2	0	Set channel 2
		1	Do not set channel 2
2	Reserved	-	
3	Channel 4	0	Set channel 4
		1	Do not set channel 4
4	Reserved	-	
5	Channel 6	0	Set channel 6
		1	Do not set channel 6
6	Reserved	-	
7	Channel 8	0	Set channel 8
		1	Do not set channel 8

5.9 Counters and encoders

The module is equipped with 4 internal counter functions with 2 counter registers each.

5.9.1 Counter event functions

Each of the 4 counter functions has 2 counter event functions.

5.9.1.1 Configure counter mode

Name:
CfO_Counter1config to CfO_Counter4config

The counting mode for the counter function can be configured in these registers. Each counter function can be operated in 3 different modes (see "Counters and encoders" on page 18).

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	CfO_Counter**N**config N(2): 0 N(3): 1

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0 - 1	Counter mode	00	Edge counter
		01	Encoder AB (bus controller default setting)
		11	Up/Down counter
2 - 7	Reserved	-	

5.9.1.2 Configuring the calculation of internal counters

Name:
CfO_Counter1configReg0 to CfO_Counter4configReg0 ("counter1")
CfO_Counter1configReg1 to CfO_Counter4configReg1 ("counter2")

The calculation of internal registers "counter1" and "counter2" can be configured in these registers. For information about using these internal registers, see "Counter value calculation" on page 19.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	CfO_Counter**N**configReg0 N(2): 1 N(3): 13 CfO_Counter**N**configReg1 N(2.3): 0

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0	counter 1 - use	0	0 is added instead of "counter 1"
		1	"counter 1" is used for addition
1	counter 1 - sign	0	The sign of the "counter 1" register is not changed for addition
		1	The sign of the "counter 1" register is reversed for addition
2	counter 2 - use	0	0 is added instead of "counter 2"
		1	"counter 2" is used for addition
3	counter 2 - sign	0	The sign of the "counter 2" register is not changed for addition
		1	The sign of the "counter 2" register is reversed for addition
4 - 7	Reserved	-	

5.9.1.3 Offset value for referencing

Name:
CfO_Counter1PresetValue1 to CfO_Counter4PresetValue1
CfO_Counter1PresetValue1_32Bit to CfO_Counter4PresetValue1_32Bit (SW_reference_counter1)

CfO_Counter1PresetValue2 to CfO_Counter4PresetValue2
CfO_Counter1PresetValue2_32Bit to CfO_Counter4PresetValue2_32Bit (SW_reference_counter2)

These registers can be used to define an offset value for referencing. This value is copied to the internal "SW_reference_counter" on page 19 register of the respective counter register.

Data type	Value	Information
INT	-32768 to 32767	Bus controller default setting: 0[1)]
DINT	-2,147,483,648 to 2,147,483,647	

1) The bus controller default value applies only to the register numbers specified in function model 254.

5.9.1.4 Counter register

Name:
ABEncoder01 to ABEncoder04
ABREncoder01 to ABREncoder02
Counter01 to Counter04
EventCounter01 to EventCounter08

Different names are used for these registers depending on the function (see "Counters and encoders" on page 18).

The result of the counter value calculation for the respective register is indicated in these registers. Depending on the function, this corresponds to either the encoder position or the counter value.

For the relationship between physical channels, the count registers and the names used, see "Counters and encoders" on page 18 and "Description of channel assignments" on page 12.

Data type	Value	Information
INT	-32768 to 32767	Encoder position or counter value
DINT[1)]	-2,147,483,648 to 2,147,483,647	Encoder position or counter value

1) Only in function model 1

5.9.1.5 Status of the ABR encoder

Name:
StatusABR01 to StatusABR02

These registers contain the homing state of the ABR encoder.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	0	
2	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
3	State change when referencing is complete	0 or 1	
4	Bit is always 1 after the first reference pulse.	0	No reference pulses have occurred since the start of referencing.
		1	The first reference pulse has occurred.
5 - 7	Continuous counter	xxx	Increased with each reference pulse.

Examples of possible values

0b00000000	= 0x00	Referencing disabled or homing procedure already active.
0b00111100	= 0x3C	First reference complete, reference value applied in the "ABREncoder0" on page 45 register
0bxxx11100	= 0xxB	Bits 5 to 7 are subsequently modified with each reference pulse.
0bxxx1x100	= 0xxx	Continuous changing of bits with continuous referencing setting, the reference value is transferred to register "ABREncoder0[x]" on page 45 with each reference pulse.

5.9.1.6 Configure ABR referencing mode

Name:
ReferenceModeABR01 to ReferenceModeABR02

The bits in this register are used to configure the reaction to the configured reference pulse.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Sets the referencing mode	00	Homing disabled
		01	Single shot referencing
		10	Reserved
		11	Continuous referencing
2 - 5	Reserved	-	
6 - 7	Reserved	11	Must always be 11!

This results in the following values:

0b00000000	= 0x00	Homing disabled
0b11000001	= 0xC1	Single shot referencing → When starting over after the referencing process is complete, the value 0x00 must be written to start again. Wait until the "StatusABR" on page 45 register also takes on the value 0x00, then the value 0xC1 can be written again.
0b11000011	= 0xC3	Continuous referencing → is performed automatically with each reference pulse.

5.9.2 Comparator functions

The AB, ABR and up/down counters have a comparator function.

5.9.2.1 Configure event ID for comparator

Name:
CfO_Counter1event0IDwr to CfO_Counter4event0IDwr (event function 1)
CfO_Counter1event1IDwr to CfO_Counter4event1IDwr (event function 2)

The event IDs that the counter event function should trigger are written to these registers. For a list of all possible event IDs, see "List of event IDs" on page 13.

Data type	Value	Information
INT	192 to 7,489	ID of counter event function Bus controller default setting:[1)] CfO_Counter3event0IDwr: 545 All others: 0

1) The bus controller default value applies only to the register numbers specified in function model 254.

5.9.2.2 Configure calculation of comparator

Name:
CfO_Counter1event0config to CfO_Counter4event0config (event function 1)
CfO_Counter1event1config to CfO_Counter4event1config (event function 2)

The counter event function of the respective counter function can be configured in these registers.

Bits 0 to 3 configure the calculation of the comparison or latch the value used. This calculation is analogous to the calculation of the counter registers (see "Counter value calculation" on page 19).

Bits 8 to 13 can be used to limit the number of bits used for the comparison. A mask is created from 2^n - 1 in which an AND operation is performed before the comparison. This makes it possible to generate a comparator pulse every 2^n increments.

Data type	Values	Bus controller default setting[1)]
UINT	See the bit structure.	0

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0	counter1 - Use	0	0 is added instead of register "counter1" (bus controller default setting).
		1	"counter1" is used for addition.
1	counter1 - Sign	0	The sign of register "counter1" is not changed for addition (bus controller default setting).
		1	The sign of register "counter1" is reversed for addition.
2	counter2 - Use	0	0 is added instead of register "counter2" (bus controller default setting).
		1	"counter2" is used for addition.
3	counter2 - Sign	0	The sign of register "counter2" is not changed for addition (bus controller default setting).
		1	The sign of register "counter2" is reversed for addition.
4 - 7	Reserved	-	
8 - 13	Number of bits for the comparator mask	x	The mask value is calculated from 2^n-1, where n is the value set in these bits. (Bus controller default setting: 0)
14	Reserved	-	
15	Comparison mode of the width of the window	0	MarginComparator ≥ (Current position - OriginComparator) (bus controller default setting)
		1	MarginComparator > (Current position - OriginComparator)

5.9.2.3 Configure mode and latching of comparator function

Name:
CfO_Counter1event0mode to CfO_Counter4event0mode (event function 1)
CfO_Counter1event1mode to CfO_Counter4event1mode (event function 2)

It is possible to set the mode of the comparator function as well as possible copying of the latched registers in these registers.

All comparator functions can be operated in 4 different modes. For a description, see "Comparator modes" on page 21.

Bits 4 to 7 can be used to define hardware referencing actions.

For each counter event, the counter value of internal absolute value counters "abs1" or "abs2" can be applied to the respective "HW_reference_counter" register according to these bits (see "Counter value calculation" on page 19). This is intended for direct hardware referencing of the counter values.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	0

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Individual
		2	State change
		3	Continuous
2 - 3	Reserved	-	
4	Copy abs1 counter value	0	No action
		1	For FALSE event → Hardware reference counter 1 = abs1
5	Copy abs2 counter value	0	No action
		1	For FALSE event → Hardware reference counter 2 = abs2
6	Copy abs1 counter value	0	No action
		1	For TRUE event → Hardware reference counter 1 = abs1
7	Copy abs2 counter value	0	No action
		1	For TRUE event → Hardware reference counter 2 = abs2

5.9.2.4 Comparator origin

Name:
OriginComparator01 to OriginComparator02 (ABR encoder)
OriginComparator01 and OriginComparator03 (AB encoder and up/down counter)

This register is available for the comparator function of the AB/ABR encoder and up/down counter.

It defines the position value at which the respective configured comparator output channel is set.

Data type	Value	Information
INT	-32768 to 32767	Comparator window origin, 16-bit
DINT	-2,147,483,648 to 2,147,483,647	Comparator window origin, 32-bit

5.9.2.5 Width of the comparator

Name:
MarginComparator01 to MarginComparator02 (ABR encoder)
MarginComparator01 and MarginComparator03 (AB encoder and up/down counter)

This register is available for the comparator function of the AB/ABR encoder and up/down counter.

It defines the width of the comparator window in the positive direction.

Data type	Value	Information
INT	-32768 to 32767	Width of comparator window, 16-bit
DINT	-2,147,483,648 to 2,147,483,647	Width of comparator window, 32-bit

5.9.2.6 Read latch position or counter value

Name:
Latch01AB01 to Latch01AB04
Latch01Counter01 to Latch01Counter04
Latch01ABR01 to Latch01ABR02
Latch02AB01 to Latch02AB04
Latch02Counter01 to Latch02Counter04

Different names are used for these registers depending on the function (see "Latch function" on page 22).

If the comparator returns TRUE, then the current counter value is latched and copied to these registers. The calculation of the comparator value used for the latch can be configured in register "CfO_Counter[x]event[y]config" on page 47.

Data type	Value	Information
INT	-32768 to 32767	Latched encoder position or counter value
DINT[1)]	-2,147,483,648 to 2,147,483,647	Latched encoder position or counter value

1) Only in function model 1

5.10 SSI encoder interface

The module provides 2 SSI encoders that are directly supported by the hardware.

5.10.1 SSI event functions

The 2 SSI counters each consist of an event function with an event input. The SSI cycle is started when an event is received on this input.

5.10.1.1 Configure event ID for SSI

Name:
CfO_SSI1eventIDwr to CfO_SSI2eventIDwr

The event IDs that should trigger the SSI cycle are written to these registers. For a list of all possible event IDs, see "List of event IDs" on page 13.

Data type	Value	Information
INT	192 to 7,233	ID of event function Bus controller default setting: 225[1)]

1) The bus controller default value applies only to the register numbers specified in function model 254.

5.10.1.2 Configure SSI

Name:
CfO_SSI1cfg to CfO_SSI2cfg

This configuration register sets the encoding, clock rate and number of bits.

Data type	Values	Bus controller default setting[1)]
UINT	See the bit structure.	0

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0 - 5	SSI value valid bits	x	
6 - 7	Clock rate	00	1 MHz (bus controller default setting)
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros
14	Reserved	0	
15	Keying	0	Binary encoding (bus controller default setting)
		1	Gray encoding

5.10.1.3 SSI advanced configuration

Name:
ConfigAdvanced01 to ConfigAdvanced02

This configuration register is used to set the encoding, clock rate, bit count and monostable multivibrator check settings.

It only differs from "CfO_SSI1cfg" on page 49 by data length and additional monostable multivibrator testing.

Data type	Value	Bus controller default setting[1)]
UDINT	See bit structure.	0x10000

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Name	Value	Information
0 - 5	SSI value valid bits	x	Bus controller default setting: 0
6 - 7	Clock rate	00	1 MHz (bus controller default setting)
		01	500 kHz
		10	250 kHz
		11	125 kHz
8 - 13	SSI number of bits	x	Number of bits including leading zeros Bus controller default setting: 0
14	Reserved	0	
15	Encoding	0	Binary encoding (bus controller default setting)
		1	Gray encoding
16 - 17	Monostable multivibrator check	00	Check OFF, no additional clock bit
		01	Check set to high level (bus controller default setting)
		10	Check set to low level
		11	Level is clocked but ignored
18 - 31	Reserved	0	

5.10.1.4 Enable SSI event function

Name:
CfO_SSI1control to CfO_SSI2control

The 2 "SSI encoder events" on page 23 can be enabled/disabled using this register.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	0

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0	Event: "SSI valid"	0	Not transmitted (bus controller default setting)
		1	Sent
1	Event: "SSI ready"	0	Not sent
		1	Sent
2 - 7	Reserved	-	

5.10.1.5 Read SSI position

Name:
SSIEncoder01 to SSIEncoder02

The last transferred SSI position can be read out from this register. The SSI encoder value is displayed as a 32-bit position value. This position value is calculated synchronously with the X2X cycle.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Last SSI position transferred

5.10.2 SSI comparator function

A permanently assigned comparator function is available on the module for the SSI function.

5.10.2.1 Configure event ID for SSI comparator

Name:
CfO_SSI1event0IDwr to CfO_SSI2event0IDwr

The event IDs that should trigger the SSI comparator function are written to these registers. For a list of all possible event IDs, see "List of event IDs" on page 13.

Data type	Value	Information
INT	192 to 7,233	ID of comparator function Bus controller default setting: 0[1)]

1) The bus controller default value applies only to the register numbers specified in function model 254.

5.10.2.2 Configure the mode of the SSI comparator function

Name:
CfO_SSI1event0mode to CfO_SSI2event0mode

The mode of the comparator function can be set in these registers.

All comparator functions can be operated in 4 different modes. For a description, see "Comparator modes" on page 21.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	0

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0 - 1	Comparator mode	0	Off
		1	Individual
		2	State change
		3	Continuous
2 - 7	Reserved	-	

5.10.2.3 Configure calculation of SSI comparator

Name:
CfO_SSI1event0config and CfO_SSI2event0config

The position value used for calculating the comparison is configured in this register.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	0

1) The bus controller default setting value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0 - 5	SSI data bits	x	Number of data bits used for masking
6 - 7	Reserved	-	
8 - 13	Comparator mask	x	The mask value is calculated from 2^n-1, where n is the value configured in SSI data bits. Default: 0
14	Comparator mode	0	MarginComparator ≥ SSI position - OriginComparator
		1	MarginComparator > SSI position - OriginComparator

5.10.2.4 Origin of the SSI comparator

Name:
OriginComparator01_SSI to OriginComparator02_SSI

This register contains the origin of the window comparator.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Origin of the window comparator.

5.10.2.5 Width of the SSI comparator

Name:
MarginComparator01_SSI to MarginComparator02_SSI

This register provides the width of the window comparator.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Width of the SSI window comparator

5.10.2.6 Read SSI latch position

Name:
Latch01SSI01 to Latch01SSI02

If the SSI window comparator returns "True", then the current SSI position is latched and saved in this register.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Latched SSI position

5.11 PWM - Pulse width modulation

The module provides 4 PWM functions that are directly supported by the hardware. One 24 V output channel is permanently set for each PWM function and cannot be modified.

5.11.1 Configure PWM prescaler

Name:
CfO_PWM0prescaler to CfO_PWM3prescaler

This register is used to set the length of the PWM cycle.

Data type	Value	Information
UINT	2 to 65535	Prescaler for PWM cycle Bus controller default setting: 480[1)]

1) The bus controller default setting value applies only to the register numbers specified in function model 254.

5.11.2 Output PWM values

Name:
PWMOutput02, PWMOutput04, PWMOutput06, PWMOutput08

This register is used to set the proportion in 1/10% steps of the PWM cycle for which the PWM output is switched to logical 1. Logical 1 means that the PWM output is switched on.

Data type	Value	Information
UINT	0	PWM output always off
	1 to 999	Switch-on time in 1/10% increments
	1000	PWM output always on

5.12 Time measurement function

The module has a time measurement function for each I/O channel. It can be configured separately for rising and falling edges on each channel.

5.12.1 Enable time measurement function

Name:
CfO_EdgeTimeglobalenable

This register is used to enable or disable the time measurement function for the entire module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Time measurement function	0	Disabled for entire module
		1	Enabled for entire module
1 - 7	Reserved	-	

5.12.2 Configure time measurement function for the falling edge

Name:
CfO_EdgeTimeFallingMode01 to CfO_EdgeTimeFallingMode08

These registers can be used to configure the time measurement function for the falling edge of the respective channel.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Selects the channel for the starting edge	0	Channel 1
		...	
		7	Channel 8
4	Selects the edge for the starting edge	0	The falling edge of the channel configured in bits 0 to 3 serves as the starting edge.
		1	The rising edge of the channel configured in bits 0 to 3 serves as the starting edge.
5 - 6	Reserved	-	
7	Trigger	0	Triggered[1]
		1	Continuous[2]
8 - 11	Previous start edge	0 to 15	The value determines which entry in the starting edge FIFO should be used to calculate the time difference.
12 - 15	Time measurement resolution	0	8 Mhz
		1	4 Mhz
		2	2 Mhz
		3	1 Mhz
		4	500 kHz
		5	250 kHz
		6	125 kHz
		7	625 kHz

1) The time measurement is triggered by the corresponding bit in the "TriggerRisingCH" on page 54 register.
2) Time measurement runs continuously and is triggered at every edge.

5.12.3 Configure time measurement function for the rising edge

Name:
CfO_EdgeTimeRisingMode01 to CfO_EdgeTimeRisingMode08

These registers can be used to configure the time measurement function for the rising edge of the respective channel.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Selects the channel for the starting edge	0	Channel 1
		...	
		7	Channel 8
4	Selects the edge for the starting edge	0	The falling edge of the channel configured in bits 0 to 3 serves as the starting edge.
		1	The rising edge of the channel configured in bits 0 to 3 serves as the starting edge.
5 - 6	Reserved	-	
7	Trigger	0	Triggered[1]
		1	Continuous[2]
8 - 11	Previous start edge	0 to 15	The value determines which entry in the starting edge FIFO should be used to calculate the time difference.
12 - 15	Time measurement resolution	0	8 Mhz
		1	4 Mhz
		2	2 Mhz
		3	1 Mhz
		4	500 kHz
		5	250 kHz
		6	125 kHz
		7	625 kHz

1) The time measurement is triggered by the corresponding bit in the "TriggerRisingCH" on page 54 register.
2) Time measurement runs continuously and is triggered at every edge.

5.12.4 Trigger falling edge detection

Name:
TriggerFallingCH01 to TriggerFallingCH08

If bit 7 "Trigger" is cleared in register "CfO_EdgeTimeFallingMode" on page 53, then detection of a falling edge on the respective input can be triggered using the respective bit in this register. After a bit has been set, the next falling edge on the corresponding channel is detected.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TriggerFallingCH01	0	Falling edges on channel 1 are not detected
		1	The next falling edge on channel 1 will be detected
...		...	
7	TriggerFallingCH08	0	Falling edges on channel 8 are not detected
		1	The next falling edge on channel 8 will be detected

5.12.5 Trigger rising edge detection

Name:
TriggerRisingCH01 to TriggerRisingCH08

If bit "Continued/Triggered" in register "CfO_EdgeTimeRisingMode" on page 53 is cleared, then detection of a rising edge on the respective input can be triggered using the respective bit in this register. After a bit has been set, the next rising edge on the corresponding channel is detected.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Trigger rising edge - Channel 1	0	Rising edges on channel 1 are not detected
		1	The next rising edge on channel 1 will be detected
...		-	
7	Trigger rising edge - Channel 8	0	Rising edges on channel 8 are not detected
		1	The next rising edge on channel 8 will be detected

5.12.6 Show first falling trigger edge

Name:
BusyTriggerFallingCH01 to BusyTriggerFallingCH08

If edges are triggered via the bits in register "TriggerFallingCH" on page 54, a set bit in this register indicates that no falling edge has occurred on the corresponding channel since the respective bit in register "TriggerFallingCH" was set. If a falling edge occurs on the respective channel, the corresponding BusyTriggerFalling bit is deleted again.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	BusyTriggerFallingCH01	0	Falling edge detected on channel 1
		1	Module waiting for a falling edge on channel 1
...		...	
7	BusyTriggerFallingCH08	0	Falling edge detected on channel 8
		1	Module waiting for a falling edge on channel 8

5.12.7 Show first rising trigger edge

Name:
BusyTriggerRisingCH01 to BusyTriggerRisingCH08

If edges are triggered via the bits in register "TriggerRisingCH" on page 54, a set bit in this register indicates that no rising edge has occurred on the corresponding channel since the respective bit in register "TriggerRisingCH" was set. If a rising edge occurs on the respective channel, the corresponding BusyTriggerRising bit is deleted again.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	BusyTriggerRisingCH01	0	Rising edge detected on channel 1
		1	Module waiting for a rising edge on channel 1
...		...	
7	BusyTriggerRisingCH08	0	Rising edge detected on channel 8
		1	Module waiting for a rising edge on channel 8

5.12.8 Count falling trigger edges

Name:
CountFallingCH01 to CountFallingCH08

These registers contain cyclic counters that are incremented with each falling edge detected on the respective channel.

Data type	Value	Information
USINT	0 to 255	Counter for falling edges

5.12.9 Count rising trigger edges

Name:
CountRisingCH01 to CountRisingCH08

These registers contain cyclic counters that are incremented with each rising edge detected on the respective channel.

Data type	Value	Information
USINT	0 to 255	Counter for rising edges

5.12.10 Time stamp of falling edge

Name:
TimeStampFallingCH01 to TimeStampFallingCH08

When a falling edge occurs on the respective channel, the current counter value of the module timer is copied to these registers.

Data type	Value	Information
UINT	0 to 65535	Timestamp for rising edges

5.12.11 Time stamp of the rising edge

Name:
TimeStampRisingCH01 to TimeStampRisingCH08

When a rising edge occurs on the respective channel, the current counter value of the module timer is copied to these registers.

Data type	Value	Information
UINT	0 to 65535	Timestamp for rising edges

5.12.12 Time difference of falling edge

Name:
TimeDiffFallingCH01 to TimeDiffFallingCH08

When a falling edge occurs on the respective channel, the time difference compared to the starting edge configured in bit 4 of the "CfO_EdgeTimeFallingMode" on page 53 register is copied to this register.

Data type	Value	Information
UINT	0 to 65,535	Time difference from starting edge

5.12.13 Time difference of rising edge

Name:
TimeD-iffRisingCH01 to TimeDiffRisingCH08

When a rising edge occurs on the respective channel, the time difference compared to the starting edge configured in bit 4 of the "CfO_EdgeTimeRisingMode" on page 53 register is copied to this register.

Data type	Value	Information
UINT	0 to 65,535	Time difference from starting edge

5.13 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
128 µs

5.14 Maximum cycle time

The maximum cycle time specifies the time up to which the bus cycle can be increased without internal counter overflows causing module malfunctions.

Maximum cycle time
16 ms

5.15 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
128 µs