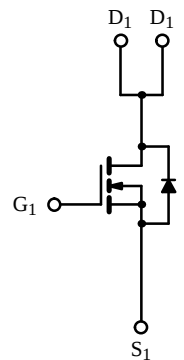
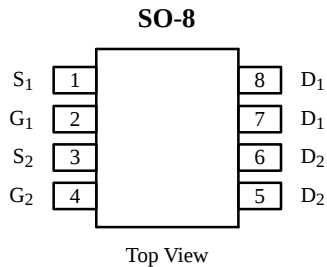


Dual N- and P-Channel 60-V, 175°C Rated MOSFET

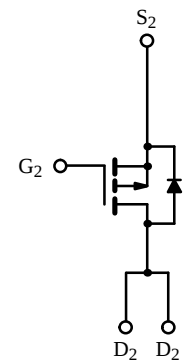
Product Summary

	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
N-Channel	60	0.055 @ V _{GS} = 10 V	± 4.5
		0.075 @ V _{GS} = 4.5 V	± 3.9
P-Channel	-60	0.120 @ V _{GS} = -10 V	± 3.1
		0.150 @ V _{GS} = -4.5 V	± 2.8

175°C Rated
Maximum Junction Temperature
TrenchFET™
Power MOSFETs



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	60	−60	V
Gate-Source Voltage		V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 175 °C) ^a	T _A = 25 °C	I _D	± 4.5	± 3.1	A
	T _A = 70 °C		± 3.8	± 2.6	
Pulsed Drain Current		I _{DM}	± 30	± 30	
Continuous Source Current (Diode Conduction) ^a		I _S	2.0	−2.0	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	2.4		W
	T _A = 70 °C		1.7		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 175		°C

Thermal Resistance Ratings

Parameter	Symbol	N- or P- Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70167.

Specifications (T_J = 25 °C Unless Otherwise Noted)

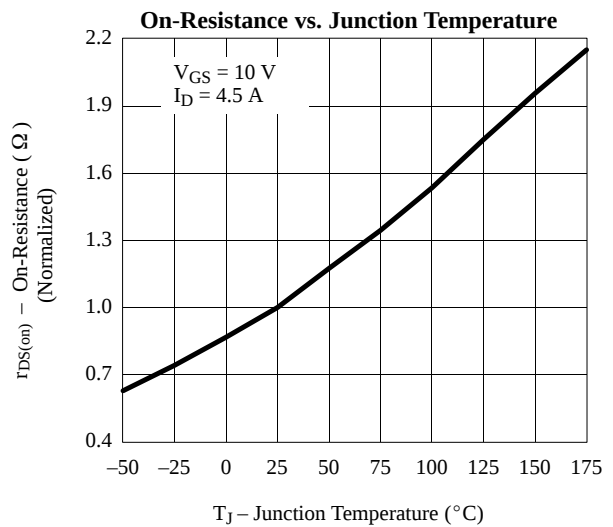
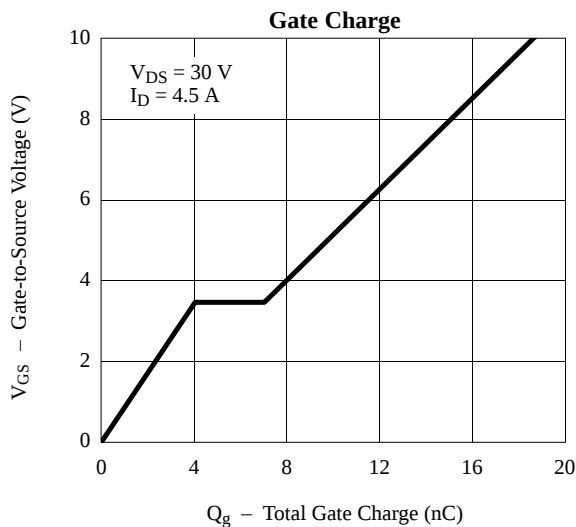
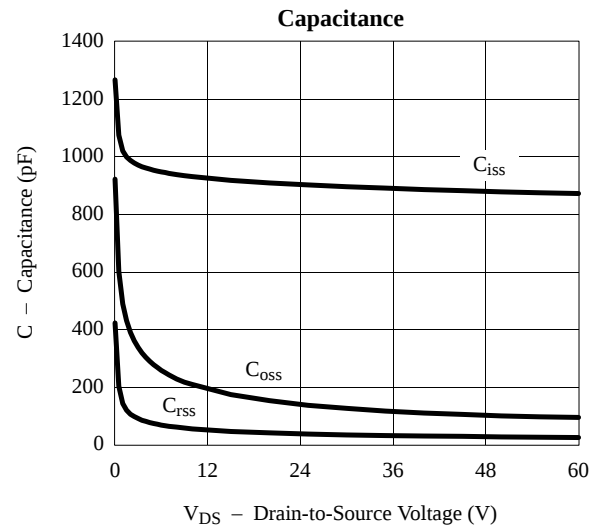
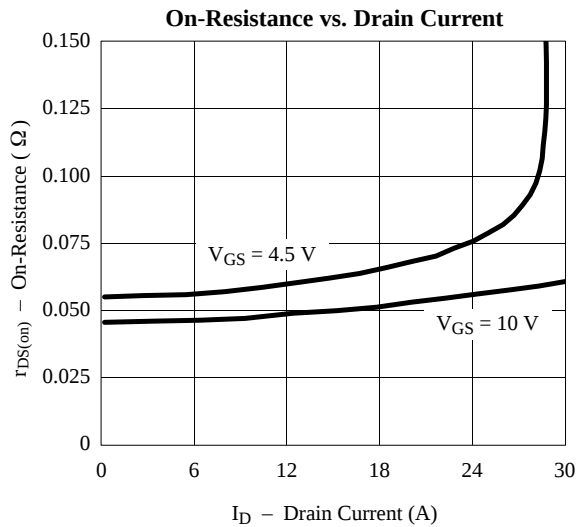
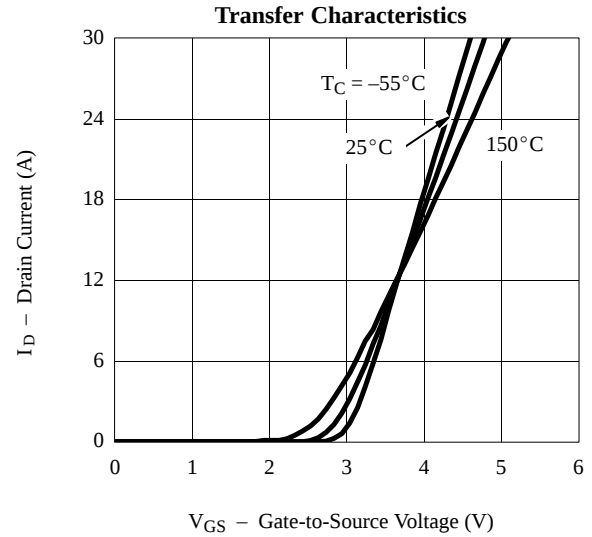
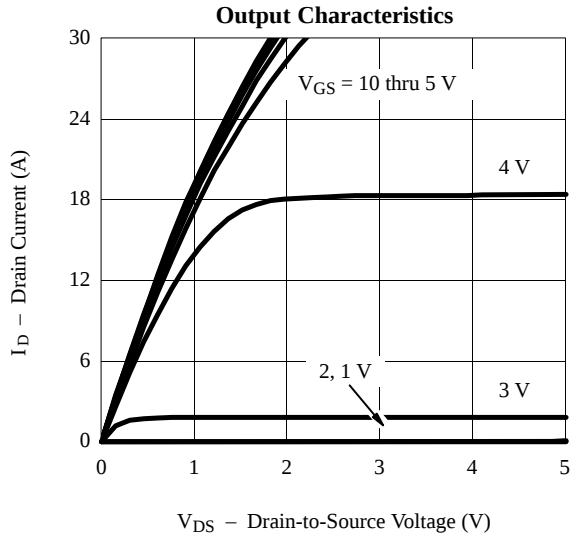
Parameter	Symbol	Test Condition		Min	Typ ^a	Max	Unit	
Static								
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1			V	
		V _{DS} = V _{GS} , I _D = −250 μA	P-Ch	−1				
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	N-Ch			± 100	nA	
			P-Ch			± 100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V	N-Ch			2	μA	
		V _{DS} = −60 V, V _{GS} = 0 V	P-Ch			−2		
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			25		
		V _{DS} = −60 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			−25		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	20			A	
		V _{DS} ≤ −5 V, V _{GS} = −10 V	P-Ch	−20				
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 4.5 A	N-Ch		0.045	0.055	Ω	
		V _{GS} = −10 V, I _D = −3.1 A	P-Ch		0.100	0.120		
		V _{GS} = 4.5 V, I _D = 3.9 A	N-Ch		0.055	0.075		
		V _{GS} = −4.5 V, I _D = −2.8 A	P-Ch		0.125	0.150		
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 4.5 A	N-Ch		13		S	
		V _{DS} = −15 V, I _D = −3.1 A	P-Ch		7.5			
Diode Forward Voltage ^b	V _{SD}	I _S = 2.0 A, V _{GS} = 0 V	N-Ch		0.9	1.2	V	
		I _S = −2.0 A, V _{GS} = 0 V	P-Ch		−0.8	−1.2		
Dynamic ^a								
Total Gate Charge	Q _g	N-Channel V _{DS} = 30 V, V _{GS} = 10 V, I _D = 4.5 A P-Channel V _{DS} = −30 V, V _{GS} = −10 V I _D = −3.1A	N-Ch		19	30	nC	
Gate-Source Charge	Q _{gs}		P-Ch		16	25		
			N-Ch		4			
			P-Ch		4			
Gate-Drain Charge	Q _{gd}	N-Ch		3				
		P-Ch		1.6				
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 30 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = −30 V, R _L = 30 Ω I _D ≅ −1 A, V _{GEN} = −10 V, R _G = 6 Ω	N-Ch		13	20	ns	
Rise Time	t _r		P-Ch		8	15		
			N-Ch		11	20		
			P-Ch		10	20		
Turn-Off Delay Time	t _{d(off)}		N-Ch		36	60		
			P-Ch		12	25		
Fall Time	t _f		N-Ch		11	20		
			P-Ch		35	50		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2 A, di/dt = 100 A/μs	N-Ch		35	60		
		I _F = −2 A, di/dt = 100 A/μs	P-Ch		60	90		

Notes

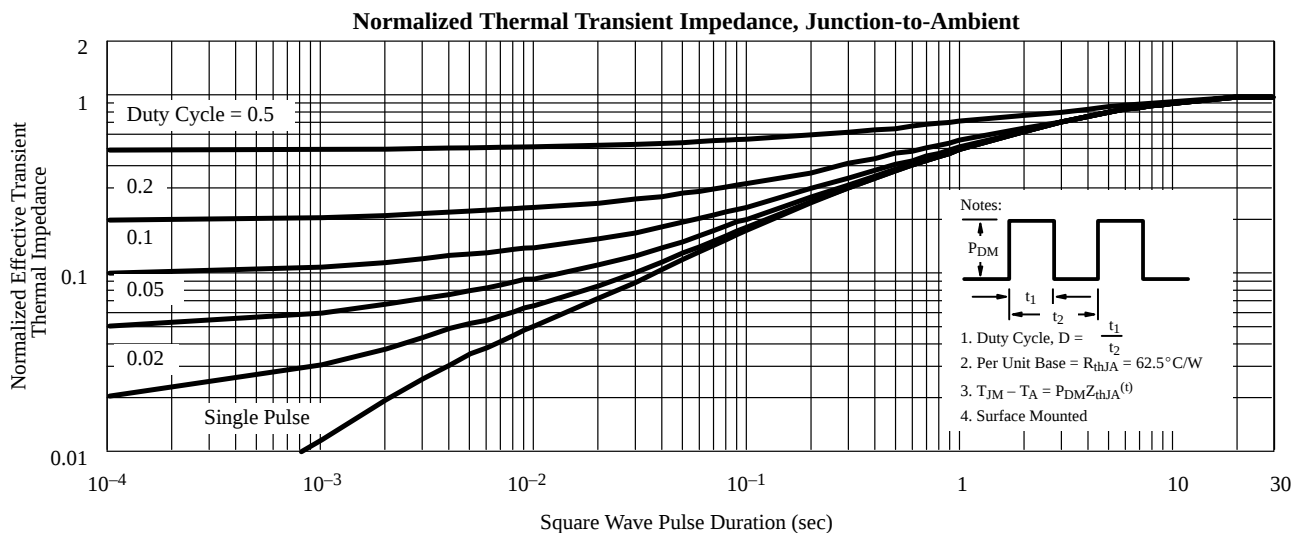
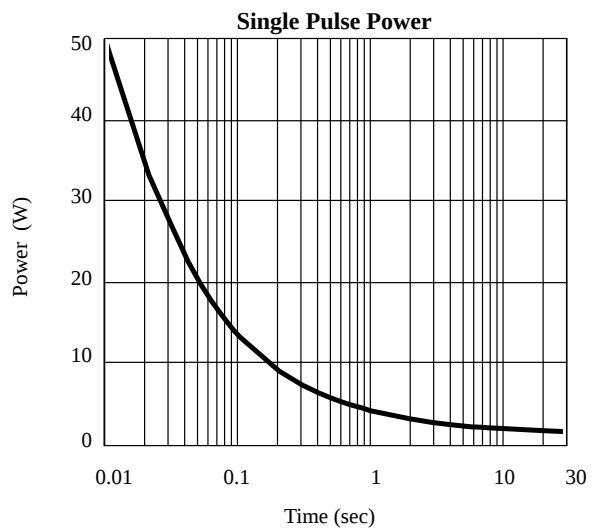
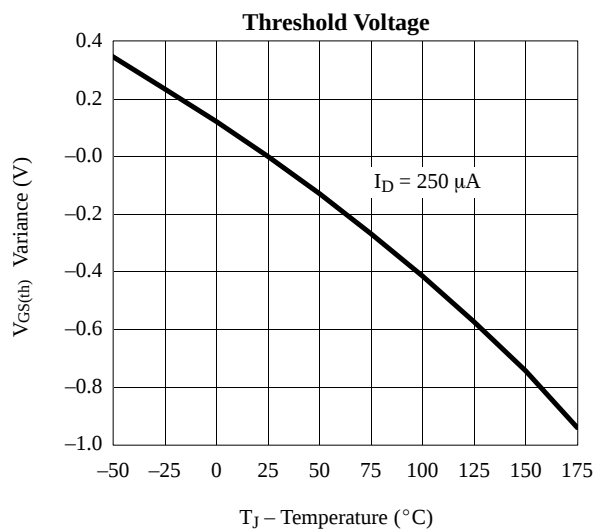
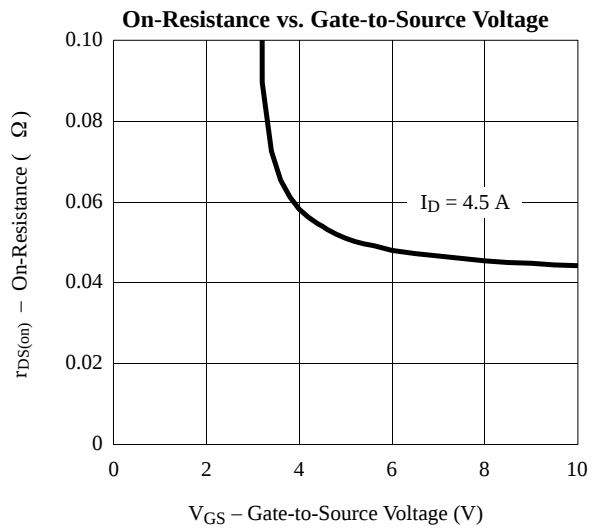
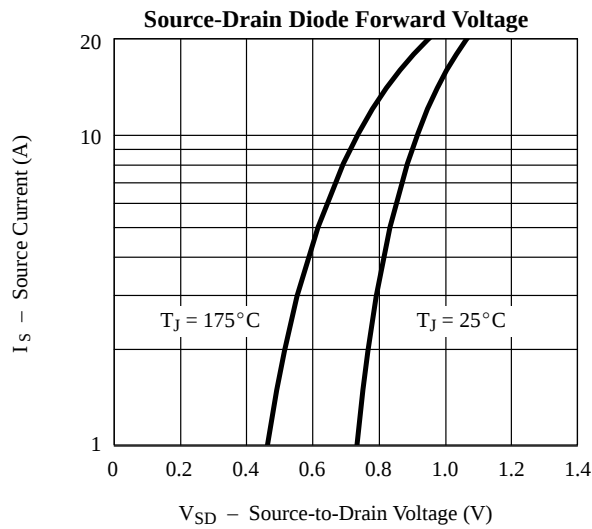
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Typical Characteristics (25°C Unless Otherwise Noted) N-Channel

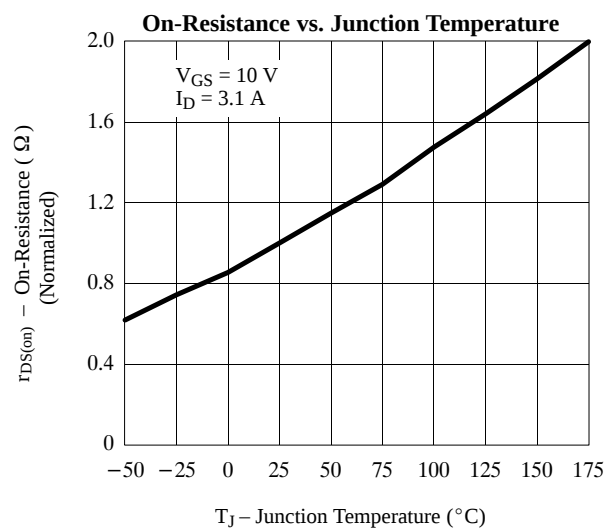
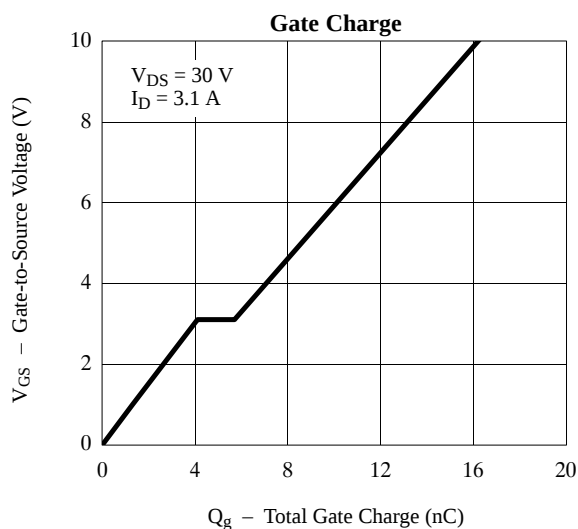
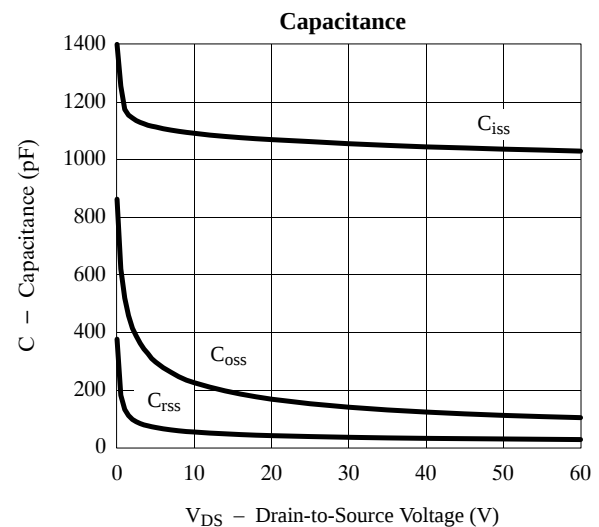
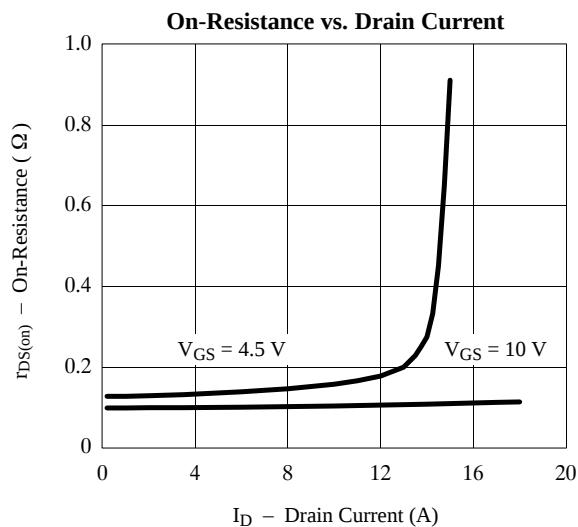
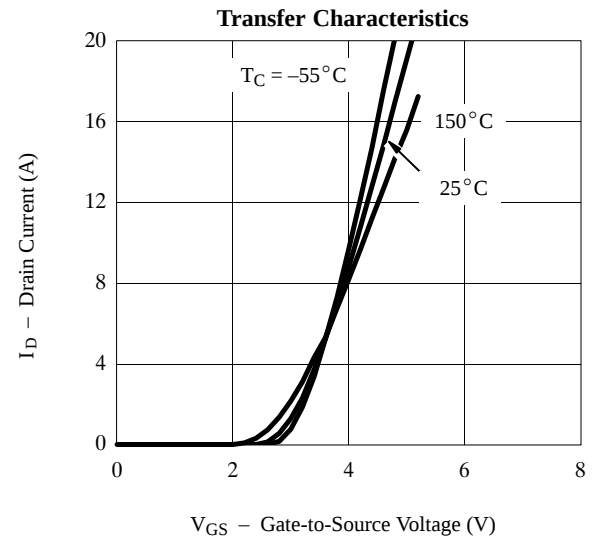
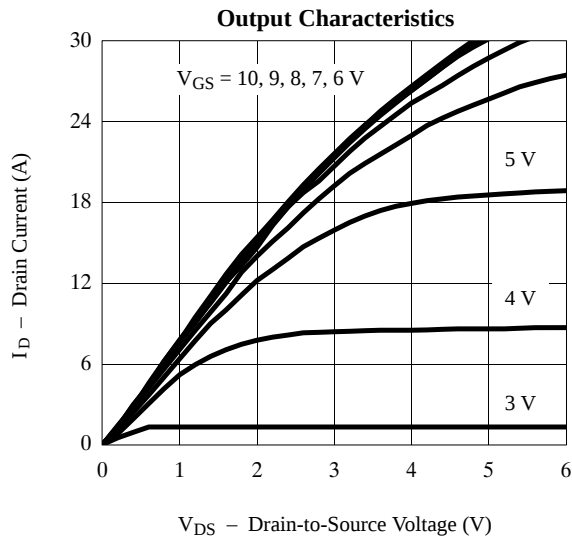


Typical Characteristics (25°C Unless Otherwise Noted) N-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel



Typical Characteristics (25°C Unless Noted)

P-Channel

