TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7W126FU

Dual BUS Buffer

The TC7W126FU is a high speed C^2MOS Dual BUS Buffers fabricated with silicon gate C^2MOS technology.

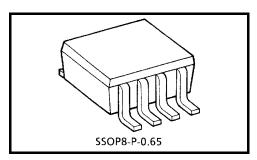
It achieves the high speed operation similar to equivalent LSTTL while maintaining the C²MOS low power dissipation.

The require 3-state control input G to be set low to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $t_{pd} = 10 \text{ ns (typ.)}$ at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 2 \mu A \text{ (max)}$ at $T_{a} = 25 \text{°C}$
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: | I_{OH} | = I_{OL} = 6 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: VCC (opr) = 2 to 6 V



Weight: 0.02 g (typ.)

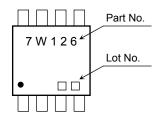
Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	–0.5 to 7	V
DC input voltage	V _{IN}	-0.5 to V_{CC} + 0.5	٧
DC output voltage	V _{OUT}	-0.5 to V_{CC} + 0.5	٧
Input diode current	I _{IK}	±20	mA
Output diode current	lok	±20	mA
DC output current	lout	±35	mA
DC V _{CC} /ground current	I _{CC}	±37.5	mA
Power dissipation	PD	300	mW
Storage temperature range	T _{stg}	-65 to 150	°C
Lead temperature (10 s)	TL	260	°C

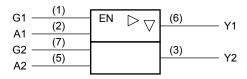
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

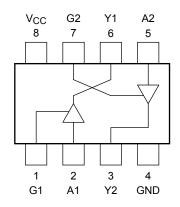
Marking



Logic Diagram



Pin Configuration (top view)



Truth Table

Inp	Output			
G	Α	Y		
L	Х	Z		
Н	L	L		
Н	Н	Н		

X: Don't care

Z: High impedance

Operating Ranges

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2 to 6	V
Input voltage	V _{IN}	0 to V _{CC}	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature range	T _{opr}	−40 to 85	°C
		0 to 1000 (V _{CC} = 2.0 V)	ns
Input rise and fall time	t _r , t _f	0 to 500 (V _{CC} = 4.5 V)	
		0 to 400 (V _{CC} = 6.0 V)	

2

Electrical Characteristics

DC Electrical Characteristics

Characteristics Symbol Test Co		Symbol	Symbol Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
		V _{CC} (V)		Min	Тур.	Max	Min	Max			
F		V _{IH}	_		2.0	1.5	_	_	1.5	_	-
	High level				4.5	3.15	_	_	3.15	_	
Input voltage					6.0	4.2		_	4.2		V
input voitage					2.0		_	0.5	_	0.5	V
	Low level	VIL	_		4.5	_	_	1.35	_	1.35	
					6.0	_	_	1.8	_	1.8	
	High level V		V _{IN} = V _{IH}	I _{OH} = -20 μA	2.0	1.9	2.0	_	1.9	_	V
		Vон			4.5	4.4	4.5	_	4.4	_	
					6.0	5.9	6.0	_	5.9	_	
				I _{OH} = -6 mA	4.5	4.18	4.31	_	4.13	_	
Output				$I_{OH} = -7.8 \text{ mA}$	6.0	5.68	5.80	_	5.63	_	
voltage	Low level V _O	V _{OL}	V _{OL} V _{IN} = V _{IH} or V _{IL}	Ι _{ΟL} = 20 μΑ	2.0	_	0	0.1	_	0.1	
					4.5	_	0	0.1	_	0.1	
					6.0	_	0	0.1	_	0.1	
				I _{OL} = 6 mA	4.5	_	0.17	0.26	_	0.33	
				I _{OL} = 7.8 mA	6.0	_	0.18	0.26	_	0.33	
3-state output off-state current		l _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		6.0	_	_	±0.5	_	±5.0	μА
Input leakage current I_{IN} $V_{IN} = V_{CC}$ or GND		r GND	6.0	_	_	±0.1	_	±1.0	μΑ		
Quiescent supply current I_{CC} $V_{IN} = V_{CC}$ or GND		r GND	6.0			2.0	_	20.0	μА		

3 2009-09-30

AC Electrical Characteristics (input $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = -40 to 85°C		Unit
	,		C_{L}	V _{CC} (V)	Min	Тур.	Max	Min	Max	
	t _{TLH}	_	50	2.0	_	20	60	_	75	ns
Output transition time				4.5	_	6	12	_	15	
	-1112			6.0		5	10	_	13	
			50	2.0		30	90	_	115	
				4.5		11	18	_	23	
Propagation delay time	t _{pLH}			6.0		10	15	_	20	ns
Tropagation delay time	t _{pHL}	_		2.0		42	130	_	165	113
			150	4.5		14	26	_	33	
				6.0		12	22	_	28	
	^t pZL ^t pZH	$R_L = 1 \text{ k}\Omega$	50	2.0		30	90	_	115	- ns
				4.5		11	18	_	23	
Output enable time				6.0		10	15	_	20	
Output chable time			150	2.0		42	130	_	165	
				4.5		14	26	_	33	
				6.0		12	22	_	28	
Output disable time			50	2.0	_	24	100	_	125	ns
	t _{pLZ} t _{pHZ}	$R_L = 1 \text{ k}\Omega$		4.5	_	12	20	_	25	
	φηΖ			6.0	_	10	17	_	21	
Input capacitance	C _{IN}	_	_	_	_	5	10	_	10	pF
Output capacitance	C _{OUT}	_		_		10	_	_	_	pF
Power dissipation capacitance	C _{PD}	(Note)	_	_	_	32	_	_	_	pF

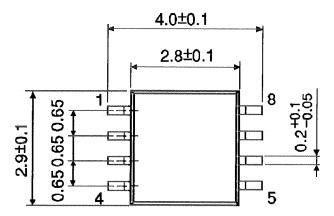
Note: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load.

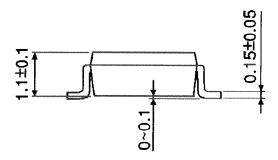
Average operating current can be obtained by the equation:

 $I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per gate)}$

Package Dimensions

SSOP8-P-0.65 Unit: mm





5

Weight: 0.02 g (typ.)

2009-09-30

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