National Semiconductor

March 1993

54ACQ/74ACQ573 • 54ACTQ/74ACTQ573 Quiet Series Octal Latch with TRI-STATE® Outputs

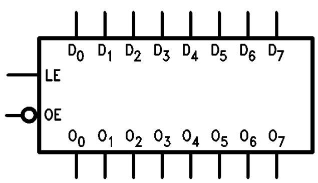
General Description

The ’ACQ/’ACTQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs. The ’ACQ/’ACTQ573 is functionally identical to the ’ACQ/’ACTQ373 but with inputs and outputs on opposite sides of the package. The ’ACQ/’ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard ’ACT573
- 4 kV minimum ESD immunity
- Standard Military Drawing (SMD)
  — ’ACTQ573: 5962-8766402

Logic Symbols



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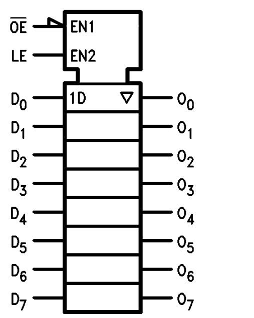
IEEE/IEC



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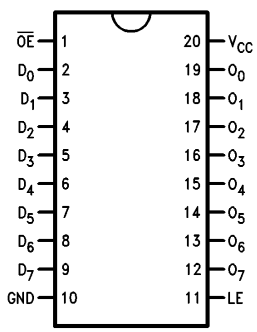
Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

Connection Diagrams

Pin Assignment for DIP, Flatpak, QSOP and SOIC



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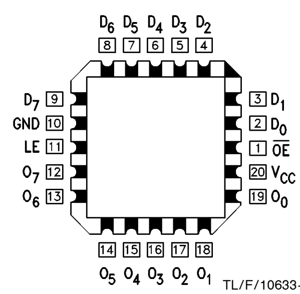
Pin Assignment for LCC



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RRD-B30M75/Printed in U. S. A.

54ACQ/74ACQ573 • 54ACTQ/74ACTQ573 Quiet Series Octal Latch with TRI-STATE Outputs

Functional Description

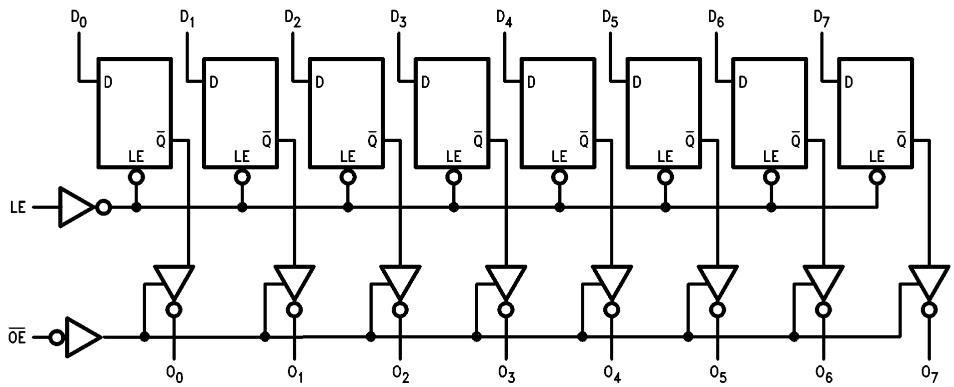
The 'ACQ/'ACTQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
DC Latchup Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACQ	2.0V to 6.0V
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACQ/ACTQ	−40°C to +85°C
54ACQ/ACTQ	−55°C to +125°C
Minimum Input Edge Rate ΔV/Δt 'ACQ Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.0V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40°C to +125°C.

DC Characteristics for 'ACQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACQ T_A = +25°C Typ	74ACQ T_A = +25°C Guaranteed Limits	54ACQ T_A = −55°C to +125°C Guaranteed Limits	74ACQ T_A = −40°C to +85°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = −50 μA
		3.0 4.5 5.5		2.56 3.86 4.86	2.4 3.7 4.7	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} −12 mA I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5		0.36 0.36 0.36	0.50 0.50 0.50	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACQ $T_A = +25°C$ Typ	74ACQ $T_A = +25°C$ Guaranteed Limits	54ACQ $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACQ $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND (Note 1)
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65\ V_{Max}$
I_{OHD}		5.5			−50	−75	mA	$V_{OHD} = 3.85\ V_{Min}$
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
I_{OZ}	Maximum TRI-STATE Leakage Curent	5.5		±0.25	±5.0	±2.5	μA	$V_I(OE) = V_{IL}, V_{IH}$ $V_I = V_{CC}$, GND $V_O = V_{CC}$, GND
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 2-12, 13* (Note 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 2-12, 13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	3.1	3.5			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.9	1.5			V	(Notes 2, 4)

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.
I_{CC} for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n − 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$ Typ	74ACTQ $T_A = +25°C$ Guaranteed Limits	54ACTQ $T_A = -55°C$ to $+125°C$ Guaranteed Limits	74ACTQ $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50\ \mu A$
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	$I_{OUT} = 50\ \mu A$
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74ACTQ $T_A = +25°C$		54ACTQ $T_A = -55°C$ to $+125°C$	74ACTQ $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5		±0.25	±5.0	±2.5	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V$ Max
I_{OHD}		5.5			−50	−75	mA	$V_{OHD} = 3.85V$ Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND (Note 1)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.1	1.5			V	*Figures 2-12*, *13* (Notes 2, 3)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−0.6	−1.2			V	*Figures 2-12*, *13* (Notes 2, 3)
V_{IHD}	Minimum High Level Dynamic Input Voltage	5.0	1.9	2.2			V	(Notes 2, 4)
V_{ILD}	Maximum Low Level Dynamic Input Voltage	5.0	1.2	0.8			V	(Notes 2, 4)

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Plastic DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n − 1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$ $C_L = 50$ pF			54ACQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0	2.5 1.5	8.5 5.5	10.5 7.0	1.5 1.5	16.0 11.0	2.5 1.5	11.0 7.5	ns
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	3.3 5.0	2.5 2.0	8.5 6.0	12.0 8.0	1.5 1.5	15.0 11.0	2.5 2.0	12.5 8.5	ns
t_{PZL}, t_{PZH}	Output Enable Time	3.3 5.0	2.5 1.5	8.5 6.0	13.0 8.5	1.5 1.5	13.5 10.0	2.5 1.5	13.5 9.0	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	9.0 6.0	14.5 9.5	1.5 1.0	13.0 10.5	1.0 1.0	15.0 10.0	ns
t_{OSHL}, t_{OSLH}	Output to Output Skew** D_n to O_n	3.3 5.0		1.0 0.5	1.5 1.0				1.5 1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACQ $T_A = +25°C$ $C_L = 50$ pF		54ACQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	3.0 3.0	4.0 4.0	3.0 3.0	ns
t_H	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0	1.5 1.5	2.0 2.0	1.5 1.5	ns
t_W	LE Pulse Width, HIGH	3.3 5.0	2.0 2.0	4.0 4.0	5.0 5.0	4.0 4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V
Voltage Range 3.3 is 3.3V ±0.3V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF			54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Propagation Delay D_n to O_n	5.0	2.0	6.5	7.5	1.5	10.0	2.0	8.0	ns
t_{PLH}, t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	7.0	8.5	1.5	11.0	2.5	9.0	ns
t_{PZL}, t_{PZH}	Output Enable Time	5.0	2.0	7.0	9.0	1.5	11.0	2.0	9.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	5.0	1.0	8.0	10.0	1.5	11.0	1.0	10.5	ns
t_{OSHL} t_{OSLH}	Output to Output Skew** D_n to O_n	5.0		0.5	1.0				1.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

**Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL} or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACTQ $T_A = +25°C$ $C_L = 50$ pF		54ACTQ $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACTQ $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_S	Setup Time, HIGH or LOW D_n to LE	5.0	0	3.0	3.5	3.0	ns
t_H	Hold Time, HIGH or LOW D_n to LE	5.0	0	1.5	1.5	1.5	ns
t_W	LE Pulse Width, HIGH	5.0	2.0	4.0	5.0	4.0	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	42.0	pF	V_{CC} = 5.0V

FACT Noise Characteristics

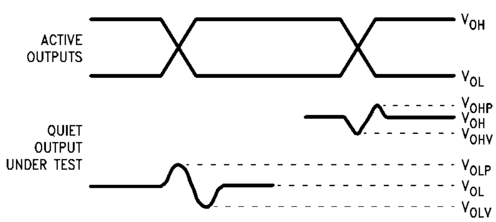
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are the correct voltage.
4. Set V_{CC} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.



TL/F/10633–6

FIGURE 1. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

6. Set the word generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output durnig the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next increase the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

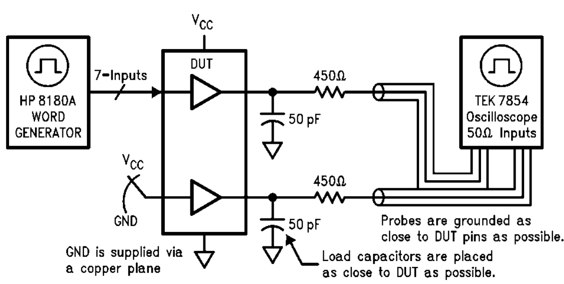


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FIGURE 2. Simultaneous Switching Test Circuit

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74ACTQ 573 P C QR

Temperature Range Family
- 74ACQ = Commercial
- 54ACQ = Military
- 74ACTQ = Commercial TTL-Compatible
- 54ACTQ = Military TTL-Compatible

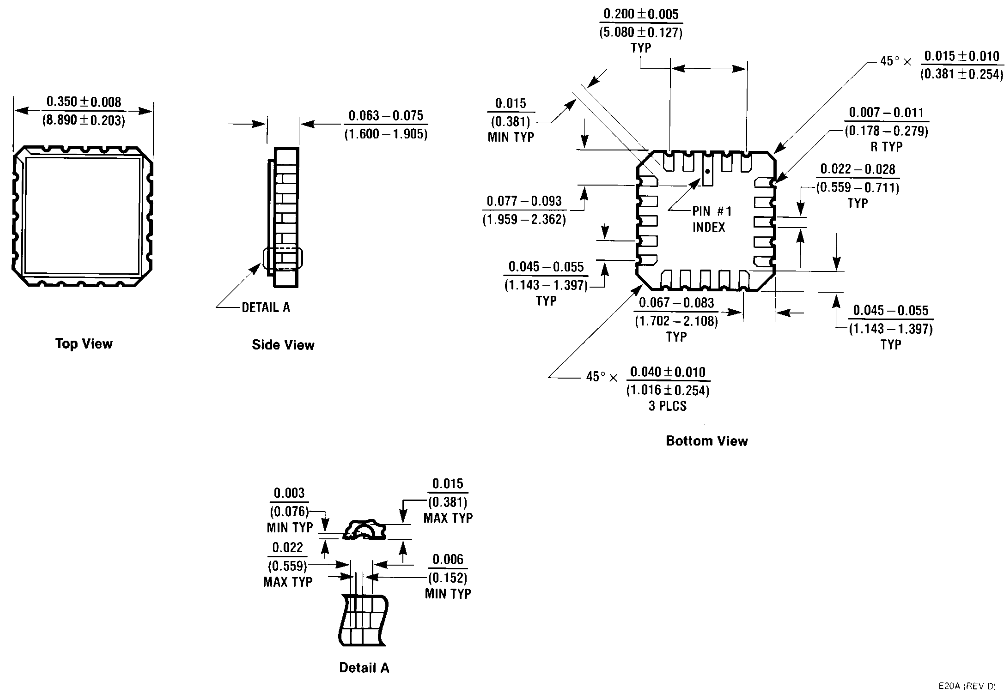
Device Type

Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Ceramic Chip Carrier (LCC)
- S = Small Outline Package (SOIC)
- QS = Quarter Size Outline Package (QSOP)

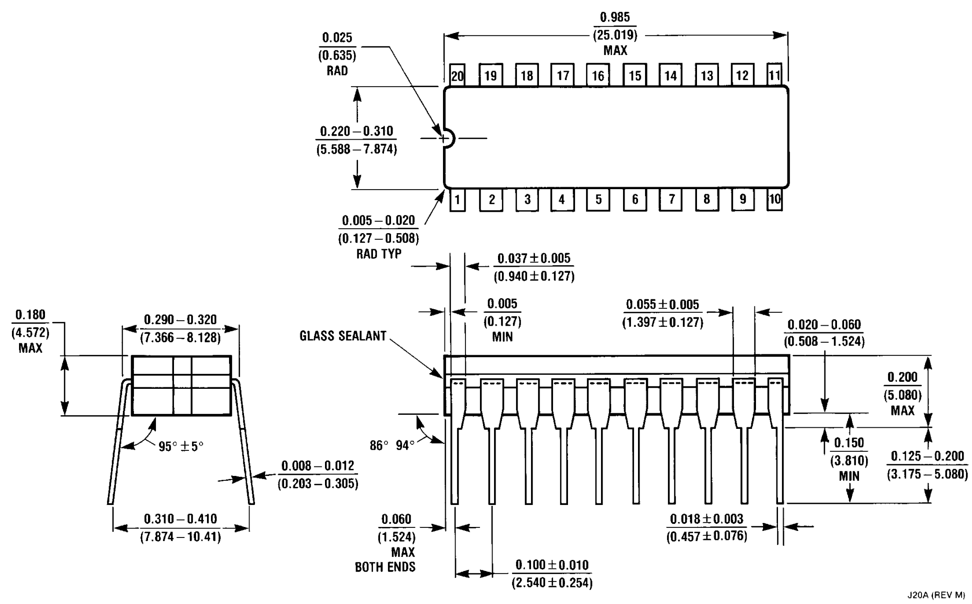
Special Variations
- X = Device shipped in 13″ reels
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes

Temperature Range
- C = Commercial (−40°C to +85°C)
- M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)

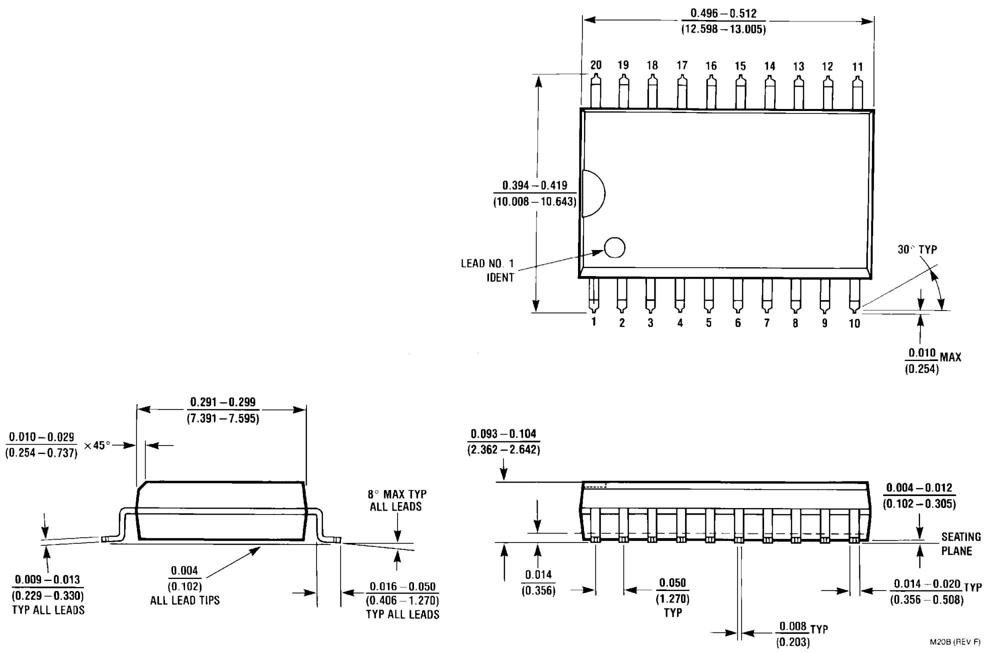


20-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

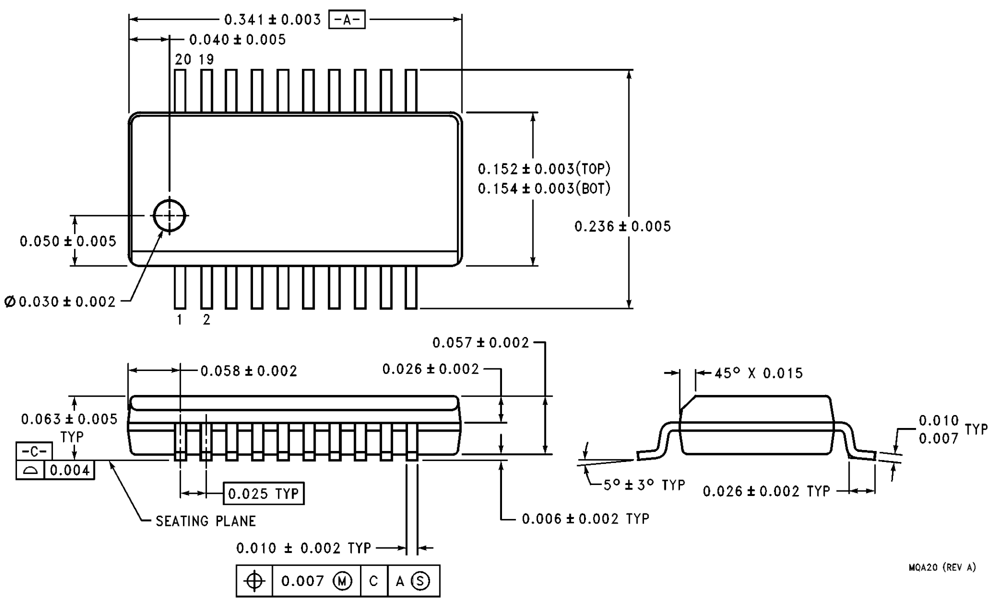


20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) (Continued)

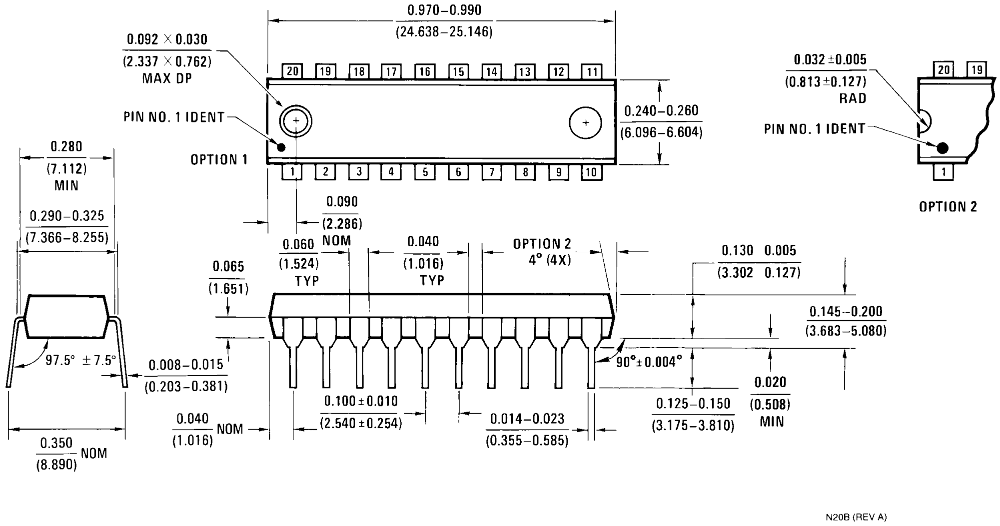


20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B



20-Lead Quarter Size Outline Package (QS)
NS Package Number MQA20

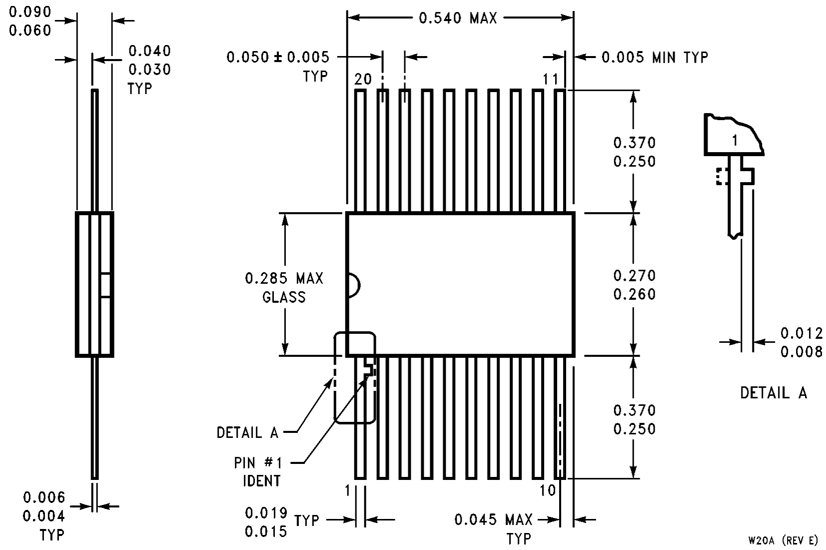
Physical Dimensions inches (millimeters) (Continued)



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114669



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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