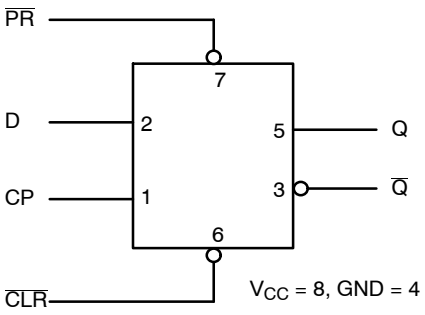
Single D Flip Flop

NL17SZ74

The NL17SZ74 is a high performance, full function Edge triggered D Flip Flop, with all the features of a standard logic device such as the 74LCX74.

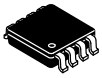
Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.6 ns t_{PD} at V_{CC} = 5 V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in US8 and UQFN8 Packages
- Chip Complexity < 100 FETs
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



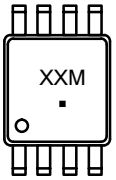
Pin numbers indicated are for US8 and UDFN8 packages.

Figure 1. Logic Symbol



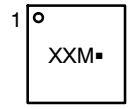
US8
US SUFFIX
CASE 493

Commercial



Automotive

UQFN8, 1.6x1.6
MQ1 SUFFIX
CASE 523AN



XX, XXXX	= Specific Device Code
A	= Assembly Location
L	= Lot Code
Y	= Year Code
W	= Week Code
M	= Date Code
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 8 of this data sheet.

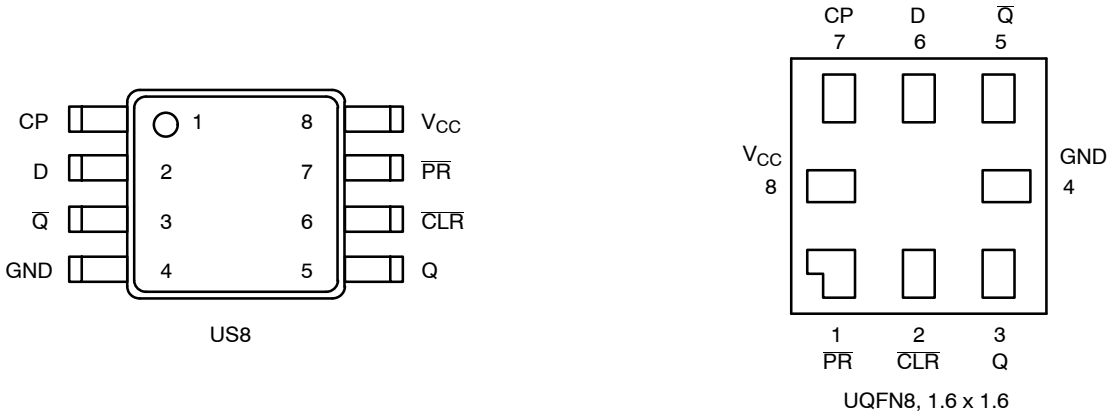


Figure 2. Pinout (Top View)

PIN ASSIGNMENT

Pin	US8	UQFN8, 1.6x1.6
1	CP	$\overline{PR}$
2	D	$\overline{CLR}$
3	$\overline{Q}$	Q
4	GND	GND
5	Q	$\overline{Q}$
6	$\overline{CLR}$	D
7	$\overline{PR}$	CP
8	V_{CC}	V_{CC}

FUNCTION TABLE

Inputs				Outputs		
$\overline{PR}$	$\overline{CLR}$	CP	D	Q	$\overline{Q}$	Operating Mode
L H L	H L L	X X X	X X X	H L H	L H H	Asynchronous Set Asynchronous Clear Undertermined
H H	H H	↑ ↑	h l	H L	L H	Load and Read Register
H	H	↥	X	NC	NC	Hold

H = High Voltage Level
h = High Voltage Level One Setup Time Prior to Low−to−High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to Low−to−High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
↑ = Low−to−High Transition
↥ = Not a Low−to−High Transition
For I_{CC} reasons, DO NOT FLOAT Inputs

MAXIMUM RATINGS

Symbol	Characteristics		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_{OUT}	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	US8 UQFN8	250 210	°C/W
P_D	Power Dissipation in Still Air	US8 UQFN8	500 595	mW
MSL	Moisture Sensitivity		Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 1000	V
$I_{Latchup}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm−by−1inch, 2 ounce copper trace no air flow per JESD51−7.
3. HBM tested to ANSI/ESDA/JEDEC JS−001−2017. CDM tested to EIA/JESD22−C101−F. JEDEC recommends that ESD qualification to EIA/JESD22−A115−A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	DC Input Voltage		0	5.5	V
V_{OUT}	DC Output Voltage	Active−Mode (High or Low State) Tri−State Mode (Note 1) Power−Down Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 5.5	
T_A	Operating Temperature Range		−55	+125	°C
t_R, t_F	Input Rise and Fall Rate	V_{CC} = 1.65 V to 1.95 V V_{CC} = 2.3 V to 2.7 V V_{CC} = 3.0 V to 3.6 V V_{CC} = 4.5 V to 5.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = 25 °C			−55 °C ≤ T_A ≤ 125 °C		Units
				Min	Typ	Max	Min	Max	
V_{IH}	High−Level Input Voltage		1.65 to 1.95	0.65 x V_{CC}			0.65 x V_{CC}		V
			2.3 to 5.5	0.70 x V_{CC}			0.70 x V_{CC}		
V_{IL}	Low−Level Input Voltage		1.65 to 1.95			0.35 x V_{CC}		0.35 x V_{CC}	V
			2.3 to 5.5			0.30 x V_{CC}		0.30 x V_{CC}	
V_{OH}	High−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OH} = −100 μA I_{OH} = −4 mA I_{OH} = −8 mA I_{OH} = −12 mA I_{OH} = −16 mA I_{OH} = −24 mA I_{OH} = −32 mA	 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	 V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	 V_{CC} 1.4 2.1 2.4 2.7 2.5 4.0	 − − − − − − −	 V_{CC} − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	 − − − − − − −	V
V_{OL}	Low−Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_{OL} = 100 μA I_{OL} = 4 mA I_{OL} = 8 mA I_{OL} = 12 mA I_{OL} = 16 mA I_{OL} = 24 mA I_{OL} = 32 mA	 1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	 − − − − − − −	 − 0.08 0.2 0.22 0.28 0.38 0.42	 0.1 0.24 0.3 0.4 0.4 0.55 0.55	 − − − − − − −	 0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	1.65 to 5.5	−	−	±0.1	−	±1.0	μA
I_{OFF}	Power Off Leakage Current	V_{IN} = 5.5 V or V_{OUT} = 5.5 V	0	−	−	1.0	−	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5	−	−	1.0	−	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

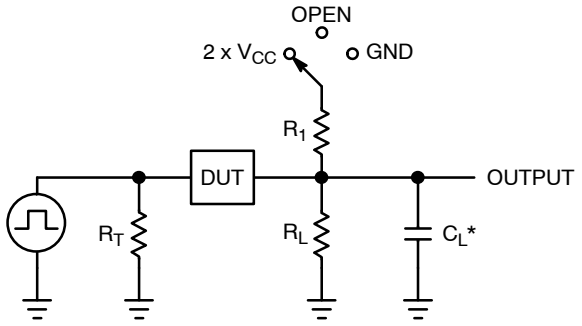
Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = 25 °C			T_A = −55 to 125 °C		Units
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Figures 3 and 5)	1.65 to 1.95	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	75	–	–	75	–	MHz
		2.3 to 2.7		150	–	–	150	–	
		3.0 to 3.6		200	–	–	200	–	
		4.5 to 5.5		250	–	–	250	–	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω, S_1 = Open	175	–	–	175	–	
		4.5 to 5.5		200	–	–	200	–	
t_{PLH}, t_{PHL}	Propagation Delay, CP to Q or $\overline{Q}$ (Figures 3 and 4)	1.65 to 1.95	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	–	6.5	12.5	–	13	ns
		2.3 to 2.7		–	3.8	7.5	–	8.0	
		3.0 to 3.6		–	2.8	6.5	–	7.0	
		4.5 to 5.5		–	2.2	4.5	–	5.0	
		3.0 to 3.6	C_L = 50 pF, R_D = 500 Ω, S_1 = Open	–	3.4	7.0	–	7.5	
		4.5 to 5.5		–	2.6	5.0	–	5.5	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$ (Figures 3 and 4)	1.65 to 1.95	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	–	6.5	14	–	14.5	ns
		2.3 to 2.7		–	3.8	9.0	–	9.5	
		3.0 to 3.6		–	2.8	6.5	–	7.0	
		4.5 to 5.5		–	2.2	5.0	–	5.5	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω, S_1 = Open	–	3.4	7.0	–	7.5	
		4.5 to 5.5		–	2.6	5.0	–	5.5	
t_S	Setup Time, D to CP (Figures 3 and 5)	1.65 to 1.95	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	6.5	–	–	6.5	–	ns
		2.3 to 2.7		3.5	–	–	3.5	–	
		3.0 to 3.6		2.0	–	–	2.0	–	
		4.5 to 5.5		1.5	–	–	1.5	–	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω, S_1 = Open	2.0	–	–	2.0	–	
		4.5 to 5.5		1.5	–	–	1.5	–	
t_H	Hold Time, D to CP (Figures 3 and 5)	1.65 to 1.95	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	0.5	–	–	0.5	–	ns
		2.3 to 2.7		0.5	–	–	0.5	–	
		3.0 to 3.6		0.5	–	–	0.5	–	
		4.5 to 5.5		0.5	–	–	0.5	–	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω, S_1 = Open	0.5	–	–	0.5	–	
		4.5 to 5.5		0.5	–	–	0.5	–	
t_W	Pulse Width, CP, $\overline{CLR}$, $\overline{PR}$ (Figures 3 and 5)	1.65 to 1.95	C_L = 15 pF, R_L = 1 MΩ, S_1 = Open	6.0	–	–	6.0	–	ns
		2.3 to 2.7		4.0	–	–	4.0	–	
		3.0 to 3.6		3.0	–	–	3.0	–	
		4.5 to 5.5		2.0	–	–	2.0	–	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω, S_1 = Open	3.0	–	–	3.0	–	
		4.5 to 5.5		2.0	–	–	2.0	–	
t_{REC}	Recover Time $\overline{PR}$; $\overline{CLR}$ to CP (Figures 3 and 5)	1.65 to 1.95	C_L = 15 pF, R_D = 1 MΩ, S_1 = Open	8.0	–	–	8.0	–	ns
		2.3 to 2.7		4.5	–	–	4.5	–	
		3.0 to 3.6		3.0	–	–	3.0	–	
		4.5 to 5.5		3.0	–	–	3.0	–	
		3.0 to 3.6	C_L = 50 pF, R_L = 500 Ω, S_1 = Open	3.0	–	–	3.0	–	
		4.5 to 5.5		3.0	–	–	3.0	–	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/2$ (per flip−flop). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, V_{CC} = 3.3 V, V_{IN} = 0 V or V_{CC} 10 MHz, V_{CC} = 5.5 V, V_{IN} = 0 V or V_{CC}	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

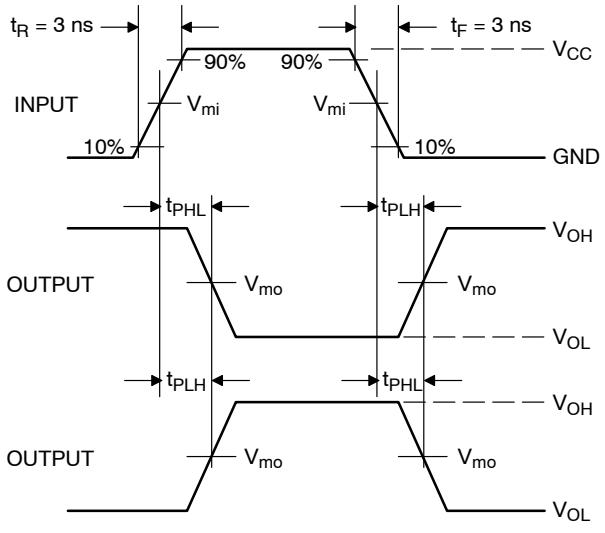


C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz

Figure 3. Test Circuit

Test	Switch Position	C_L, pF	R_L, Ω	R_1, Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	2 x V_{CC}	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care



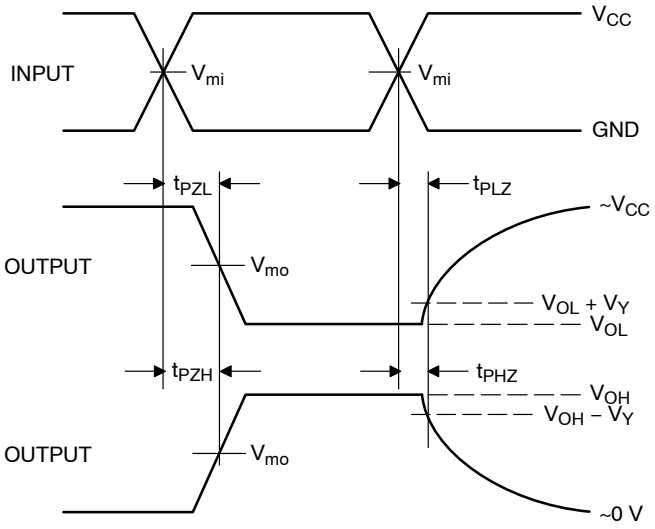


Figure 4. Switching Waveforms

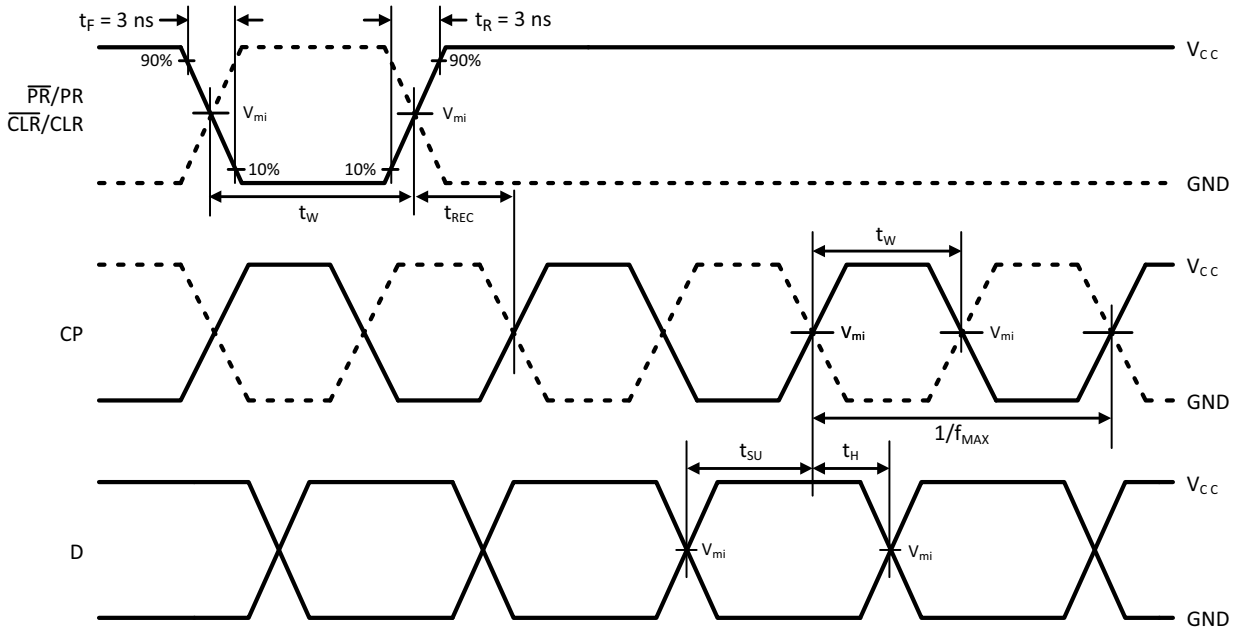


Figure 5. Setup, Hold and Recovery Time Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}	
1.65 to 1.95	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	0.3

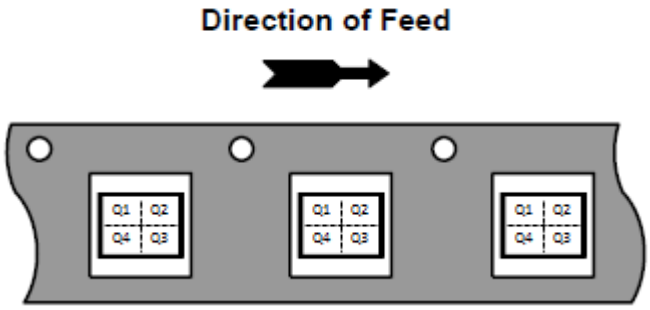
DEVICE ORDERING INFORMATION

Device	Packages	Marking	Pin 1 Orientation (See below)	Shipping†
NL17SZ74USG	US8	MH	Q4	3000 / Tape & Reel
NL17SZ74USG−Q*	US8	MH	Q4	3000 / Tape & Reel
NL17SZ74MQ1TCG	UQFN8, 1.6 x 1.6, 0.5P	AA	Q4	3000 / Tape & Reel
NL17SZ74MQ1TCG−Q*	UQFN8, 1.6 x 1.6, 0.5P	AA	Q4	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

* −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

Pin 1 Orientation in Tape and Reel



REVISION HISTORY

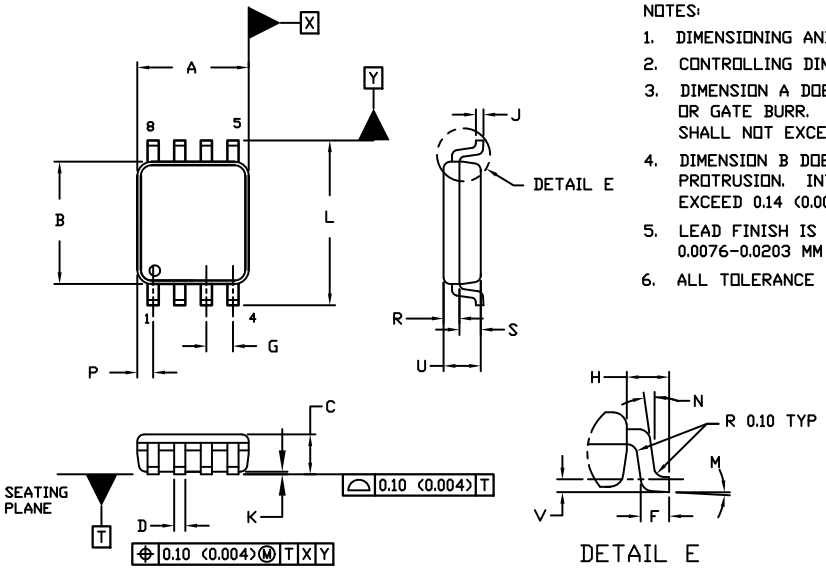
Revision	Description of Changes	Date
19	Removed three package ordering options and OPNs	2/3/2026

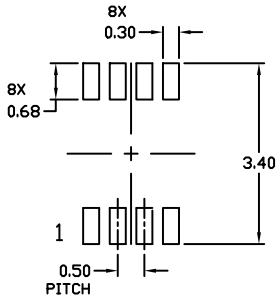
* Please note that this document has been previously updated prior to the inclusion of this revision history table and that the changes tracked only reflect what has occurred on the noted approval dates.

SCALE 4 :1

US8
CASE 493
ISSUE F

DATE 01 SEP 2021





RECOMMENDED *
MOUNTING FOOTPRINT

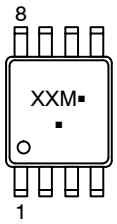
* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR. MOLD FLASH, PROTRUSION, OR GATE BURR SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076–0.0203 MM (0.003–0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 MM (0.002").

	MILLIMETERS		INCHES	
DIM	MIN.	MAX.	MIN.	MAX.
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.25	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

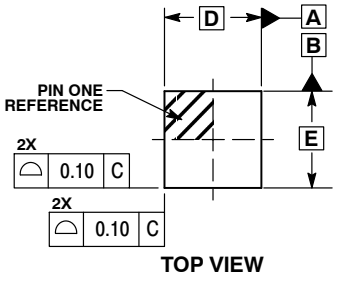
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON04475D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**US8**		**PAGE 1 OF 1**

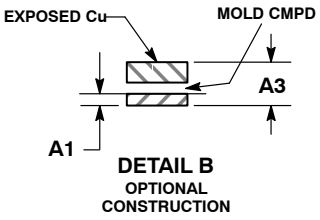
SCALE 4:1

UQFN8, 1.60x1.60, 0.50P
CASE 523AN
ISSUE O

DATE 26 NOV 2008



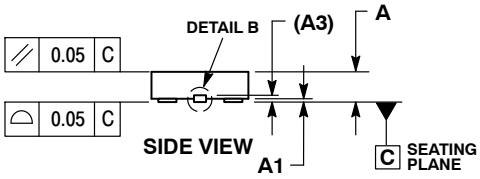
TOP VIEW

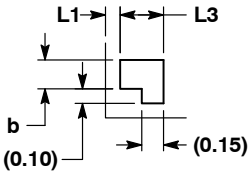


DETAIL B
OPTIONAL CONSTRUCTION

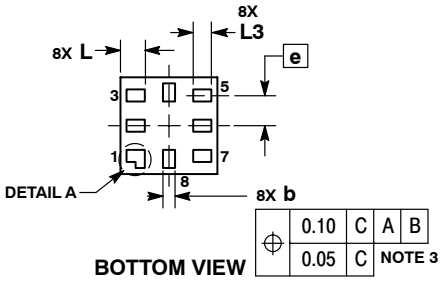
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.60 BSC	
E	1.60 BSC	
e	0.50 BSC	
L	0.35	0.45
L1	---	0.15
L3	0.25	0.35



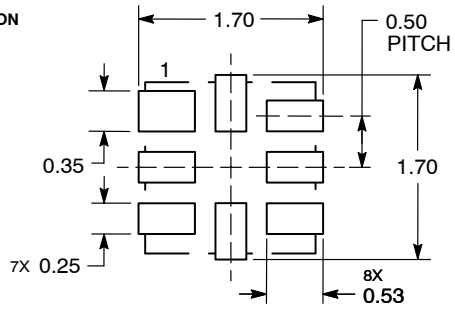


DETAIL A
OPTIONAL CONSTRUCTION



BOTTOM VIEW

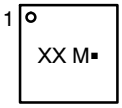
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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