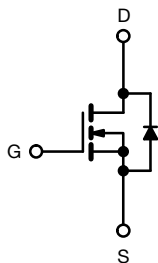
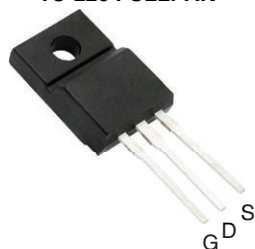


SF Series Power MOSFET With Fast Body Diode

TO-220 FULLPAK


N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	700	
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V	0.100
Q_g max. (nC)	125	
Q_{gs} (nC)	22	
Q_{gd} (nC)	45	
Configuration	Single	

FEATURES

- Latest generation SF series technology
- Low figure of merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free and halogen-free	SiHF110N65SF-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-source voltage			V_{DS}	650	V
Gate-source voltage			V_{GS}	± 20	
Continuous drain current ($T_J = 150\text{ }^{\circ}\text{C}$) ^e	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	I_D	12	A
		$T_C = 100\text{ }^{\circ}\text{C}$		7	
Pulsed drain current ^a			I_{DM}	88	
Linear derating factor				2.5	W/ $^{\circ}\text{C}$
Single pulse avalanche energy ^b			E_{AS}	411	mJ
Maximum power dissipation			P_D	39	W
Operating junction and storage temperature range			T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$
Drain-source voltage slope		$T_J = 125\text{ }^{\circ}\text{C}$	dv/dt	100	V/ns
Reverse diode dv/dt ^d				100	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 120$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 5.4$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, di/dt = 850 A/ μ s, starting $T_J = 25$ °C
- Limited by maximum junction temperature

**THERMAL RESISTANCE RATINGS**

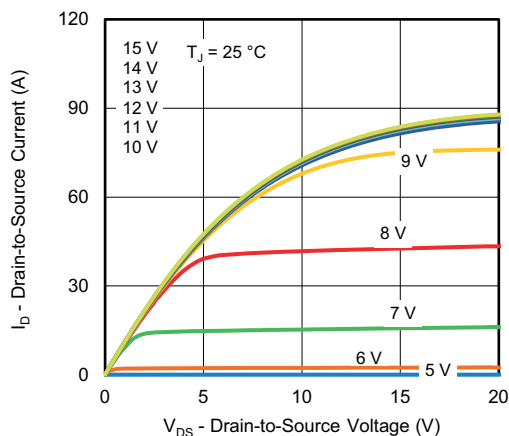
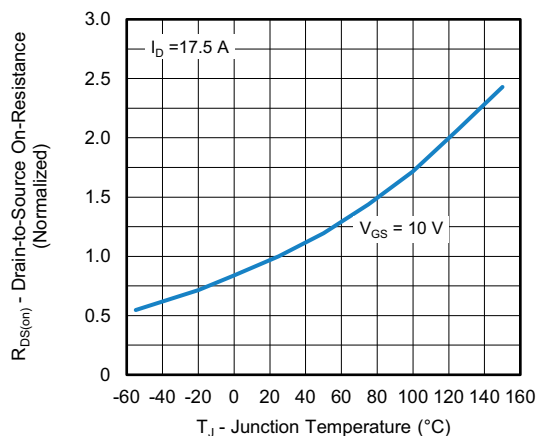
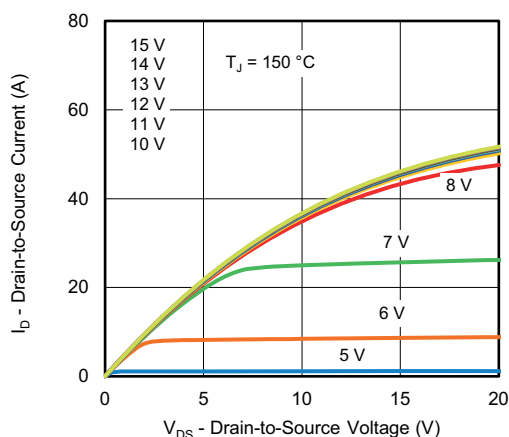
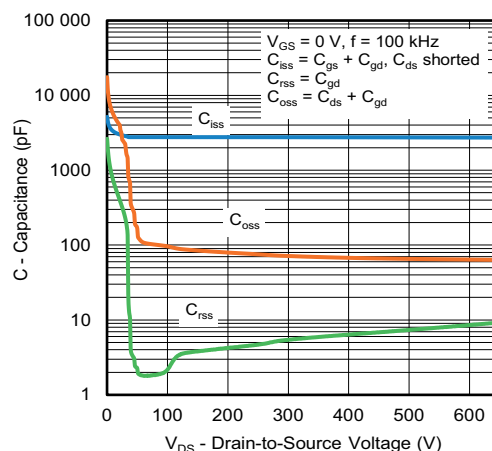
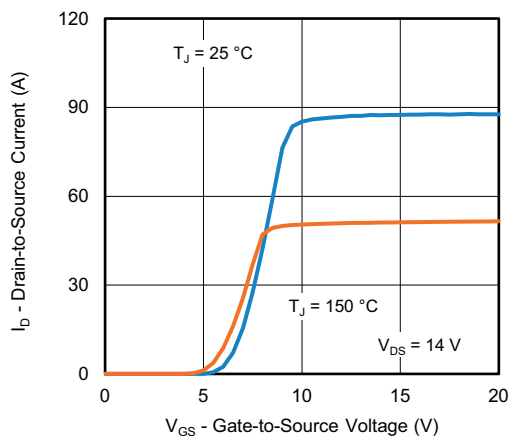
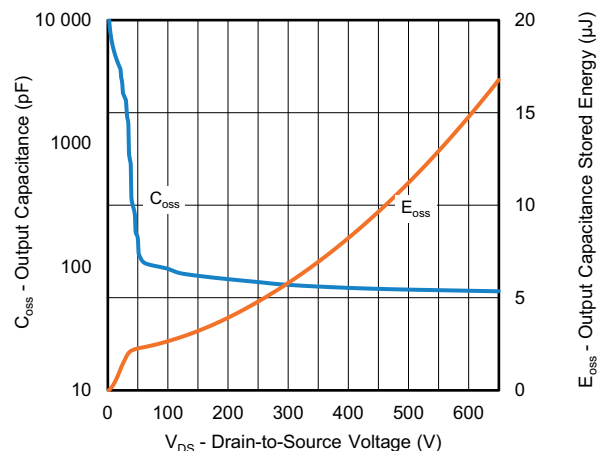
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	65	°C/W
Maximum junction-to-case (drain)	R_{thJC}	-	3.2	

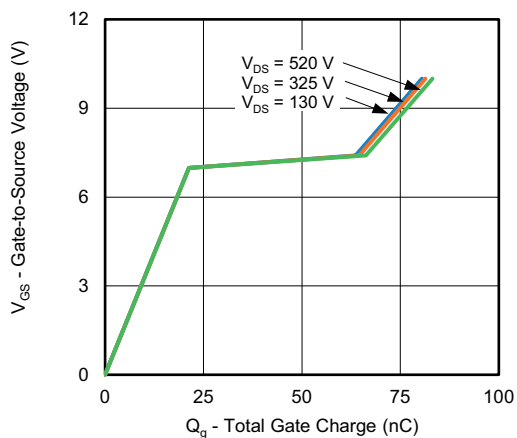
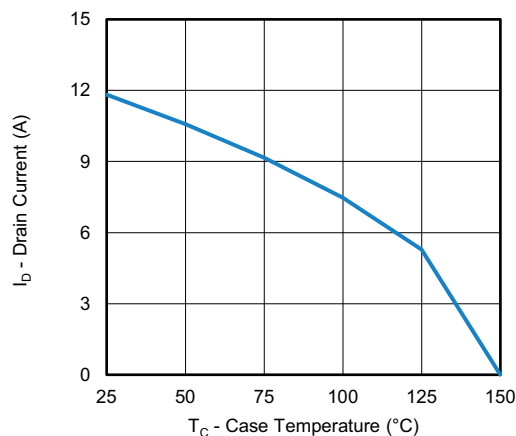
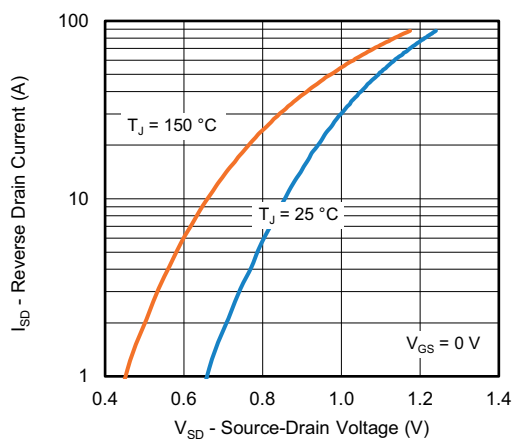
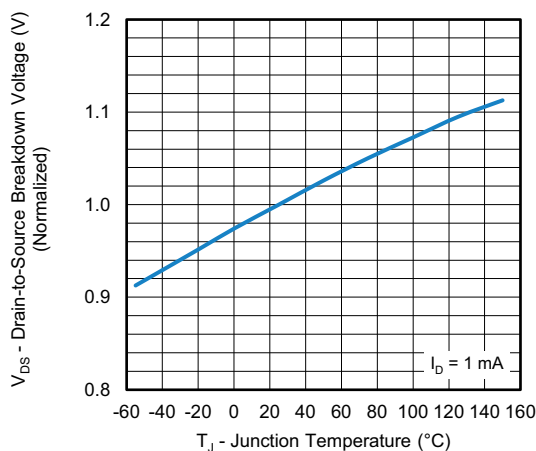
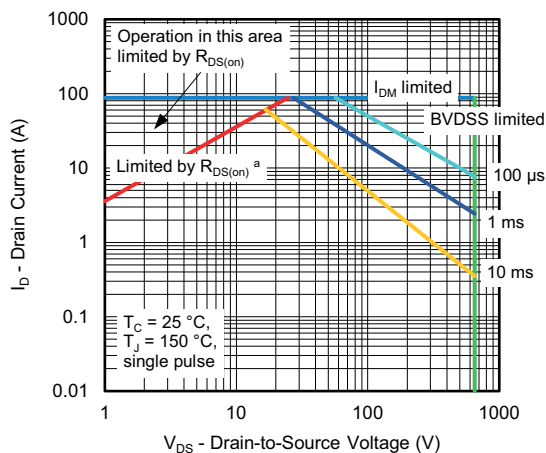
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		650	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$		-	0.62	-	V/ $^{\circ}\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 650\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	1	μA
		$V_{DS} = 520\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		-	-	2	mA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 17.5\text{ A}$	-	0.100	0.115	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 20\text{ V}$, $I_D = 17.5\text{ A}$		-	26	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 100\text{ KHz}$		-	2772	-	pF
Output capacitance	C_{oss}			-	92	-	
Reverse transfer capacitance	C_{rss}			-	3	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 400\text{ V}$, $V_{GS} = 0\text{ V}$		-	103	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	505	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 17.5\text{ A}$, $V_{DS} = 520\text{ V}$	-	83	125	nC
Gate-source charge	Q_{gs}			-	22	-	
Gate-drain charge	Q_{gd}			-	45	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 520\text{ V}$, $I_D = 17.5\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 10.1\text{ }\Omega$		-	30	60	ns
Rise time	t_r			-	50	100	
Turn-off delay time	$t_{d(off)}$			-	100	150	
Fall time	t_f			-	21	42	
Gate input resistance	R_g	$f = 1\text{ MHz}$, open drain		0.7	1.5	3.0	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	12	A
Pulsed diode forward current	I_{SM}			-	-	88	
Diode forward voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 17.5\text{ A}$, $V_{GS} = 0\text{ V}$		-	-	1.4	V
Reverse recovery time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 17.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 400\text{ V}$		-	151	302	ns
Reverse recovery charge	Q_{rr}			-	0.8	1.6	μC
Reverse recovery current	I_{RRM}			-	9.6	-	A

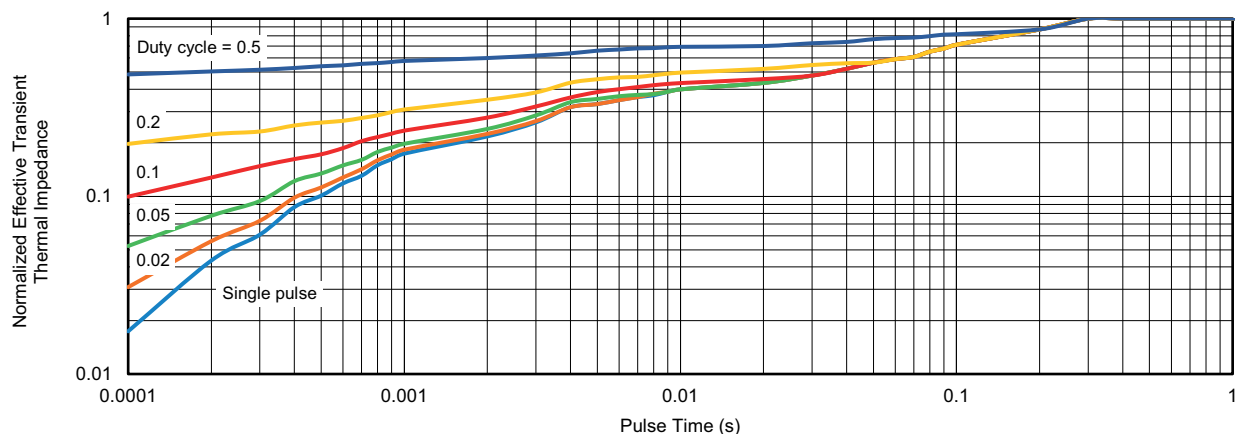
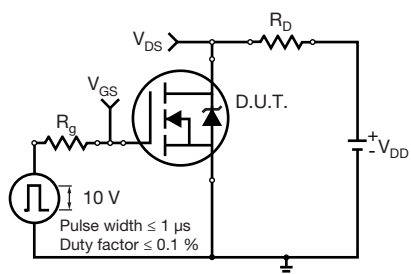
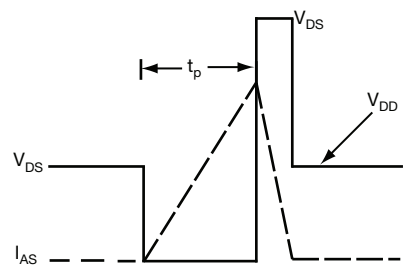
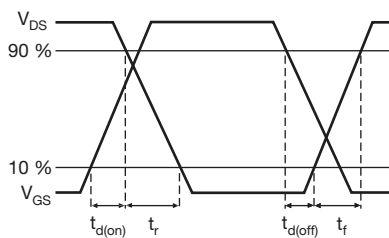
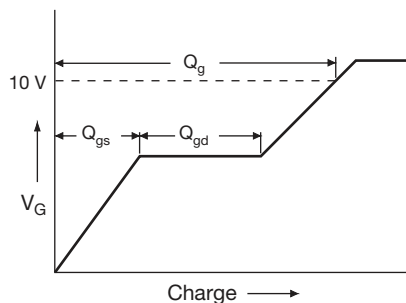
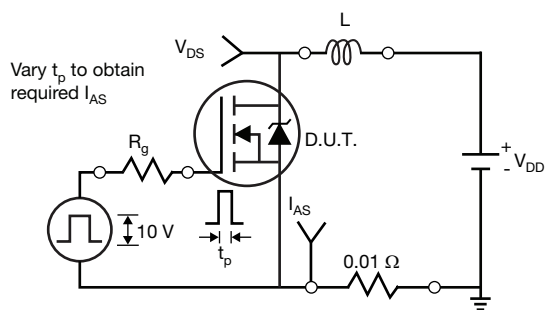
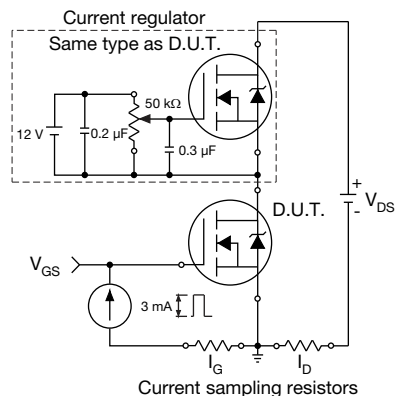
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 V to 400 V
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to 400 V

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit

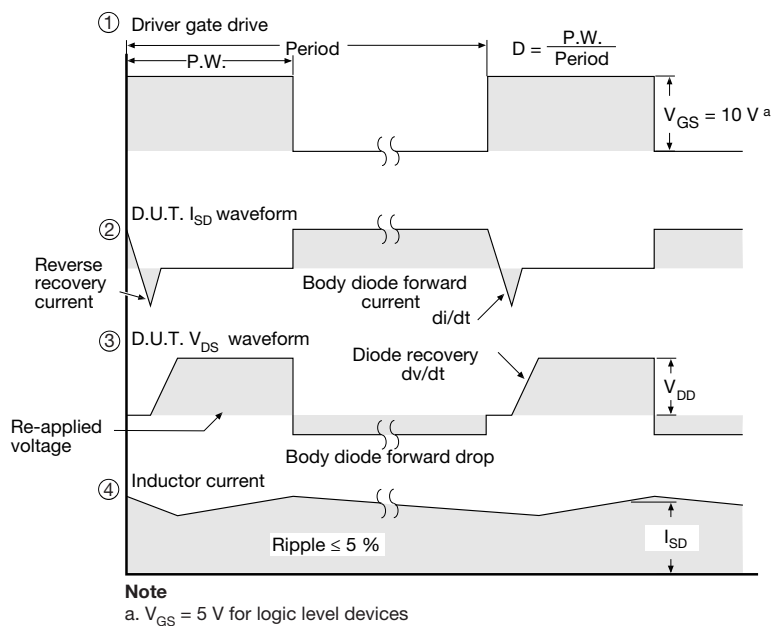
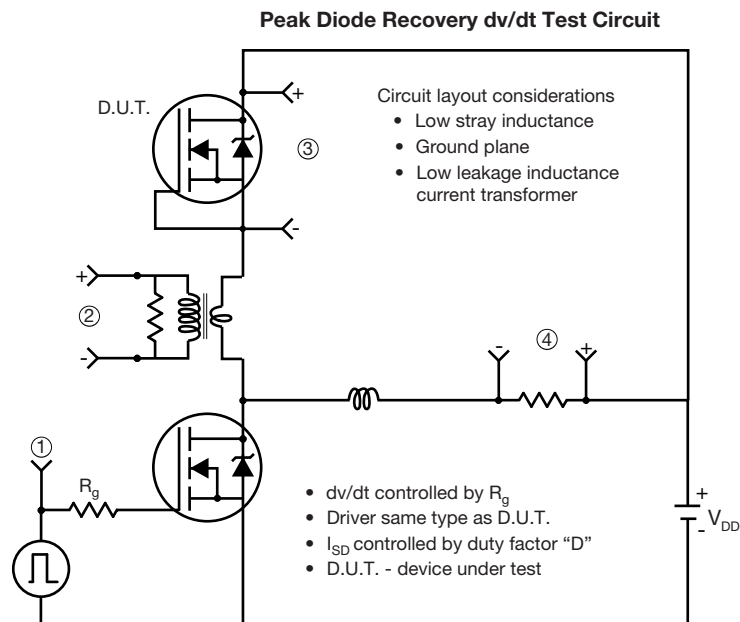


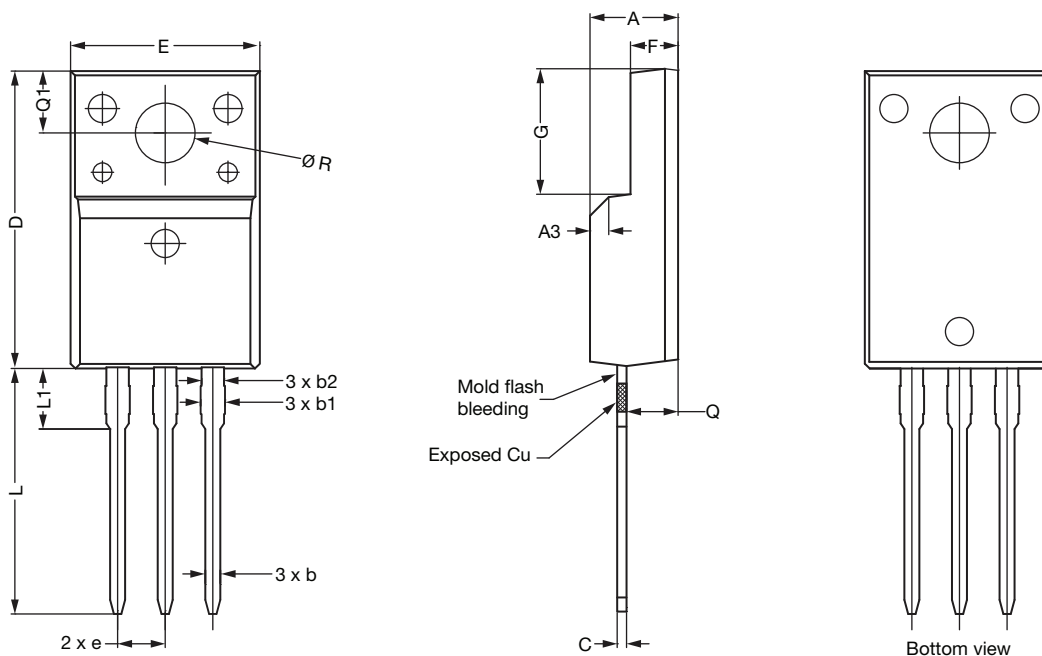
Fig. 19 - For N-Channel

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TO-220 FULLPAK (High Voltage)

OPTION 1: FACILITY CODE = 9



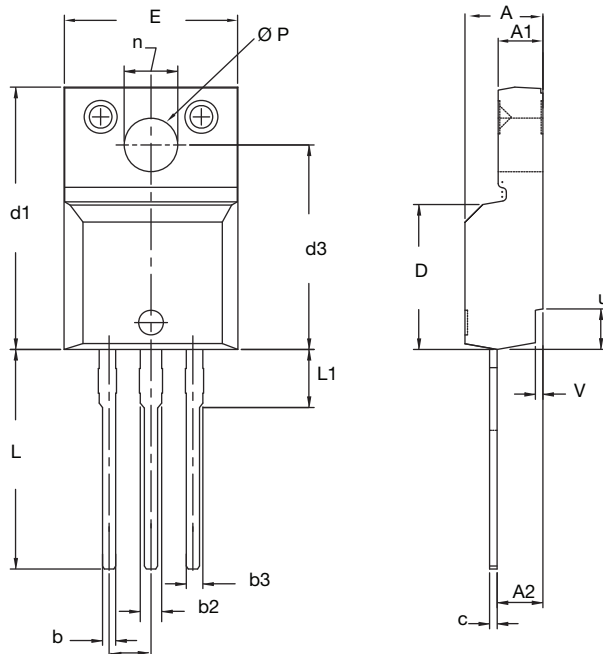
DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
Ø R	3.08	3.18	3.28

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1st character located at the 2nd row of the unit marking



OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019
DWG: 5972

Notes

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2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet $C_{pk} > 1.33$
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