High-Side and Low-Side Gate Driver

MCP14LH2106/MCP14LH21064

Description

The MCP14LH2106 and MCP14LH21064 are high-voltage, high-speed gate driver capable of driving N-channel MOSFETs and IGBTs in a high-side/low-side configuration. The high voltage process used enables the MCP14LH2106(4)'s high-side to switch to 600V in a bootstrap operation.

The MCP14LH2106(4) logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The MCP14LH2106 is available in an SOIC-8 narrow package, while the MCP14LH21064 is available in an SOIC-14 narrow package and both operate over an extended −40°C to +125°C temperature range.

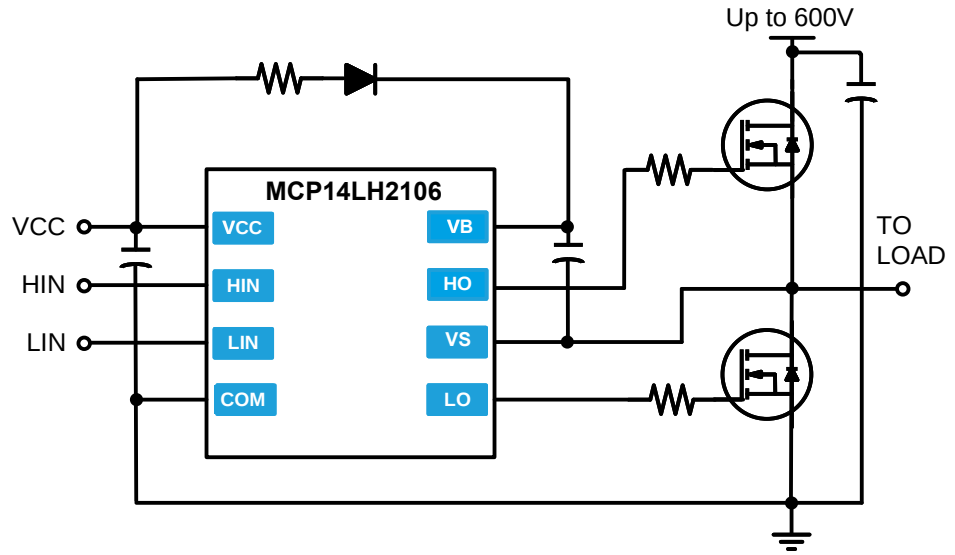
Features

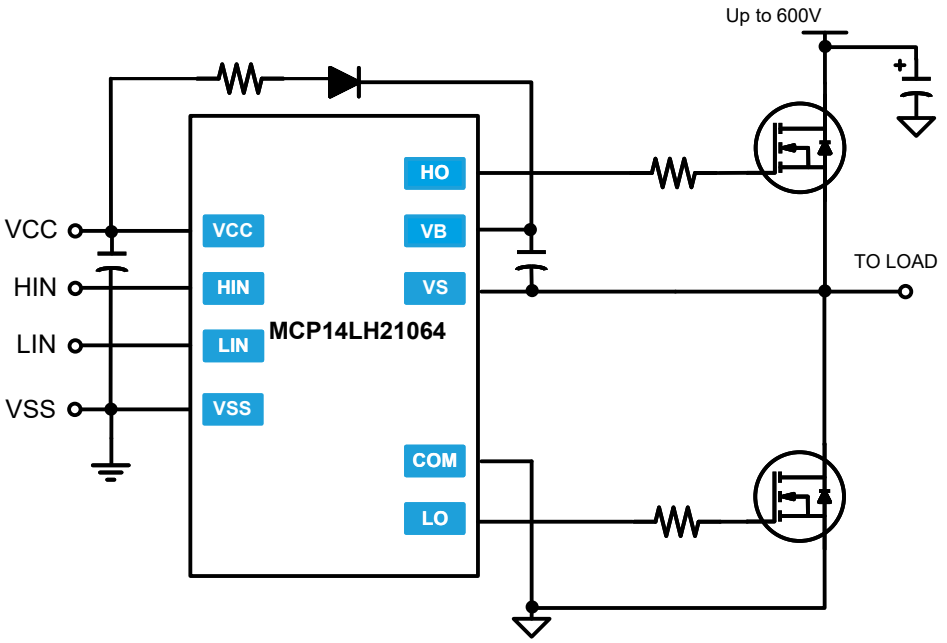
- Floating High-Side Driver in Bootstrap Operation to 600V
- Drives Two N-channel MOSFETs or IGBTs in High-Side/Low-Side Configuration
- Outputs Tolerant to Negative Transients
- Wide Low-Side Gate Driver and Logic Supply: 10V to 20V
- Wide Logic Supply Offset Voltage: −5V to 5V
- Logic Inputs (HIN and LIN) 3.3V Capability
- Schmitt Triggered Logic Inputs With Internal Pull Down
- Undervoltage Lockout for High-Side and Low-Side Drivers
- Available in Space-Saving SOIC-8 (MCP14LH2106) or SOIC-14 (MCP14LH21064) Package
- Extended Temperature Range: −40°C to +125°C

Applications

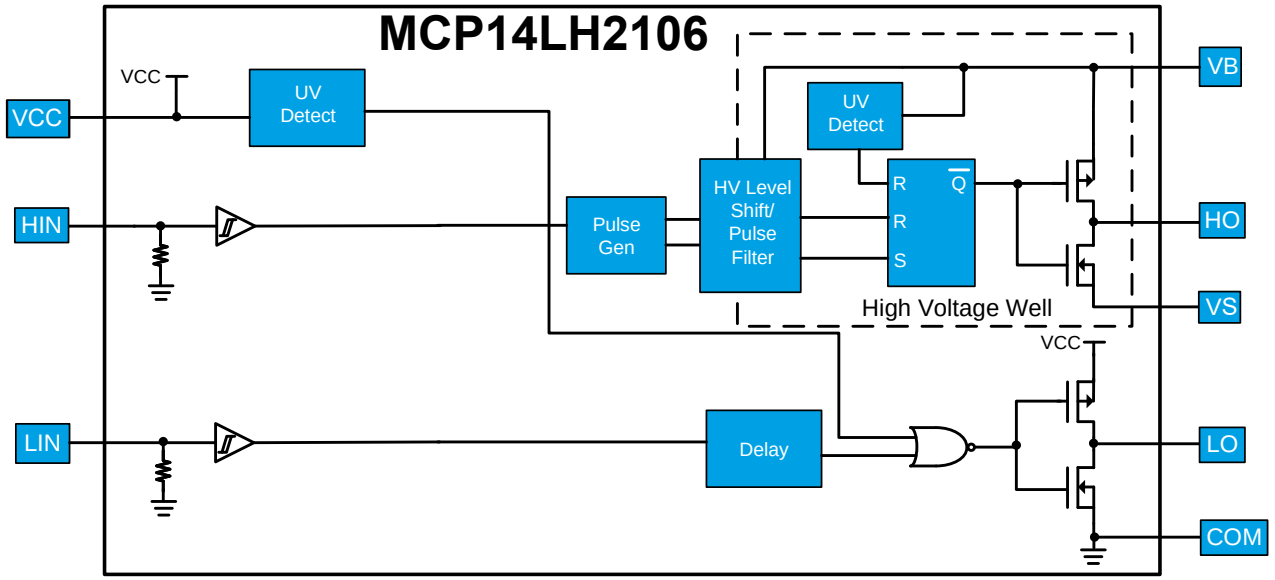
- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

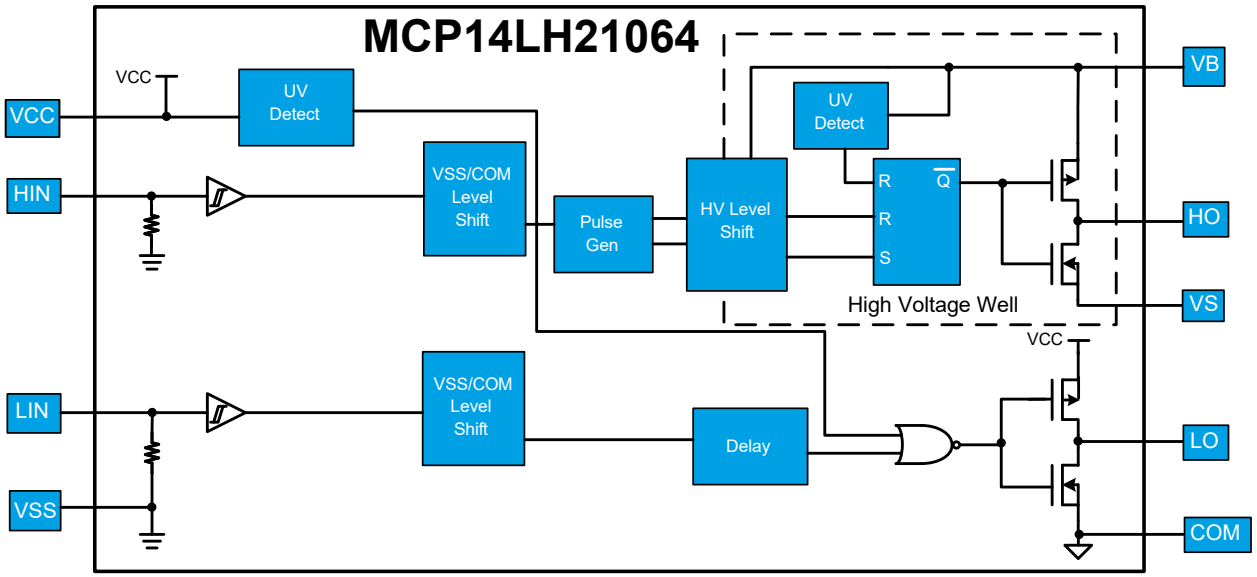
Typical Applications





Block Diagrams





1. Pin Configuration

Pin Name	Pin No. MCP14LH2106	Pin No. MCP14LH21064	Pin Description
VCC	1	1	Low-side and logic fixed supply
HIN	2	2	Logic input for high-side gate driver outputs, in phase with HO (referenced to VSS).
LIN	3	3	Logic input for low-side gate driver outputs, in phase with LO (referenced to VSS).
NC	—	4	Not connected
VSS	—	5	Logic ground
COM	4	6	Low-side return
LO	5	7	Low-side gate drive output
NC	—	8	Not connected
NC	—	9	Not connected
NC	—	10	Not connected
VS	6	11	High-side floating supply return
HO	7	12	High-side gate drive output
VB	8	13	High-side floating supply
NC	—	14	Not connected

1.1. Package Type

Figure 1-1. SOIC-8 Package - MCP14LH2106 (Top View)

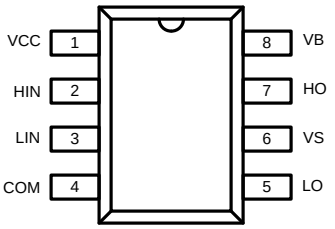
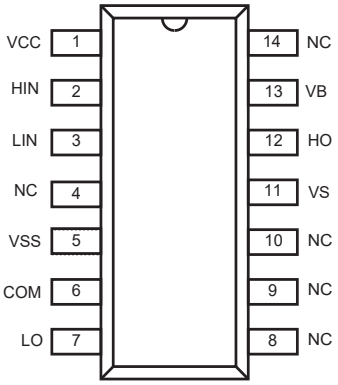


Figure 1-2. SOIC-14 Package - MCP14LH21064 (Top View)



2. Electrical Characteristics

2.1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
High-Side Floating Supply Voltage	V_B	−0.3	624	V
High-Side Floating Supply Offset Voltage	V_S	V_B − 24	V_B + 0.3	V
High-Side Floating Output Voltage	V_{HO}	V_S − 0.3	V_B + 0.3	V
Offset Supply Voltage Transient	dV_S/dt	—	50	V/ns
Programmable Dead Time Pin Voltage	V_{DT}	V_{SS} − 0.3	V_B + 0.3	V
Low-Side and Logic Fixed Supply Voltage	V_{CC}	−0.3	24	V
Low-Side Output Voltage	V_{LO}	−0.3	V_{CC} + 0.3	V
Logic Supply Offset Voltage (**MCP14LH21064**)	V_{SS}	V_{CC} − 24	V_{CC} + 0.3	V
Logic Input Voltage (HIN and LIN)	V_{IN}	V_{SS} − 0.3	V_{CC} + 0.3	V
SOIC-14 Package Power Dissipation at $T_A \leq 25°C$	P_D	—	1.0	W
SOIC-14 Thermal Resistance (See Note)	θ_{JA}	—	120	°C/W
Junction Operating Temperature	T_J	—	+150	°C
Lead Temperature (Soldering, 10s)	T_L	—	+300	°C
Storage Temperature	T_{stg}	−55	+150	°C

⚠ WARNING Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: When mounted on a standard JEDEC 2-layer FR-4 board.

2.2. Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit
High-Side Floating Supply Absolute Voltage	V_B	V_S + 10	V_S + 20	V
High-Side Floating Supply Offset Voltage	V_S	See Note	600	V
High-Side Floating Output Voltage	V_{HO}	V_S	V_B	V
Low-Side and Logic Fixed Supply Voltage	V_{CC}	10	20	V
Low-Side Output Voltage (**MCP14LH2106**)	V_{LO}	0	V_{CC}	V
Low-Side Output Voltage (**MCP14LH21064**)	V_{LO}	COM	V_{CC}	V
Logic Input Voltage (HIN and LIN) (**MCP14LH2106**)	V_{IN}	0	5	V
Logic Input Voltage (HIN and LIN) (**MCP14LH21064**)	V_{IN}	V_{SS}	5	V
Programmable Deadtime Pin Voltage (**MCP14LH21064**)	V_{DT}	V_{SS}	V_{CC}	V
Logic Gound (**MCP14LH21064**)	V_{SS}	−5	5	V
Ambient Temperature	T_A	−40	125	°C

Note: Device operational to V_S = −8V (typical) for V_{BS} = 15V.

2.3. DC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS}= COM, and T_A = 25°C, unless otherwise specified.						
Parameter (Note 1)	Symbol	Min.	Typ.	Max.	Unit	Conditions
Logic "1" Input Voltage	V_{IH}	2.5	—	—	V	V_{CC} = 10 V to 20 V
Logic "0" Input Voltage (**MCP14LH2106**)	V_{IL}	—	—	0.8	V	V_{CC} = 10 V to 20 V
Logic "0" Input Voltage (**MCP14LH21064**)	V_{IL}	—	—	0.6	V	V_{CC} = 10 V to 20 V
High Level Output Voltage, V_{BIAS} – V_O	V_{OH}	—	0.05	0.2	V	I_O = 2 mA
Low Level Output Voltage, V_O	V_{OL}	—	0.02	0.1	V	I_O = 2 mA
Offset Supply Leakage Current	I_{LK}	—	—	50	µA	V_B = V_S = 600V
Quiescent V_{BS} Supply Current	I_{BSQ}	20	75	130	µA	V_{IN} = 0V or 5V
Quiescent V_{CC} Supply Current	I_{CCQ}	60	120	180	µA	V_{IN} = 0V or 5V
Logic "1" Input Bias Current	I_{IN+}	—	5	20	µA	V_{IN} = 5V
Logic "0" Input Bias Current (**MCP14LH2106**)	I_{IN-}	—	—	2	µA	V_{IN} = 0V
Logic "0" Input Bias Current (**MCP14LH21064**)	I_{IN-}	—	—	5	µA	V_{IN} = 0V
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	7.0	8.4	9.8	V	
V_{BS} Supply Undervoltage Negative Going Threshold	V_{BSUV-}	6.4	7.8	9.0	V	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	7.0	8.4	9.8	V	
V_{CC} Supply Undervoltage Negative Going Threshold	V_{CCUV-}	6.4	7.8	9.0	V	
Undervoltage Lockout Hysteresis (**MCP14LH2106**)	V_{UVLOH}	0.3	0.7	—	V	
Hysteresis (**MCP14LH21064**)	V_{CCUVH}, V_{BSUVH}	0.3	0.7	—	V	
Output High Short Circuit Pulsed Current	I_{O+}	130	290	—	mA	V_O = 0V, PW ≤ 10 µs
Output Low Short Circuit Pulsed Current	I_{O-}	270	600	—	mA	V_O = 15V, PW ≤ 10 µs

Notes:

1. For the **MCP14LH2106**, the V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.
2. For the **MCP14LH21064**, the V_{IN}, V_{TH}, and I_{IN} parameters are referenced to VSS and are applicable to the two logic input pins: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.
3. For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum, with a Pulse Width (PW) of at least 440 µs.

2.4. AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 100 pF, V_{SS} = COM, and T_A = 25°C, unless otherwise specified.						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Turn-on Propagation Delay	t_{ON}	—	220	300	ns	V_S = 0V, See Figure 3-2
Turn-off Propagation Delay	t_{OFF}	—	200	280	ns	V_S = 0V or 600V, See Figure 3-2
Turn-on Rise Time	t_r	—	100	220	ns	V_S = 0V, See Figure 3-2
Turn-off Fall Time	t_f	—	35	80	ns	V_S = 0V, See Figure 3-2
Delay Matching	t_{DM}	—	0	30	ns	See Figure 3-3

3. Timing Waveforms

Figure 3-1. Input/Output Timing Diagram

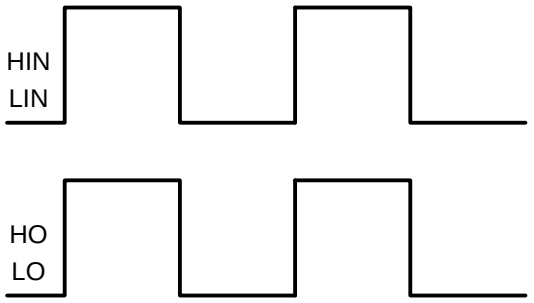


Figure 3-2. Switching Time Waveform Definitions

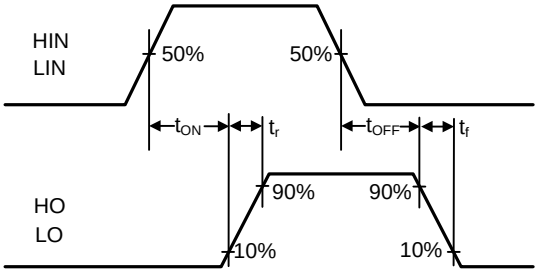
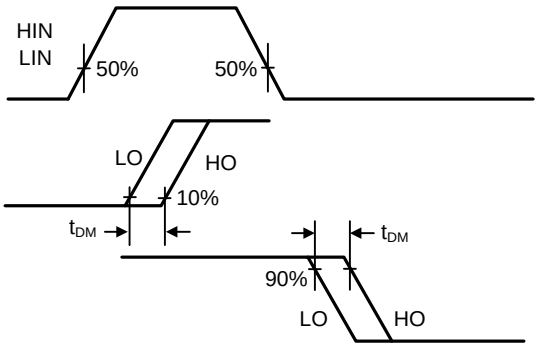


Figure 3-3. Delay Matching Waveform Definitions



4. Typical Performance Curves

Figure 4-1. Output Source Current vs. Supply Voltage

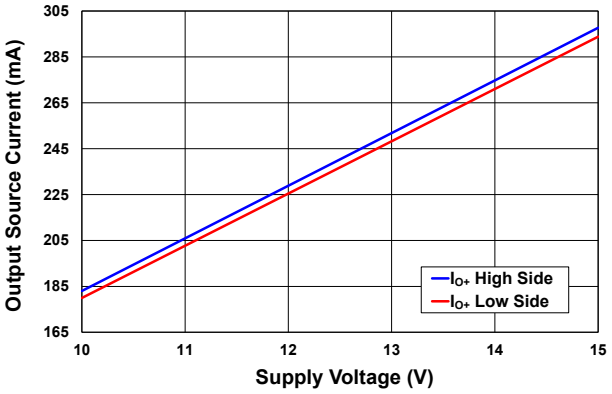


Figure 4-2. Output Source Current vs. Temperature

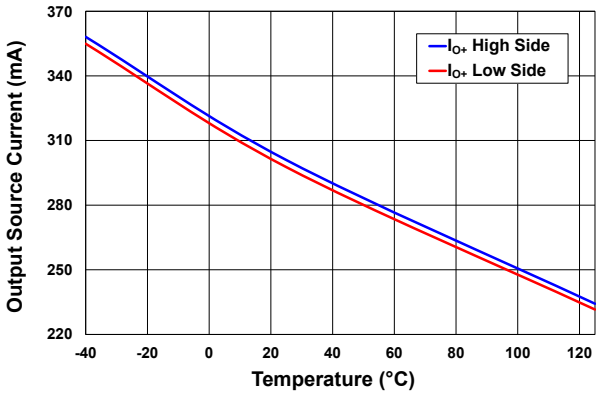


Figure 4-3. Output Sink Current vs. Supply Voltage

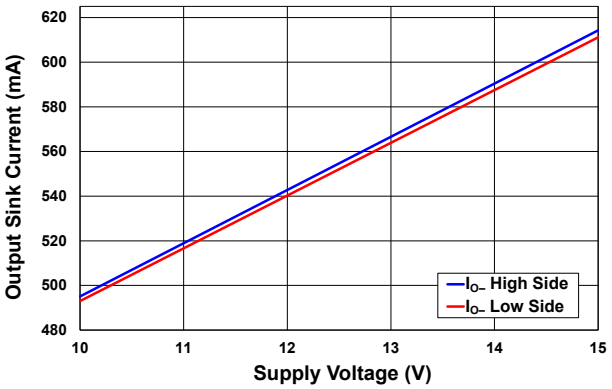


Figure 4-4. Output Sink Current vs. Temperature

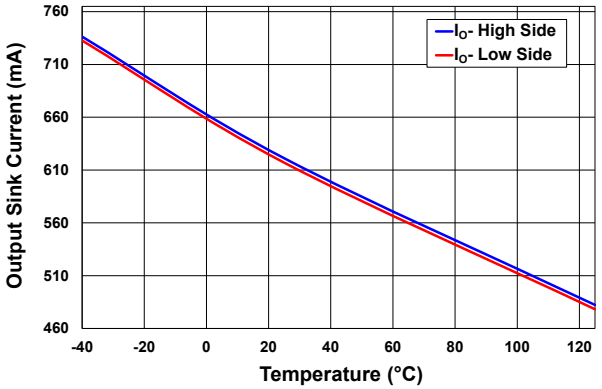


Figure 4-5. Logic 1 Input Voltage vs. Supply Voltage

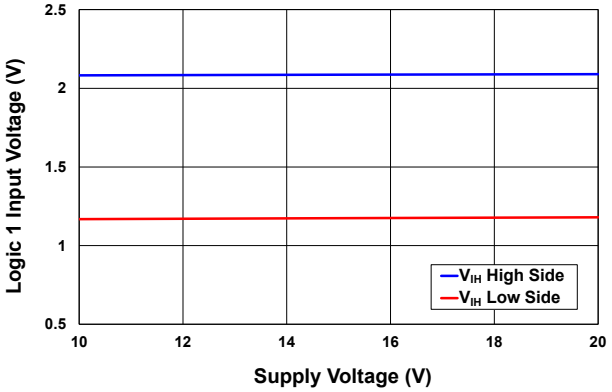


Figure 4-6. Logic 1 Input Voltage vs. Temperature

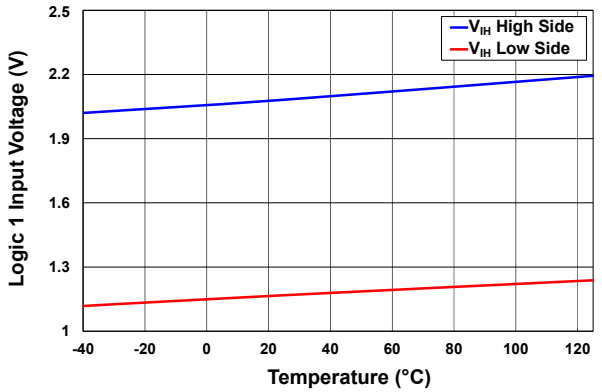


Figure 4-7. Logic 0 Input Voltage vs. Supply Voltage

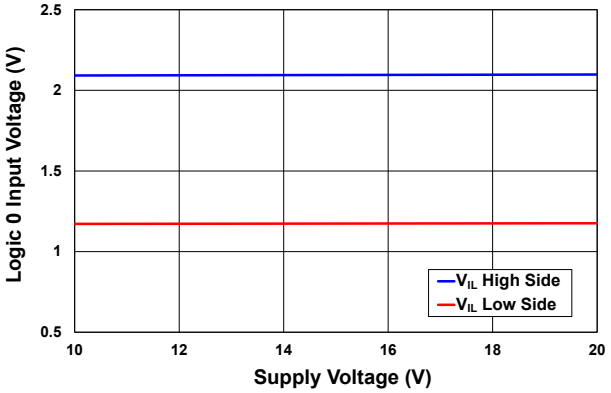


Figure 4-8. Logic 0 Input Voltage vs. Temperature

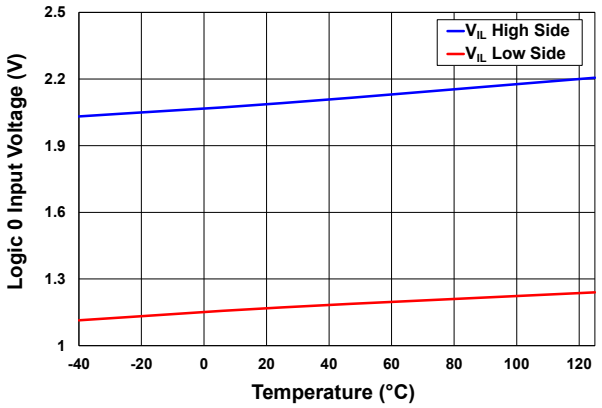


Figure 4-9. Quiescent Current vs. Supply Voltage

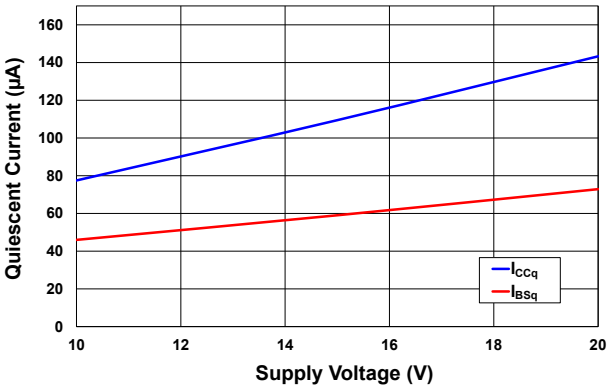


Figure 4-10. Quiescent Current vs. Temperature

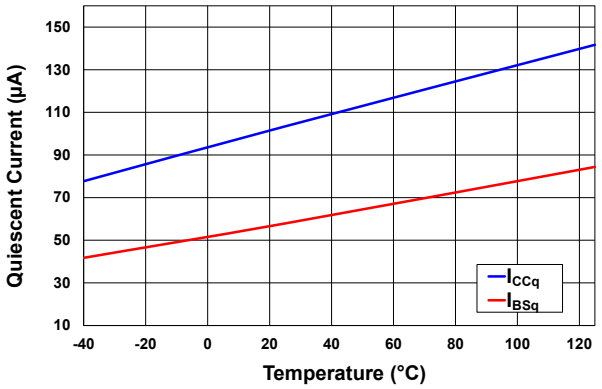


Figure 4-11. Turn-on Propagation Delay vs. Supply Voltage

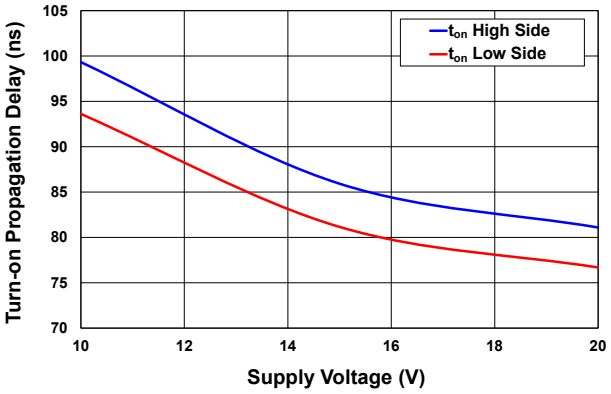


Figure 4-12. Turn-on Propagation Delay vs. Temperature

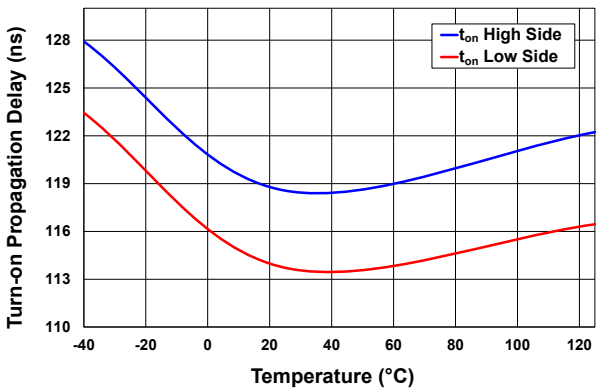


Figure 4-13. Turn-off Propagation Delay vs. Supply Voltage

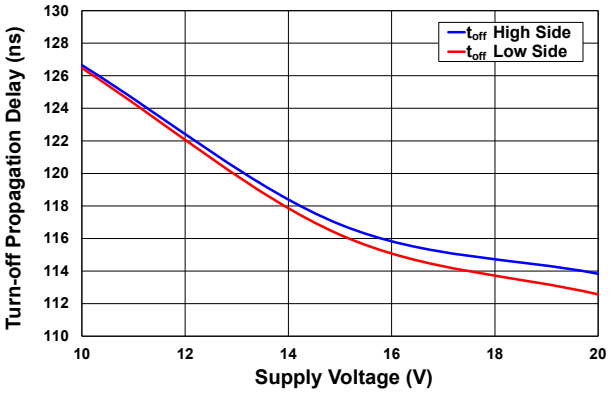


Figure 4-14. Turn-off Propagation Delay vs. Temperature

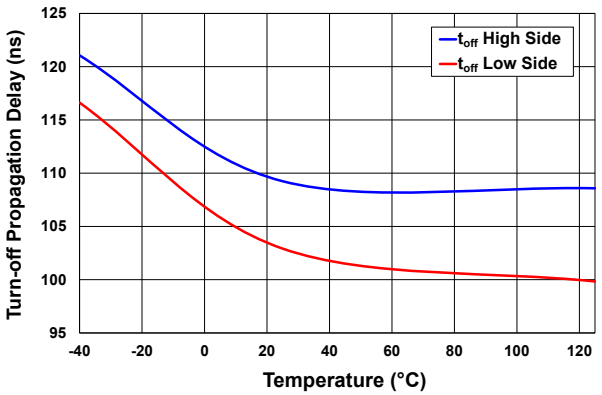


Figure 4-15. Rise Time vs. Supply Voltage

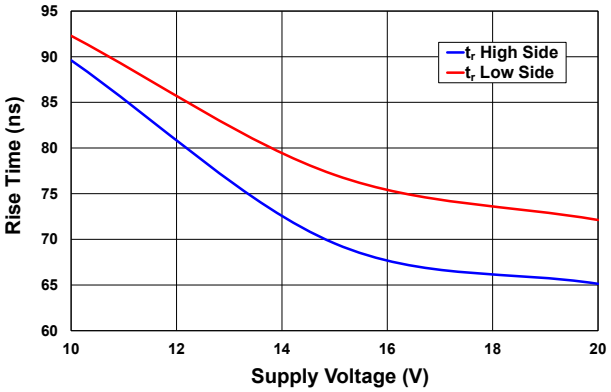


Figure 4-16. Rise Time vs. Temperature

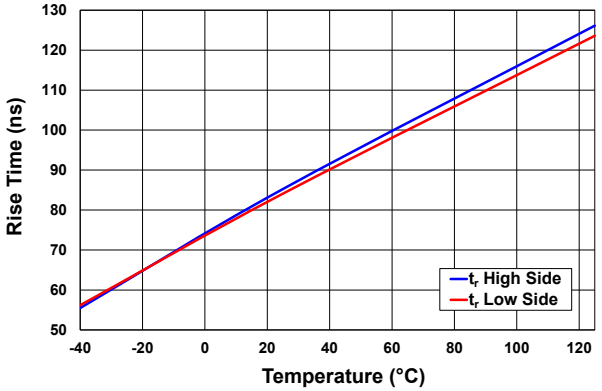


Figure 4-17. Fall Time vs. Supply Voltage

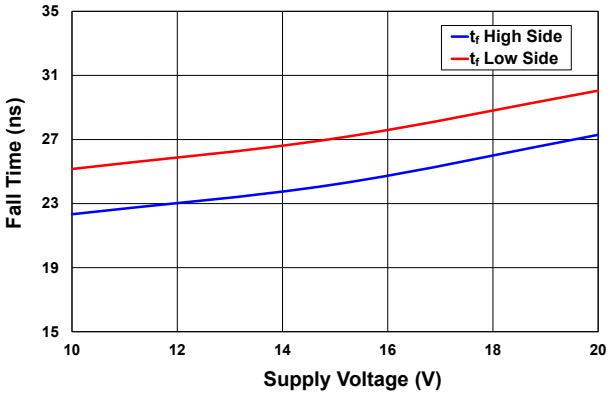


Figure 4-18. Fall Time vs. Temperature

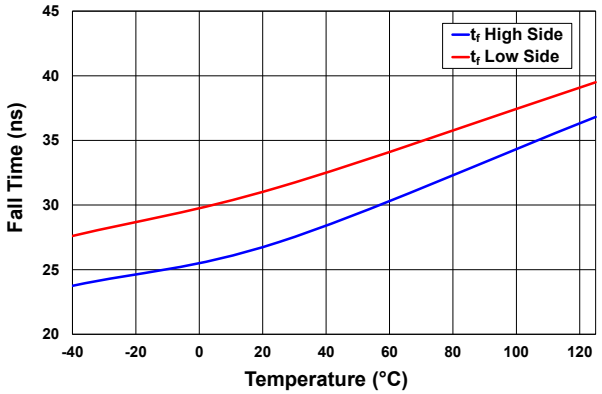


Figure 4-19. Delay Matching vs. Supply Voltage

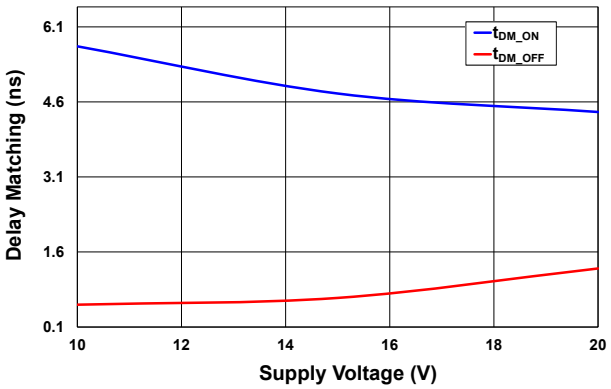


Figure 4-20. Delay Matching vs. Temperature

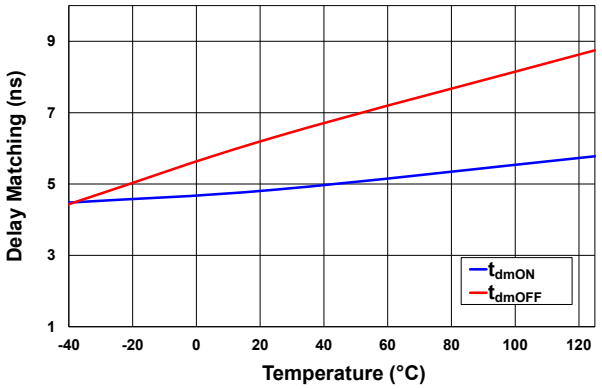


Figure 4-21. V_{CC} UVLO vs. Temperature

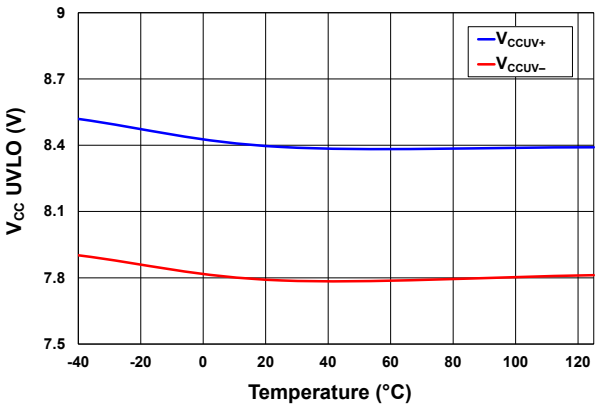


Figure 4-22. V_{BS} UVLO vs. Temperature

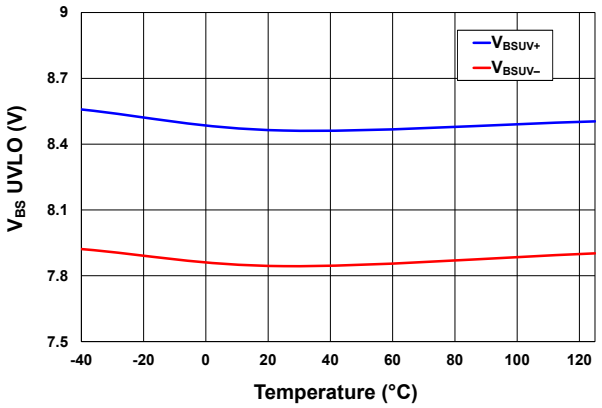
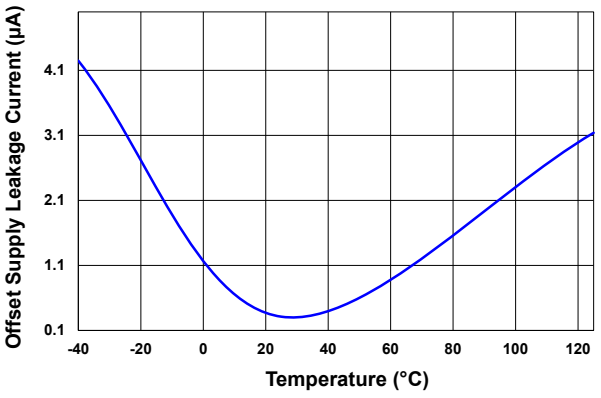


Figure 4-23. Offset Supply Leakage Current Temperature



5. Functional Description

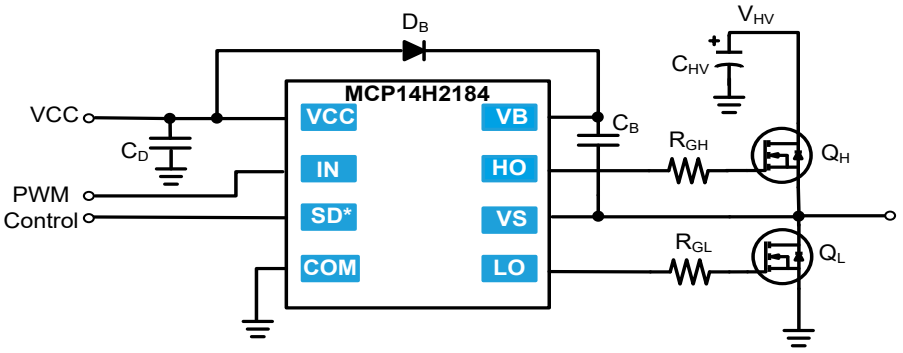
5.1. Halfbridge Configuration

A common configuration used for the MCP14LH2106(4) is a half-bridge (see Figure 5-1). In a half-bridge configuration the source of the high-side MOSFET (Q_H) and the drain of the low-side MOSFET (Q_L) are connected, ensuring the line (V_S) is both the return for the high side in the gate driver IC and the output of the half-bridge. When Q_H is ON and Q_L is OFF, V_S swings to high voltage, and when Q_H is OFF and Q_L is ON, V_S swings to GND. Hence, the output switches from GND to high voltage at the frequency of HIN and LIN, this line drives a transformer for a power supply, or a coil on a motor.

In this half-bridge configuration, high voltage DC is input to the MOSFETs, and converted to a high voltage switching signal to output to load (Figure 5-1). The MOSFETs operate in saturation mode and an important function of the gate driver is to turn ON the MOSFET quickly to minimize switching losses from the linear region of the MOSFET (turn ON and turn OFF). The MCP14LH2106(4) has a typical rise/fall time of 100 ns/35 ns for a 1 nF load.

Another important function of the gate driver IC in a half-bridge configuration is to convert the logic of the control signals (MCP14LH2106(4) operates at logic 3.3V), to a voltage and current level sufficient to drive the gate of the MOSFET and IGBT. This requires driving large currents initially to turn ON/turn OFF the MOSFET quickly. Also, the floating well of the high-side allows high voltage configurations during bootstrap operation.

Figure 5-1. MCP14LH2106 in a Half-bridge Configuration

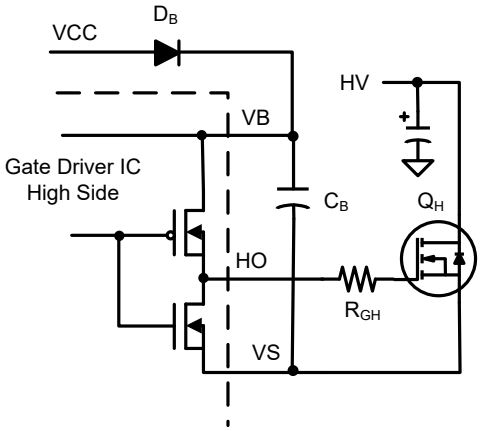


5.2. Bootstrap Operation

The supply for the MCP14LH2106(4) High-Side is provided by the bootstrap capacitor C_B (see Figure 5-2). In the half-bridge configuration, V_S swings from 0V to V_{HV} depending on the PWM input of the IC. When V_S is 0V, V_{BS} will go below V_{CC}, and V_{CC} will charge C_B . When HO goes high, V_S swings to V_{HV}, and V_{BS} remains at V_{CC} minus a diode drop (D_B), due to the voltage on C_B . This is the supply for the high side gate driver and allows the gate driver to function with the floating well (V_S) at the high voltage.

When considering the value of the bootstrap capacitor C_B , it is important to size it so that it provides enough energy to quickly drive the gate of Q_H . Values of 1 µF to 10 µF are recommended. The exact value depends on gate capacitance and the noise level appropriate for the application. It is key to use a low ESR capacitor that is close to the device. This will quickly supply charge to the gate of the MOSFET.

Figure 5-2. MCP14LH2106(4) High-side in Bootstrap Operation



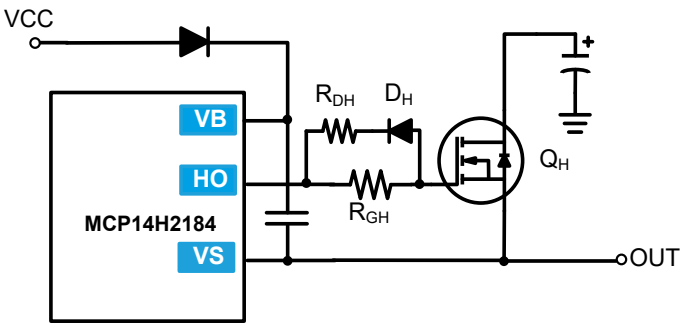
5.3. Gate Drive Control

The most crucial time in the gate drive is the turn ON and turn OFF of the MOSFET, and performing this function quickly, with minimal noise and ringing. If the rise/fall time is too fast, it can cause unnecessary ringing, and too slow of a rise/fall time will increase switching losses in the MOSFET.

An example of just the high side gate driver is shown in Figure 5-3 (any selection of gate driver components should be the same for high side and low side drive). Two extra components are shown, R_{DH} and D_H. With the careful selection of R_{GH} and R_{DH}, it is possible to selectively control the rise time and fall time of the gate drive. For turn ON, all current will go from the IC through R_{GH} and charge the MOSFET gate capacitor, hence increasing or decreasing R_{GH} will increase or decrease rise time in the application. With the addition of D_H, the fall time can be separately controlled as the turn OFF current flows from the MOSFET gate capacitor, through D_H and R_{DH} to the driver in the IC to VS. So increasing or decreasing R_{DH} will increase or decrease the fall time.

Increasing turn ON and turn OFF has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. For gate resistor value selection, the exact value depends on the type of application and desired level of noise and ringing. Generally, power supplies switch at a fast speed, and want to squeeze out efficiency from the MOSFETs, so lower values are recommended, for example R_{GH} = 5Ω - 20Ω. For motors, the switching speed is generally slower, and the application has more inherent noise, so higher values are recommended, for example R_{GH} = 10Ω - 100Ω.

Figure 5-3. Gate Drive Control



6. Application Information

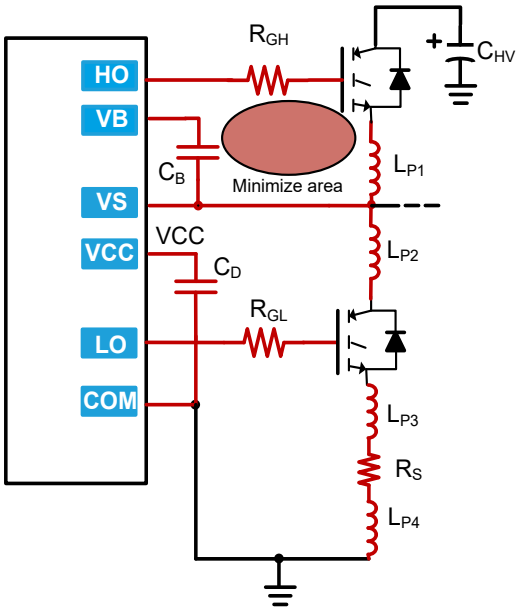
Layout Considerations

Layout plays a considerable role in noise and ringing in a circuit. Unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 6-1 shows a half bridge schematic with parasitic inductance in the high current path (L_{P1}, L_{P2}, L_{P3}, L_{P4}) which would be caused by inductance in the metal of the trace. Considering Figure 6-1, the length of the tracks in red should be minimized, and the bootstrap capacitor (C_B) and the decoupling capacitor (C_D) should be placed as close to the IC as possible. Low ESR ceramic capacitors should be used to minimize inductance. Finally, the gate resistors (R_{GH} and R_{GL}) and the sense resistor (R_S) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

A layout example is seen in Figure 6-2. Here there are two bootstrap capacitors (CB1 and CB2) and two decoupling capacitors (C1 and C2). All of these capacitors are placed as close as possible to the HVIC. Even when only using one boostrap capacitor and one decoupling capacitor, it needs to be as close as possible to minimize inductance between the capacitor and the driver.

Generally, for the decoupling capacitor on VCC, at least one low ESR capacitor is recommended, and it should be placed as close to the device as possible. Figure 6-2 shows an example. The recommended values are 1 µF to 10 µF. A second smaller decoupling capacitor is sometimes added to provide better high frequency response (for example, 0.1 µF).

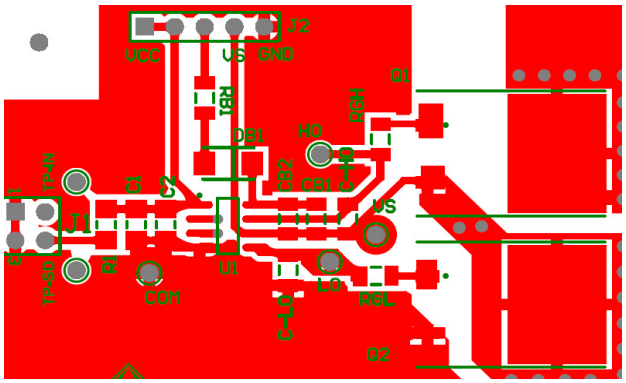
Figure 6-1. Layout Suggestions for MCP14LH2106(4) in a Half-bridge Configuration



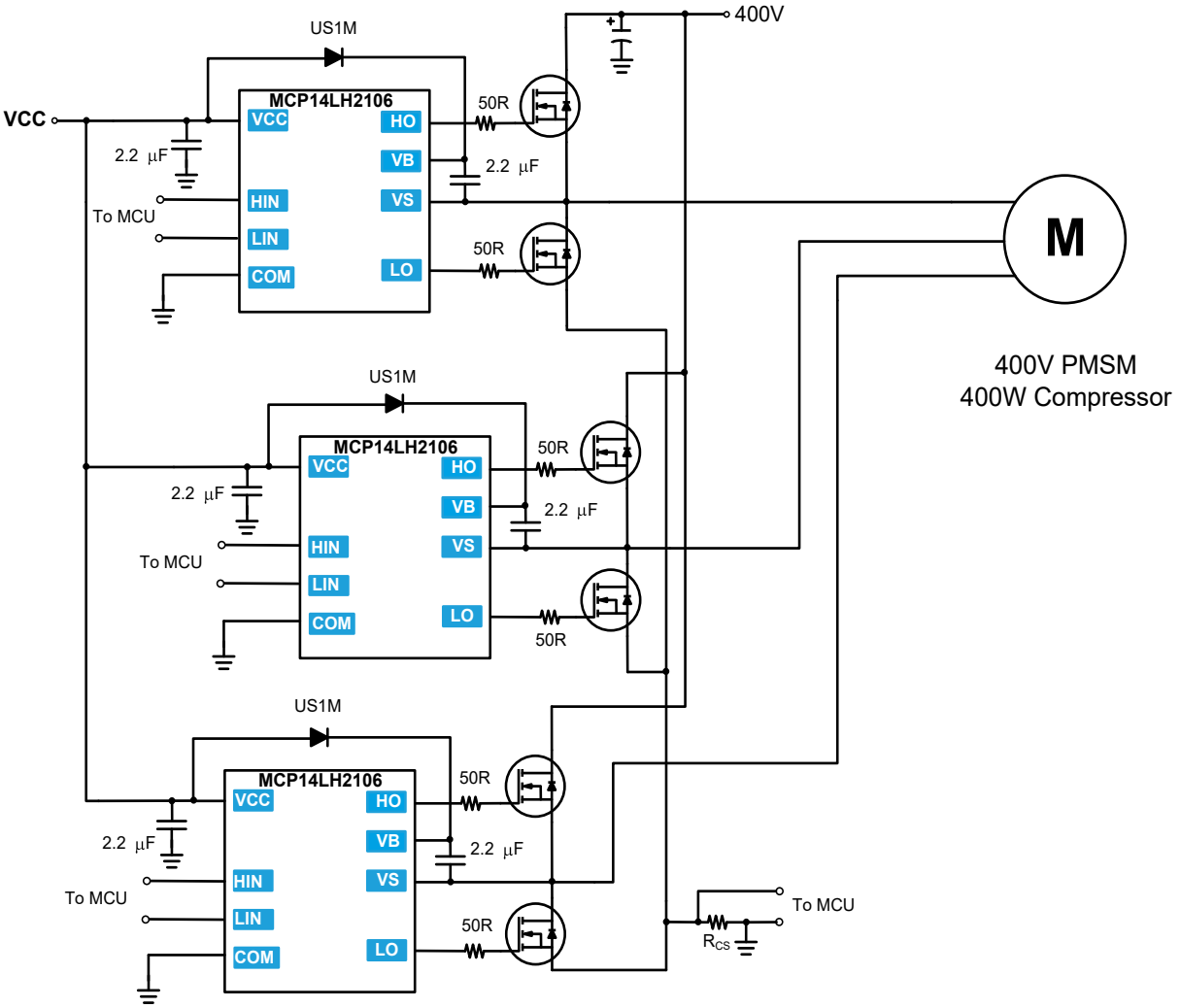
Note: Please keep high voltage and high current lines away from logic and analog lines.

Figure 6-2. Layout Example for MCP14LH2106(4) (U1) in a Half-bridge Configuration

Please note the bootstrap capacitors (CB1, CB2), V_{CC} capacitors (C1 and C2), and the bootstrap diode (DB1) adjacent to the IC (U1).

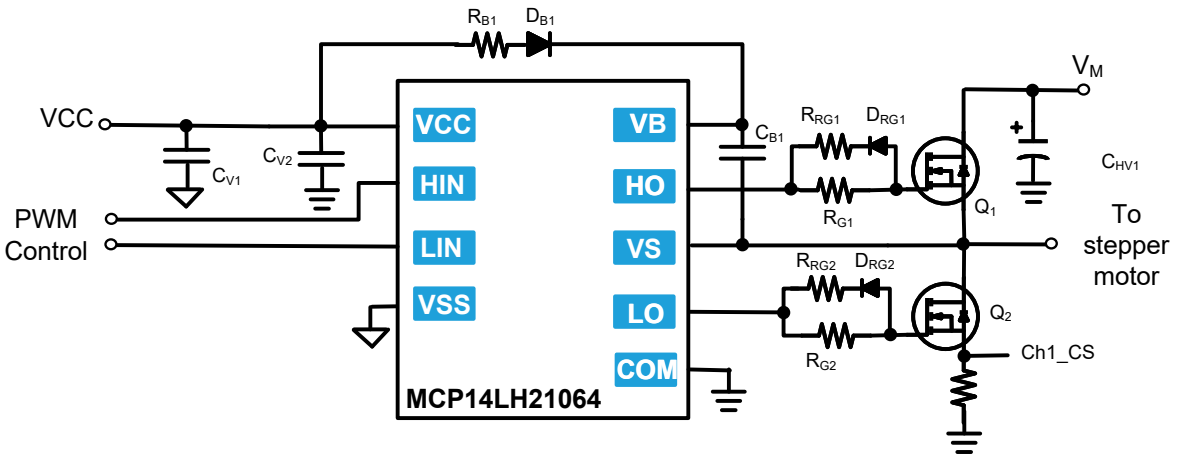


Application Example for MCP14LH2106



Application Example for MCP14LH21064

Figure 6-3. Single Phase (of four) for Stepper Motor Driver Application Using the MCP14LH21064

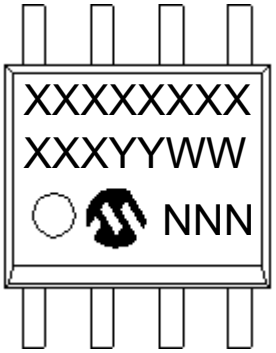


- R_{RG1} and R_{RG2} values are typically between 0Ω and 10Ω. The exact value is decided based on the MOSFET junction capacitance and the drive current of gate driver. A value of 10Ω is used in this example.
- It is **highly recommended** that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for VDD = 15V), with a minimum pulse width of 440 ns.
- R_{G1} and R_{G2} values are typically between 10Ω and 100Ω. The exact value is decide based on the MOSFET junction capacitance and drive current of the gate driver. A value of 50Ω is used in this example.
- R_{B1} value is typically between 3Ω and 20Ω. The exact value is calculated based on the bootstrap capacitor value and the amount of current limiting required for bootstrap capacitor charging. A value of 10Ω is used in this example. Also, D_{B1} should be an ultra fast diode with a minimum rating of 1A and a voltage rating greater than the system operating voltage.

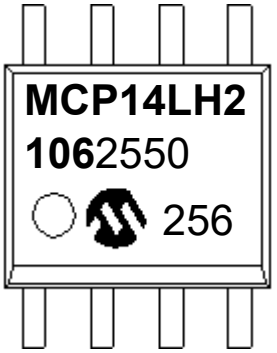
7. Packaging Information

Package Marking Information

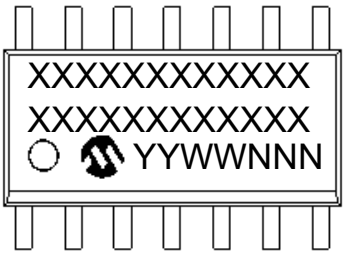
8-Pin SOIC(MCP14LH2106):



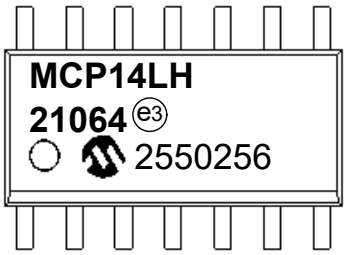
Example:



14-Pin SOIC (MCP14LH21064):



Example:



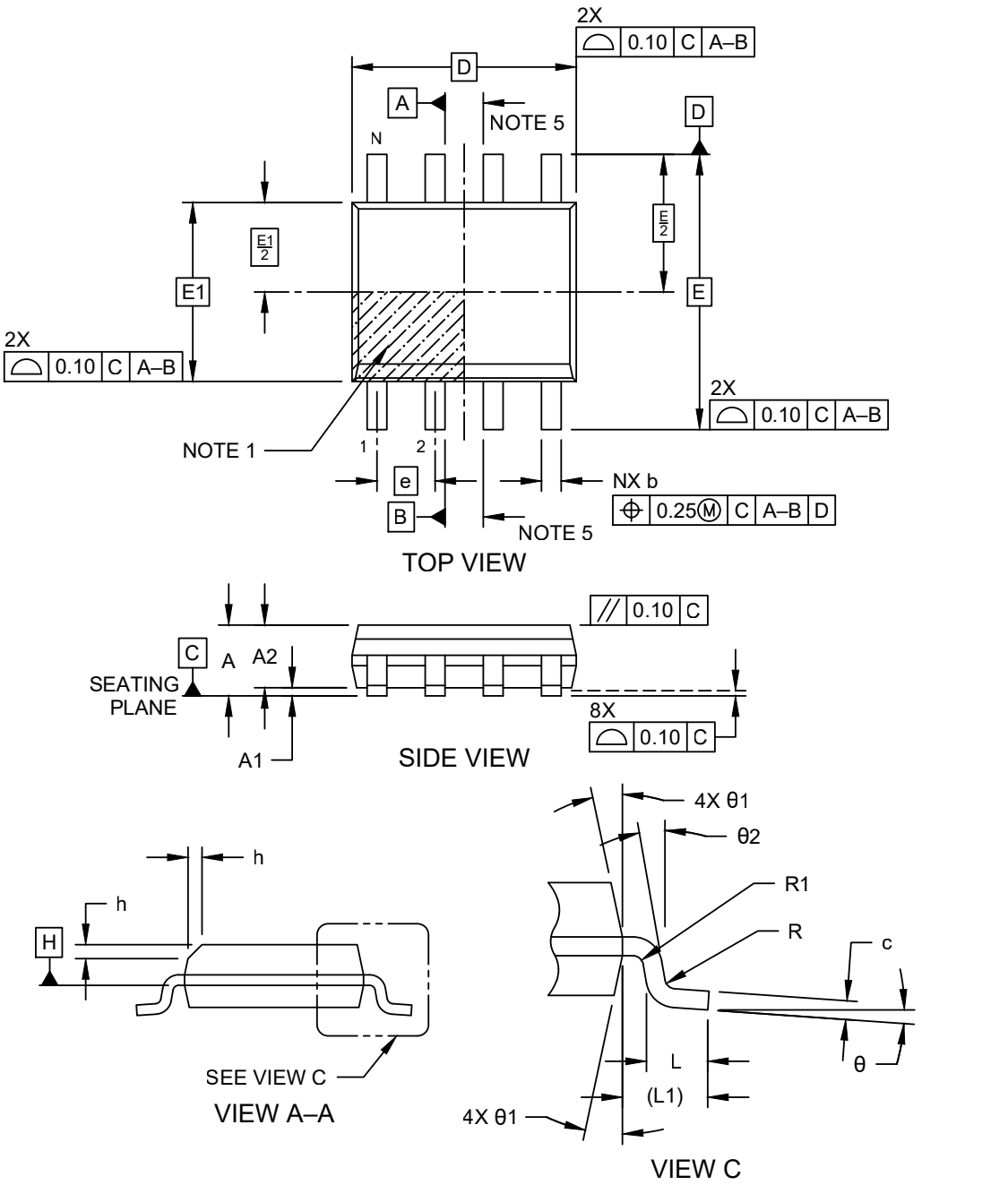
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

Package Outline Drawings

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

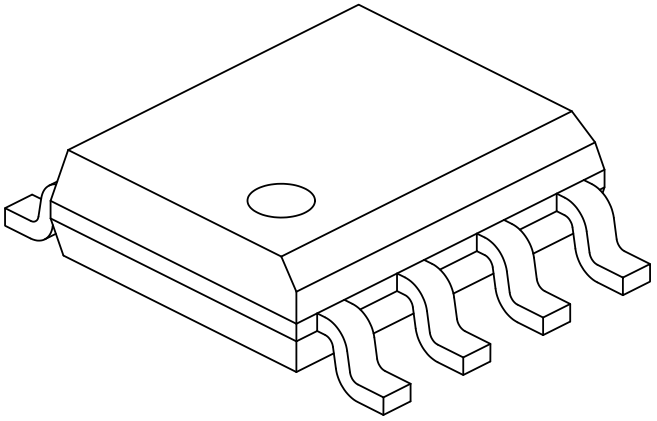
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

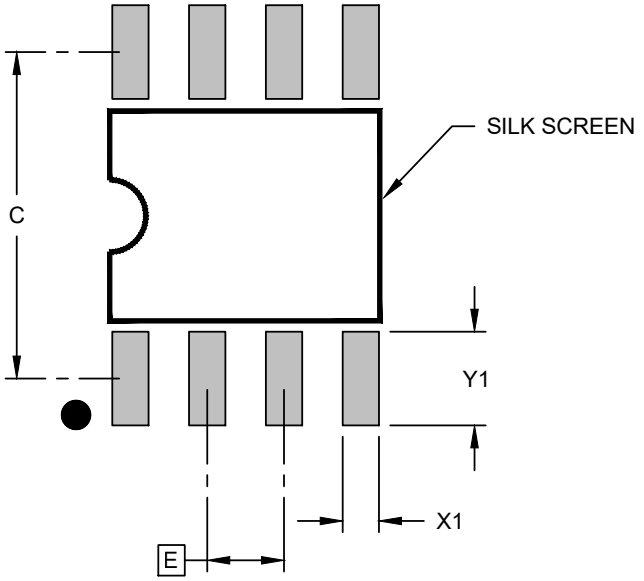
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-00057-SN Rev L Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

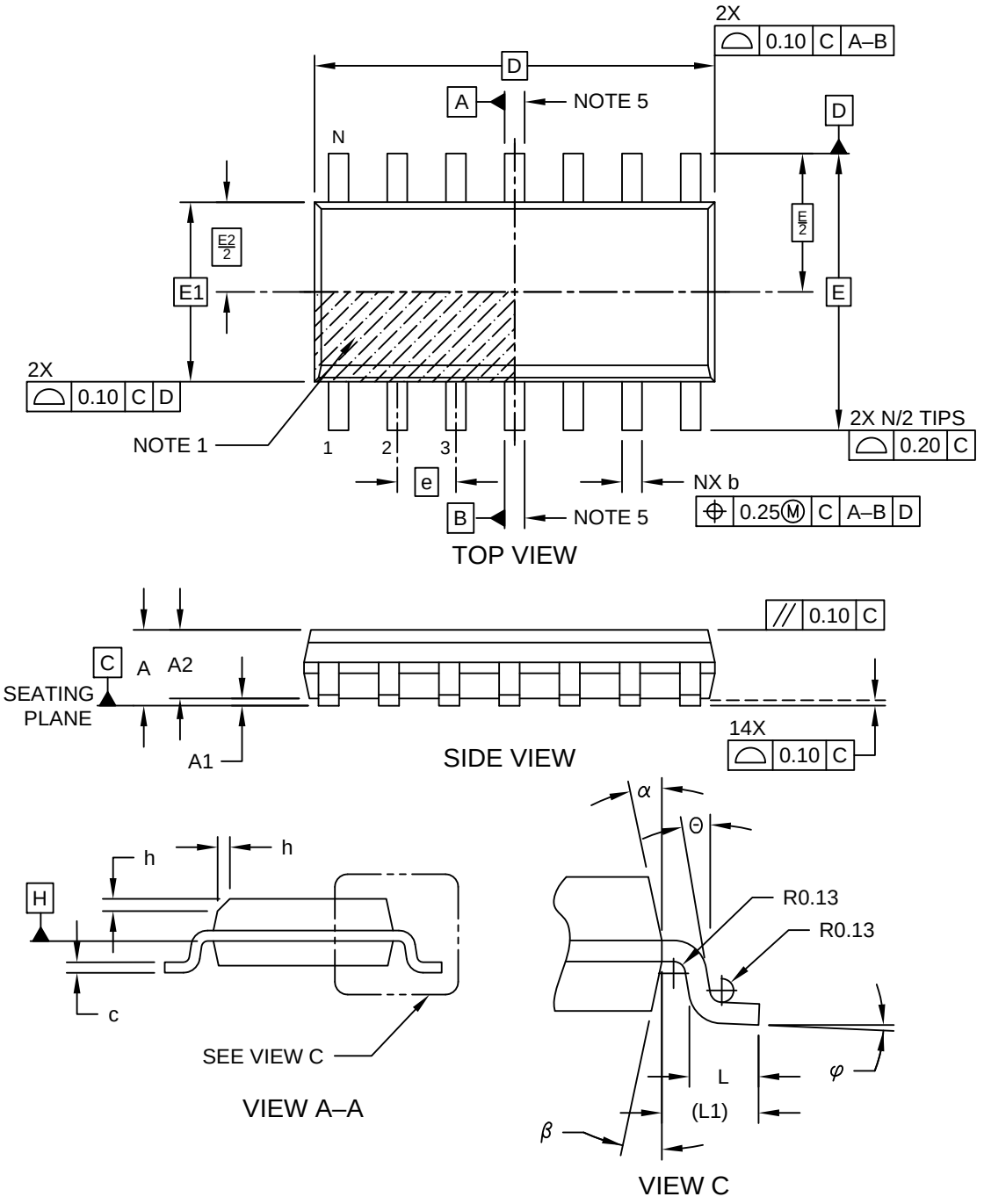
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-02057-SN Rev L

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

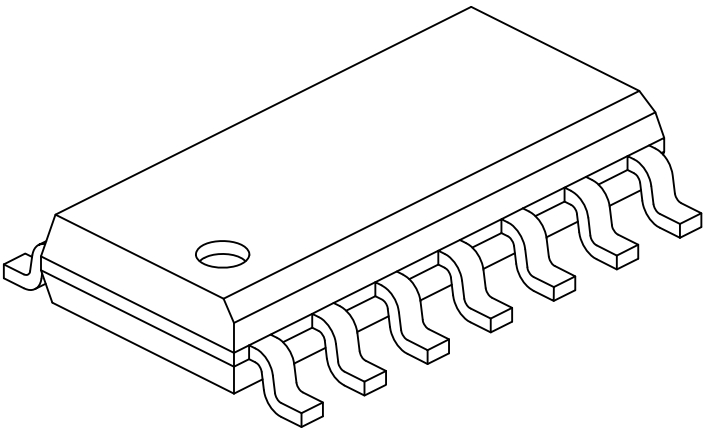
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

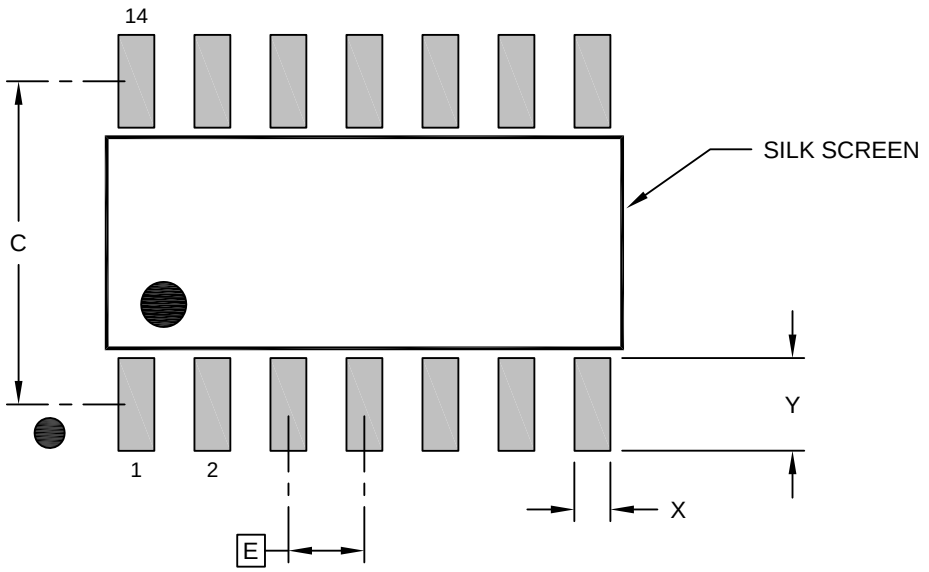
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

8. Revision History

Doc. Rev.	Date	Section	Comments
A	November 2025		Initial release of this document.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.

Device:	MCP14LH2106(4): High-Side and Low-Side Gate Driver	
Tape and Reel Option(1):	Blank	= Tube
	T	= Tape and Reel
Temperature Range:	E	= −40°C to +125°C (Extended)
Package:	SN	= Plastic Small Outline IC, 3.90 mm, SOIC, 8-Pin
	SL	= Plastic Small Outline, 3.90 mm, SOIC, 14-Pin

Examples:

- MCP14LH2106-E/SN: Half-Bridge Gate Driver, Tape and Reel, Extended temperature range, SOIC-8 package
- MCP14LH21064-E/SL: Half-Bridge Gate Driver, Tape and Reel, Extended temperature range, SOIC-14 package

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package.

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ISBN: 979-8-3371-2370-7

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