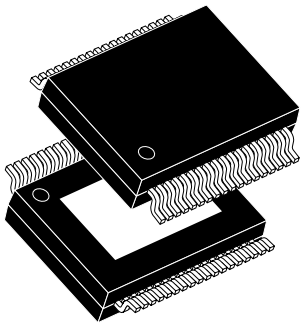
L99VR02XP

Datasheet

Dual automotive linear voltage regulator with configurable output voltage (2x250 mA current capability)



PowerSSO-36
exposed pad down

Product status link
L99VR02XP

Product summary	
Order code	L99VR02XPTR
Package	PowerSSO-36
Packing	Tape and reel

Features

Max supply voltage (load dump)	$V_{S\_LDO1,2}$	40 V
Max. output voltage tolerance	ΔV_O	±2%
Output current	$I_{O\_LDO1,2}$	2 x 250 mA
Quiescent current	$I_{qn\_LDO1,2}$	≤ 1 µA(1)

1. *Maximum value with regulator disabled, valid per each single output.*

- AEC-Q100 qualified
- Operating DC power supply voltage range from 2.15 V to 28 V
- Outputs protected versus short to battery
- Battery and post regulation operating modes are allowed
- Low dropout voltage
- Low quiescent current consumption
- Dual output voltages
- User-selectable output voltage (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V or 5 V)
- Output voltage precision ±2%
- Enable input for enabling/disabling the voltage regulator
- Output voltage monitoring with reset output
- Negligible ESR effect on output voltage stability for load capacitor
- Programmable autonomous watchdog and reset pulse delay through external capacitors
- Undervoltage-lockout UVLO
- Fast output discharge
- Thermal shutdown and short-circuit protection
- Advanced thermal warning and overvoltage diagnostic
- Thermal clusters
- Programmable short-circuit output current
- Wide operating temperature range (from T_J = -40 °C to 175 °C)
- Automatic voltage (de)tracking of LDO2 respect LDO1 or of an external voltage regulator
- Limited documentation available for customers that need support when dealing with ASIL requirements as per ISO 26262

Description

The L99VR02XP is a low dropout dual linear regulator designed for automotive applications available in a PowerSSO-36 package. The LDO delivers an output current up to 2 x 250 mA, and consumes a quiescent current as low as 1 µA (per each output) when the regulator is disabled.

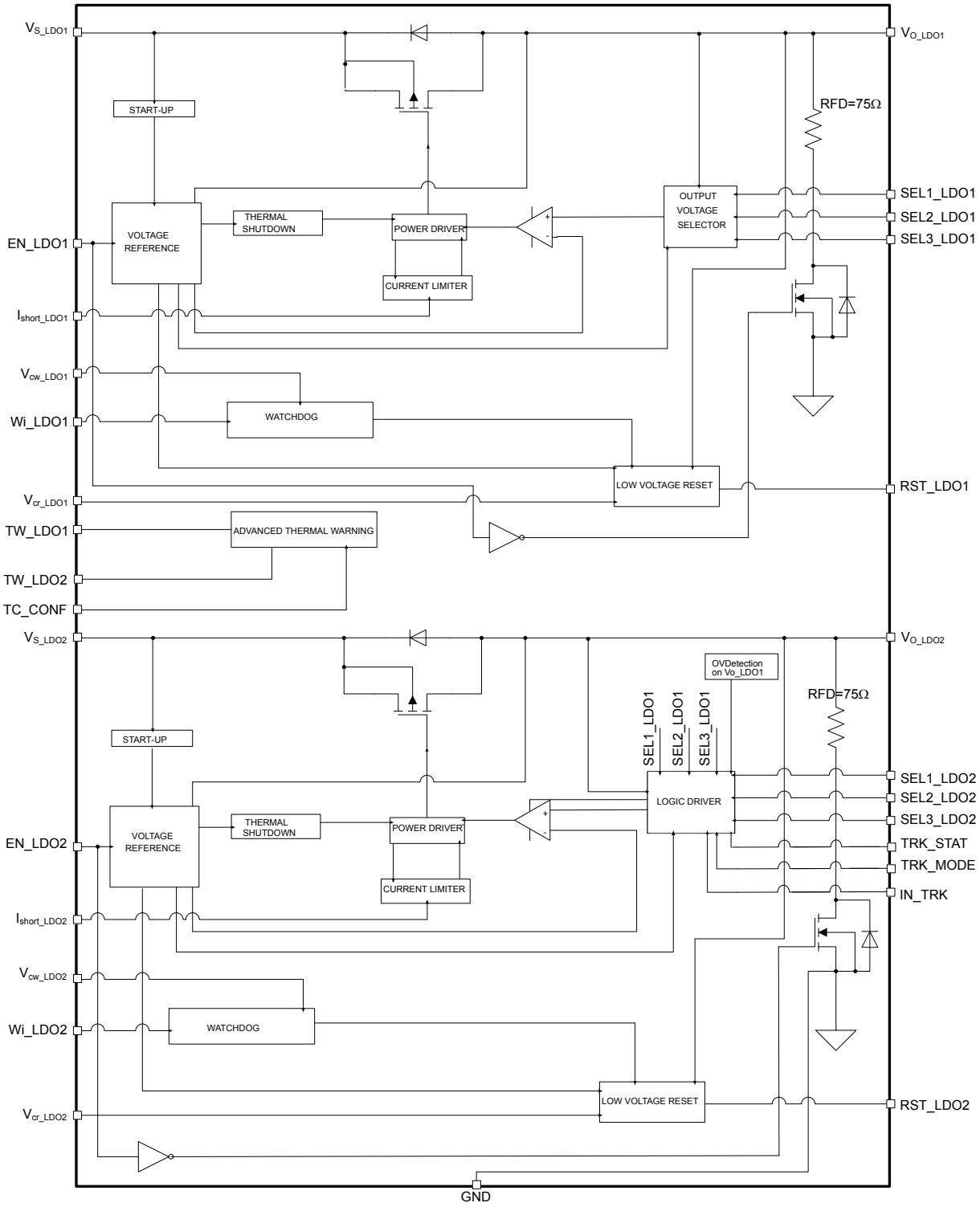
The input is 40 V tolerant to withstand load dump, while the operating input voltage range is between 2.15 V and 28 V. Each of the L99VR02XP outputs can be configured, through SELx pins, to generate a fixed output voltage (0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 2.8 V, 3.3 V or 5 V). High output voltage accuracy (±2%) is kept over wide temperature range, line and load variation.

The L99VR02XP features enable, reset, autonomous watchdog, advanced thermal warning, thermal cluster, fast output discharge. Automatic voltage (de)tracking of LDO2 respect the internal LDO1 or of an external voltage regulator and IShort control. The regulator output current is internally limited so the device is protected against short circuit and overload, besides it features over temperature protection; the short current value is configurable by an external resistance. The L99VR02XP can operate both in post regulation, attached to a pre-regulated voltage, or directly connected to the battery.

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



1.2 Pin description

Figure 2. **Pins configuration (top view)**

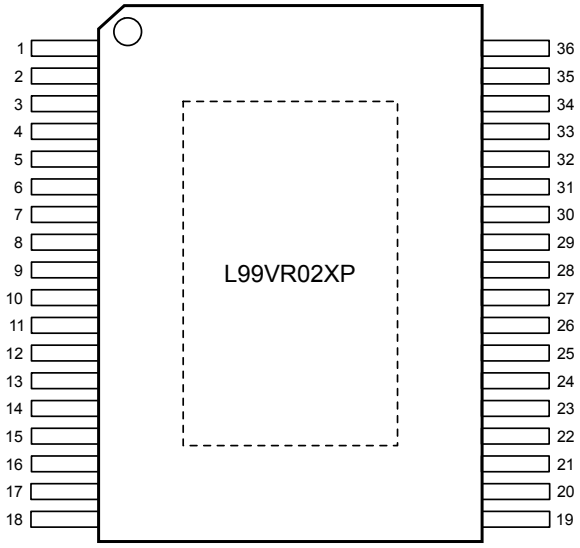


Table 1. **Pins description**

#	Pin name	Function
1	GND	Ground reference
2	SEL1_LDO1	Output voltage selectors for LDO1
3	SEL2_LDO1	
4	SEL3_LDO1	
5	NC	-
6	V_{S_LDO1}	Supply voltage for LDO1. Block directly to ground with ceramic capacitor ≥ 4.7 µF and a 100 nF capacitator as close as possible to the pin.
7	NC	-
8	EN_LDO1	Enable input for LDO1. With the Enable high, regulator, watchdog and reset are operating. With the Enable low, regulator, watchdog and reset are shutdown, while the fast discharge circuit is turned on. Connect the enable to V_{S_LDO1} to keep the device always enabled.
9	IN_TRK	Input pin for the reference voltage in tracking mode, connected to either V_{O_LDO1} or an external voltage regulator output.
10	V_{O_LDO1}	Voltage regulator output for LDO1. Block to ground with a capacitor ≥ 3.3 µF (needed for regulator stability).
11	RST_LDO1	Reset output for LDO1. It is pulled down when output voltage goes below V_{O_th} or frequency at Wi_LDO1 is too low. Leave floating if not used.
12	V_{cr_LDO1}	Reset timing adjust for LDO1. A capacitor between V_{cr_LDO1} pin and GND. Sets the reset delay time (T_{rd}). Leave floating if reset is not used.
13	GND	Ground reference
14	I_{Short_LDO1}	Programmable short circuit output current input pin for LDO1. A resistor between I_{Short_LDO1} pin and GND sets the short-circuit output current value.

#	Pin name	Function
15	Wi_LDO1	Watchdog refresh input for LDO1. If the square wave frequency at this input pin is too low, a low pulse at RST pin is generated.
16	V_{cw_LDO1}	Watchdog timer adjust for LDO1. A capacitor between V_{cw_LDO1} pin and GND sets the time response of the watchdog monitor.
17	TW_LDO1	Advanced thermal warning output. If the device detects a junction temperature above the warning threshold, the pin is pulled low. If an overvoltage condition occurs, a square wave is provided through the TW TW_LDO1 output. Leave floating if not used.
18	TC_CONF	Thermal shutdown configuration
19	TRK_STAT	Output pin. To indicate if LDO2 is in tracking mode.
20	TW_LDO2	Advanced Thermal warning output. If the device detects a junction temperature above the warning threshold, the pin is pulled low. If an overvoltage condition occurs, a square wave is provided through the TW_LDO2 output. Leave floating if not used.
21	V_{cw_LDO2}	Watchdog timer adjust for LDO2. A capacitor between V_{cw_LDO2} pin and GND sets the time response of the watchdog monitor.
22	Wi_LDO2	Watchdog refresh input for LDO2. If the square wave frequency at this input pin is too low, a low pulse at RST pin is generated.
23	I_{Short_LDO2}	Programmable short circuit output current input pin for LDO2. A resistor between I_{Short_LDO2} pin and GND sets the short circuit output current value
24	GND	Ground reference
25	V_{cr_LDO2}	Reset timing adjust for LDO2. A capacitor between V_{cr_LDO2} pin and GND sets the reset delay time (T_{rd}). Leave floating if reset is not used.
26	RST_LDO2	Reset output for LDO2. It is pulled down when output voltage goes below V_{O_th} or frequency at Wi_LDO2 is too low. Leave floating if not used.
27	V_{O_LDO2}	Voltage regulator output for LDO2. Block to ground with a capacitor ≥ 3.3 µF (needed for regulator stability).
28	TRK_MODE	Input pin selecting the tracking mode (either from LDO1 or an external regulator)
29	EN_LDO2	Enable input for LDO2. With the enable high, regulator, watchdog and reset are operating. With the enable low, regulator, watchdog and reset are shutdown, while the fast discharge circuit is turned on. Connect the Enable to V_{S_LDO2} to keep the device always enabled
30	NC	-
31	V_{S_LDO2}	Supply voltage for LDO2. Block directly to ground with ceramic capacitor ≥ 4.7 µF and a 100 nF capacitator as close as possible to the pin.
32	NC	-
33	SEL3_LDO2	Output voltage selectors for LDO2
34	SEL2_LDO2	
35	SEL1_LDO2	
36	NC	-
TAB	-	The TAB is connected to ground

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{S\_LDO1,2}$	DC supply voltage	-0.3 to 28	V
$V_{S\_LDO1,2}$	Single pulse/t_{max} < 400 ms “transient load dump”	40	V
$I_{S\_LDO1,2}$	Input current	Internally limited	-
$V_{O\_LDO1,2}$	DC output voltage	-0.3 to $V_{S\_LDO1,2}$ + 0.3 up to 25	V
$I_{O\_LDO1,2}$	DC output current	Internally limited	-
VIN_TRK	DC input voltage	-0.3 to 28(1)	V
$V_{Wi\_LDO1,2}$	Watchdog input voltage	-0.3 to 6.7	V
$V_{cw\_LDO1,2}$	Watchdog delay voltage	- 0.3 to 25	V
$V_{rst\_LDO1,2}$	Reset output voltage	-0.3 to 25	V
$I_{rst\_LDO1,2}$	Reset output current	Internally limited	-
$V_{cr\_LDO1,2}$	V_{cr} voltage	- 0.3 to 25	V
$V_{TW\_LDO1,2}$	Thermal warning output voltage	-0.3 to 25	V
$I_{TW\_LDO1,2}$	Thermal warning output current	Internally limited	-
V_{TC_CONF}	Thermal cluster configuration input voltage	-0.3 to 28(1)	V
$V_{sh\_ctrl\_LDO1,2}$	“Short current” control voltage	-0.3 to 4.6	V
$V_{EN\_LDO1,2}$	Enable input	-0.3 to 28(1)	V
$V_{SELx\_LDO1,2}$	Selectors input voltage	-0.3 to 28(1)	V
V_{TRK_MODE}	Selector input for tracking mode	-0.3 to 28(1)	V
V_{TRK_STAT}	Tracking status output pin	-0.3 to 25	V
VESD HBM	ESD HBM voltage level (HBM-MIL STD 883C)	±2	kV
VESD CDM	ESD CDM voltage level (CDM AEC-Q100-011)	±500	V
	ESD CDM voltage level on corner pins (CDM AEC-Q100-011)	±750	V

1. *Up to 40 V load dump.*

2.2 Thermal data

2.2.1 Thermal resistance

Table 3. Operation junction temperature

Item	Symbol	Parameter	Value(1)	Unit
A.001	$R_{thj\text{-}case}$	Junction to case thermal resistance	4.6	°C/W
A.002	$R_{thj\text{-}amb\_auto}$	Junction to ambient thermal resistance single LDO	23.5	°C/W
A.066	$R_{thj\text{-}amb\_mutual}$	Junction to ambient thermal resistance when EN1 is high and EN2 low	18	°C/W

1. *Measured on V_S.*

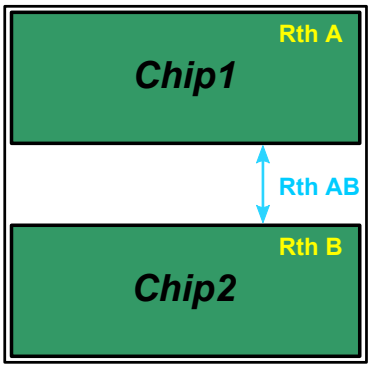
The values quoted are for PCB 129 mm x 60 mm x 1.6 mm, FR4, four layers; Cu thickness 0.070 mm (outer layers). Cu thickness 0.035 mm (inner layers), thermal via separation 1.2 mm, thermal via diameter 0.3 mm ±0.08 mm, Cu thickness on via 0.025 mm. Footprint dimension 4.1 mm x 6.5 mm.

To calculate the T_J of the device, the following cases are then taken into account:

Table 4. T_J calculation

LDO1	LDO2	ΔT_JLDO1	ΔT_JLDO2
ON	OFF	$Pd_{LDO1} * R_{thA}$	$Pd_{LDO1} * R_{thAB}$
OFF	ON	$Pd_{LDO2} * R_{thAB}$	$Pd_{LDO2} * R_{thB}$
ON	ON	$Pd_{LDO1} * R_{thA} + Pd_{LDO2} * R_{thAB}$	$Pd_{LDO2} * R_{thB} + Pd_{LDO1} * R_{thAB}$

Figure 3. R_{th_amb} junction to ambient thermal resistance



In the case of only LDO1 is switched on, the T_J will be:

$T_J = T_{amb} + (Pd_{LDO1} * R_{thA}) + (Pd_{LDO1} * R_{thAB})$

In case both LDO1 and LDO2 are switched on, T_J will be:

$T_J = T_{amb} + (Pd_{LDO1} * R_{thA} + Pd_{LDO2} * R_{thAB}) + (Pd_{LDO2} * R_{thB} + Pd_{LDO1} * R_{thAB})$

Where:

- Pd is power dissipation of the device
- R_{thA} and R_{thB} are $R_{thj\text{-}amb\_auto}$
- R_{thAB} is $R_{thj\text{-}amb\_mutual}$

2.2.2 Thermal protection

Table 5. Temperature threshold

Item	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.003	T_{prot}	Thermal protection temperature(1)		175	-	205	°C
A.004	T_{prot_hyst}	Thermal protection hysteresis		-	11	-	°C
A.005	T_J	Operating junction temperature	T_J	-40	-	175	°C
A.006	T_{stg}	Storage temperature	T_{stg}	-	-	150	°C

1. *Thermal protection is guaranteed by design and characterization.*

2.3 Electrical characteristics

Values specified in this section are for $V_{S\_LDO1,2}$ = 2.15 V to 18 V, T_j = -40 °C to +150 °C, unless otherwise stated.

Table 6. Electrical characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.007	$V_{O\_LDO1,2}$	V_{O_000}	Output voltage	$V_{S\_LDO1,2}$ = 2.15 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [0;0;0]	0.784	0.8	0.816	V
		V_{O_001}		$V_{S\_LDO1,2}$ = 2.15 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [0;0;1]	1.176	1.2	1.224	
		V_{O_010}		$V_{S\_LDO1,2}$ = 2.15 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [0;1;0]	1.470	1.5	1.530	
		V_{O_011}		$V_{S\_LDO1,2}$ = 2.45 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [0;1;1]	1.764	1.8	1.836	
		V_{O_100}		$V_{S\_LDO1,2}$ = 3.15 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [1;0;0]	2.450	2.5	2.550	
		V_{O_101}		$V_{S\_LDO1,2}$ = 3.45 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [1;0;1]	2.744	2.8	2.856	
		V_{O_110}		$V_{S\_LDO1,2}$ = 3.95 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [1;1;0]	3.234	3.3	3.366	
		V_{O_111}		$V_{S\_LDO1,2}$ = 5.65 to 18 V $I_{O\_LDO1,2}$ = 1 to 250 mA SELx_LDOy_CONF = [1;1;1]	4.9	5	5.1	
A.008	V_{O_LDO2}	Vtrk1	Output voltage tracking of LDO2 with respect to IN_TRK	$V_{O\_LDO1,2}$ = 1.5 V; 1.2 V; 0.8 V $V_{S\_LDO1,2}$ = 3.3 V (V_{S_LDO1} shorted to V_{S_LDO2}) I_{O_LDO1} = 50 mA I_{O_LDO2} = 1 mA to 100 mA	-10	-	10	mV
A.060		Vtrk2		$V_{O\_LDO1,2}$ = 5 V; 3.3 V; 2.8 V;2.5 V;1.8 V $V_{S\_LDO1,2}$ = 6 V (V_{S_LDO1} shorted to V_{S_LDO2}) I_{O_LDO1} = 50 mA I_{O_LDO2} = 1 mA to 100 mA	-20	-	20	mV
A.009	$V_{O\_LDO1,2}$	$I_{O\_LDO1,2}$	DC maximum output currents	V_O = 0.8 V; 1.2 V, 1.5 V; 1.8 V; 2.5 V; 2.8 V; 3.3 V; 5 V	-	-	250	mA
A.010	$V_{O\_LDO1,2}$	$I_{short\_LDO1,2}$	Short circuit current lower value(1)	$V_{S\_LDO1,2}$ = 4 V for $V_{o\_LDO1,2}$=3.3 V $V_{S\_LDO1,2}$ = 5.8 V for $V_{o\_LDO1,2}$= 5 V with $I_{short\_LDO1,2}$ pin connected to GND	60	110	175	mA

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.011	$V_{O\_LDO1,2}$	$I_{short\_LDO1,2}$	Short circuit current upper value	$V_{S\_LDO1,2}$ = 4 V for $V_{o\_LDO1,2}$= 3.3 V $V_{S\_LDO1,2}$ = 5.8 V for $V_{o\_LDO1,2}$ = 5 V with $I_{short\_LDO1,2}$ pin floating $I_{short\_LDO1,2}$ > $I_{O\_LDO1,2}$	270	405	540	mA
A.012	$V_{S\_LDO1,2}$, $V_{O\_LDO1,2}$	$\Delta V_{O\_LDO1,2}$/ $V_{O\_LDO1,2}$	Static line regulation	$V_{S\_LDO1,2}$ is from V_{s_low}(2) to 18 V $I_{O\_LDO1,2}$ = 1mA; 100 mA; 250 mA $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	-	1	%
		$\Delta V_{O\_LDO1,2}$/ $V_{O\_LDO1,2}$	Dynamic line regulation(3)	$V_{S\_LDO1,2}$ is from V_{s_low}(2) to 18 V T_r, f = 1 ms $I_{O\_LDO1,2}$ = 1 mA; 50 mA; 250 mA $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	-	3	%
A.013	$V_{O\_LDO1,2}$	$\Delta V_{O\_LDO1,2}$/ $V_{O\_LDO1,2}$	Static load regulation(4)	$I_{O\_LDO1,2}$ = 1 mA to 100 mA $V_{O\_LDO1,2}$ = 3.3 V $V_{S\_LDO1,2}$ = 5 V $V_{O\_LDO1,2}$= 5 V $V_{S\_LDO1,2}$ = 6 V	-	-	1	%
		$\Delta V_{O\_LDO1,2}$/ $V_{O\_LDO1,2}$	Dynamic load regulation(3)(4)	$I_{O\_LDO1,2}$ = 10 mA to 100 mA T_r, f = 10 µs $V_{O\_LDO1,2}$ = 3.3 V $V_{S\_LDO1,2}$ = 5 V $V_{O\_LDO1,2}$= 5 V $V_{S\_LDO1,2}$ = 6 V	-	-	3	%
A.014	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$V_{dp\_LDO1,2}$	Drop voltage(5)	$I_{O\_LDO1,2}$ = 250 mA $V_{O\_LDO1,2}$ = 5 V	-	-	500	mV
		$V_{dp\_LDO1,2}$		$I_{O\_LDO1,2}$ = 250 mA $V_{O\_LDO1,2}$ = 3.3 V	-	-		
		$V_{dp\_LDO1,2}$		$I_{O\_LDO1,2}$ = 250 mA $V_{O\_LDO1,2}$ = 2.8 V	-	-		
		$V_{dp\_LDO1,2}$		$I_{O\_LDO1,2}$ = 250 mA $V_{O\_LDO1,2}$ = 2.5 V	-	-		
		$V_{dp\_LDO1,2}$		$I_{O\_LDO1,2}$ = 250 mA $V_{O\_LDO1,2}$ = 1.8 V	-	-		
A.015	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	PSRR(3)	Power supply rejection ratio	V_S = 13.5 V V_O = 5 V I_O = 250 mA fr = 1 kHz	-	75(3)	-	dB
A.017	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$I_{qn\_LDO1,2}$	Current consumption with regulator disabled $I_{qn\_LDO1,2}$ = $I_{S\_LDO1,2}$ - $I_{O\_LDO1,2}$	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V EN_LDO1,2 = Low	-	-	1	µA

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.067	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$I_{qn\_LL\_LDO1,2}$	Current consumption from each V_{S_LDOx} pin with regulator enabled $I_{qn\_LL} = I_S - I_O$	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V $I_{O\_LDO1,2}$ = 0 µA	-	115	160	µA
A.018	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$I_{qn\_0\_LDO1,2}$	Current consumption from each V_{S_LDOx} pin with regulator enabled $I_{qn\_0\_LDO1,2} = I_{S\_LDO1,2} - I_{O\_LDO1,2}$	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V $I_{O\_LDO1,2}$ > 0 to 50 µA	-	140	200	µA
A.019	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$I_{qn\_50\_LDO1,2}$	Current consumption from each V_{S_LDOx} pin with regulator enabled $I_{qn\_50\_LDO1,2} = I_{S\_LDO1,2} - I_{O\_LDO1,2}$	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V $I_{O\_LDO1,2}$ = 50 mA	-	325	500	µA
A.020	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$I_{qn\_150\_LDO1,2}$	Current consumption from each V_{S_LDOx} pin with regulator enabled $I_{qn\_150\_LDO1,2} = I_{S\_LDO1,2} - I_{O\_LDO1,2}$	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V $I_{O\_LDO1,2}$ = 150 mA	-	500	700	µA
A.021	$V_{S\_LDO1,2}$ $V_{O\_LDO1,2}$	$I_{qn\_250\_LDO1,2}$	Current consumption from each V_{S_LDOx} pin with regulator enabled $I_{qn\_250\_LDO1,2} = I_{S\_LDO1,2} - I_O$	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V $I_{O\_LDO1,2}$ = 250 mA	-	0.6	1.5	mA
A.022	$V_{O\_LDO1,2}$	$V_{UVLO\_fall\_LDO1,2}$	Undervoltage lockout, falling	$V_{O\_LDO1,2}$= 0.8 V; 1.2 V; 1.5 V; 1.8 V	1.5	1.6	1.7	V
				$V_{O\_LDO1,2}$= 2.5 V; 2.8 V; 3.3 V	2.25	2.4	2.55	
				$V_{O\_LDO1,2}$= 5 V	4.5	4.8	4.98	
A.023	$V_{O\_LDO1,2}$	$V_{UVLO\ rise\_LDO1,2}$	Undervoltage lockout, rising	$V_{O\_LDO1,2}$= 0.8 V; 1.2V; 1.5 V; 1.8 V	1.7	1.8	2.1	V
				$V_{O\_LDO1,2}$= 2.5 V; 2.8 V; 3.3 V	2.6	2.7	2.8	
				$V_{O\_LDO1,2}$= 5 V	4.9	5.1	5.3	

1. *$I_{short\_LDO1,2}$ typical value of 120 mA for t = 400 µs during the power on.*
2. *V_{s_low} = 3.5 V at V_O = 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V; V_{s_low} = 5 V at V_O = 2.8 V, 3.3 V; V_{s_low} = 6 V at V_O= 5 V.*
3. *Parameters are guaranteed by design.*
4. *Referred to the Figure 29.*
5. *Considering that the minimum operating input voltage is 2.15 V, the dropout voltage ($V_{dp\_LDO1,2}$) is not defined for output voltages below 1.8 V.*

Table 7. Fast output discharge characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.024	$V_{O\_LDO1,2}$	R_{FD}	Fast discharge, pull-down resistor	$V_{S\_LDO1,2}$ = 3.95 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V EN_LDO1,2 = Low	50	75	120	Ω

Table 8. Reset characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.025	$R_{ST\_LDO1,2}$	$V_{rstl\_LDO1,2}$	Reset output low voltage	V_s = 5 V; 13.5 V R_{ext} ≥ 4.7 kΩ to $V_{O\_LDO1,2}$ $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	-	0.2xV_O	V
A.026	$R_{ST\_LDO1,2}$	$I_{rst\_lkg\_LDO1,2}$	Reset output high leakage current	$V_{rs\_LDO1,2t}$ = 0.8 V	-	-	1	µA
A.028	$R_{ST\_LDO1,2}$	$V_{O\_th\_LDO1,2}$	V_O out of regulation, low threshold	$V_{S\_LDO1,2}$ = 5 V 13.5 V decreasing $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	13.5%	10%	6.5%	Below $V_{O\_LDO1,2}$
A.064	$R_{ST\_LDO1,2}$	$V_{O\_th\_hyst\_LDO1,2}$	V_O out of regulation – low threshold hysteresis	$V_{S\_LDO1,2}$ = 5 V; 13.5 V_O increasing $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	2%	-	$V_{O\_th\_LDO1,2}$
A.031	$I_{cr\_LDO1,2}$	$I_{cr\_LDO1,2}$	Charge current	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	8	15	30	µA
A.033	RST_LDO1,2	T_{rr}	Reset reaction time	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	10	16	37	µs
A.034	RST_LDO1,2	T_{rd}	Reset delay time	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V Without external capacitor	5	16	37	µs
A.061		T_{rd}		$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V $C_{tr1,2}$ = 3.5 nF	320[1]	500	620	

1. *T_{rd}= 240 µs for V_s < 3.5 V.*

Table 9. Watchdog characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Item	Unit
A.035	$W_{i\_LDO1,2}$	V_{ih}_LDO1,2	Input high voltage[1]	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	0.7x $V_{O\_LDO1,2}$	-	-	V

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Item	Unit
A.036	$W_{i\_LDO1,2}$	V_{il}_LDO1,2	Input low voltage(1)	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	-	0.25x $V_{O\_LDO1,2}$	V
A.038	$W_{i\_LDO1,2}$	$I_{wi\_LDO1,2}$	Pull down current	$V_{Wi\_LDO1,2}$ = 3.3 V	-	6	10	µA
A.039	$V_{cw\_LDO1,2}$	$V_{wlth\_LDO1,2}$	Low threshold	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	10%	13%	16%	$V_{O\_LDO1,2}$
A.040	$V_{cw\_LDO1,2}$	$V_{whth\_LDO1,2}$	High threshold	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	44 %	47 %	50 %	$V_{O\_LDO1,2}$
A.041	V_{cw}_LDO1,2	$I_{CWc\_LDO1,2}$	Charge current	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V $V_{cw\_LDO1,2}$ = 0.1 V	5	10	20	µA
A.042	V_{cw}_LDO1,2	$I_{CWd\_LDO1,2}$	Discharge current	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V $V_{cw\_LDO1,2}$ = 2.5 V	1.25	2.5	5	µA
A.045	V_{cw}_LDO1,2	$I_{w\_off\_LDO1,2}$	Watchdog deactivation current threshold	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	0.4	1.05	1.5	mA
A.046	V_{cw}_LDO1,2	$I_{w\_on\_LDO1,2}$	Watchdog activation current threshold	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	1.8	3.35	4.8	mA

1. *Watchdog input requires a square wave signal (duty cycle of 50%).*

Table 10. Enable characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.047	EN_LDO1,2	$V_{EN\_low\_LDO1,2}$	EN_LDO1,2 input low voltage		-	-	0.6	V
A.048	EN_LDO1,2	$V_{EN\_highLDO1,2\_}$	EN_LDO1,2 input high voltage		1.5	-	-	V
A.050	EN_LDO1,2	$I_{EN\_LDO1,2}$	Pull down current	$V_{S\_LDO1,2}$ = 13.5 V	-	4	12	µA

Table 11. Output voltages selectors characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.051	SELx_LDO1,2	$V_{SELx\_low\_LDO1,2}$	SELx input low voltage		-	-	0.3	V
A.052	SELx_LDO1,2	$V_{SELx\_high\_LDO1,2}$	SELx input high voltage		0.7	-	-	V
A.053	SELx_LDO1,2	$I_{SELx\_LDO1,2}$	Pull-down current	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V	-	0.1	0.4	µA

Table 12. Tracking mode characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.069	TRK_MODE	VTRK_MODE low	TRK_MODE input low voltage		-	-	0.3	V
A.070	TRK_MODE	V TRK_MODE high	TRK_MODE input high voltage		0.7	-	-	V

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.071	TRK_MODE	ITRK_MODE	Pull-down current	$V_{S\_LDO1,2}$ = 13.5 V	-	0.1	0.4	µA
A.072	IN_TRK	$OV_{\_trk}$	IN_TRK overvoltage in tracking mode	V_{S_LDO2} = 5 V; 13.5 V V_O increasing V_{O_LDO2} = 3.3 V V_{O_LDO2} = 5 V	6.5%	10%	13.5%	Above IN_TRK
A.073	IN_TRK	$OV_{\_trk\_hyst}$	IN_TRK overvoltage hysteresis in tracking mode	V_{S_LDO2} = 5 V; 13.5 V V_O decreasing V_{O_LDO2} = 3.3 V V_{O_LDO2} = 5 V	-	1.2%	-	$OV_{\_trk}$
A.074	IN_TRK	$UV_{\_trk}$	IN_TRK undervoltage in tracking mode	V_{S_LDO2} = 5 V; 13.5 V decreasing V_{O_LDO2} = 3.3 V V_{O_LDO2} = 5 V	13.5%	10%	6.5%	Below IN_TRK
A.075	IN_TRK	$UV_{\_trk\_hyst}$	IN_TRK undervoltage hysteresis in tracking mode	V_{S_LDO2} = 5 V; 13.5 V V_O decreasing V_{O_LDO2} = 3.3 V V_{O_LDO2} = 5 V	-	1.2%	-	$UV_{\_trk}$
A.084	-	IN_trk_filt	IN_trk monitor filter time		8	16	44	µs
A.085 A.076	V_{O_LDO2}	$T_{\_detrk}$	Filtering time between a fault detection and shutdown of LDO2 in detracking	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	0	-	30	µs

Table 13. Tracking status characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.078	TRK_STAT	V_{TRK_STAT}	TRK_STAT output low voltage	V_S = 5 V; 13.5V R_{ext} ≥ 4.7 kΩ to V_{O_LDO2} V_{O_LDO2} = 3.3 V V_{O_LDO2} = 5 V	-	-	$0.2xV_O$	V
A.079	TRK_STAT	$I_{TRK\_STAT\_lkg\_LDO2}$	TRK_STAT output high leakage current	$V_{TRK\_STAT\_LDO2}$ = 0.8 V	-	-	1	µA

Table 14. Thermal warning and protection characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.054	TW_LDO1,2	$V_{TW\_low\_LDO1,2}$	Thermal warning output low voltage	R_{ext} ≥ 4.7 kΩ to $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	-	0.2x $V_{O\_LDO1,2}$	V
A.055	TW_LDO1,2	$T_{warn\_LDO1,2}$	Thermal warning temperature		140	150	165	°C
A.056	TW_LDO1,2	$T_{warn\_hyst\_LDO1,2}$	Thermal warning hysteresis		3	11	15	°C

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.065	TW_LDO1,2	$OV_{\_LDO1,2}$	$V_{O\_LDO1,2}$ over voltage	$V_{S\_LDO1,2}$ = 5 V; 13.5 V V_O increasing $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	6.5%	10%	13.5%	Above $V_{O\_LDO1,2}$
A.062	TW_LDO1,2	$OV_{\_hyst\_LDO1,2}$	V_O_LDO1,2 Over voltage hysteresis	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ decreasing $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	-	2%	-	OV_LDO1,2
A.063	TW_LDO1,2	$T_{w\_per\_LDO1,2}$(1)	Thermal warning square wave period	$V_{S\_LDO1,2}$ = 5 V; 13.5 V $V_{O\_LDO1,2}$ = 3.3 V $V_{O\_LDO1,2}$ = 5 V	160(1)	250	350	µs

1. T_{w_per} = 130 µs for V_S < 3.5 V.

Table 15. Thermal warning selector characteristics

Item	Pin	Symbol	Parameter	Test condition	Min	Typ	Max	Unit
A.057	TC_CONF	$V_{tc\_conf\_low}$	TC configuration input low voltage		-	-	0.6	V
A.058	TC_CONF	$V_{tc\_conf\_high}$	TC configuration input high voltage		1.5	-	-	V
A.059	TC_CONF	I_{tc_conf}	Pull down current	$V_{S\_LDO1,2}$ = 3.5 V; 13.5 V	-	4	12	µA

Note: All parameters are guaranteed in the junction temperature range -40 °C to 150 °C (unless otherwise specified). The device is still operative and functional at higher temperatures (up to 175 °C). Parameters limit at higher junction temperature than 150 °C may change respect to what is specified as per the standard temperature range. Device Functionality at high junction temperature is guaranteed by characterization.

All parameters are guaranteed by design for V_O not reported in test condition.

Minimum input voltage values are achievable adopting an input ceramic capacitator: C5750X7R2A475M230KA - ceramic capacitor multistrate SMD, 4.7 µF, 100 V, ±20%, X7R, C Series TDK.

2.4 Electrical characteristics curves

Figure 4. Output voltage vs T_J

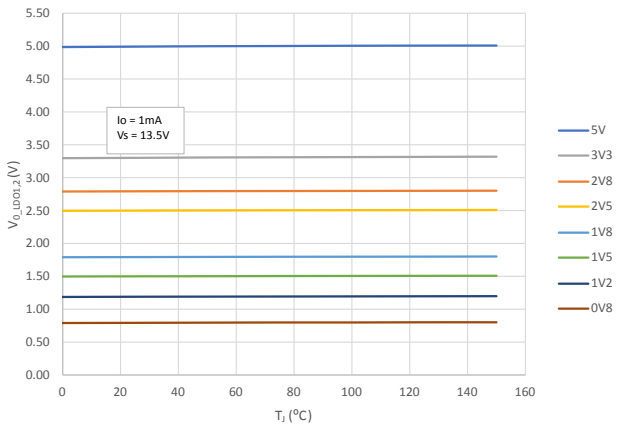


Figure 5. Output voltage vs $V_{S\_LDO1,2}$

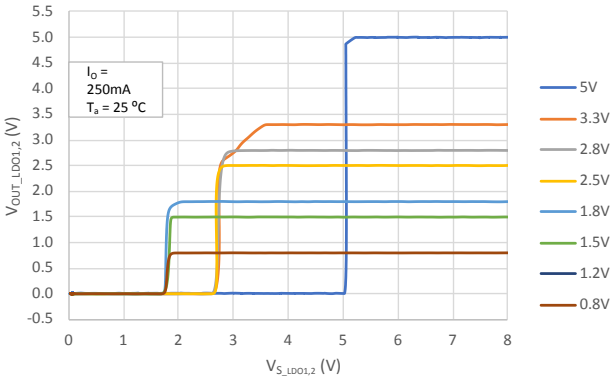


Figure 6. Drop voltage vs output current

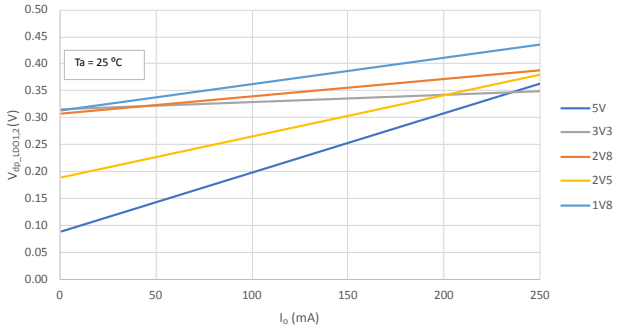


Figure 7. Current consumption vs output current

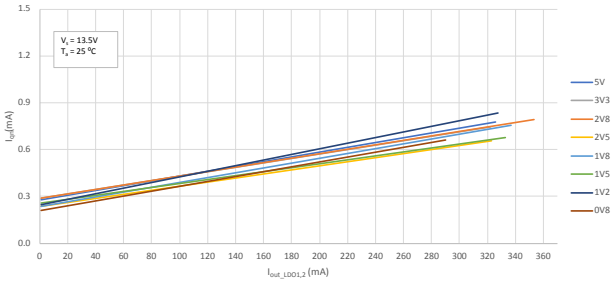


Figure 8. Current consumption vs input voltage (I_O < 1 mA)

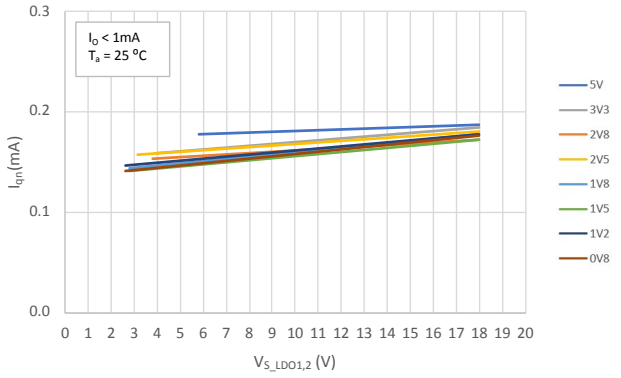


Figure 9. Current consumption vs input voltage (I_O = 50 mA)

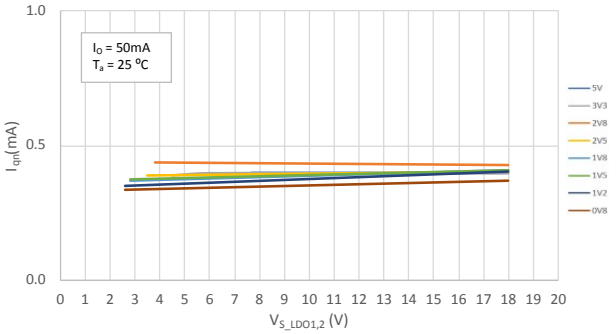


Figure 10. Current consumption vs input voltage (I_O = 150 mA)

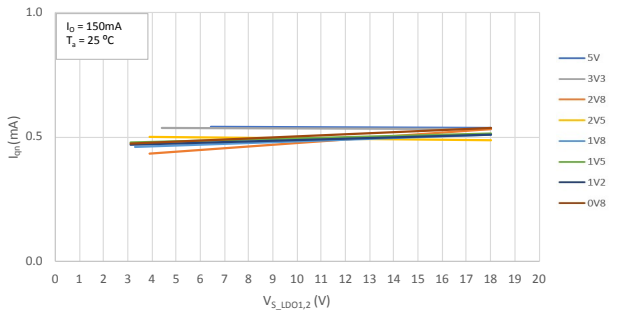


Figure 11. Short circuit current vs T_J (I_{short} pin tied to GND)

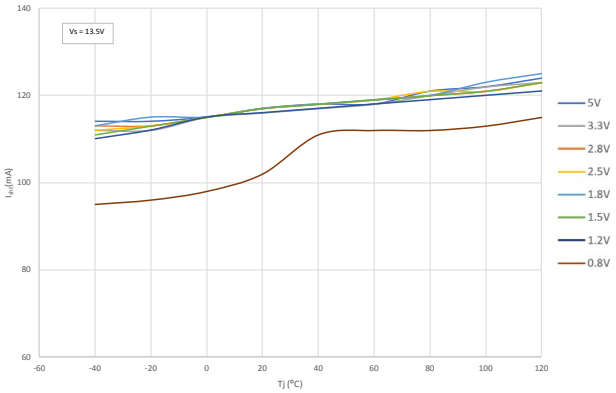


Figure 12. Short-circuit current vs T_J (I_{short} pin floating)

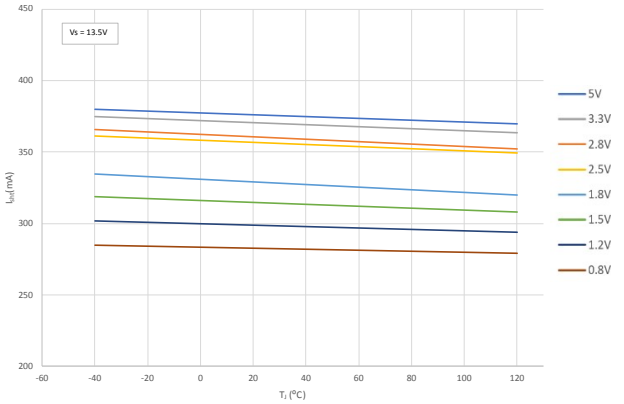


Figure 13. Short-circuit current vs input voltage

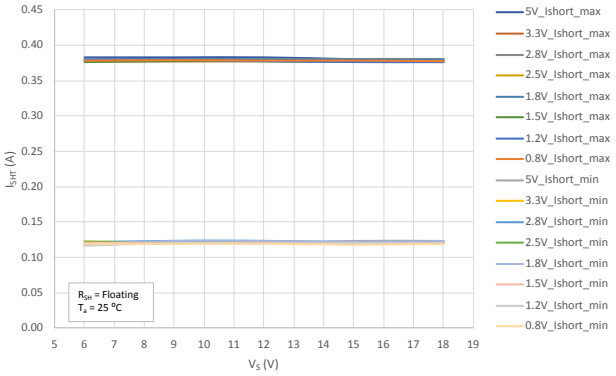


Figure 14. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 0.8 V)

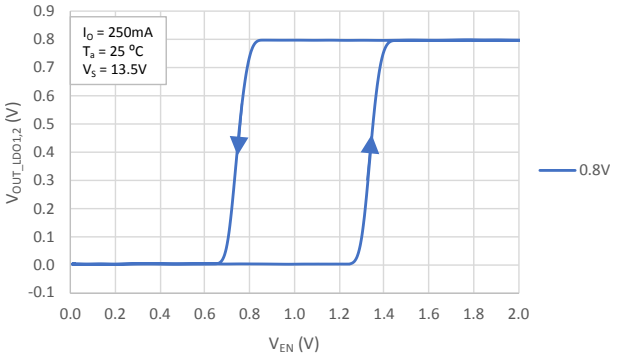


Figure 15. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 1.2 V)

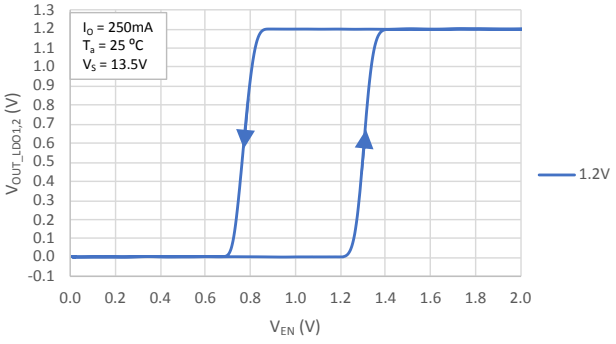


Figure 16. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 1.5 V)

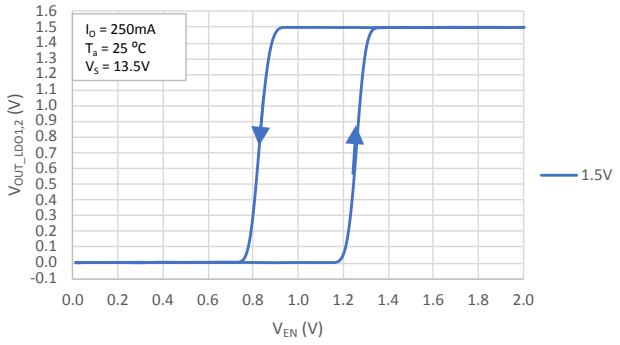


Figure 17. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 1.8 V)

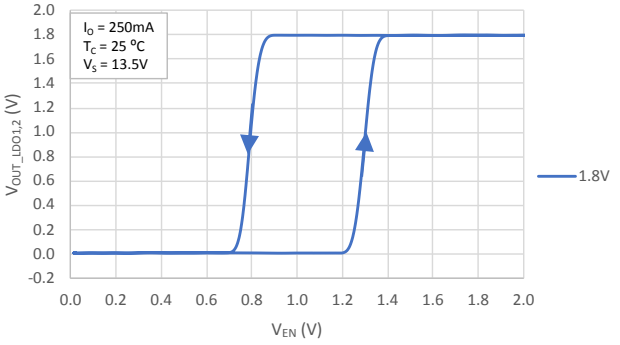


Figure 18. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 2.5 V)

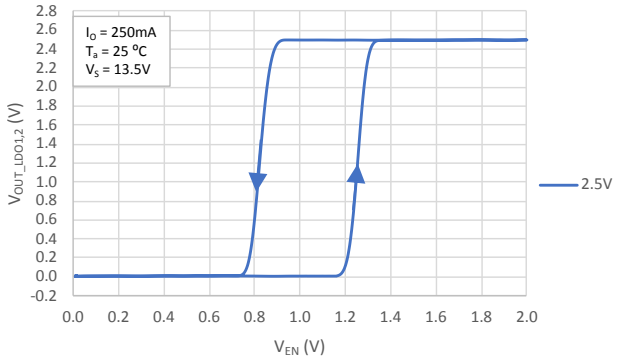


Figure 19. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 2.8 V)

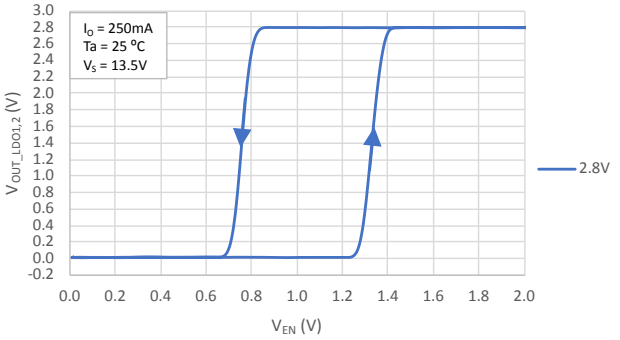


Figure 20. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 3.3 V)

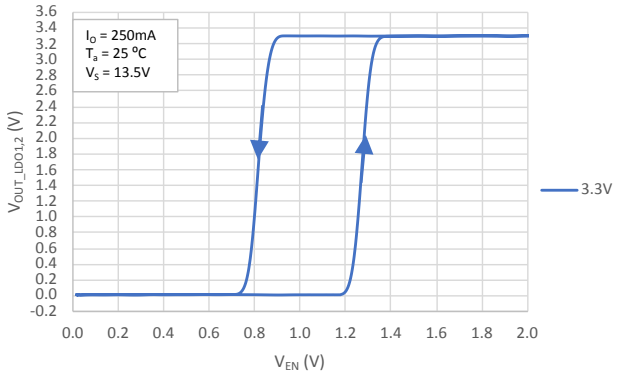


Figure 21. Output voltage vs enable voltage ($V_{O\_LDO1,2}$ = 5 V)

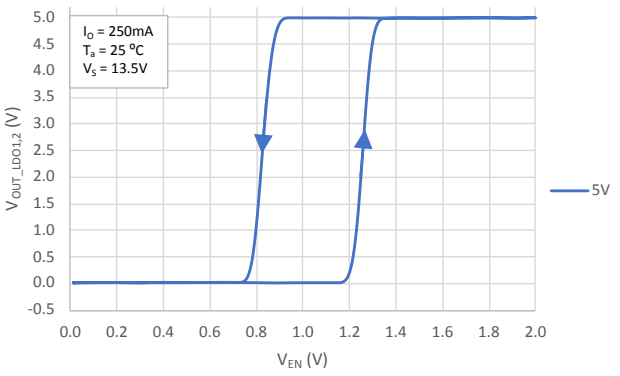


Figure 22. $V_{EN\_high\_LDO1,2}$ vs T_J

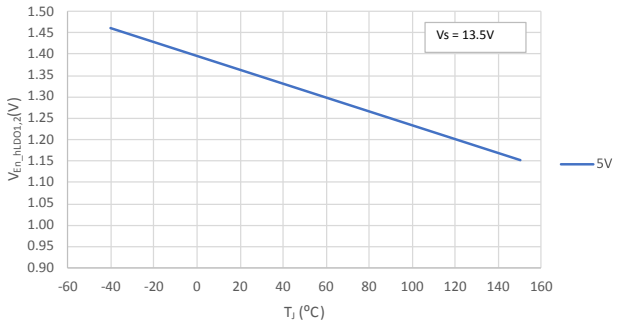


Figure 23. $V_{EN\_low\_LDO1,2}$ vs T_J

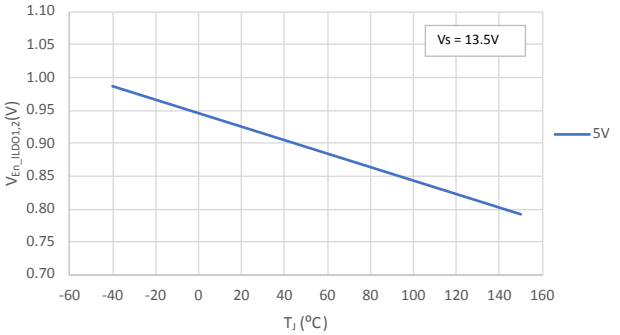


Figure 24. $V_{whth\_LDO1,2}$ vs T_J

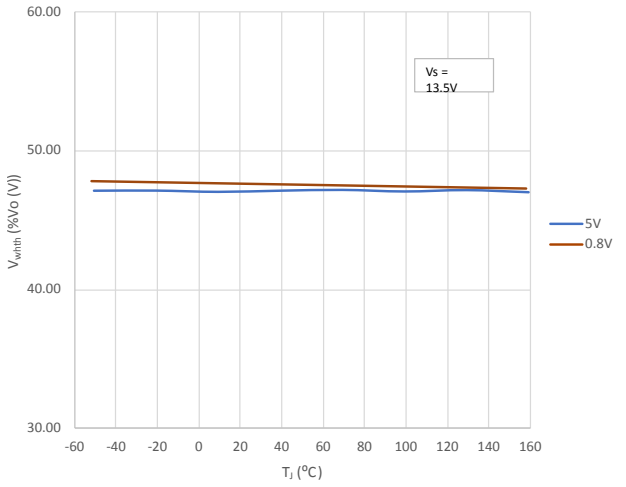


Figure 25. $V_{wlth\_LDO1,2}$ vs T_J

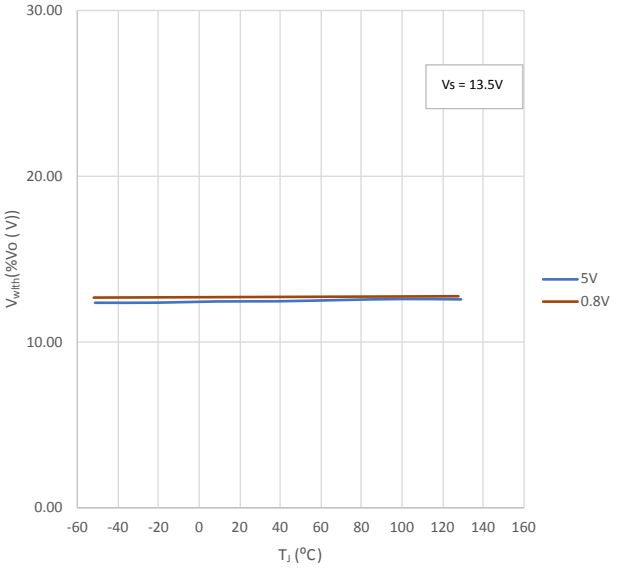


Figure 26. $I_{CWc\_LDO1,2}$ vs T_J

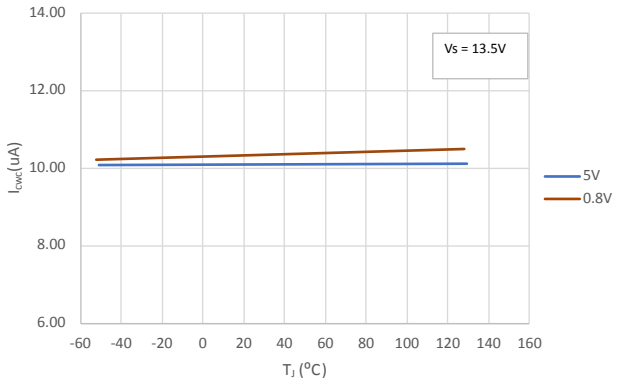


Figure 27. $I_{CWd\_LDO1,2}$ vs T_J

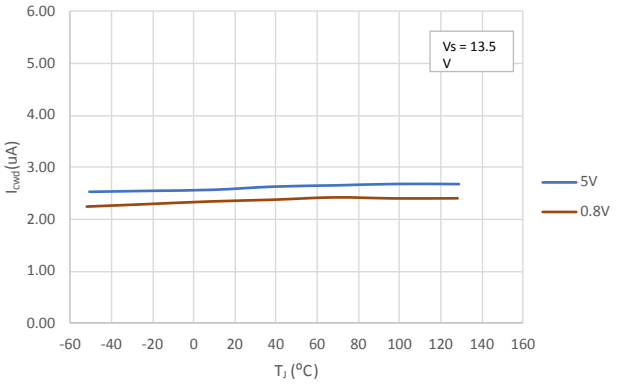


Figure 28. $I_{cr\_LDO1,2}$ vs T_J

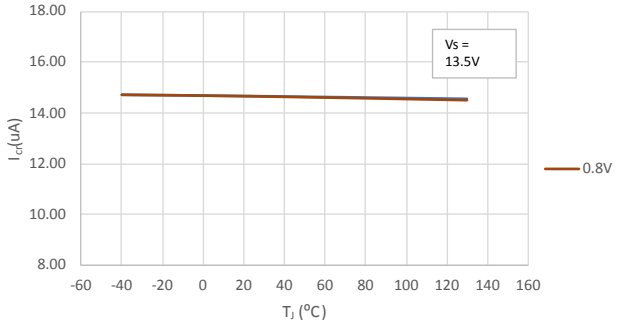


Figure 29. T_{wop} vs T_J

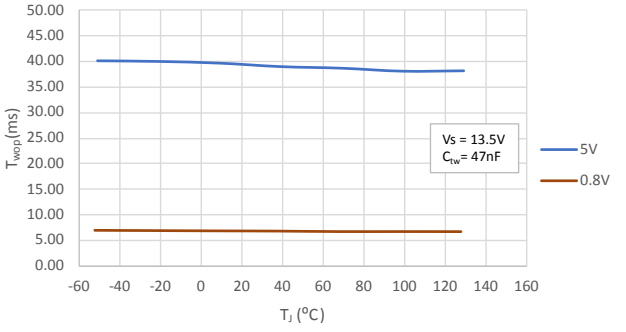


Figure 30. $I_{SELx\_LDO1,2}$ vs $V_{S\_LDO1,2}$

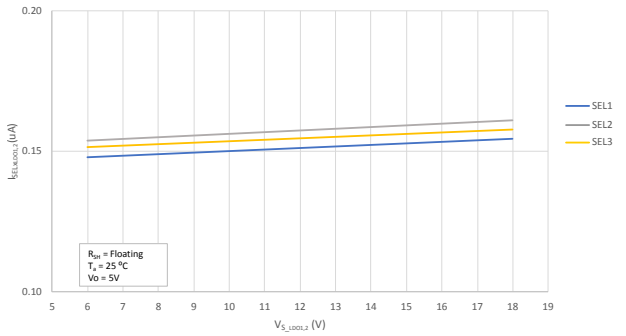


Figure 31. V_{trk} vs temperature ($V_{O\_LDO1,2}$ = 5 V, 3.3 V, 2.8 V, 2.5 V, 1.8 V)

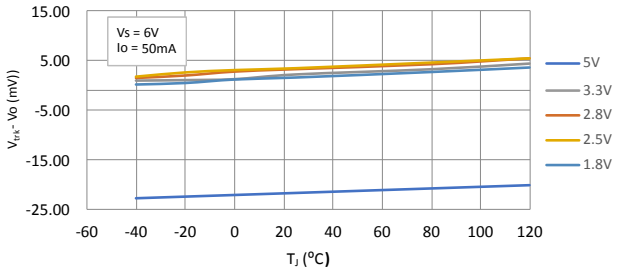


Figure 32. V_{trk} vs temperature ($V_{O\_LDO1,2}$ = 1.5 V, 1.2 V, 0.8 V)

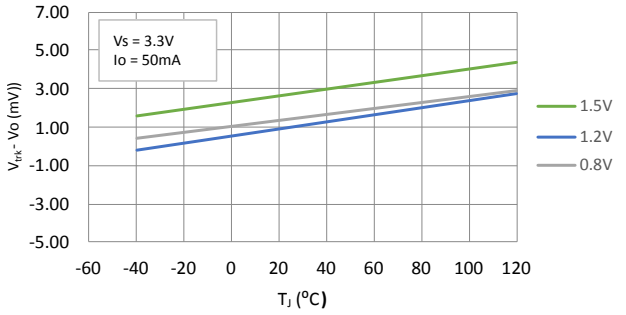
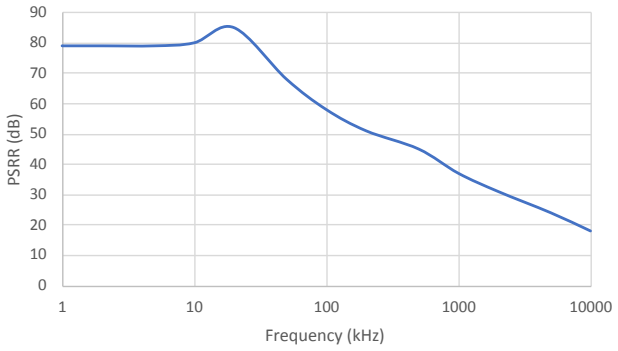


Figure 33. PSRR



3 Test circuit and waveforms plot

3.1 Load regulation

Figure 34. **Load regulation test circuit**

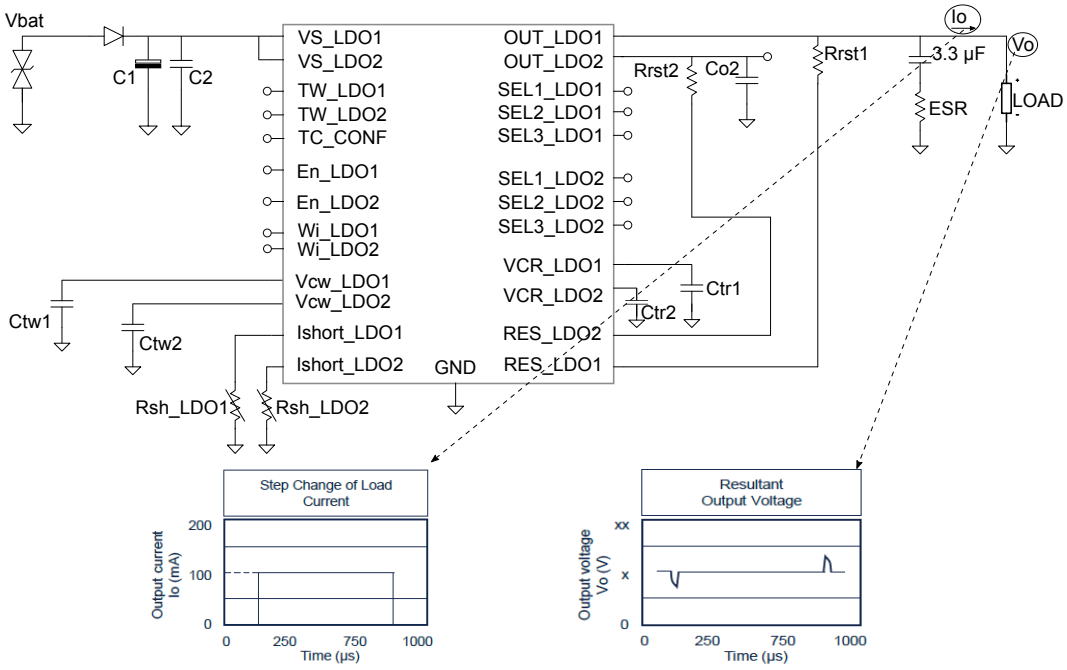


Figure 35. **Maximum load variation response (5 V)**

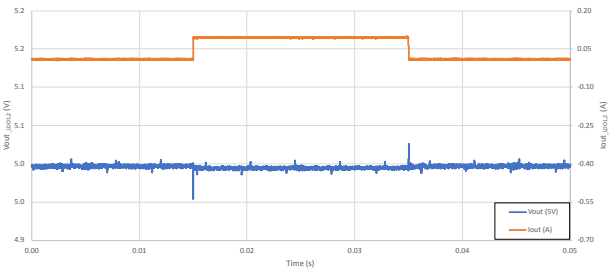
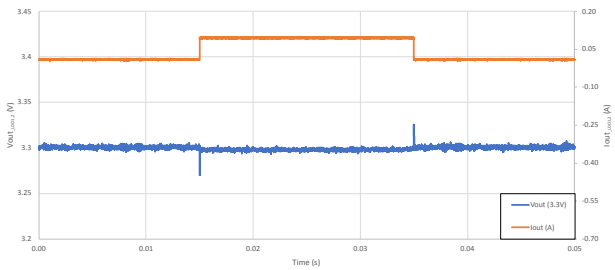


Figure 36. **Maximum load variation response (3.3 V)**



4 Application information

Figure 37. **Application schematic - Single rail line, dual outputs**

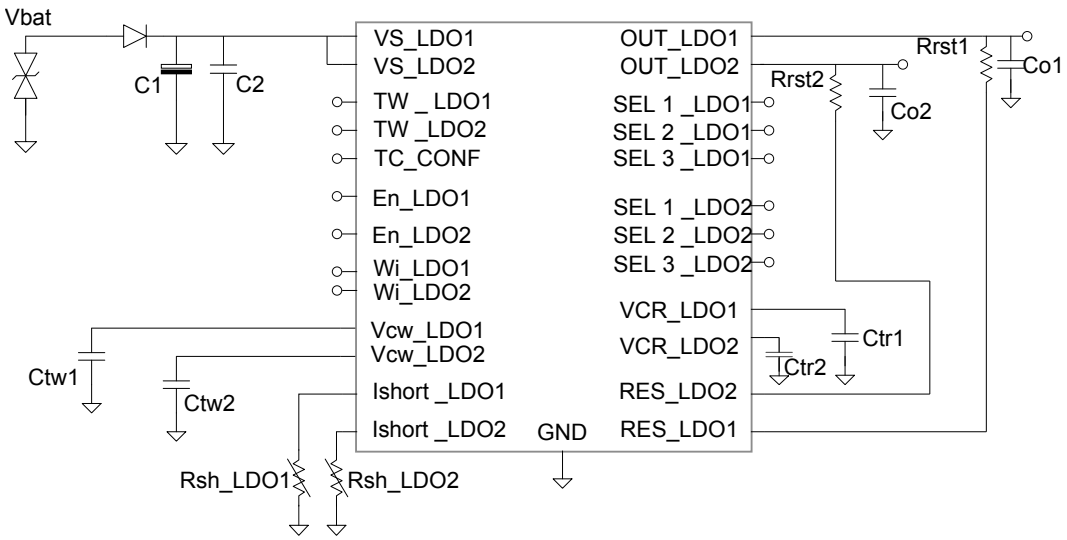


Figure 38. **Application schematic - Dual rail input lines, dual outputs**

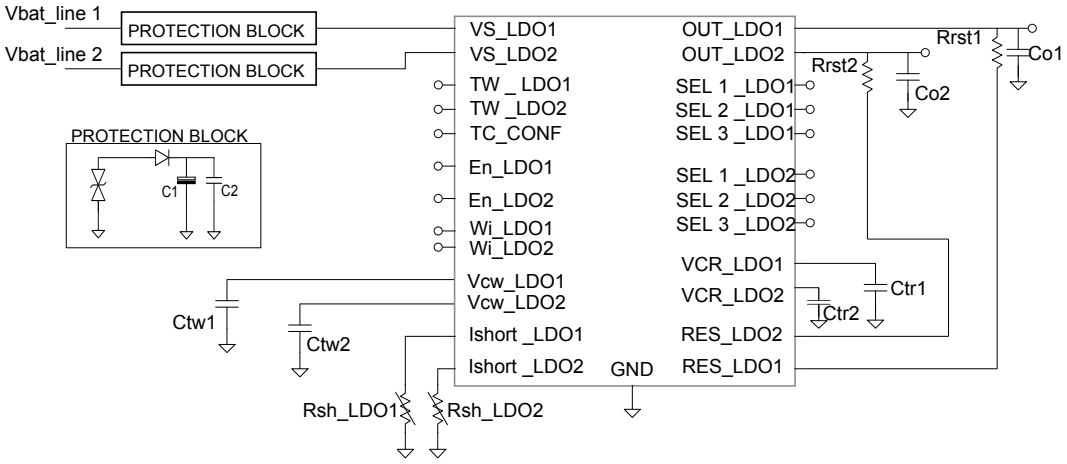
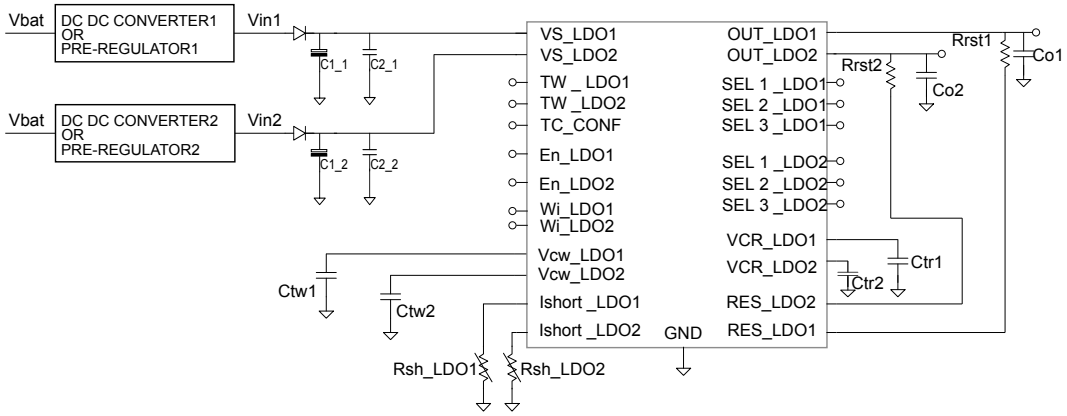


Figure 39. **Application schematic - Dual rail input lines, post regulation**



Input ceramic capacitors $C_{2\_1,2} \geq 4.7$ µF are necessary for the regulator to operate properly. The other input capacitors $C_{1\_1,2}$ can be used as backup supply for the application. The C_0 capacitors, connected to the output pins, are for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is $C_0 = 3.3$ µF.

The ESR of the SMD output ceramic capacitor has a negligible effect on the stability of the L99VRx family for capacitors with low ESR. A ceramic SMD capacitor is recommended on V_O pin.

4.1 Voltage regulator

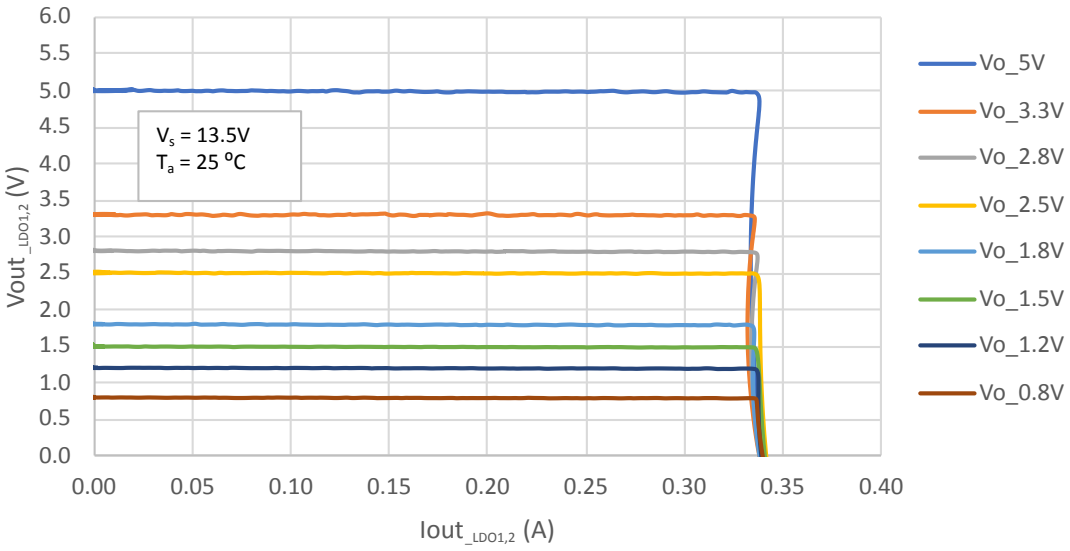
Two embedded voltage regulators use p-channel MOSFET transistors as regulating elements. With this structure, a very low dropout voltage at current up to $I_{O\_LDO1,2} = 250$ mA in split output voltages is obtained.

The high-precision of the output voltage (±2%) is obtained with a pretrimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to $I_{qn\_0\_LDO1,2} = 115$ µA only (low consumption mode). The L99VR02XP operates with reduced input voltage (post regulation) minimizing the internal power dissipation and maximizing the output current.

4.2 Output current limitation

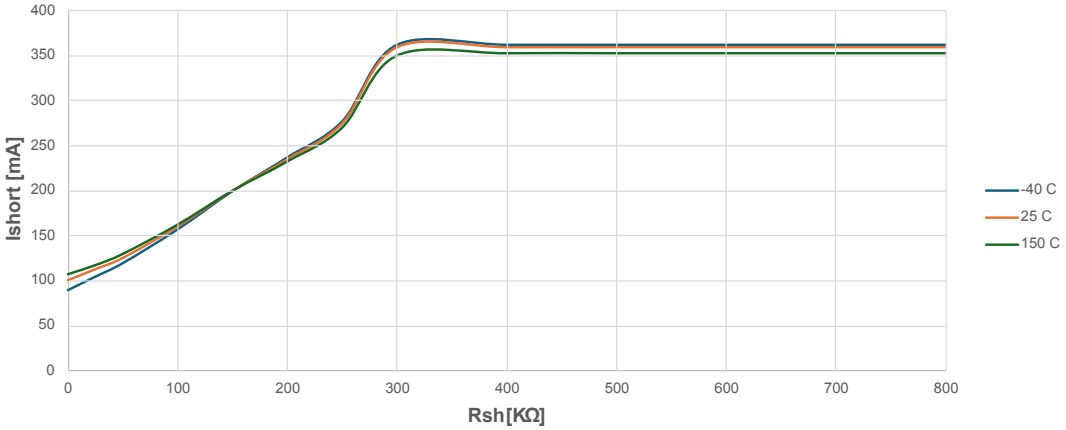
Output current limitation is present to protect the regulator and the application from overload condition, such as short to ground.

Figure 40. Behavior of regulated voltage $V_{O\_LDO1,2}$ versus output current



The I_{short} current can be set in the range between 110 mA (typ) to 405 mA (typ) through an external resistor R_{sh} connected between I_{short} pin and ground.

Figure 41. I_{short} versus R_{sh}



Open pins (no resistance on the $I_{short\_LDO1,2}$ pins), is seen as a max resistance corresponding to the maximum I_{short} current.

4.3 Output voltage selection

The L99VR02XP can provide one out of 8 different output voltages for each of the two outputs. The combination of three digital input selectors (SELx_LDOy) determines the output voltage according to the following truth table.

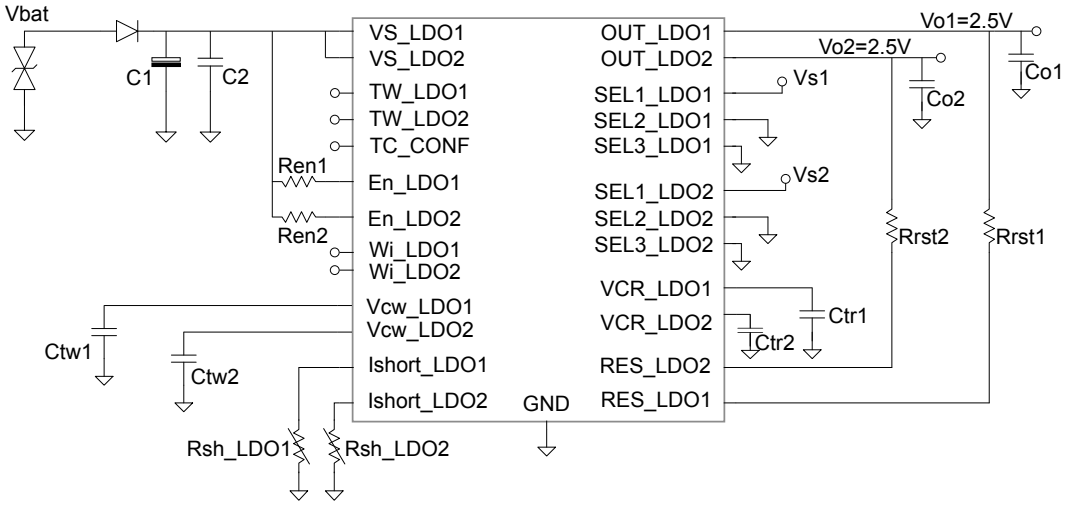
Table 16. **Truth table**

$V_{O\_LDO1,2}$	SEL1_LDOY	SEL2_LDOY	SEL3_LDOY
5	1	1	1
3.3	1	1	0
2.8	1	0	1
2.5	1	0	0
1.8	0	1	1
1.5	0	1	0
1.2	0	0	1
0.8 (Default)	0	0	0

The SELx_LDOy pins configuration is acquired at the device startup (EN_LDO1,2 from low to high) and once configuration is acknowledged, it cannot be changed until the next EN_LDO1,2 transition.

When all the pins are left not connected, the default configuration is selected.

Figure 42. **Example of output voltage selection**

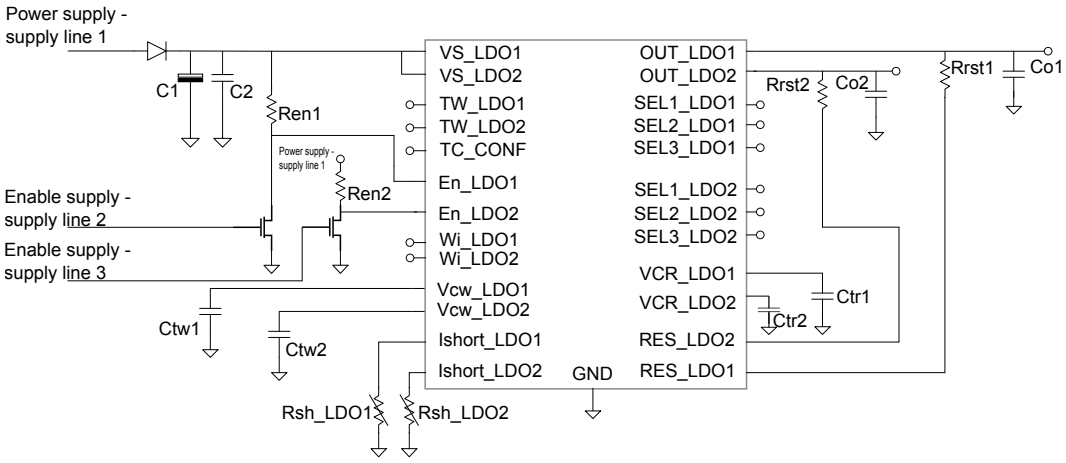


The SELx_LDOy pins are internally connected to GND via pull-down current source.

4.4 Enable

The L99VR02XP is enabled/disabled by two independently enable inputs; a high voltage signal switches the regulator ON. When the enabled pins are set to low, the outputs are switched-off, the current consumption of the device becomes as low as 1 µA and the fast output discharge circuit is activated. It may happen that the enable pins must be driven by components supplied at a voltage different from the regulator supply voltage. In this case the EN_LDO1,2 input pins must be set high only once V_S > 1.5 V. A solution to drive the enable pin is depicted in the Figure 43.

Figure 43. **Typical example of enable control**



In any case, since the enable input voltage is linked to the maximum dc supply voltage (V_{S_LDOy}) applied to the L99VR02XP (-0.3 V ≤ $V_{EN\_LDO1,2}$ ≤ + 28 V), special care must be adopted in driving EN_LDO1,2 pins to avoid exceeding the absolute maximum rating. External resistances in a range of 1 kΩ through 33 kΩ can be connected to the EN pins to further limit the current flow.

4.5 Reset

Two independently reset circuits supervise the output voltages $V_{O\_LDO1,2}$. If at least one output voltage falls below $V_{o\_th\_LDO1,2}$ then RST_LDO1,2 is pulled low with a reaction time T_{rr}.

When the output voltage rises above $V_{o\_th\_LDO1,2}$ + $V_{o\_th\_hyst\_LDO1,2}$ then RST_LDO1,2 is pulled high with a delay time T_{rd}. The delay is generated by an internal circuit.

The reset circuit is active when EN_LDO1,2 is high. Being RST_LDO1,2 an open-drain output an external resistance (R_{rst}) is needed between the RST_LDO1,2 pin and the $V_{O\_LDO1,2}$ pin. The external resistance value can be in a range between 4.7 kΩ and 20 kΩ. Leave the RST pin floating if not used. Be aware that the current flowing through the RST pin drawn from $V_{O\_LDO1,2}$ when the RST pin is pulled low may affect the watchdog activation/deactivation based on the regulator output current consumption monitoring.

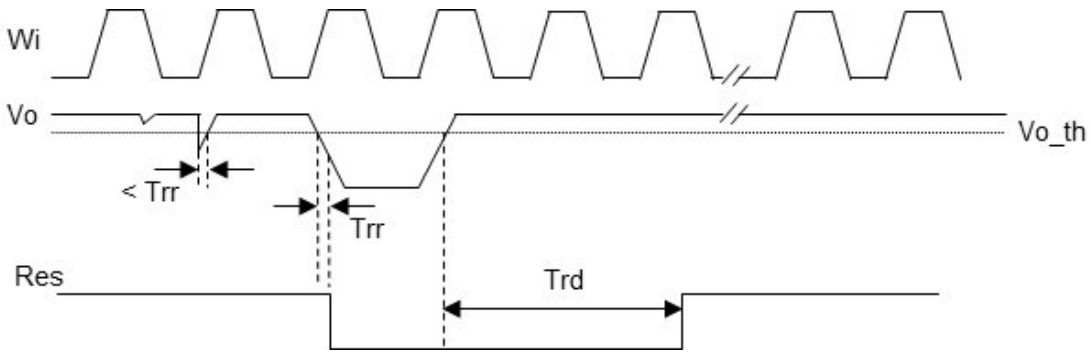
T_{rd} is set by an external capacitor in $V_{cr\_LDO1,2}$ pins, following the below rule:

$$T_{rd} = \frac{2.2\,V}{I_{cr\_LDO1,2}} C_{tr} \quad (1)$$

Where:

T_{rd} = 16 µs if $V_{cr\_LDO1,2}$ pins are floating.

Figure 44. Reset timing diagram



4.6 Autonomous watchdog

Up to two supplied microcontrollers are monitored by the watchdog inputs Wi_LDO1,2. If pulses are missing, the relative RST_LDO1,2 output pins are set to low. The watchdog timeout can be set within a wide range with the external capacitor, C_{tw}. The watchdog circuits discharge the capacitor C_{twx}, with the constant current $I_{CWd\_LDO1,2}$.

The value of the watchdog ignore time changes according to the value of the capacity used, according to the following formula:

If the lower threshold $V_{wlth\_LDO1,2}$ is reached, a watchdog reset is generated. To prevent this from happening the microcontrollers must generate a positive edge during the discharge of the capacitors before the voltage reaches the threshold $V_{wlth\_LDO1,2}$. To calculate the sawtooth period "T_{wop}", taking care that the microcontroller triggers the positive edge during the discharge phase of C_{twx} (T_d), the following equation can be used:

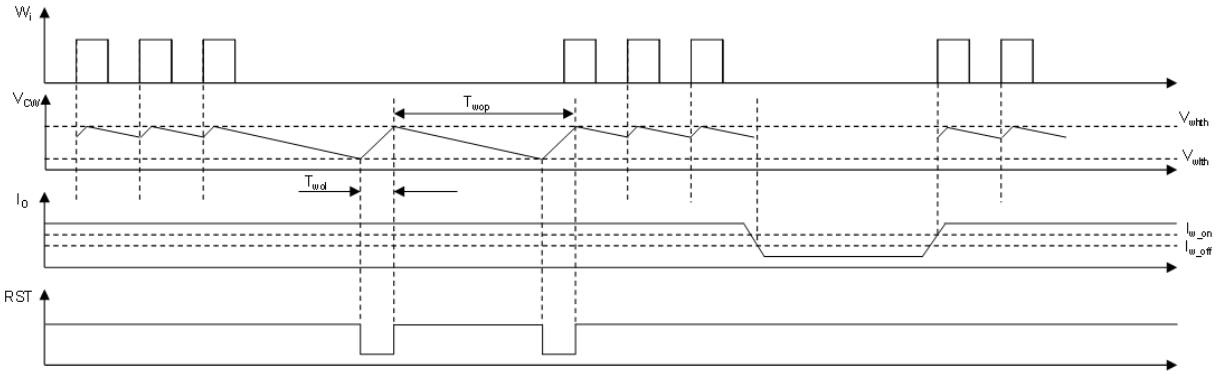
$$\left(V_{whth\_LDO1,2} - V_{wlth\_LDO1,2}\right) \times C_{tw} = I_{CWd\_LDO1,2} \times T_d \quad (2)$$

$$\left(V_{whth\_LDO1,2} - V_{wlth\_LDO1,2}\right) \times C_{tw} = I_{CWc\_LDO1,2} \times T_{wol} \quad (3)$$

$$T_{wop} = T_d + T_{wol} \quad (4)$$

Every wi-positive edge switches the current source from discharging to charging. The same happens when the lower threshold is reached. When the voltage reaches the upper threshold, $V_{whth\_LDO1,2}$, the current switches from charging to discharging. The result is a sawtooth voltage at the watchdog timer capacitor C_{twx}. If a microcontroller operates in low power mode it will not be able to generate any pulse to refresh the voltage regulator watchdog, so triggering the microcontroller reset. In such a case, to avoid generating the microcontroller reset, the watchdog functionality is automatically deactivated any time the microcontroller current consumption falls under the $I_{w\_off\_LDO1,2}$ threshold. On the other hand, when the current consumption rises above the $I_{w\_on\_LDO1,2}$ threshold the watchdog functionality is once again activated. Once the regulator is enabled for the first time, if $I_{O\_LDO1,2} < I_{w\_off\_LDO1,2}$ the watchdog will not be activated, while if $I_{O\_LDO1,2} > I_{w\_off\_LDO1,2}$ the watchdog is activated.

Figure 45. Watchdog timing diagram



Since the RST_LDO1,2 output pins are shared between the watchdog circuit and the output voltage monitoring circuit, for applications where the watchdog is not needed, to prevent the watchdog from generating RST pulses without anyway losing the reset functionality of the $V_{O\_LDO1,2}$ monitoring, the $V_{cw\_LDO1,2}$ pins have to be connected to $V_{O\_LDO1,2}$. $V_{cw\_LDO1,2}$ pins must be always tied to the ground by an external capacitor (C_{twx}) when watchdog function is used.

Note:

- *When the watchdog timer is used to and the regulator recovers from a thermal shut-down event or recovers from an output undervoltage event (including the recovery from output undervoltage event at the regulator output turning on), the reset pin might be pulled back high with a delay longer than T_{rd}, in the range between T_{rd} and T_{rd} +T_{wol} due to the watchdog that might affect the RST pin release. The watchdog will not affect the RST pin release in the case where recovering from a thermal shut-down event or recovering from an output undervoltage event (including the recovery from output undervoltage event at the regulator output turning on) the Io drops below I_{w_off} before T_{rd}. The output current Io consists in the load current, the current drawn from the RST pin and the TW pin through the pull-down resistors connected to V_O when the RST and the TW pins are asserted low and the current needed to charge/discharge the output capacitor is C_O.*
- *When the watchdog timer is used, in case of an output undervoltage event not making V_O drop to zero volt, since the watchdog will still be running during the output undervoltage condition, the first watchdog timeout after the reset pin is released coming out of the output undervoltage event might occur before expected ($0 \le Timeout \le T_{wop} - T_{wol}$).*

Table 17. Watchdog timer

Usage of watchdog timer	Connection of $V_{cw\_LDO1,2}$ pin
Watchdog timer is not used	Connect to the $V_{O\_LDO1,2}$ pin
Watchdog timer is used	Connect to an external capacitor C_{tw}

4.7 Thermal warning and thermal shutdown

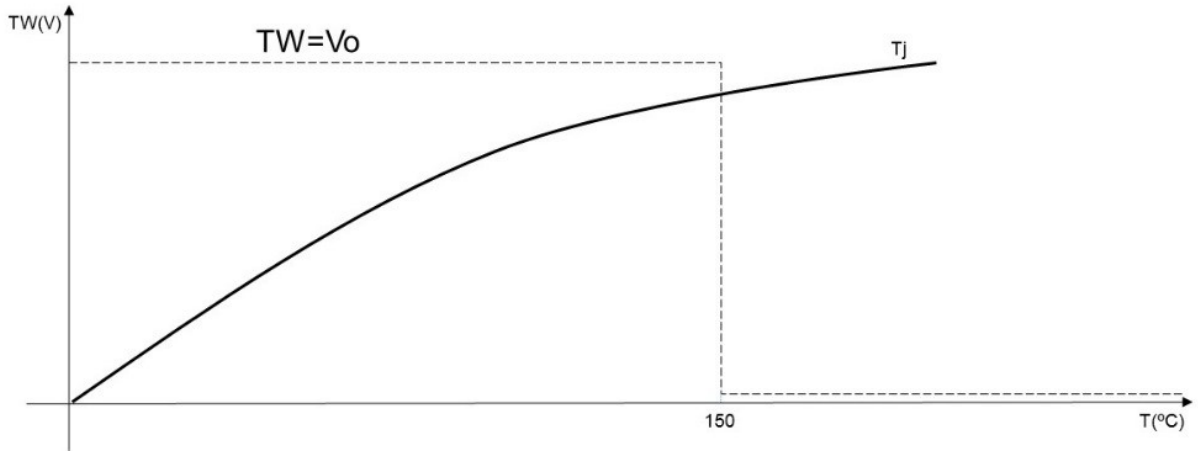
To warn the microcontroller about a severe temperature increase, two thermal warning outputs have been implemented (one for each regulator). Through TC_CONF it is possible to set the management of a thermal shutdown event.

Table 18. TC_CONF setup

Event	TC_CONF in DEFAULT conf. (TC_CONF = GND)	TC_CONF in OR conf. (TC_CONF = V_{S_LDO1})
THERMAL SHUTDOWN	LDO1 and LDO2 are fully independent of each other and monitored by two different thermal clusters In tracking mode: if LDO1 is in thermal shutdown and TRK_MODE = GND (see the Table 19), LDO2 is untied by LDO1 and keeps the normal activity. In case of TRK_MODE = V_S, LDO2 is fully independent by LDO1 and keeps the normal activity according to the behavior of an external voltage regulator	If LDO1 is in thermal shutdown, also LDO2 is switched off If LDO2 is in thermal shutdown, LDO1 keeps the normal activity
OVERVOLTAGE/ THERMAL WARNING	Events indicated respectively on the TW_LDO1 and TW_LDO2 pins	Events indicated respectively on the TW_LDO1 and TW_LDO2 pins

If a cluster of the device detects a junction temperature above $T_{warn\_LDO1,2}$, the relative advanced thermal warning (TW_LDO1,2) pin is pulled low while the specific voltage regulator and its features are still active. The TW_LDO1,2 pin returns to its high logic level (equal to $V_{O\_LDO1,2}$ output value) once the temperature falls below the threshold $T_{warn\_LDO1,2}$ - $T_{warn\_hyst\_LDO1,2}$.

Figure 46. Thermal warning diagram



When junction temperature reaches the T_{prot} shutdown threshold the device is quickly shuts-off through the internal fast output discharge circuit; to be reactivated, junction temperature has to decrease below T_{prot} - T_{prot_hyst}. Being TW_LDO1,2 open-drain outputs an external resistance (R_{TW}) is needed between the TW_LDO1,2 pins and the V_O_LDO1,2 pins. The external resistance value can be in a range between 4.7 kΩ and 20 kΩ. Be aware that the current flowing through the TW_LDO1,2 pins drawn from $V_{O\_LDO1,2}$ when the TW_LDO1,2 pins are pulled low may affect the watchdog activation/deactivation based on the regulator output current consumption monitoring. Leave floating if not used.

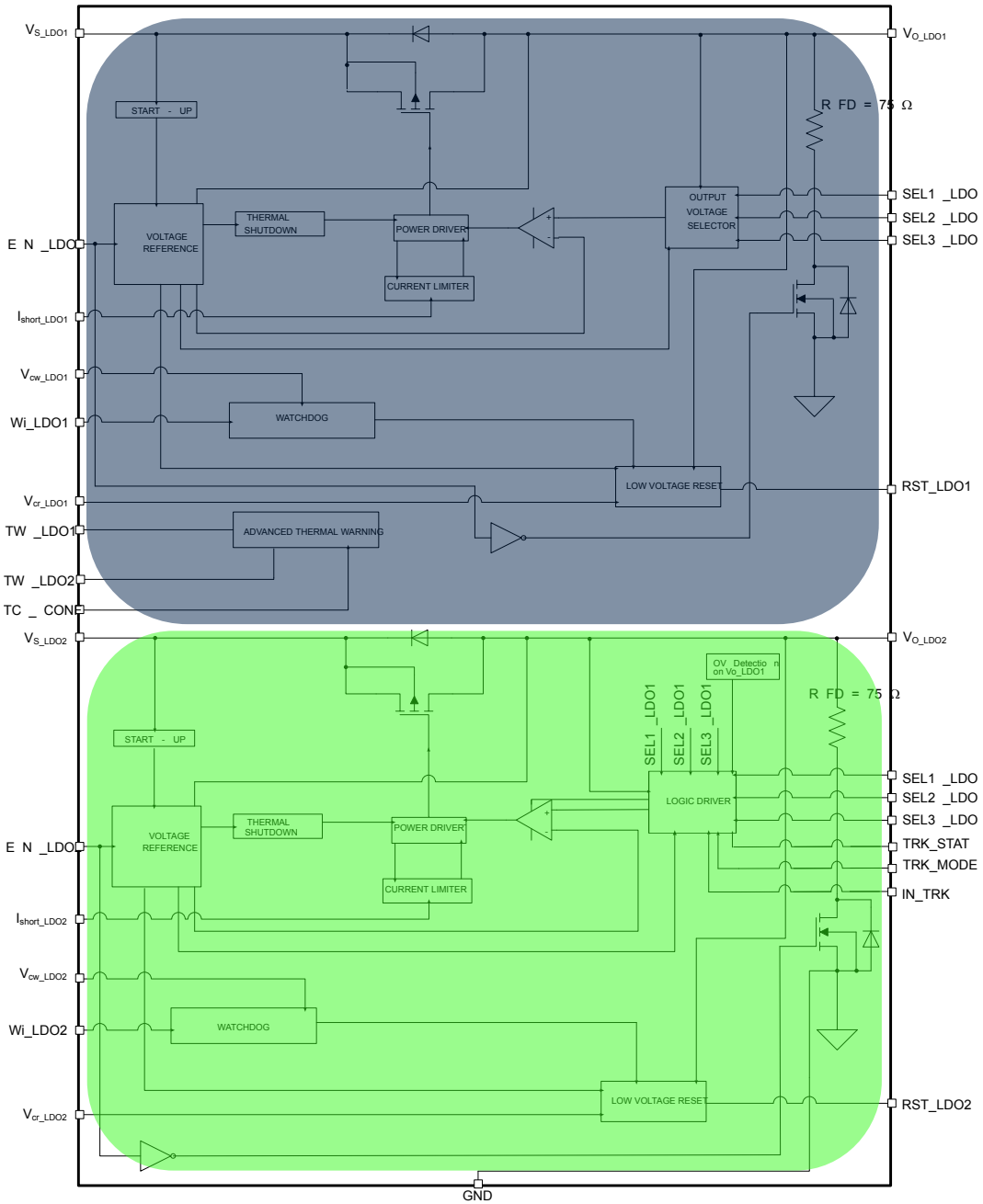
4.8 Thermal clusters

To provide an advanced on-chip temperature control, the L99VR02XP outputs are split in two different temperature clusters with dedicated thermal sensors; the sensors are suitably located on the device (see the Figure 47). If the temperature of a cluster reaches the thermal protection threshold (T_{prot}), only the relevant output is turned off while the other output remain active.

Thermal clusters can be configured according to the Table 16 using TC_CONF pin:

- "OR" mode (TC_CONF = V_{S_LDO1}): two clusters are linked to each other;
  - If LDO1 is in thermal shutdown, LDO2 also is switched off.
  - If LDO2 is in thermal shutdown, LDO1 keeps the normal activity.
- "DEFAULT" mode (TC_CONF = GND): only the cluster which reached protection temperature is switched off;
  - LDO1 and LDO2 are fully independent of each other and monitored by two different thermal clusters.
  - In tracking mode: if LDO1 is in thermal shutdown and TRK_MODE = GND (see the Table 19), LDO2 is untied by LDO1 and keeps the normal activity.

Figure 47. Thermal clusters identification

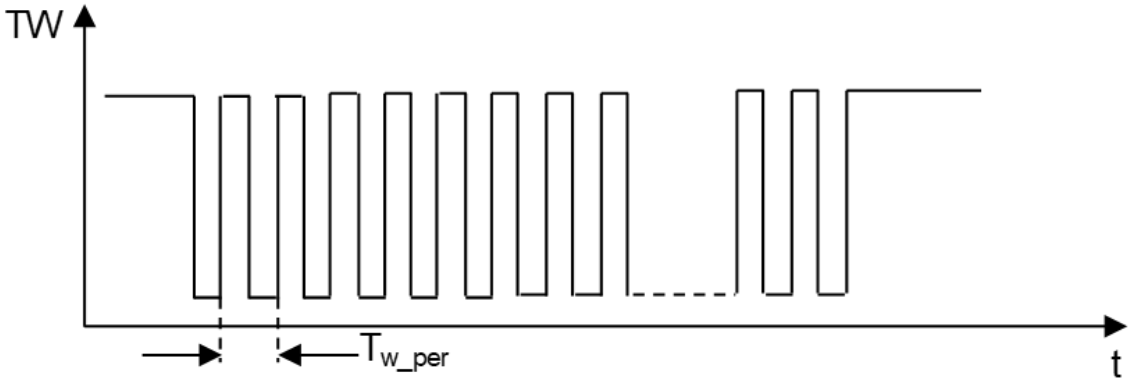


4.9 Overvoltage detection by advanced thermal warning read-out

The TW_LDO1,2 pins also provide diagnostics about output overvoltage (OV_LDO1,2); to distinguish between a thermal warning event and an output overvoltage event, two different signals are generated at the same TW_LDO1,2 output pins. How reported in the Section 4.7: Thermal warning and thermal shutdown a thermal warning event detection sets the TW_LDO1,2 pins LOW, instead an overvoltage event generates a square wave at the TW_LDO1,2 pins (see the Figure 48).

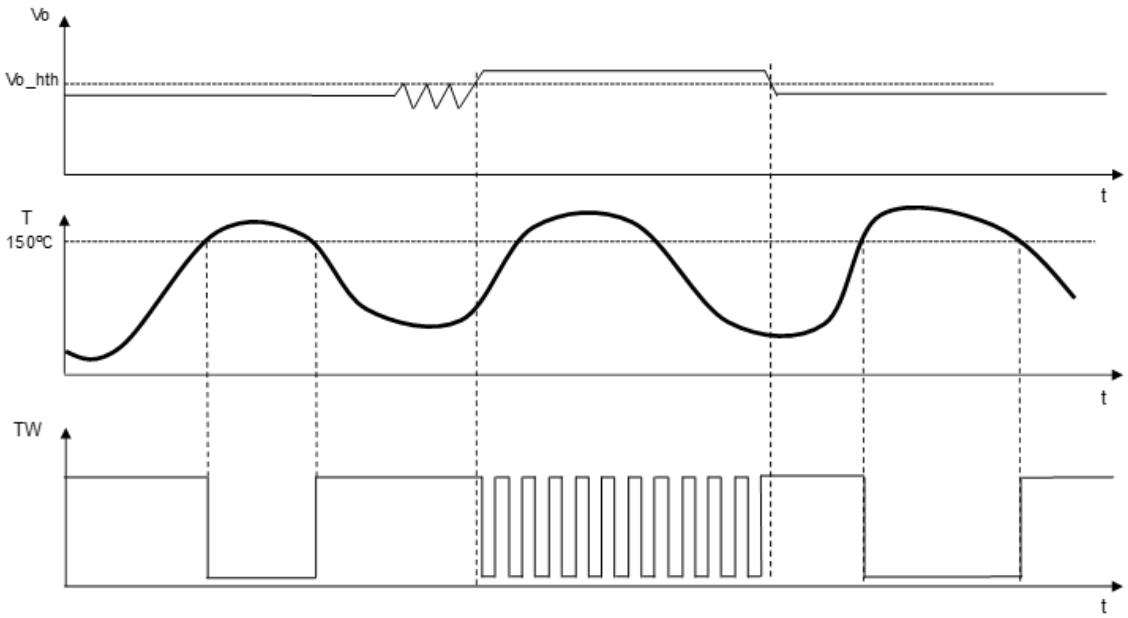
Overvoltage detection has a higher priority than thermal warning detection so that concurrence of thermal warning and over voltage events lead to a square wave like in the case of overvoltage detection (as shown in the Figure 48).

Figure 48. Square ware on TW_LDO1,2 pins generated during an overvoltage



A typical example of over temperature and overvoltage management failures is depicted in the Figure 49.

Figure 49. Warning signal caused by overvoltage and thermal warning on TW_LDO1,2 pins



4.10 Fast output discharge

To assure a quick discharge of the external capacitors tied on the output pins down to around 1.3 V the L99VR02XP uses two internal pull-down circuits. When the EN_LDO1,2 pins go low, during thermal shut-down and during undervoltage lockout, the output currents flow through the pull-down resistors of the fast output discharge circuit to the ground. The fast output discharge feature is available for the output voltages $V_{O\_LDO1,2}$ = 2.5 V (SELx = [1;0;0]) $V_{O\_LDO1,2}$ = 2.8 V (SELx = [1;0;1]) $V_{O\_LDO1,2}$ = 3.3 V (SELx = [1;1;0]) and $V_{O\_LDO1,2}$ = 5 V (SELx = [1;1;1]).

4.11 Automatic voltage (de)tracking of LDO1 or tracking of an external LDO

Voltage (de)tracking is a solution adopted when long cable supplies off-board loads with voltage regulators located on the main module. Under that operative condition short to GND and short to battery protection have to be granted to contrast electrical failures caused by damaging of the cable. Moreover, to guarantee high accuracy of data acquisition by microcontrollers, a very low discrepancy between the rails on-board and off-board is assured.

In L99VR02XP, LDO2 can be a tracker of LDO1 or an external voltage regulator.

This function is enabled by TRK_MODE pin, IN_TRK pin and TRK_STAT, according to the following table:

Table 19. Tracking mode configuration

Pin	Function
TRK_MODE = GND IN_TRK = LDO1 TRK_STAT = High	LDO2 automatically trackers LDO1 if SELx_LDO1 = SELx_LDO2 in case of SELx_LDO1 ≠ SELx_LDO2, LDO2 becomes a fully independent regulator.
TRK_MODE = V_S IN_TRK = external LDO TRK_STAT = High	LDO2 trackers of an external voltage regulator output. The user MUST guarantee the same rails for the external output voltage regulator and LDO2. Also, if SELx_LDO1 = SELx_LDO2 such internal voltage regulators (LDO1 and LDO2) are always untied.
TRK_MODE = V_S IN_TRK = GND TRK_STAT = Low	LDO2 works as a fully independent regulator.

The TRK_STAT pin is required to communicate to the MCU, if LDO2 is in tracking mode or working as an independent regulator.

During the startup phase (soft-start), if the tracking mode is disabled or LDO2 is in UV/OV the TRK_STAT pin is set low.

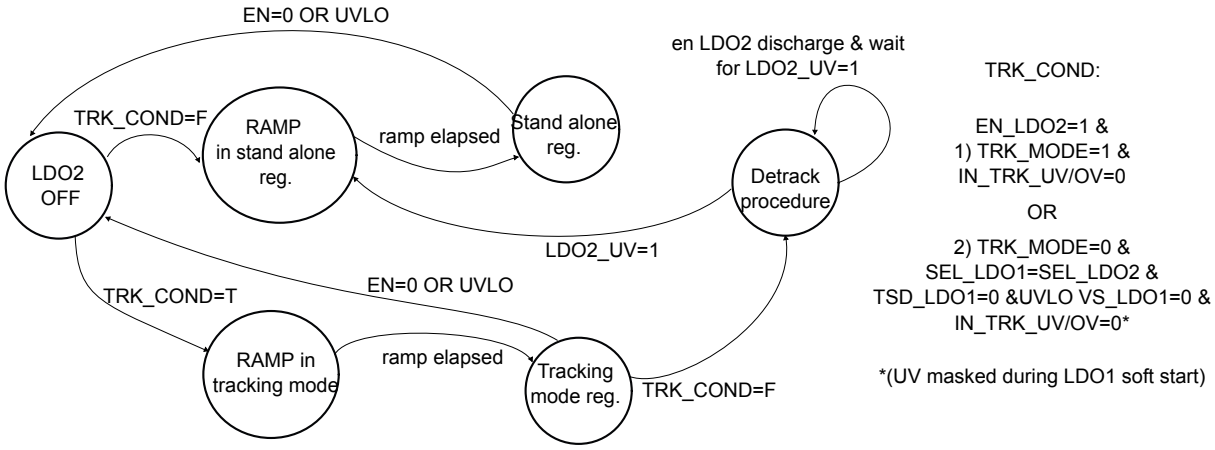
After startup, without UV/OV faults, when the tracking mode is activated the TRK_STAT pin goes high.

If the device is configured with LDO2 tracker of LDO1 and the soft start signal of LDO1 is high (soft start phase in progress), the tracking comparators are ignored to avoid unwanted transient effects during standard startup in the tracking with LDO1.

Tracking mode = 1 → If V(IN_TRK) and all other conditions are correct when LDO2 is enabled, tracking mode is enabled otherwise it is disabled during all the LDO2 soft start.

Tracking mode = 0 → If V(IN_TRK) and all the other conditions are correct OR if V(IN_TRK) is in UV condition but softstart in ongoing on LDO, the LDO2 is powered un in tracking. Otherwise the power-up is in standalone regulation mode.

Figure 50. Finite state machine



In tracking mode, by LDO1 or an external regulator, in case of thermal shutdown which occurs on L99VR02XP or LDO1 or undervoltage or overvoltage events detected on IN_TRK pin, LDO2 automatically goes in detracking mode. In such case LDO2 is switched-off (V_{O_LDO2} = 0 V) in T_detrk time and resumes with soft start and works as an independent regulator.

To activate the tracking functionality of the LDO2 again, it is necessary to reactivate the device with the EN. Before activating LDO2 for tracking functionality, it is important that the reference to be tracked is stable, to avoid detracking.

Figure 51. Power-up when LDO2 is tracker of LDO1

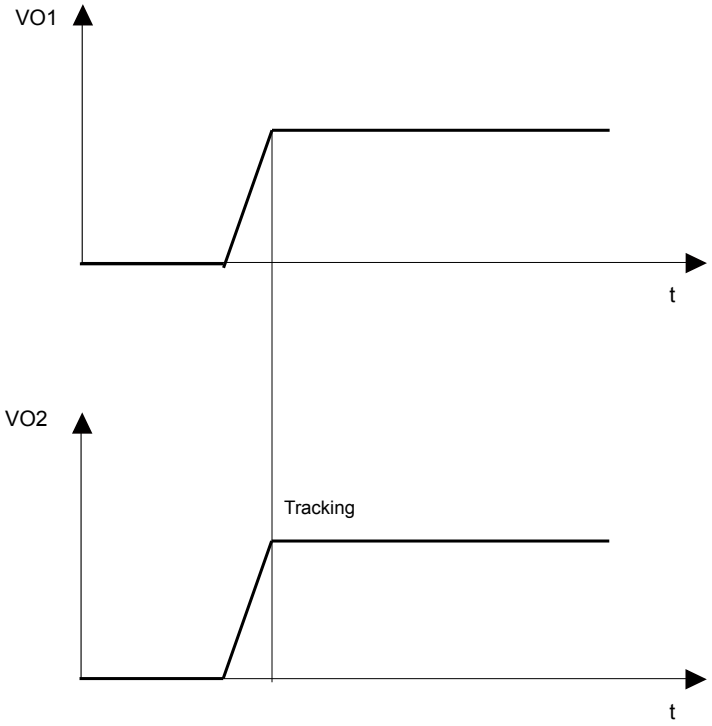


Figure 52. **Power-up when LDO2 is tracker of external regulator**

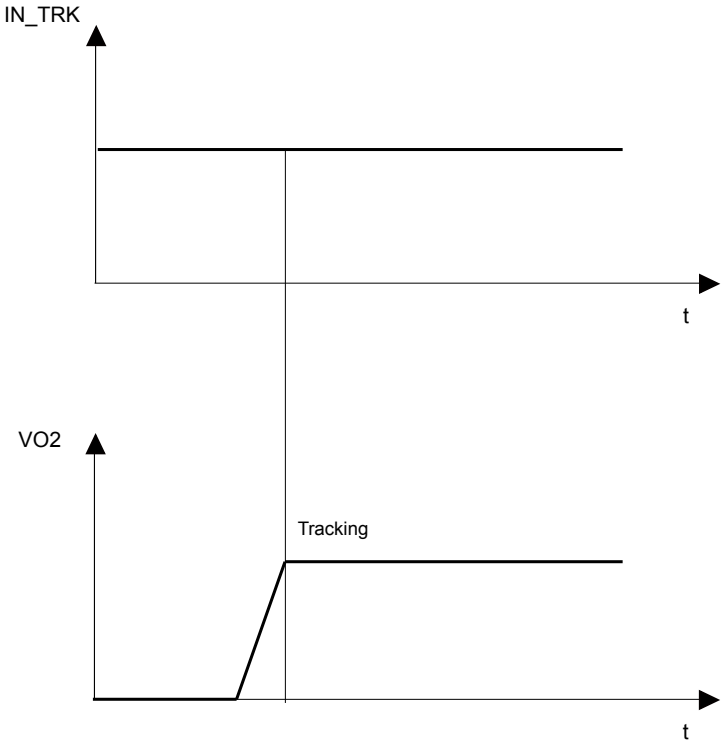


Figure 53. **Detracking timing diagram in case of UV**

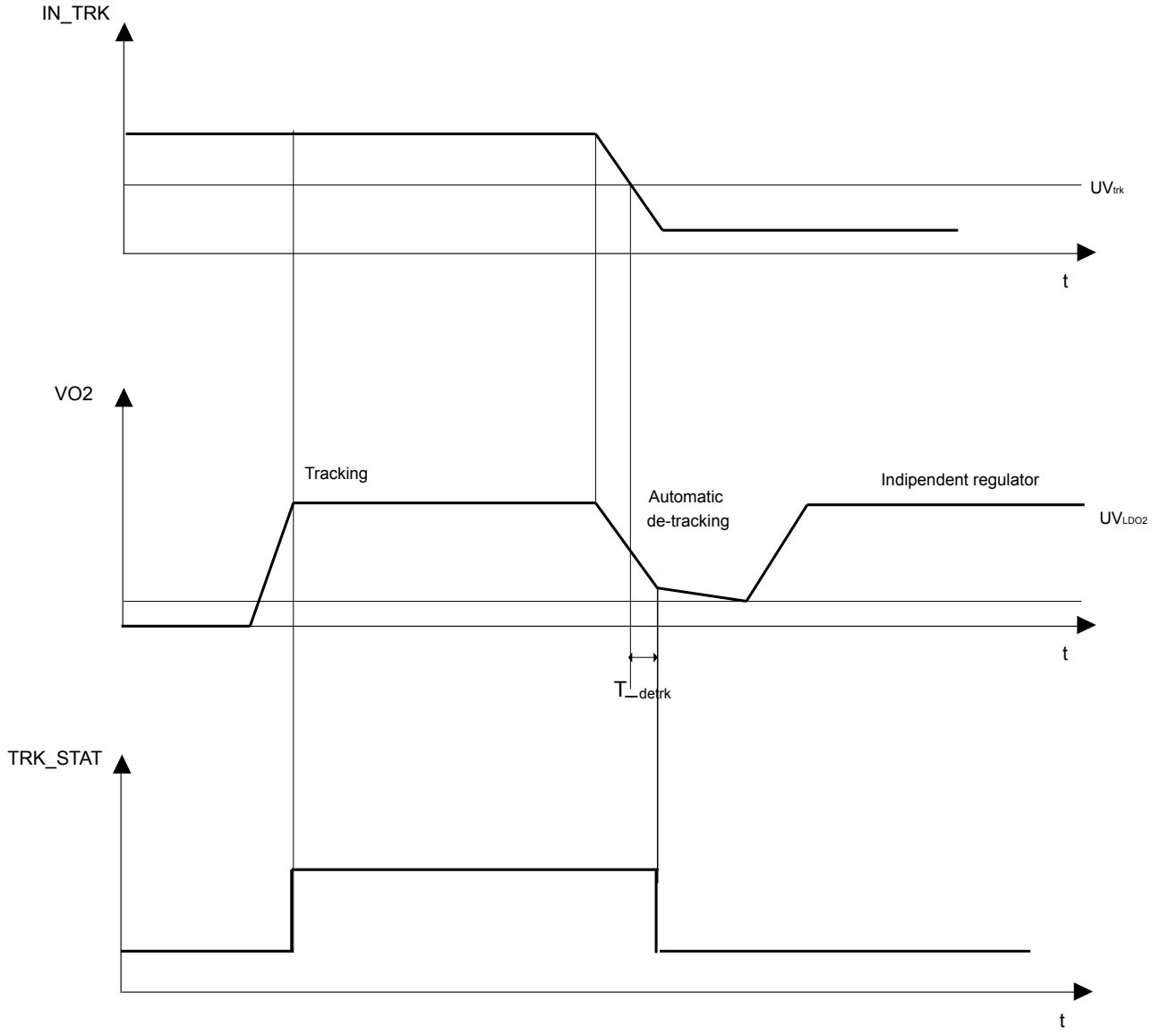


Figure 54. **Detracking timing diagram in case of OV**

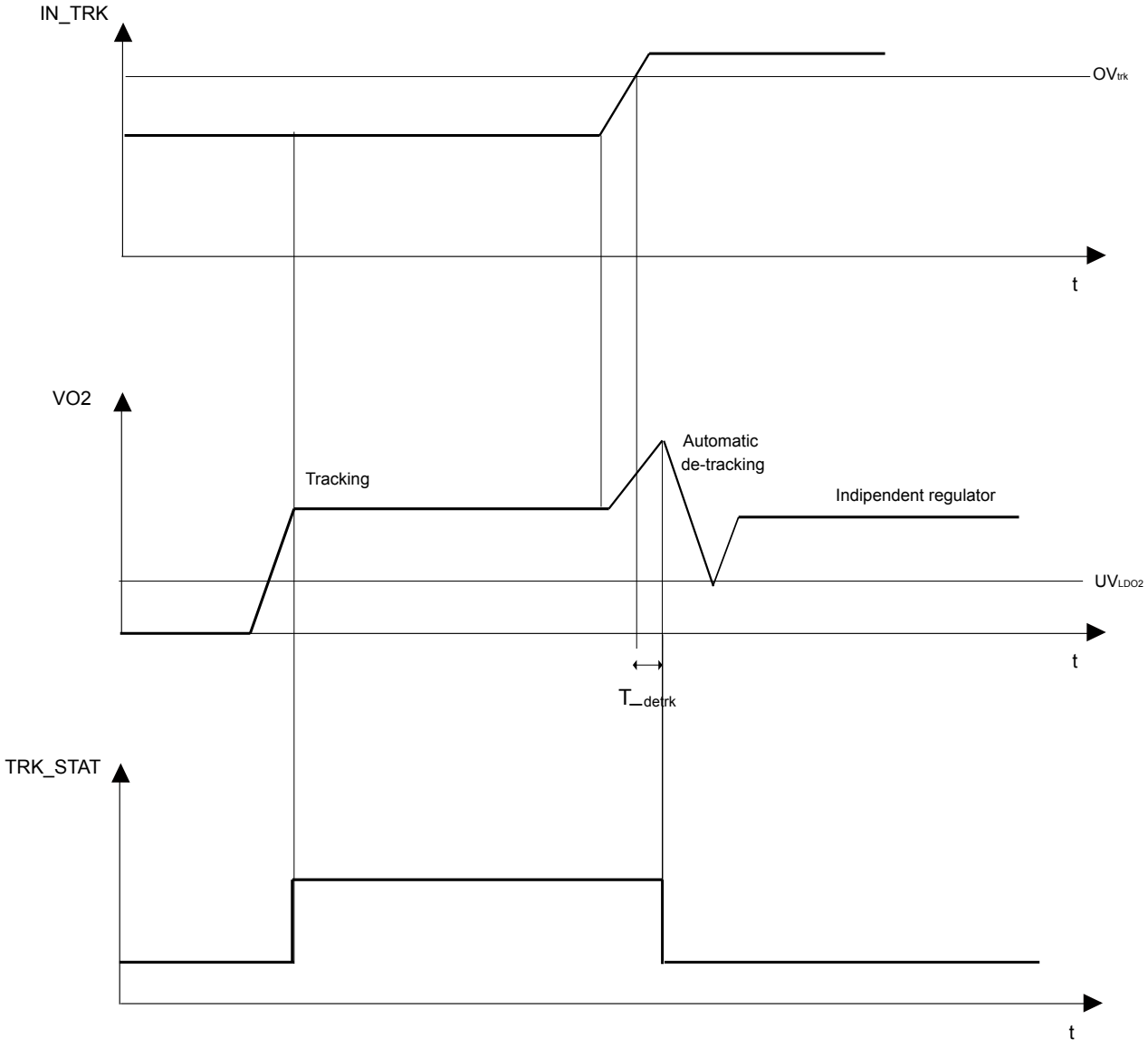
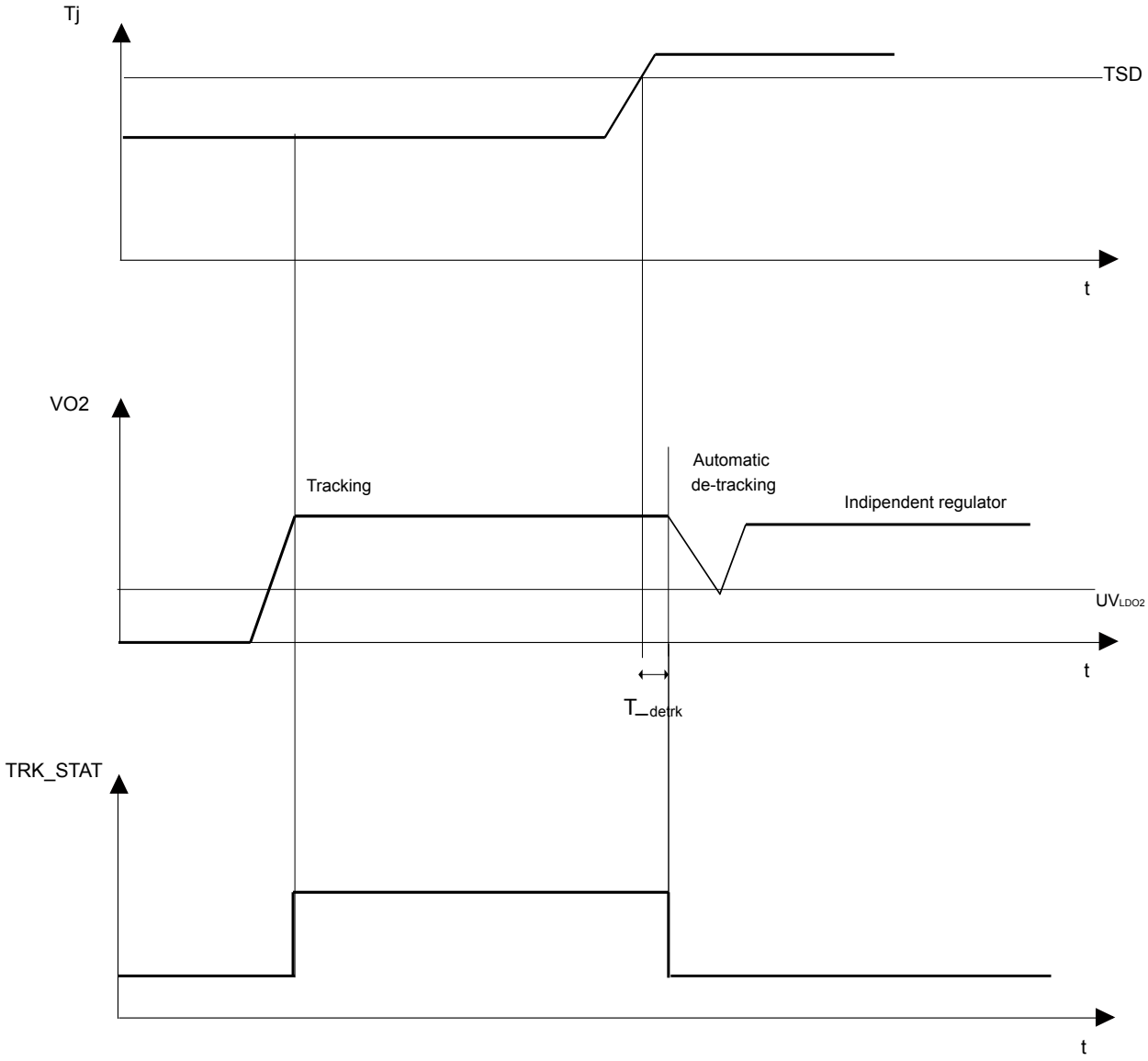


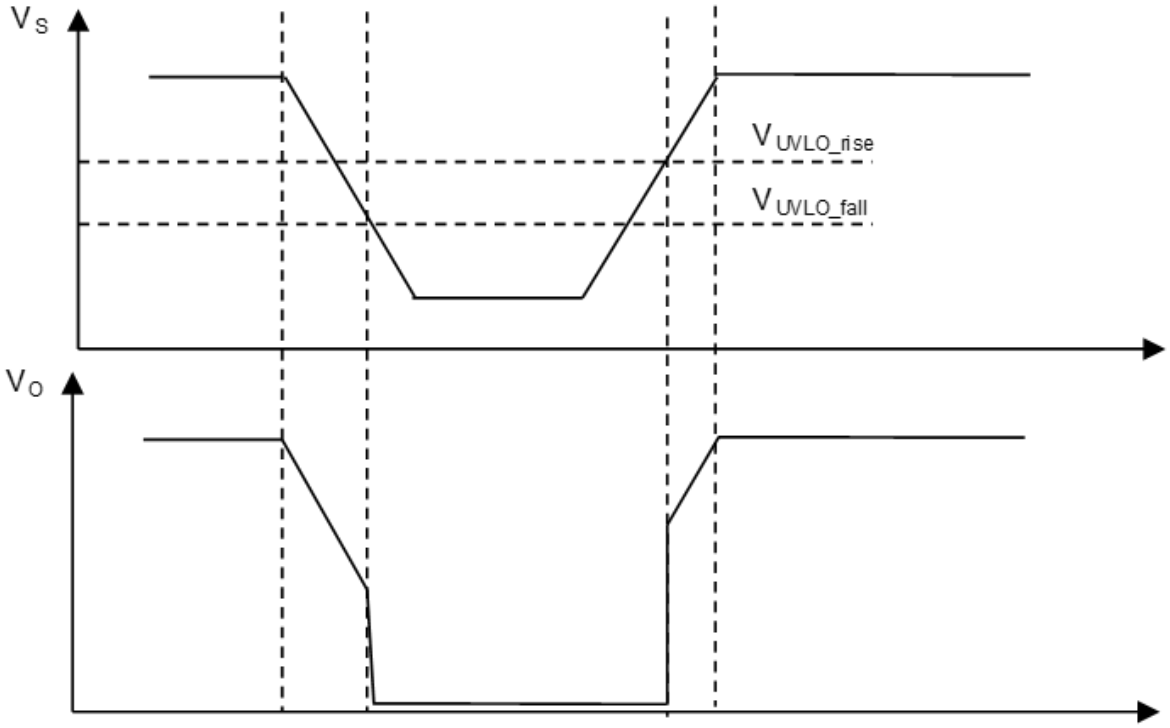
Figure 55. **Detracking timing diagram in case of thermal fault**



4.12 Undervoltage lockout (UVLO)

The undervoltage lockout (UVLO) circuit allows a fast regulating element to turn-off (activating the internal fast output discharge circuit) if the input voltage drops below the threshold, VUVLO_fall, avoiding so undesired unknown output state during low input voltage. When the input voltage is above the VUVLO_rise threshold, the regulating element is again turned on.

Figure 56. Undervoltage lock out on output voltage



4.13 Support to ISO26262

Even if not designed as a safety hardware element, the device contains some features that can be used to support applications that need to fulfill functional safety requirements. Analysis of the IC's capability to reach the required safety level, should be made at system level under user responsibility.

The following safety mechanisms have been implemented:

Table 20. Implemented safety mechanism

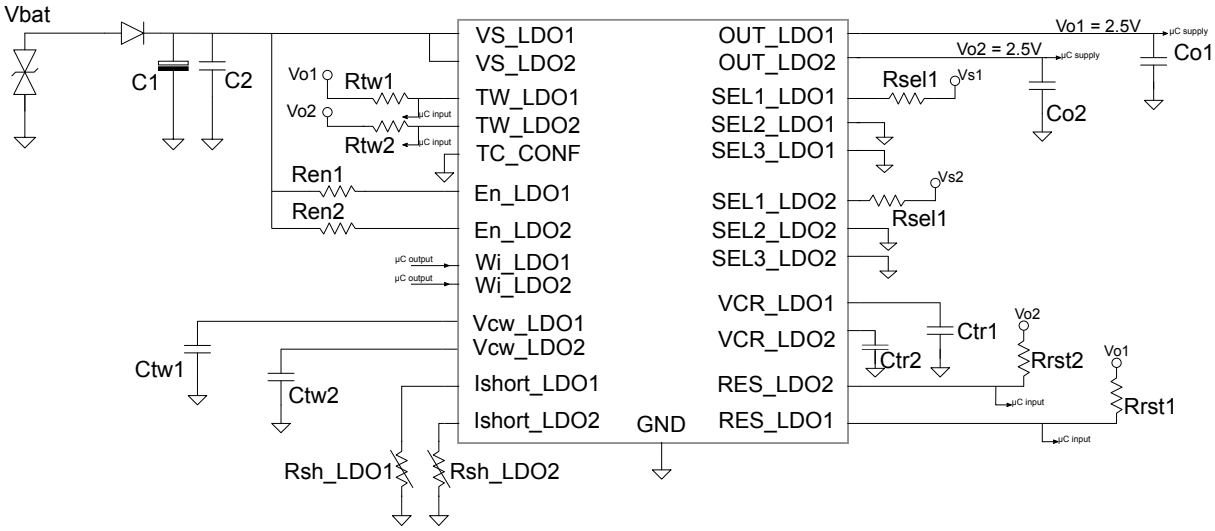
ID	Description
SM1	Thermal sensor acting by TW pin
SM2	Overtemperature protection
SM3	Limitation on maximum output current
SM4	Output voltage V_O monitoring for undervoltage detection
SM5	Output voltage V_O monitoring for overvoltage detection
SM6	RST reset assertion in case of V_O undervoltage detection

Besides the internal watchdog to check microcontroller correct functionality can be considered as a safety mechanism at system level.

More details about functional safety can be found in the device safety manual, provided on customer request.

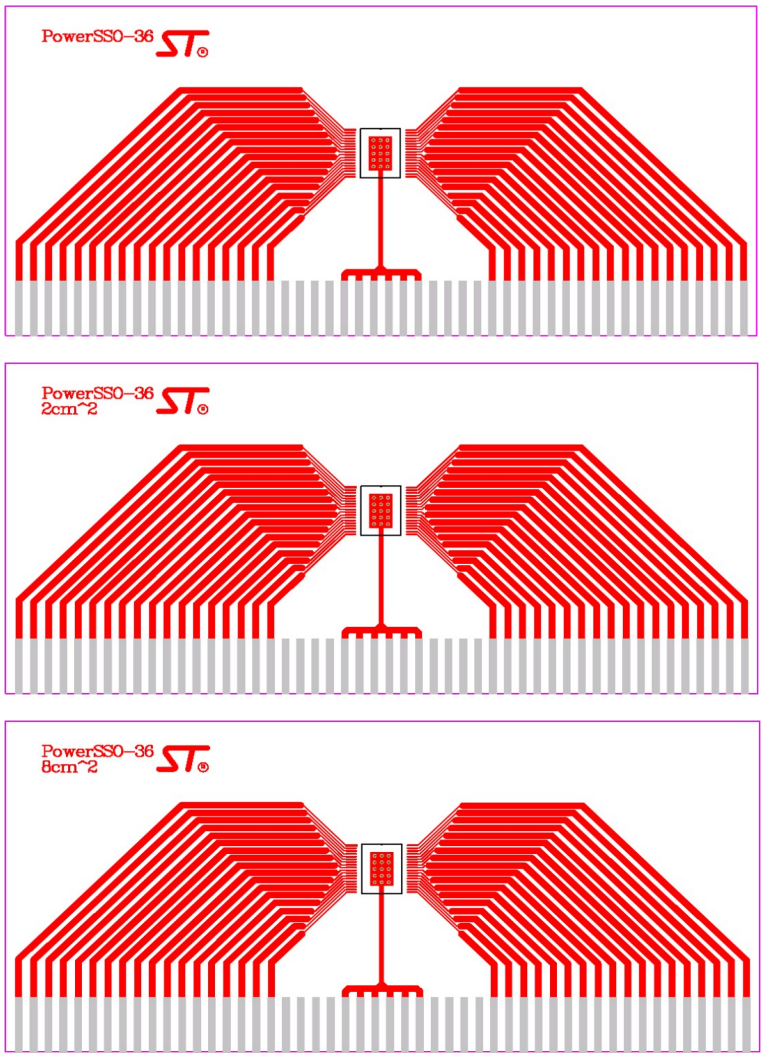
5 Application

Figure 57. **Typical application**



6 PowerSSO-36 PCB thermal data

Figure 58. **PowerSSO-36 on two-layers PCB (2s0p to JEDEC JESD 51-5)**



Note: Layout condition of Rth and Zth measurements (board finish thickness 1.6 mm ±10% board double layer, board dimension 129x60, board material FR4, Cu thickness 0.070 mm (front and back side), thermal vias separation 1.2 mm, thermal via diameter 0.3 mm ±0.08 mm,Cu thickness on vias 0.025 mm).

Figure 59. **PowerSSO-36 on four-layers PCB (2s2p to JEDEC JESD 51-7)**

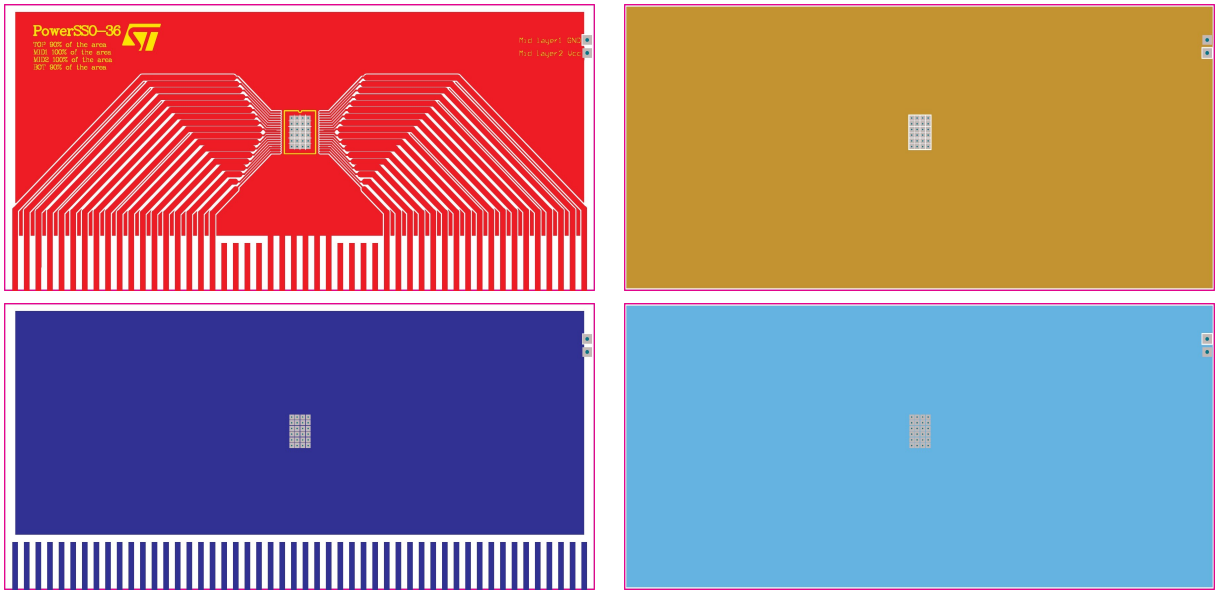


Figure 60. **PowerSSO-36 thermal resistance junction to ambient vs PCB 4 layer copper area**

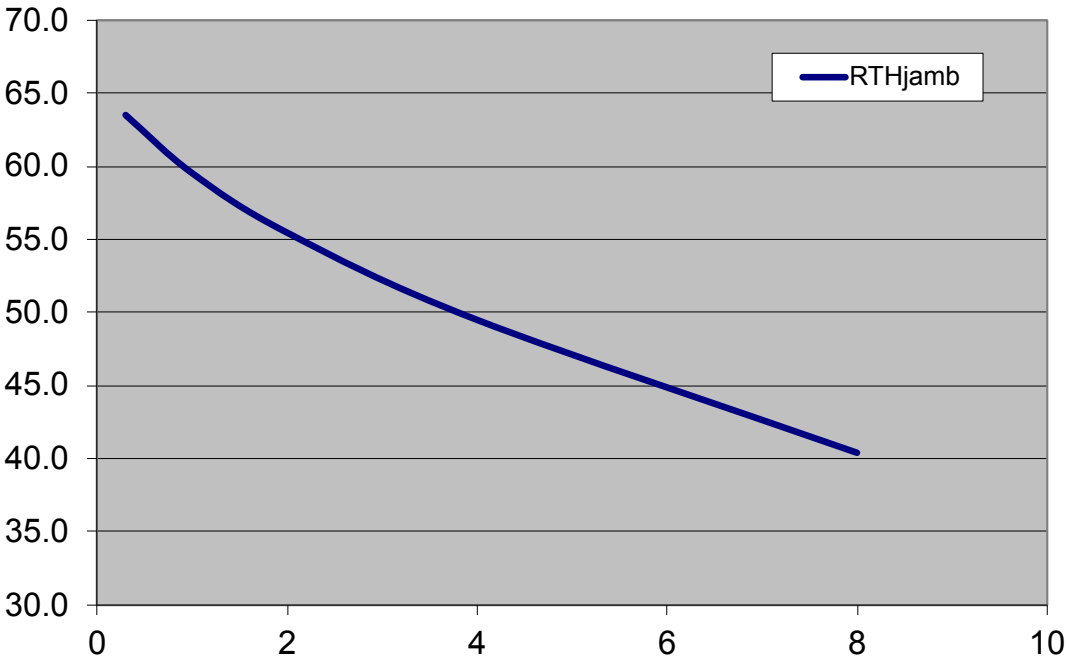
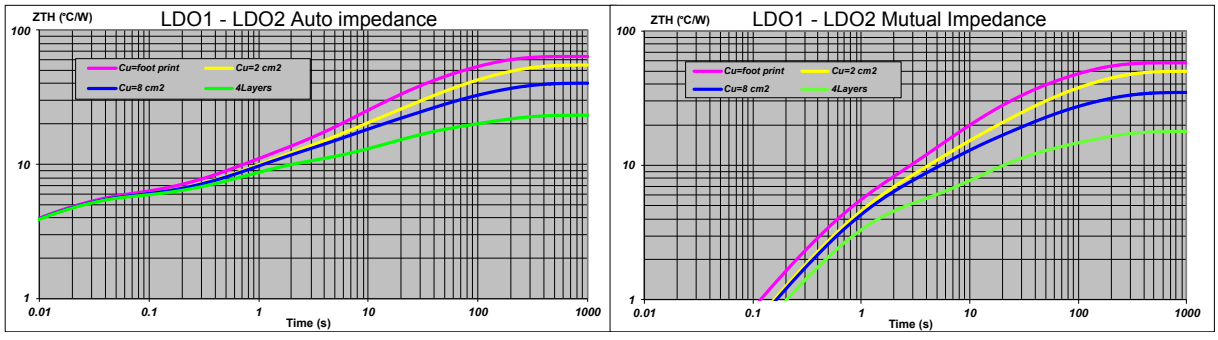


Figure 61. **PowerSSO-36 thermal impedance junction to ambient vs PCB copper area**



Pulse calculation formula:

$$Z_{TH\delta} = R_{TH} . \delta + Z_{THtp}(1 - \delta) \quad (5)$$

Where:
δ = tp/T

Figure 62. Thermal fitting model of a Vreg in PowerSSO-36

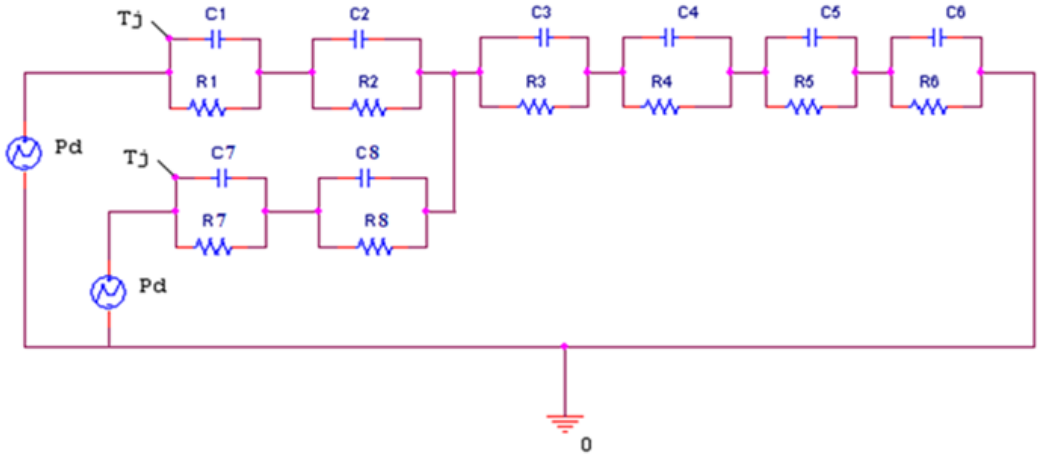


Table 21. PowerSSO-36 thermal parameter

Area/island (cm²)	FP	2	8	4L
R1 (°C/W)	2.5	-	-	-
R2 (°C/W)	3	-	-	-
R3 (°C/W)	4	4	4	4
R4 (°C/W)	6	6	6	5
R5 (°C/W)	18	14	10	2
R6 (°C/W)	30	26	15	7
R7 (°C/W)	2.5	-	-	-
R8 (°C/W)	3	-	-	-
C1 (W·s/°C)	0.001	-	-	-
C2 (W·s/°C)	0.005	-	-	-
C3 (W·s/°C)	0.15	0.2	0.2	0.2
C4 (W·s/°C)	0.9	0.9	0.9	3
C5 (W·s/°C)	1	2	3	10
C6 (W·s/°C)	3	5	9	18
C7 (W·s/°C)	0.001	-	-	-
C8 (W·s/°C)	0.005	-	-	-

7 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSSO-36 (exposed pad down) package information

Figure 63. PowerSSO-36 (exposed pad down) package outline

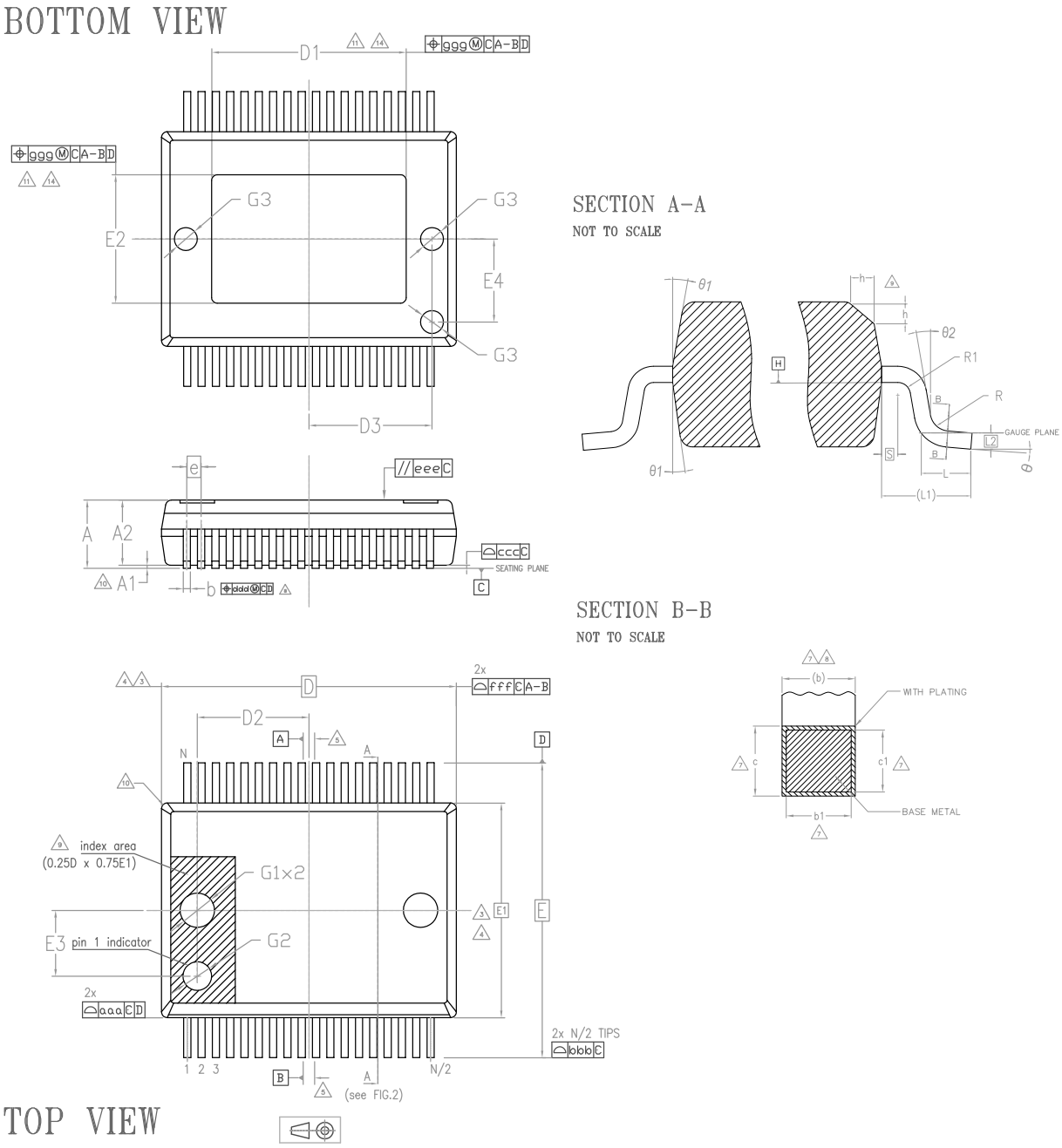
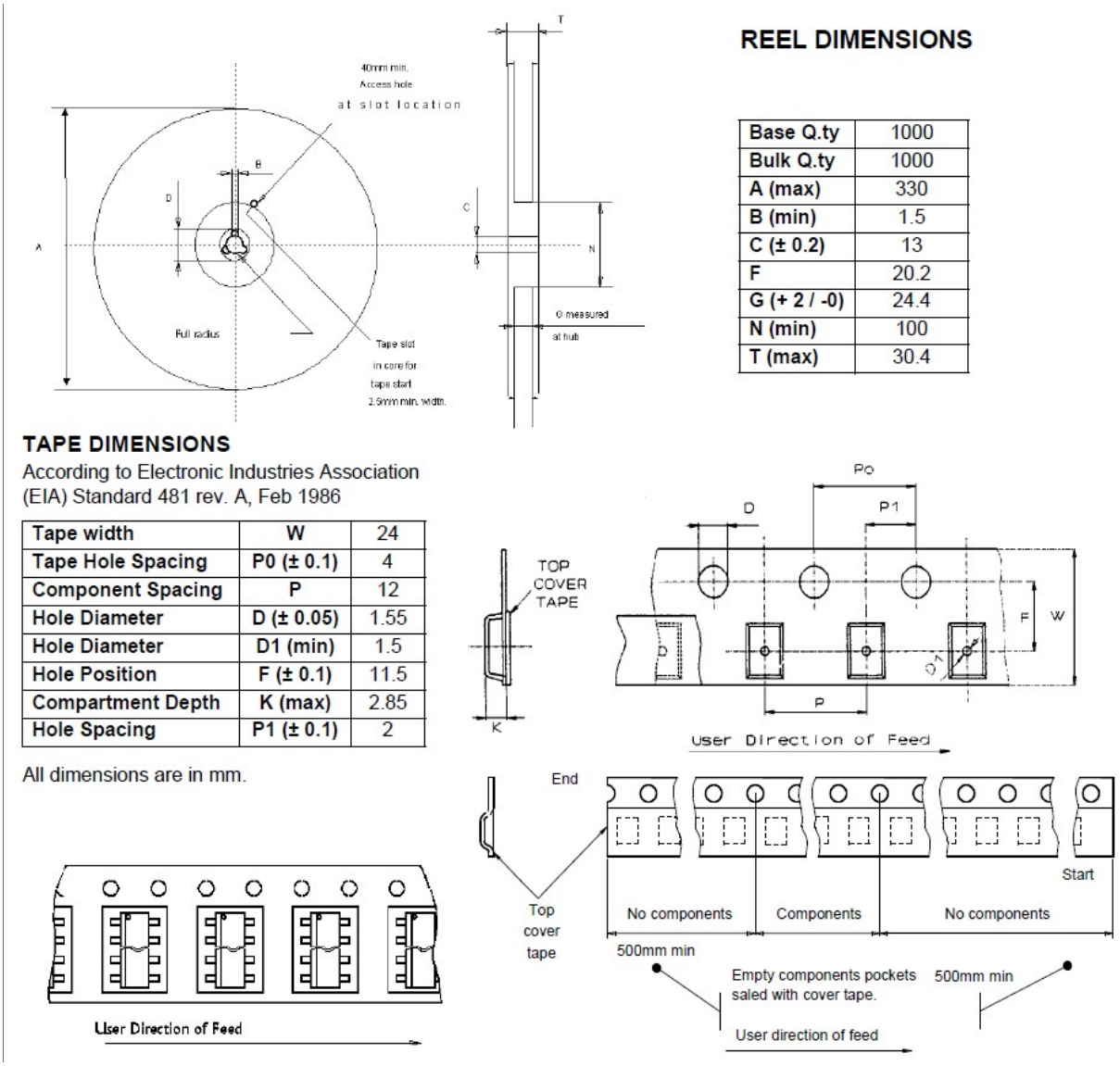


Table 22. **PowerSSO-36 (exposed pad down) package mechanical data**

Ref.	Dimensions in mm		
	Min.	Typ.	Max.
Θ	0°	-	8°
Θ1	5°	-	10°
Θ2	0°	-	-
A	2.15	-	2.45
A1	0.00	-	0.10
A2	2.15	-	2.35
b	0.18	-	0.32
b1	0.13	0.25	0.30
c	0.23	-	0.32
c1	0.20	0.20	0.30
D	10.30 BSC		
D1	6.90	-	7.50
D2	-	3.65	-
D3	-	4.30	-
e	0.50 BSC		
E	10.30 BSC		
E1	7.50 BSC		
E2	4.30	-	5.20
E3	-	2.30	-
E4	-	2.90	-
G1	-	1.20	-
G2	-	1.00	-
G3	-	0.80	-
h	0.30	-	0.40
L	0.55	0.70	0.85
L1	1.40		
L2	0.25 BSC		
N	36		
R	0.30	-	-
R1	0.20	-	-
S	0.25	-	-
Tolerance of form and position			
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
eee	0.10		
ffff	0.20		
ggg	0.15		

7.2 PowerSSO-36 (exposed pad down) packaging information

Figure 64. **PowerSSO-36 tape and reel shipment**



Revision history

Table 23. **Document revision history**

Date	Version	Changes
12-Mar-2025	1	Initial release.

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