10BASE-T1S Ethernet PHY Transceiver

LAN8670/1

Description

Part Number	Rev C2	Rev D0	Package
LAN8670	✓	✓	32-VQFN
LAN8671	✓	✓	24-VQFN
LAN8672	✓	—	36-VQFN

The LAN8670/1/2 is a high-performance 10BASE-T1S single-pair Ethernet PHY transceiver for 10 Mbit/s half-duplex networking over a single pair of conductors. This device enables sensor/actuator networks to be implemented in standard Ethernet technology, which reduces application costs by eliminating the gateways necessary with legacy networking technologies. Further, the ability to connect multiple PHYs onto a common mixing segment saves implementation costs by switch ports and cabling. The LAN8670/1/2 is designed for use in high-reliability cost sensitive automotive, industrial, building automation, and sensor/actuator applications.

Highlights

- High-performance 10BASE-T1S Ethernet PHY designed according to IEEE Std 802.3™-2022
  - 10 Mbit/s over single balanced pair
  - Half-duplex multidrop mixing segments up to at least 25m with up to at least 8 PHYs
- Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) media access control
- Physical Layer Collision Avoidance (PLCA)
  - Allows for high bandwidth utilization by avoiding collisions on the medium
  - Burst mode for transmission of multiple packets for latency-sensitive applications
  - Minimize latency for time-sensitive applications by assigning multiple PLCA IDs per node
- Topology Discovery support (Revision D0)
- Cable fault (open/short) diagnostics and Signal Quality Indication (SQI) support
- Over-temperature and under-voltage detection
- EtherGREEN™ Energy Efficiency
  - Low power 10BASE-T1S PHY operation
  - Ultra-low power sleep mode
  - Wake up triggered by either MDI Wake-Up Tone (WUT) or local WAKE_IN, allowing OA TC10 compliant wake/sleep and partial networking (Revision D0)
  - WAKE_OUT pulse assertion
  - INH output for enable/disable of ECU supply
- IEEE Std 802.1AS™ / IEEE 1588™ application support
  - Enables high-precision clock recovery with ultra-low jitter for microcontrollers without Time-Sensitive Networking (TSN) support
- Enhanced electromagnetic compatibility / electromagnetic interference (EMC/EMI) performance
  - Low RF emissions
  - Digital output drive strength adjust
  - Simple low cost bus interface network
- Single 3.3V supply with integrated 1.8V regulator
- Small footprint 24-pin (4 x 4 mm), 32-pin (5 x 5 mm), and 36-pin (6 x 6 mm) VQFN with wettable flanks
- -40°C to +125°C extended temperature range
- AEC-Q100 qualification
- Functional Safety Support (ISO 26262, ASIL B)
  - ISO 26262 compliant development
  - Functional Safety Package, including Safety Manual, FMEDA, and Dependent Failure Analysis (DFA)

Target Applications

- In-vehicle networking and automotive zonal architecture
- Sensor/actuator networks
- Industrial control cabinets and machine control
- Building automation
- LED lighting

Conformity

Table 1 shows the conformity relationship between data sheet, silicon, and product revisions. This data sheet applies to silicon revision 5 (0101b) and revision 6 (0110b) as shown below.

Table 1. Conformity Table

Product Revision[1]	Silicon Revision[2]	Part Numbers Available in this Revision	Data Sheet Revision
A0	Rev 0 (0000b)	LAN8670, LAN8671, LAN8672	DS60001573A
B1	Rev 2 (0010b)	LAN8670, LAN8671, LAN8672	DS60001573C
C1	Rev 4 (0100b)	LAN8670, LAN8671, LAN8672	DS60001573G
C2	Rev 5 (0101b)	LAN8670, LAN8671, LAN8672	DS60001573K
D0	Rev 6 (0110b)	LAN8670, LAN8671	DS60001573K

Notes:

1. The product revision is noted in the package top marking.
2. The silicon revision is obtained by reading the Manufacturer's Model Revision from the PHY Identifier 2 register.

Related Links

Package Marking Information

PHY_ID2

PHY Identifier 2 Register

Table of Contents

1. Preface

1.1. General Terms

Table 1-1. General Terms

Term	Description
10BASE-T	10 Mbit/s Ethernet over twisted pair, IEEE Std 802.3™ Clause 14
10BASE-T1L	10 Mbit/s Ethernet over long-reach single pair of conductors, IEEE Std 802.3 Clause 146
10BASE-T1S	10 Mbit/s Ethernet over short-reach single pair of conductors, IEEE Std 802.3 Clause 147
ACMA	Application Controlled Media Access
BIN	Bus Interface Network
BT	Bit Time, 100 ns for 10 Mbps Ethernet
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CSR	Control and Status Register
DFA	Dependent Failure Analysis
FMEDA	Failure Modes, Effects, and Diagnostic Analysis
Host	External local system (Includes controller, application firmware, etc.)
IPG	Inter-packet gap time (96 BT), IEEE Std 802.3 Clause 4
LDO	Low Dropout Regulator
MAC	Media Access Controller
MDI	Medium Dependent Interface
MII	Media Independent Interface, IEEE Std 802.3 Clause 22
PCS	Physical Coding Sublayer
PLCA	Physical Layer Collision Avoidance, IEEE Std 802.3 Clause 148
PMA	Physical Medium Attachment sublayer
PMD	Physical Medium Dependent sublayer
POR	Power-on Reset
RMII	Reduced Media Independent Interface
RS	Reconciliation Sublayer
SC-MII	Single Clock Media Independent Interface. This is a variant of the MII described in IEEE Std 802.3 Clause 22 in which the PHY drives a single clock to the MAC for both transmit and receive data.
SFD	Start-of-Frame Delimiter. This is the 4-bit value indicating the end of the preamble and the beginning of an Ethernet frame.
SMI	Serial Management Interface, also known as MII Management Interface, IEEE Std 802.3 Clause 22
SQI	Signal Quality Indicator
SSD	Start-of-Stream Delimiter. The 5B symbol 'H' that is repeated twice to indicate that the preamble of a 10BASE-T1S Ethernet packet has begun.
STA	Station management entity. See also "Host"
TSSI	Time Synchronization Service Interface, IEEE Std 802.3 Clause 90

1.2. Buffer Types

Table 1-2. LAN8670/1/2 Buffer Type Descriptions

Buffer	Description
AIO	Analog bi-directional
ICLK	Crystal or reference clock oscillator input
OCLK	Crystal output
PD	55 kΩ (typical) internal pull-down. Unless otherwise noted in the pin description, internal pull-downs are not enabled. Internal pull-down resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled low, an external resistor must be added.
PU	55 kΩ (typical) internal pull-up. Unless otherwise noted in the pin description, internal pull-ups are not enabled. Internal pull-up resistors prevent unconnected inputs from floating. Do not rely on internal resistors to drive signals external to the device. When connected to a load that must be pulled high, an external resistor must be added.
VI-VDDAU	3.3V input (VDDAU power domain)
VIS-VDDP	3.3V Schmitt-triggered input (VDDP power domain)
VO-VDDP	3.3V output with configurable output drive (VDDP power domain)
VOH-VDDP	3.3V high-speed output with configurable output drive (VDDP power domain)
VODL-VDDP	3.3V n-channel open-drain sink output drive (VDDP power domain)
VODH-VDDAU	3.3V p-channel open-drain source output drive (VDDAU power domain)

Note: Digital signals are not 5V tolerant unless specified.

1.3. Register Bit Types

The following table describes the register bit attributes used throughout this document.

Table 1-3. Register Bit Types

Register Bit Type Notation	Register Bit Description
R	**Read:** A register or bit with this attribute can be read.
W	**Write:** A register or bit with this attribute can be written.
RO	**Read Only:** A register or bit with this attribute is read only; writing has no effect.
RC	**Read to Clear:** Content is cleared after the read. Writes have no effect.
SC	**Self Clearing:** A bit with this attribute will be cleared to '0' after being written as '1'. Hardware often clears such bits following the completion of some action initiated by the write.
NASR	**Not Affected by Software Reset:** The state of NASR bits do not change on assertion of a software reset.

Many of these register bit notations can be combined. Some examples of this are:

- R/W: Can be written. Will return current setting on a read.
- R/W SC: Bit is readable. When set, it will automatically be cleared by hardware once some action is complete.
- R/W1C: Bit is readable. Write a '1' to this bit to clear.

1.4. Reference Documents

1. *IEEE Standard for Ethernet*, IEEE Std 802.3™-2022.
   standards.ieee.org/standard/802_3-2022.html
2. *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*, IEEE Std 1588™-2019.
   standards.ieee.org/standard/1588-2019.html
3. *IEEE Standard for Local and Metropolitan Area Networks – Timing and Synchronization for Time-Sensitive Applications*, IEEE Std 802.1AS™-2020.
   standards.ieee.org/standard/802_1AS-2020.html
4. *LAN86xx Bus Interface Network (BIN) Reference Design Application Note*, DS60001718, Microchip.
   www.microchip.com/DS60001718
5. *LAN8670/1/2 Configuration Application Note*, DS60001699, Microchip.
   www.microchip.com/DS60001699
6. *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs*, Version 2.1, OPEN Alliance, 2025.
   opensig.org/automotive-ethernet-specifications/
7. *10BASE-T1S System Implementation Specification*, Version 1.0, OPEN Alliance, 2023.
   opensig.org/automotive-ethernet-specifications/
8. *RMII Specification*, Revision 1.2, RMII Consortium, 1999.
9. *10BASE-T1S Topology Discovery Specification*, Version 1.4, OPEN Alliance, 2024.
   opensig.org/automotive-ethernet-specifications/
10. *10BASE-T1S Sleep/Wake-Up Specification*, Version 1.0, OPEN Alliance, 2022.
    opensig.org/automotive-ethernet-specifications/
11. *10BASE-T1S PLCA Management Registers*, Version 1.4, OPEN Alliance, 2025.
    opensig.org/automotive-ethernet-specifications/
12. *Topology Discovery for 10BASE-T1S Systems*, DS00006067, Microchip.
    www.microchip.com/DS00006067

2. Introduction

2.1. General Description

The Microchip LAN8670/1/2 is a compact, low power, and cost-effective single-port 10BASE-T1S Ethernet PHY designed according to *IEEE Std 802.3-2022* Clause 147. The device provides 10 Mbit/s half-duplex transmit and receive capability over a single balanced pair of conductors such as Unshielded Twisted Pair (UTP) cable. The LAN8670/1/2 is designed for use in applications requiring an extended temperature range (-40°C to +125°C ambient) and is optimized for AEC-Q100 automotive Grade 1 use cases. The device is also compliant to automotive and industrial EMC and EMI requirements. The single power supply and simple bus interface network simplifies its integration into small form factor applications.

The LAN8670/1/2 allows for the creation of half-duplex multidrop network topologies. The multidrop mode supports up to at least 8 PHYs connected to a common mixing segment of up to at least 25m in length. The ability to connect multiple PHYs to a common mixing segment reduces weight and implementation costs by requiring fewer connectors, individual cables and switch ports.

Access to the physical medium is managed by CSMA/CD and optionally supplemented by Physical Layer Collision Avoidance (PLCA) as per *IEEE Std 802.3-2022* Clause 148. In addition to the single transmit opportunity per bus cycle in this standard, the LAN8670/1/2 has the ability to be configured with up to 8 additional transmit opportunities in each bus cycle. As an alternative to PLCA, the Application Controlled Media Access (ACMA) pin can be used to implement time-division multiple access (TDMA) to the physical medium.

The LAN8670/1/2 interfaces with an Ethernet MAC via standard MII/RMII, or via the Single Clock Media Independent Interface (SC-MII) which is similar to the MII but with fewer pins. The unique capability to use PLCA with RMII is covered by Microchip intellectual property (U.S. Pat. 11,516,855) allowing PLCA functionality with legacy reduced pin-count RMII applications. An integrated serial management interface (SMI) provides rapid register access and configuration at up to 4 MHz.

Microchip's LAN8670/1/2 EtherGREEN energy efficient technology provides low power 10BASE-T1S PHY operation along with an ultra-low power sleep mode with flexible wake options. Revision D0 of the device offers an Open Alliance TC10 compliant wake/sleep implementation, allowing for partial networking operation.

In addition, the LAN8670/1/2 can be used to implement high-precision clock synchronization. This enables implementation of the *IEEE Std 802.1AS* profile, among others, of *IEEE Std 1588* for applications utilizing AVB or other Time Sensitive Networking (TSN) standards. This feature can be used to provide a Timing Synchronization Service Interface (TSSI) as specified in *IEEE Std 802.3-2022* Clause 90 (as amended by *IEEE 802.3de*) as part of a TSN implementation.

Advanced PHY diagnostics are provided, which enable troubleshooting and monitoring capabilities such as cable defect detection of shorts or opens, a receiver Signal Quality Indicator (SQI), PLCA diagnostics, over-temperature, under-voltage detection, comprehensive status interrupt support, and various loopback and test modes. Furthermore, Revision D0 LAN8670/1 supports Topology Discovery as defined by the Open Alliance.

The LAN8670/1/2 is designed to be used in ISO 26262 Functional Safety applications. It fulfills the functional safety requirements for ASIL B. A Functional Safety Package is available, including Safety Manual; Failure Modes, Effects, and Diagnostic Analysis (FMEDA); and Dependent Failure Analysis (DFA). Please contact Microchip support for additional information.

Internal block diagrams of the LAN8670/1/2 are shown in the following figures.

Figure 2-1. LAN8670/1/2 (Rev C2) Internal Block Diagram

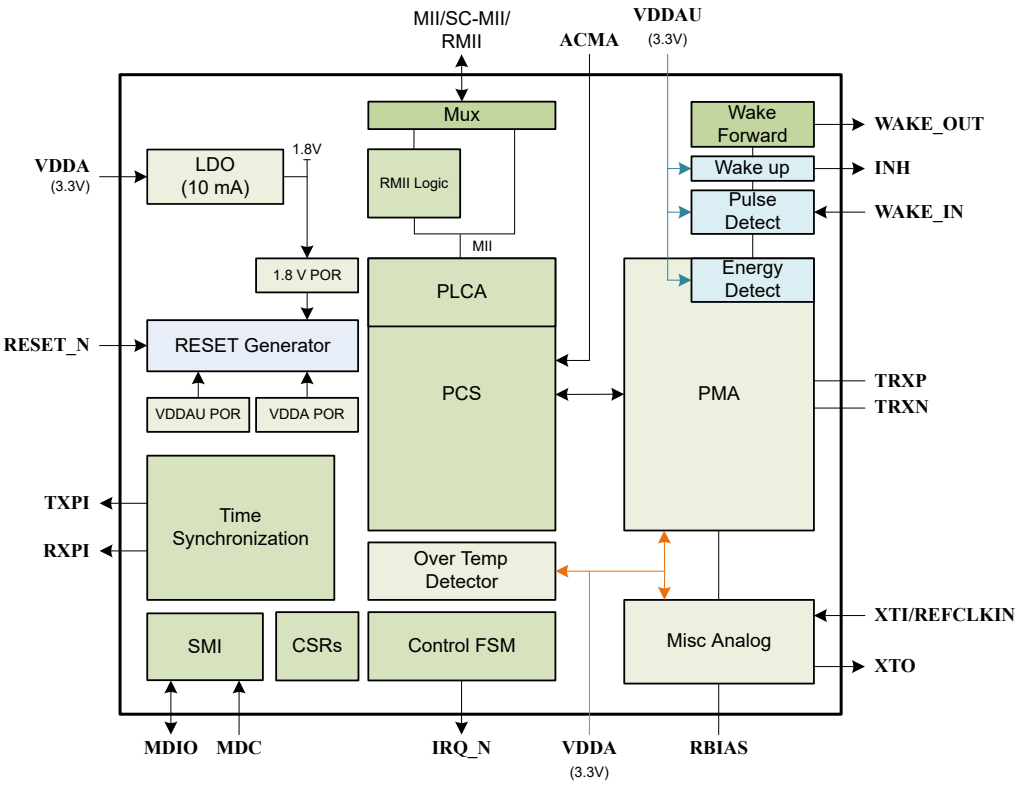
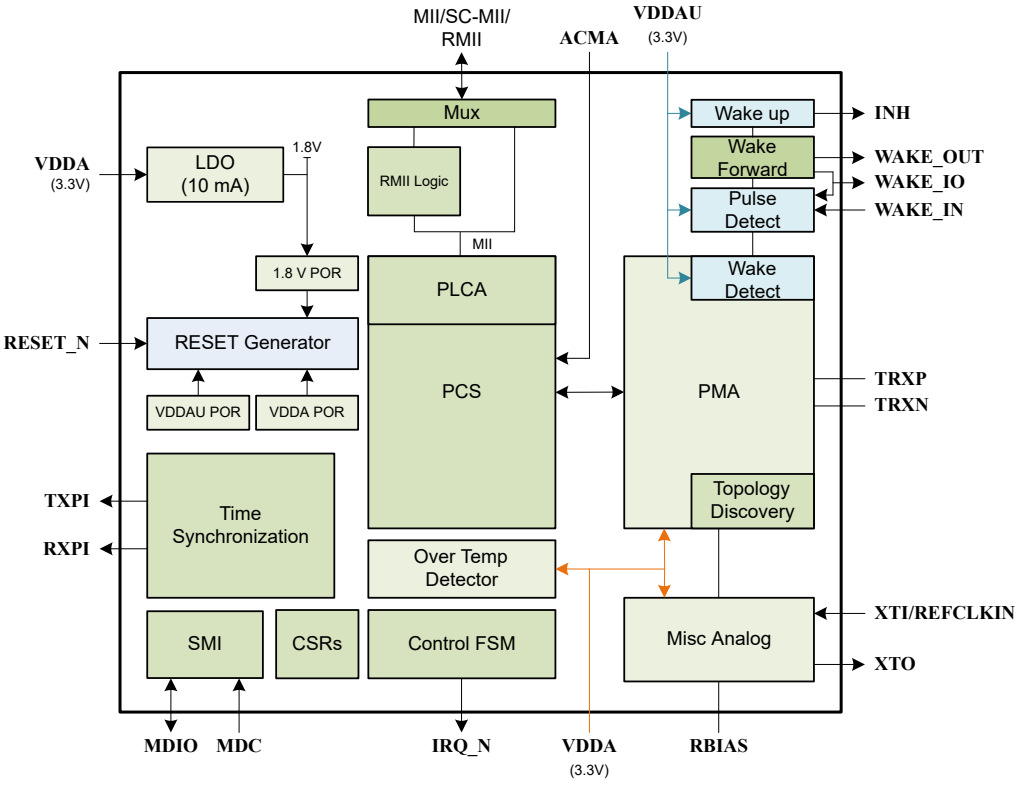


Figure 2-2. LAN8670/1 (Rev D0) Internal Block Diagram



2.2. The LAN8670/1/2 Family

The Microchip LAN8670/1/2 family includes the following devices:

- LAN8670
- LAN8671
- LAN8672 (Revision C2, only)

Device specific features that do not pertain to the entire family are called out independently throughout this document. Table 2-1 below provides a summary of the feature differences between family members.

Table 2-1. LAN8670/1/2 Family Feature Matrix

Part Number	Package	MII Support	SC-MII Support	RMII Support	PLCA Support	ACMA Support	Time Synchronization Support	INH Pin Support	MDI Wake Support	WAKE_IN Pin Support	WAKE_OUT Pin Support	WAKE_IO Pin Support[2]	AEC-Q100 -40° to +125°C
LAN8670	32-VQFN	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LAN8671	24-VQFN	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
LAN8672[1]	36-VQFN	✓	—	—	✓	✓	✓	✓	✓	✓	✓	✓	✓

Notes:

1. LAN8672 Revision C2, only.
2. LAN8670/1 Revision D0, only.

Important: Since some pins are shared between different modes, not all features are available simultaneously. For more information, see the *Pin Description and Configuration* section.

2.3. Example Systems

This section shows example of system block diagrams that apply to all family members.

Note: All family members support advanced features such as ACMA and signals for time synchronization, but they are not shown below since the pin configurations vary among the family members.

Note: The clock source for MII is a crystal connected between pins XTI and XTO. The clock source for RMII is a clock oscillator that is connected to REFCLKIN on both the MAC and the PHY. Additional information is available in the *Pin Descriptions* section.

An example system-level block diagram for the LAN8670/1/2 is shown in Figure 2-3, below. This system does not use sleep mode, so VDDA and VDDAU can be treated as the same supply and VDDP must only be properly isolated from the analog supplies through use of a ferrite bead as described in the *Power Connectivity* section.

Figure 2-3. Simple System Using LAN8670/1/2

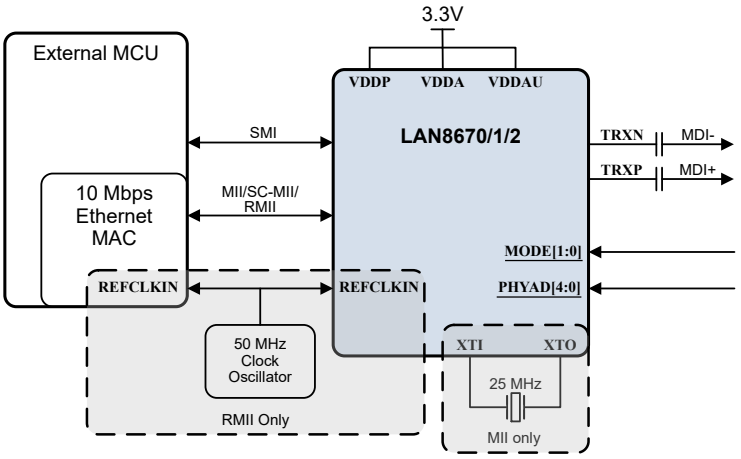
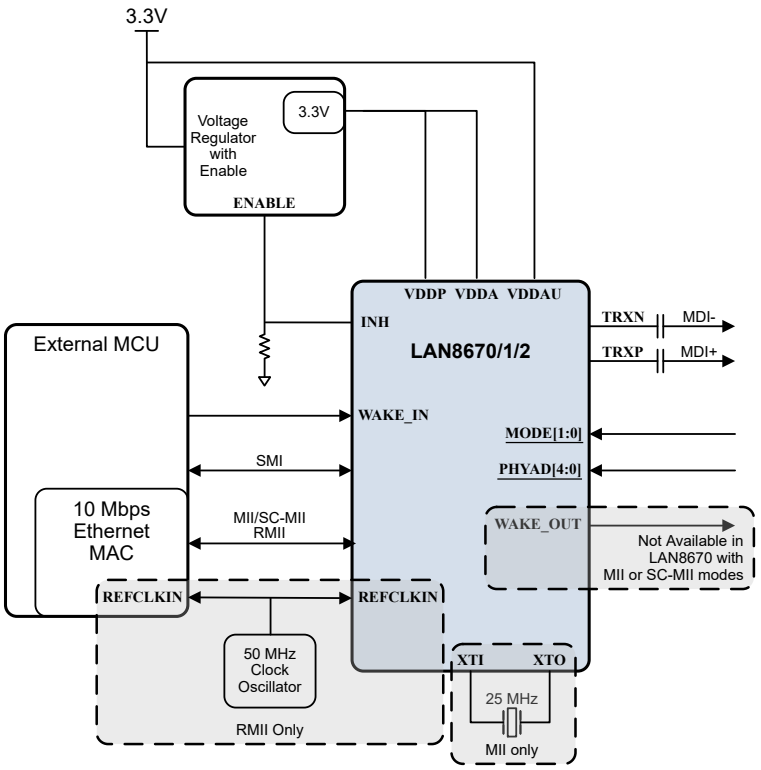


Figure 2-4 shows a system which is designed to use the low power sleep mode so the constant voltage supply VDDAU is separate from the other voltage supplies. VDDA and VDDP will be disabled in sleep mode. In this particular system, the external MCU will initiate sleep mode and then ensure that all inputs to the LAN8670/1/2 are high-impedance. In a system where external power supplies are required to remain active while other devices shut down, the LAN8670/1/2 can drive the INH pin for a programmable delay period before entering sleep mode. In this example, the external MCU will bring the LAN8670/1/2 out of sleep using WAKE_IN and other devices can then be configured to be awakened via WAKE_OUT or activity on the MDI. When the LAN8670 is in the MII or SC-MII mode, WAKE_OUT is not available. For product revision D0 and later the WAKE_IN pin may be configured as a combined WAKE_IO wake input/output. The WAKE_OUT pin is unused when this mode is enabled.

Figure 2-4. System with Sleep Mode Using LAN8670/1/2



3. Pin Description and Configuration

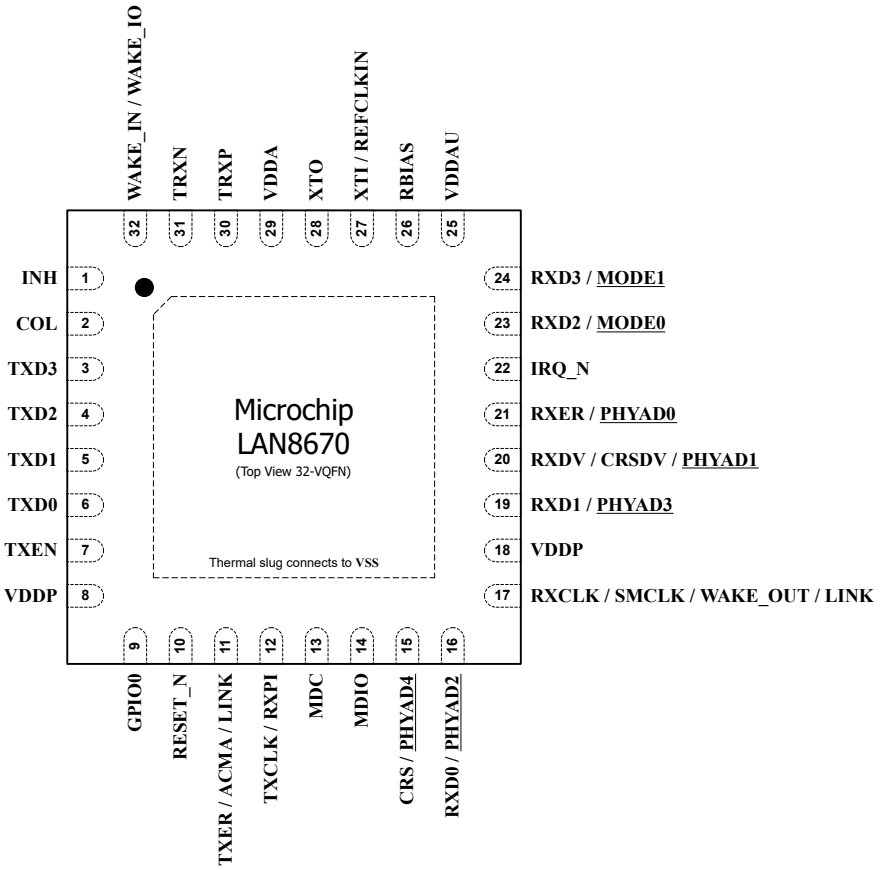
The pin assignments and descriptions for the LAN8670/1/2 are detailed in the following sections. Pin buffer type definitions are detailed in the *Buffer Types* section.

Related Links

Buffer Types

3.1. LAN8670 Pin Assignments

Figure 3-1. LAN8670 32-VQFN Pin Assignments



Note: Configuration straps are identified by an underlined signal name. Signals that function as configuration straps must be augmented with an external resistor. The WAKE_IO and LINK pins are only available on Revision D0 and later products.

Important: The exposed pad (VSS) on bottom of package must be connected to ground.

Table 3-1. LAN8670 32-VQFN Pin Assignments

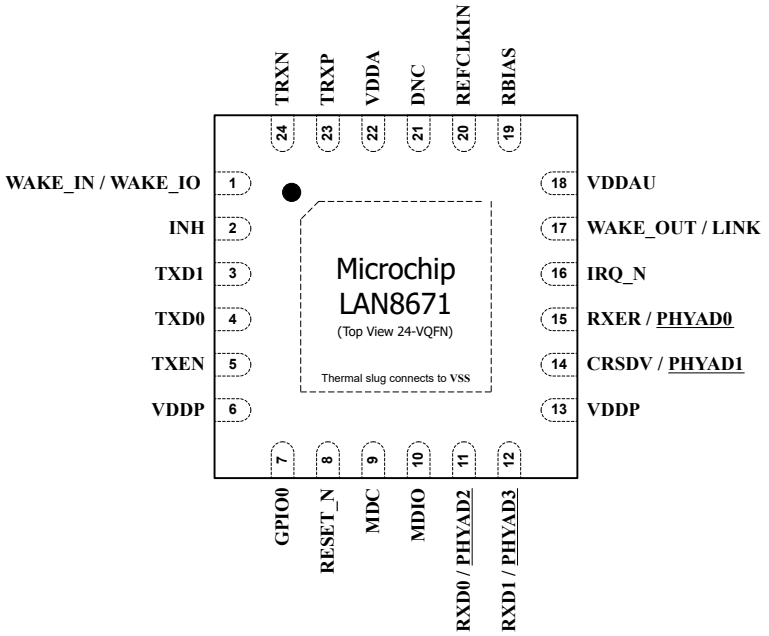
Pin Num	Pin Name	Pin Num	Pin Name
1	INH	17	RXCLK/SMCLK/WAKE_OUT/LINK[1]
2	COL	18	VDDP
3	TXD3	19	RXD1/PHYAD3
4	TXD2	20	RXDV/CRSDV/PHYAD1
5	TXD1	21	RXER/PHYAD0
6	TXD0	22	IRQ_N
7	TXEN	23	RXD2/MODE0
8	VDDP	24	RXD3/MODE1
9	GPIO0	25	VDDAU
10	RESET_N	26	RBIAS
11	TXER/ACMA/LINK[1]	27	XTI/REFCLKIN
12	TXCLK/RXPI	28	XTO
13	MDC	29	VDDA
14	MDIO	30	TRXP
15	CRS/PHYAD4	31	TRXN
16	RXD0/PHYAD2	32	WAKE_IN/WAKE_IO[1]

Note: Exposed Pad (VSS) must be connected to ground.

1. The WAKE_IO and LINK pins are only available on Revision D0 and later products.

3.2. LAN8671 Pin Assignments

Figure 3-2. LAN8671 24-VQFN Pin Assignments



Note: Configuration straps are identified by an underlined signal name. Signals that function as configuration straps must be augmented with an external resistor. The WAKE_IO and LINK pins are only available on Revision D0 and later products.

Important: The exposed pad (VSS) on bottom of package must be connected to ground.

Table 3-2. LAN8671 24-VQFN Pin Assignments

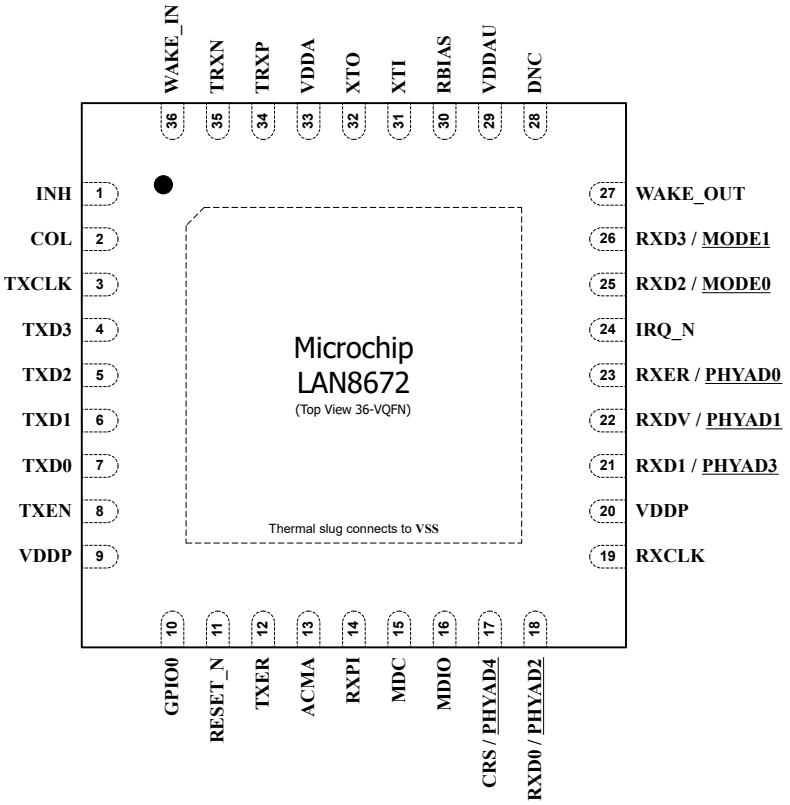
Pin Num	Pin Name	Pin Num	Pin Name
1	WAKE_IN/WAKE_IO[1]	13	VDDP
2	INH	14	CRSDV/PHYAD1
3	TXD1	15	RXER/PHYAD0
4	TXD0	16	IRQ_N
5	TXEN	17	WAKE_OUT/LINK[1]
6	VDDP	18	VDDAU
7	GPIO0	19	RBIAS
8	RESET_N	20	REFCLKIN
9	MDC	21	DNC
10	MDIO	22	VDDA
11	RXD0/PHYAD2	23	TRXP
12	RXD1/PHYAD3	24	TRXN

Note: Exposed Pad (VSS) must be connected to ground.

1. The WAKE_IO and LINK pins are only available on Revision D0 and later products.

3.3. LAN8672 Pin Assignments

Figure 3-3. LAN8672 36-VQFN Pin Assignments



Note: Configuration straps are identified by an underlined signal name. Signals that function as configuration straps must be augmented with an external resistor.

Important: The exposed pad (VSS) on bottom of package must be connected to ground.

Note: The LAN8672 36-pin package is only available for product revision C2.

Table 3-3. LAN8672 36-VQFN Pin Assignments

Pin Num	Pin Name	Pin Num	Pin Name
1	INH	19	RXCLK
2	COL	20	VDDP
3	TXCLK	21	RXD1/PHYAD3
4	TXD3	22	RXDV/PHYAD1
5	TXD2	23	RXER/PHYAD0
6	TXD1	24	IRQ_N
7	TXD0	25	RXD2/MODE0
8	TXEN	26	RXD3/MODE1
9	VDDP	27	WAKE_OUT
10	GPIO0	28	DNC
11	RESET_N	29	VDDAU
12	TXER	30	RBIAS
13	ACMA	31	XTI
14	RXPI	32	XTO
15	MDC	33	VDDA
16	MDIO	34	TRXP
17	CRS/PHYAD4	35	TRXN
18	RXD0/PHYAD2	36	WAKE_IN

Note: Exposed Pad (VSS) must be connected to ground.

3.4. Pin Descriptions

This section contains descriptions of the various LAN8670/1/2 pins. The "_N" symbol in the signal name indicates that the active, or asserted, state occurs when the signal is at a low voltage level. For example, RESET_N indicates that the reset signal is active low. When "_N" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term assert, or assertion, indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation, indicates that a signal is inactive.

Pin buffer type definitions are detailed in the *Buffer Types* section.

Table 3-4. MII/SC-MII/RMII Signals

Name	Symbol	Buffer Type	Description
Transmit Data 0	TXD0	VIS-VDDP PD	Transmit data bus bit 0 (all modes). This pin is high impedance when the device is in reset.
Transmit Data 1	TXD1	VIS-VDDP PD	Transmit data bus bit 1 (all modes). This pin is high impedance when the device is in reset.
Transmit Data 2 (MII/SC-MII modes)	TXD2	VIS-VDDP PD	Transmit data bus bit 2 (MII/SC-MII modes). In RMII mode, this signal is not used and is internally pulled-down to VSS. This pin is high impedance when the device is in reset.
Transmit Data 3 (MII/SC-MII modes)	TXD3	VIS-VDDP PD	Transmit data bus bit 3 (MII/SC-MII modes). In RMII mode, this signal is not used and is internally pulled-down to VSS. This pin is high impedance when the device is in reset.
Transmit Error (MII mode)	TXER	VIS-VDDP PD	This input is asserted to indicate that an error was detected somewhere in the packet presently being transferred to the device. This pin is unused in RMII mode and should be connected to VSS if it is not used for ACMA functionality on the LAN8670. This pin is shared with the ACMA functionality on the LAN8670. This pin is shared with the LINK functionality on Revision D0 LAN8670. This pin is high impedance when the device is in reset.
Transmit Enable	TXEN	VIS-VDDP PD	Indicates that valid transmission data is present on TXD[3:0]. In RMII mode, only TXD[1:0] provide valid data. **Note:** A pull-down resistor is recommended to prevent incidental transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization. This pin is high impedance when the device is in reset.
Transmit Clock (MII mode)	TXCLK	VO-VDDP	2.5 MHz clock used to latch data from the MAC into the device. In RMII mode, this pin is unused and is driven low. It should be left unconnected if it is not used for RXPI functionality on the LAN8670. This pin is shared with the RXPI functionality on the LAN8670. This pin is high impedance when the device is in reset.

Table 3-4. MII/SC-MII/RMII Signals (continued)

Name	Symbol	Buffer Type	Description
Receive Data 0	RXD0	VOH-VDDP	Receive data bus bit 0 (all modes). This pin shares functionality as a PHYAD2 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. This pin is an input when the device is in reset. The state of this pin is captured as PHYAD2 as the device exits reset.
Receive Data 1	RXD1	VOH-VDDP	Receive data bus bit 1 (all modes). This pin shares functionality as a PHYAD3 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. This pin is an input when the device is in reset. The state of this pin is captured as PHYAD3 as the device exits reset.
Receive Data 2 (MII/SC-MII modes)	RXD2	VO-VDDP	Receive data bus bit 2 (MII/SC-MII modes) This pin shares functionality as a MODE0 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. When the LAN8670 is configured for RMII operation, the RXD2 signal is unused except as the MODE0 configuration strap during reset. This pin is an input when the device is in reset. The state of this pin is captured as MODE0 as the device exits reset.
Receive Data 3 (MII/SC-MII modes)	RXD3	VO-VDDP	Receive data bus bit 3 (MII/SC-MII modes). This pin shares functionality as a MODE1 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. When the LAN8670 is configured for RMII operation, the RXD3 signal is unused except as the MODE1 configuration strap during reset. This pin is an input when the device is in reset. The state of this pin is captured as MODE1 as the device exits reset.
Receive Error	RXER	VOH-VDDP	This output is asserted to indicate that an error was detected somewhere in the packet presently being transferred from the device. This signal is optional in RMII mode and may be left unconnected from the MAC. This pin shares functionality as a PHYAD0 configuration strap, however, and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. This pin is an input when the device is in reset. The state of this pin is captured as PHYAD0 as the device exits reset.

Table 3-4. MII/SC-MII/RMII Signals (continued)

Name	Symbol	Buffer Type	Description
Receive Data Valid (MII/SC-MII modes)	RXDV	VOH-VDDP	Indicates that recovered and decoded data is available on the RXD[3:0] pins. This pin shares functionality as a PHYAD1 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. When the LAN8670 is configured for RMII operation, the RXDV signal is unused except as the PHYAD1 configuration strap during reset. The pin, however, is used as CRSDV. This pin is an input when the device is in reset. The state of this pin is captured as PHYAD1 as the device exits reset.
Receive Clock (MII mode)	RXCLK	VO-VDDP	In MII mode, this pin is the 2.5 MHz receive clock output. In RMII mode, this pin is unused and is driven low. It should be left unconnected if it is not used for WAKEOUT functionality on the LAN8670. This pin is shared with the WAKEOUT functionality on the LAN8670. This pin is high impedance when the device is in reset.
Single Media Clock (SC-MII mode)	SMCLK	VO-VDDP	In Single Clock MII mode, this pin is the 2.5 MHz clock output to be connected to the media access controller MII TXCLK and RXCLK input pins. This pin is shared with the WAKEOUT functionality on the LAN8670. This pin is high impedance when the device is in reset.
Carrier Sense / Receive Data Valid (RMII mode)	CRSDV	VOH-VDDP	This signal is asserted to indicate the receive medium is non-idle in RMII mode. This pin shares functionality as a PHYAD1 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. When the LAN8670 is configured for MII or SC-MII operation, the CRSDV signal is unused except as the PHYAD1 configuration strap during reset. The pin, however, is used as RXDV. This pin is an input when the device is in reset. The state of this pin is captured as PHYAD1 as the device exits reset.
Collision Detect (MII/SC-MII modes)	COL	VO-VDDP	Collision Detect. In RMII mode, this pin should be connected to VSS as it is unused and floating. This pin is high impedance when the device is in reset.
Carrier Sense (MII/SC-MII modes)	CRS	VO-VDDP	Carrier Sense. This pin shares functionality as a PHYAD4 configuration strap and, therefore, must be connected to VDDP/VSS through a pull-up/pull-down resistor, as desired. This pin is an input when the device is in reset. The state of this pin is captured as PHYAD4 as the device exits reset.

Table 3-5. Ethernet Transceiver Pins

Name	Symbol	Buffer Type	Description
Ethernet TX/RX Positive Terminal	TRXP	AIO	Positive terminal for transmit/receive signal.
Ethernet TX/RX Negative Terminal	TRXN	AIO	Negative terminal for transmit/receive signal.

Table 3-6. Serial Management Interface (SMI) Pins

Name	Symbol	Buffer Type	Description
SMI Data Input/Output	MDIO	VIS-VDDP / VO-VDDP	Serial Management Interface data input/output. Should be connected to VDDP via pull-up resistor. This pin is high impedance when the device is in reset.
SMI Clock	MDC	VIS-VDDP	Serial Management Interface clock. This pin is high impedance when the device is in reset.

Table 3-7. Power Management Pins

Name	Symbol	Buffer Type	Description
Inhibit	INH	VODH-VDDAU	Inhibit. Used to switch on/off the main external voltage regulators. This pin operates in the VDDAU domain. RESET_N assertion does not affect the state of this pin. This signal is an active high P-channel open-drain source output. The pin will be driven to VDDAU to inhibit the shutdown of external voltage regulators. When the external regulators may be shutdown, this pin will become high impedance. **Note:** When used, this pin requires a pull-down resistor. When not used, this pin should be left unconnected. This pin is high impedance when the device is in reset.
Wake Input	WAKE_IN	VI-VDDAU	Wake Input. Asserted to move the part out of sleep. When not used, this pin should be connected to VSS. This pin is high impedance when the device is in reset. **Note:** This pin operates in the VDDAU domain. **Note:** When used, this pin requires a pull-up or pull-down resistor, depending on the software configured assertion polarity. If a pull-up is used, it must be connected to VDDAU.
Wake Input/Output	WAKE_IO		Wake Input/Output. The WAKE_IN pin may alternatively be configured as a combined Wake Input/Output. When the device is asleep, a pulse detected on WAKE_IO will move the part out of sleep. An output pulse may also be driven from this pin to signal a wake event to other devices. This pin is high impedance when the device is in reset. **Note:** This pin operates in the VDDAU domain. **Note:** When used, this pin requires a pull-up or pull-down resistor, depending on the software configured assertion polarity. If a pull-up is used, it must be connected to VDDAU. **Note:** The Wake Input/Output pin is only available on revision D0 and later devices.

Table 3-7. Power Management Pins (continued)

Name	Symbol	Buffer Type	Description
Wake Output	WAKE_OUT	VO-VDDP	Wake Output. Asserted when the part wakes out of sleep. When not used, this pin should be left unconnected. This pin is high impedance when the device is in reset. **Note:** When used, this pin requires a pull-down resistor. **Note:** This pin operates in the VDDP domain. This pin is shared with the LINK functionality on LAN8671 Revision D0.

Table 3-8. Application Pins

Name	Symbol	Buffer Type	Description
Application Controlled Medium Access	ACMA	VIS-VDDP	Application Controlled Medium Access. When this feature is enabled, the station controller may assert this input to allow the PHY to transmit to the medium. When unused, this pin is an input and should be connected to VSS. This pin is high impedance when the device is in reset. This pin is shared with the LINK functionality on Revision D0 LAN8670.
Receive Packet Indication	RXPI	VO-VDDP	Receive Packet Indication. This pin is asserted by the Time Synchronization block to indicate the reception of a packet. This pin may also be asserted when the PHY receives a packet that matches a configured pattern. The packet matching feature is typically used to trigger on reception of *IEEE Std 802.1AS* gPTP packets. When unused, this pin is actively driven low and may be left unconnected. This pin is high impedance when the device is in reset.
Transmit Packet Indication	TXPI	VO-VDDP	Transmit Packet Indication. This pin is asserted by the Time Synchronization block to indicate the transmission of a packet. This pin may also be asserted when the PHY transmits a packet that matches a configured pattern. The packet matching feature is typically used to trigger on transmission of *IEEE Std 802.1AS* gPTP packets. This pin is high impedance when the device is in reset.
General Purpose Application I/O	GPIO0	VIS-VDDP / VO-VDDP	General Purpose Application I/O 0. This pin may be configured as ACMA, TXPI, RXPI, RXTXPI, or LINK. The station management entity cannot directly drive or read this pin through CSR writes or reads. When unused, this pin is actively driven low and may be left unconnected. This pin is high impedance when the device is in reset.
Link Status Indication	LINK	VO-VDDP	Link Status Indication. When this feature is enabled, this pin will be asserted high when network link status is true. **Note:** The link status output pin is only available on revision D0 and later devices.

Table 3-9. Miscellaneous Pins

Name	Symbol	Buffer Type	Description
External 25 MHz Crystal Input	XTI	ICLK	External 25 MHz crystal input (MII/SC-MII only). 25 MHz, 1.8-3.3V single-ended clock oscillator input (-40°C to +85°C ambient, only).
External 25 MHz Crystal Output	XTO	OCLK	External 25 MHz crystal output (MII/SC-MII only). **Note:** When using a single-ended clock oscillator on XTI or when the LAN8670 is in RMII mode, this pin must be left unconnected with <10 pF stray capacitance.
External Clock Input	REFCLKIN	ICLK	50 MHz, 1.8-3.3V single-ended clock oscillator input (RMII only).
Interrupt	IRQ_N	VODL-VDDP	Device interrupt request. Active low N-channel open-drain sink output. **Note:** This pin requires a 10 kΩ (typical) pull-up to VDDP. This pin is high impedance when the device is in reset.
System Reset	RESET_N	VIS-VDDP PU	System reset. This pin is active low. If unused, this pin may be connected directly to VDDP.
Bias Resistor	RBIAS	AIO	External bias resistor connection pin. This pin requires connection of a 12.4 kΩ resistor to ground. **Note:** The resistor must be within ± 1% tolerance across the entire expected operating temperature range.
Do Not Connect	DNC	—	The pin must be left floating externally unless otherwise directed by Microchip.

Table 3-10. Configuration Straps

Name	Symbol	Buffer Type	Description
Operating Mode Configuration Straps 1-0	MODE[1:0]	VIS-VDDP	These configuration straps are used to select the device's default mode of operation. See Configuration Straps for additional information. **Note:** These pins must be connected to either VDDP or VSS via a pull-up/pull-down resistor (10 kΩ, typical) to configure the desired operating mode.
PHY Address Configuration Straps 4-0	PHYAD[4:0]	VIS-VDDP	These configuration straps are used to select the device's default PHY SMI address. See Configuration Straps for additional information. **Note:** These pins must be connected to either VDDP or VSS via a pull-up/pull-down resistor (10 kΩ, typical) to configure the desired SMI address.

Table 3-11. Power Pins

Name	Symbol	Description
+3.3V Switchable I/O Power Supply Input	VDDP	+3.3V I/O power supply input. When in sleep mode, this supply must be disabled.
+3.3V Continuous VDDAU Power Supply Input	VDDAU	+3.3V continuous VDDAU power supply input. **Note:** This supply must be provided during sleep mode. **Note:** When wake/sleep support is not used, this pin is connected to the same supply as VDDA.
+3.3V Switchable Analog Power Supply Input	VDDA	+3.3V analog power supply input. When in sleep mode, this supply must be disabled.
Ground	VSS	Common ground. **Note:** This exposed pad must be connected to the ground plane with a via array.

3.5. Configuration Straps

Configuration straps allow features of the device to be automatically configured to user defined values based on signal levels at reset. They are identified by an underlined signal name in the pin assignment lists. Configuration straps do not have internal resistors to prevent the signal from floating when unconnected.

Important: The configuration straps are shared on pins with output signals. Pins identified as configuration straps must always be pulled high to VDDP or low to VSS through an external resistor.

Important: External pull-up or pull-down resistors must be sized appropriately (10 kΩ, typical) to ensure that the configuration straps reach the required voltage level prior to latching at reset. If a pull-up resistor is used, it must be connected to VDDP.

Configuration straps are latched on Power-On Reset (POR) and pin reset (RESET_N). At the completion of the reset, that is when all power supplies are above the thresholds and the RESET_N pin is no longer asserted the signals are sampled and stored in the STRAP_CTRL0.

Note: When a soft reset occurs via the Soft Reset bit of the Basic Control Register, the configuration of the device is reloaded from the STRAP_CTRL0 register, not from the state of the external pins. To ensure proper operation, the values in this register should never be changed.

Related Links

STRAP_CTRL0

Strap Control 0 Register

3.5.1. MODE[0] and MODE[1] Configuration Straps

Only the LAN8670 and Revision C2 of the LAN8672 have configuration strap pins labeled MODE[0] and MODE[1]. These pins shall be configured as follows.

LAN8670 - Configuring Device Mode

The MODE[1:0] configuration straps determine whether the interface from the LAN8670 to the MAC is MII, RMII, or SC-MII, as shown in Table 3-12 below. The value can be read in the STRAP_CTRL0 register, if needed.

Table 3-12. MODE[1:0] Configuration Straps

MODE[1:0]	Definition
00b	Reserved
01b	PHY is placed in MII mode with 25 MHz crystal
10b	PHY is placed in RMII mode with 50 MHz REFCLKIN
11b	PHY is placed in Single Clock MII (SC-MII) mode with 25 MHz crystal. (LAN8670 only) The TXCLK and TXER pins are used for other features. The RXCLK pin becomes a single MII clock output.

LAN8672

The LAN8672, Revision C2, requires the MODE[0] pin to be pulled up, and the MODE[1] pin pulled down to ensure proper device operation

3.5.2. PHYAD[] Configuration Straps - Selecting a PHY Address

In some applications, especially in switches, multiple PHYs share the same SMI, that is MDIO and MDC pins. In these systems, the controller operating the pins must be able to manage each PHY separately. This is done by assigning each device a unique address. Each PHY checks each management data frame for a matching address and each PHY will only respond to frames with its correct address.

The PHYAD[] configuration straps enable a unique address to be assigned to each PHY. The hardware design of the PHYAD[] configuration straps shall ensure that the pins are pulled high to VDDP or low to ground through external resistors during a power on or hardware reset. Each PHY on the same MDIO interface must have a unique configuration of straps to provide a unique SMI address. This address is latched into an internal register at the end of a hardware reset. Any combination of bits is valid as an address.

Note: The LAN8670/2 have five PHYAD[4:0] pins for a total of 32 possible addresses. The LAN8671 has four PHYAD[3:0] pins for a total of 16 possible addresses.

3.6. Pin Configuration

Some pins of the LAN8670/1/2 may take on multiple functions depending on the device and mode. The functionality of five pins of the LAN8670 varies depending upon the device mode set by the MODE[1:0] Configuration Straps. Table 3-13 shows the functionality assigned to these pins based on the configured device mode.

Table 3-13. LAN8670 Device Mode Pin Configuration

	MII	SC-MII	RMII
Pin 11 (TXER/ACMA)	TXER[1]	ACMA	ACMA
Pin 12 (TXCLK/RXPI)	TXCLK[2]	RXPI	RXPI
Pin 15 (CRS)	CRS	CRS	Not Used
Pin 17 (RXCLK/SMCLK/WAKE_OUT)	RXCLK	SMCLK	WAKE_OUT
Pin 20 (RXDV/CRSDV)	RXDV	RXDV	CRSDV

Notes:
1. GPIO0 may be used for ACMA
2. GPIO0 may be used for RXPI

The GPIO0 pin is a multipurpose pin that can be configured as desired for multiple uses. This feature is useful for enabling specific features that would not otherwise be available for a specific device package or configuration. For example, Time Sensitive Networking (TSN) is supported through the ability to assert output signals when packets matching a specific pattern are transmitted and/or received. The GPIO0 pin may be configured as a Transmit Packet Indication (TXPI), Receive Packet Indication (RXPI), or Receive/Transmit Packet Indication (RXTXPI) output, as needed. Additionally, GPIO0 may be configured as an Application Controlled Media Access (ACMA) input pin.

The GPIO0 pin functionality is configured by writing to the GPIO0 Signal Select (GPIO0SS) field of the Pin Control (PINCTRL) register. The GPIO0 Signal Select should be configured prior to configuring and enabling the underlying Packet Pattern Matching or Application Controlled Media Access blocks.

Valid configurations for the GPIO0 pin depend on the device in use and its operating mode. When a dedicated native pin is available, this pin must be used for the provided function rather than the

GPIO0 pin. Table 3-14 below shows the valid configurations for the GPIO0 pin. When a pin number is shown, this is an invalid configuration for the GPIO0 Signal Select and the designated dedicated pin must be used instead.

For devices of revision D0 and onward, the configuration of the GPIO0 can be overwritten by the Link Status Control (LSCTL) Register if the Link Status Pin Select (LSPSEL) field is configured to use the GPIO0 pin.

Table 3-14. GPIO0 Signals

		LAN8670			LAN8671	LAN8672[1]
GPIO0SS	Signal	MII	SC-MII	RMII	RMII	MII
00	RXPI	✓	Pin 12	Pin 12	✓	Pin 14
01	TXPI	✓	✓	✓	✓	✓
10	RXTXPI	✓	✓	✓	✓	✓
11	ACMA	✓	Pin 11	Pin 11	✓	Pin 13

Note:
1. LAN8672 Revision C2, only.

Because the LAN8670 supports all operating modes, those being Media Independent Interface (MII), Single-Clock MII (SC-MII), and Reduced Media Independent Interface (RMII), it is important to know in which mode the device will be operated in. In MII mode, GPIO0 can be configured to any of the four possible functions. However, in SC-MII and RMII modes, it is limited to only be configured as TXPI or RXTXPI functionality.

For the LAN8671, GPIO0 may again fulfill any of the four possible configurations. To be noted here, the LAN8671 is only operated in RMII mode.

For the LAN8672, revision C2, GPIO0 may again only be configured as TXPI or RXTXPI, since this device only operates in MII mode.

4. Functional Descriptions

4.1. Media Independent Interface (MII)

The integrated Media Independent Interface (MII) provides a common interface between physical layer and MAC layer devices, adhering to IEEE Std 802.3-2018 *IEEE Standard for Ethernet*.

The MII includes the following interface signals:

- Transmit Data - TXD[3:0]
- Transmit Enable - TXEN
- Transmit Clock - TXCLK
- Transmit Error - TXER
- Receive Data - RXD[3:0]
- Receive Data Valid - RXDV
- Receive Clock - RXCLK
- Receive Error - RXER
- Carrier Sense - CRS
- Collision Detect - COL

In MII mode, on the transmit path, the LAN8670/2 drives the transmit clock, TXCLK, to the controller. The controller synchronizes the transmit data to the rising edge of TXCLK and drives TXEN high to indicate valid transmit data on TXD[3:0]. The device will synchronously capture TXEN, TXER, and TXD[3:0] on the falling edge of TXCLK.

On the receive path, the device drives both the receive data, RXD[3:0], and the receive clock, RXCLK. The controller captures in the receive data on the rising edge of RXCLK when the device drives RXDV high. The device drives RXER high when a receive error is detected (e.g., an uncorrectable decoding error). The device synchronizes RXD[3:0], RXDV, and RXER to change on the falling edge of RXCLK.

The CRS and COL signals are asserted asynchronously to the clocks.

For timing information, refer to the *MII/SC-MII Timing* section. Refer to Clause 22 of the *IEEE Std 802.3 IEEE Standard for Ethernet* specification for additional MII information.

Note: Many modern controllers, often found on switches, implement a reduced pin MII assuming full-duplex point-to-point operation. These interfaces, known as *MII-Lite*, do not include the required CRS and COL signals for 10BASE-T1S half-duplex operation. Back-to-back connection of two half-duplex devices is also not supported due to the CRS and COL requirement.

Note: The connection of a 10 kΩ pull-down resistor on TXEN is recommended to prevent unintended transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization.

Related Links

MII/SC-MII Timing

4.1.1. Single Clock Media Independent Interface (SC-MII)

The Single Clock Media Independent Interface (SC-MII) provides a common interface between physical layer and MAC layer devices similar to the MII but with fewer pins while maintaining compatibility with the MII. The Single Clock MII combines the Transmit Clock (TXCLK) and Receive Clock (RXCLK) into a Single Media Clock (SMCLK) and does not include the Transmit Error (TXER) pin. The result is a reduction of two pins over the standard MII which may be used for additional features.

The Single Clock MII includes the following interface signals:

- Transmit Data - TXD[3:0]
- Transmit Enable - TXEN
- Receive Data - RXD[3:0]
- Receive Data Valid - RXDV
- Receive Error - RXER
- Single Media Clock - SMCLK
- Carrier Sense - CRS
- Collision Detect - COL

In Single Clock MII mode, the LAN8670 drives the Single Media Clock (SMCLK) to both the controller TXCLK and RXCLK input pins. On the transmit path, the controller synchronizes the transmit data to the rising edge of the SMCLK as received at its TXCLK input. The controller drives TXEN high to indicate valid transmit data on TXD[3:0]. The device will synchronously capture TXEN and TXD[3:0] on the falling edge of TXCLK. Support for TXER is not provided in Single Clock MII mode.

On the Single Clock MII receive path, the device drives receive data, RXD[3:0], synchronously to the Single Media Clock (SMCLK). When the device drives RXDV high, the controller captures in the receive data on the rising edge of SMCLK as received at its RXCLK input. The device drives RXER high when a receive error is detected (e.g., an uncorrectable decoding error). The device synchronizes RXD[3:0], RXDV, and RXER to change on the falling edge of SMCLK.

The CRS and COL signals are asserted asynchronously to the clocks.

Note: The Transmit Error (TXER) pin is not available in this mode.

Related Links
MII/SC-MII Timing

4.2. Reduced Media Independent Interface (RMII)

The integrated Reduced Media Independent Interface (RMII) provides a common low pin count interface between the physical layer and MAC layer devices, adhering to the *RMII Specification* Revision 1.2. RMII reduces the pin count of MII while retaining a serial management interface (MDIO/MDC) identical to MII. PLCA is supported through the RMII.

The RMII has the following characteristics:

- A single 50 MHz clock reference is used for both transmit and receive
- It provides independent 2-bit (di-bit) wide transmit and receive data paths

The RMII includes the following interface signals:

- Transmit Data - TXD[1:0]
- Transmit Enable - TXEN
- Receive Data - RXD[1:0]
- Receive Error - RXER
- Carrier Sense / Data Valid - CRSDV

For timing information, refer to the *RMII Timing* section. Refer to the *RMII Specification* Revision 1.2 for additional information.

When operating in RMII mode, the LAN8670/1 REFCLKIN pin must be connected to a 50 MHz reference clock source. This clock source may be driven by the MAC or from a common oscillator driving both the MAC and LAN8670/1. When a common oscillator is utilized, it is recommended to match the length of the PCB traces from the source to the LAN8670/1 and MAC to within 0.5 inches (13 mm). Care should be taken when laying out the board to prevent the LAN8670/1 clock from

becoming a victim of crosstalk as any noise introduced to the clock input of the LAN8670/1 could become radiated onto the network.

The CRSDV pin combines both carrier sense and receive data valid. On carrier sense, the CRSDV pin is asserted asynchronously to the 50 MHz reference clock. Thereafter, CRSDV is only negated synchronously to the reference clock. Carrier sense is indicated by the assertion of CRSDV during which the first di-bit of a data nibble is presented on RXD[1:0]. Similarly, receive data valid is indicated by the assertion of CRSDV when the second di-bit of a data nibble is presented on RXD[1:0]. See the *RMII Specification* Revision 1.2.

A collision is signaled on RMII by the assertion of carrier sense when the MAC is asserting TXEN. A half-duplex RMII MAC must be able to properly derive the collision indication from CRSDV and TXEN.

Note: The connection of a 10 kΩ pull-down resistor on TXEN is recommended to prevent unintended transmission if the MAC does not actively pull-down or drive this pin low at all times during its reset and initialization.

Related Links

RMII Timing

4.3. Serial Management Interface (SMI)

The Serial Management Interface (SMI) is used to control the device and obtain its status. This interface supports the standard PHY registers required by Clause 22 of *IEEE Std 802.3*, as well as "vendor-specific" registers allowed by the specification. Unimplemented registers will be read as hexadecimal "0000". Device registers are detailed in the *Register Descriptions* section.

At the system level, SMI provides two signals: MDIO and MDC. The MDC signal is an aperiodic clock provided by the station management entity (STA) host controller. MDIO is a bi-directional data SMI input/output signal that receives serial data (commands) from the STA and sends serial data (status) to the STA. The minimum time between edges of the MDC is 100 ns. There is no maximum time between edges. The minimum cycle time (i.e., the time between two consecutive rising or two consecutive falling edges) is 250 ns. These modest timing requirements allow this interface to be easily driven by the I/O port of a microcontroller. MDIO should be connected to VDDP via a pull-up resistor.

The data on the MDIO line is latched on the rising edge of the MDC. The management frame structure and timing is shown in the following figures. The timing relationships of the MDIO signals are further described in the *SMI Timing* section.

Figure 4-1. SMI Timing and Frame Structure - READ Cycle

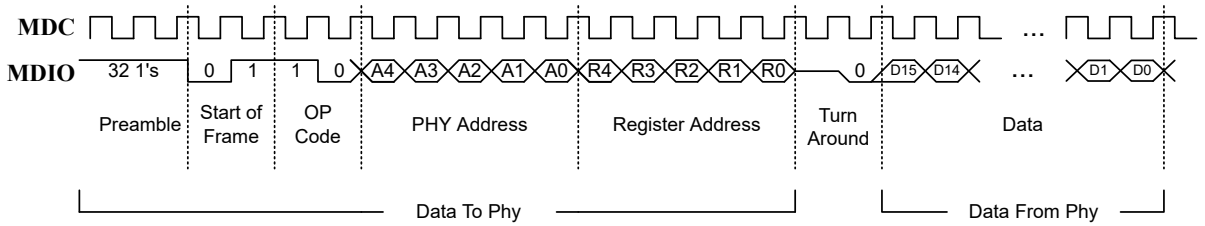
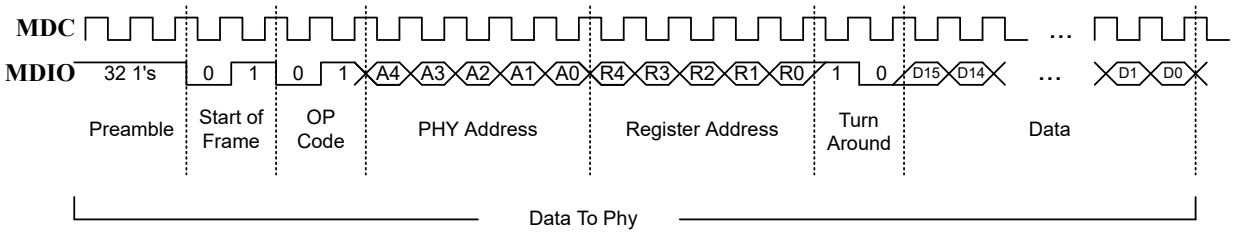


Figure 4-2. SMI Timing and Frame Structure - WRITE Cycle



Related Links

Register Descriptions

SMI Timing

4.3.1. Clause 45 Register Access

The LAN8670/1/2 only supports the MDIO management frame protocol defined in IEEE Std 802.3 Clause 22. Registers mapped into IEEE Std 802.3 Clause 45 MDIO Managed Devices (MMD) are accessed indirectly through the MMD Access Control (MMDCTRL) and MMD Access Address/Data (MMDAD) registers as described in IEEE Std 802.3 Annex 22D.

MMD Register Read

The following process is used to indirectly read Clause 45 registers using the Clause 22 access mechanism.

1. Write the MMD Access Control register with the MMD Function (FNCTN) field set to `00b` and the Device Address (DEVID) field with the MDIO Management Device (MMD) address.
2. Write the address of the desired register to be read into the MMD Access Address/Data register.
3. Write the MMD Access Control register with the MMD Function field set to `01b`, `10b`, or `11b`.
4. Read the contents of the MMD's selected register from the MMD Access Address/Data register.

Subsequent reads from the MMD Access Address/Data register will continue to reread and return the value of the selected MMD register when the MMD Function field is set to `01b` or `11b`. When the MMD Function field is set to `10b`, the MMD register address will be incremented following every read causing subsequent reads from the MMD Access Address/Data register to return data from the next higher MMD register.

MMD Register Write

The following process is used to indirectly write Clause 45 registers using the Clause 22 access mechanism.

1. Write the MMD Access Control register with the MMD Function (FNCTN) field set to `00b` and the Device Address (DEVID) field with the MDIO Management Device (MMD) address.
2. Write the address of the desired register to be written into the MMD Access Address/Data register.
3. Write the MMD Access Control register with the MMD Function field set to `01b`, `10b`, or `11b`.

Subsequent writes to the MMD Access Address/Data register will continue to write to the selected MMD register when the MMD Function field is set to `01b`. When the MMD Function field is set to `10b` or `11b`, the MMD register address will be incremented following every write causing subsequent writes to the MMD Access Address/Data register to write data to the next higher MMD register.

Related Links

MMDCTRL

MMD Access Control Register

MMDAD

MMD Access Address/Data Register

4.4. Interrupt Management

The family devices support multiple interrupt capabilities which are not part of the *IEEE Std 802.3* specification. An active low asynchronous interrupt signal may be generated on the IRQ_N pin when selected status events are detected as configured by the Interrupt Mask Registers.

To assert an interrupt on IRQ_N for a given event in the Status 1 (STS1) and Status 2 (STS2) registers, the corresponding mask bit in the Interrupt Mask 1 (IMASK1) and Interrupt Mask 2 (IMSK2) registers must be written to '0' to enable the interrupt. When an event occurs causing the associated status bit to be set, the IRQ_N pin will also be asserted. When the event to negate the status bit is true, or the corresponding bit in the Interrupt Mask Register is set disabling the interrupt, the IRQ_N pin will be deasserted.

All PHY interrupts are disabled (masked) following a reset with the exception of the Reset Complete interrupt mask bit. The Reset Complete interrupt mask is '0' by default such that the IRQ_N pin will be asserted following a reset event setting the Reset Complete status bit. This may be used to alert the station host controller that the device has been reset and is available for configuration.

Related Links

STS1

Status 1 Register

STS2

Status 2 Register

IMSK1

Interrupt Mask 1 Register

IMSK2

Interrupt Mask 2 Register

STS1 - Rev D

Status 1 Register - Rev D

STS2 - Rev D

Status 2 Register - Rev D

IMSK1 - Rev D

Interrupt Mask 1 Register - Rev D

IMSK2 - Rev D

Interrupt Mask 2 Register - Rev D

4.5. Resets

The device provides the chip-level reset sources described in the following sections.

4.5.1. Power-On Reset (POR)

A Power-On Reset occurs whenever power is initially applied to the device, or if power is removed and reapplied to the device. A timer within the device will assert the internal reset for approximately 2 ms. Configuration straps are loaded by this reset and must adhere to the timing requirements specified in Power-On Configuration Strap Timing when not using the external pin reset (RESET_N).

After power-on, the POR initially negates after the rising threshold is passed. In the event that the supply drops below the falling threshold, the POR asserts. The POR stays asserted until the rising threshold is once again crossed. The rising and falling thresholds are listed in Table 4-1.

Table 4-1. POR Supply Thresholds

POR	Rising Threshold[1]	Falling Threshold[1]
VDDA	2.5V	2.4V
VDDAU	2.5V	2.4V
1.8V[2]	1.6V	1.3V

Notes:

1. Rising and falling threshold voltages are design parameters and are neither tested nor characterized.
2. The internal 1.8V supply cannot be monitored externally.

Related Links

Power-On Configuration Strap Timing

4.5.2. External Pin Reset (RESET_N)

A hardware reset will occur when the RESET_N pin is asserted. The RESET_N pin must be connected externally to VDDP if unused. If used, the RESET_N pin must be driven for a minimum period as defined in the *RESET_N Configuration Strap Timing* section. Configuration straps are loaded by the reset.

Related Links

RESET_N Configuration Strap Timing

4.5.3. Software Reset

The software reset is available via the PHY Soft Reset (SW_RESET) bit in the Basic Control register.

Configuration straps are not loaded by a software reset.

Related Links

BASIC_CONTROL

Basic Control

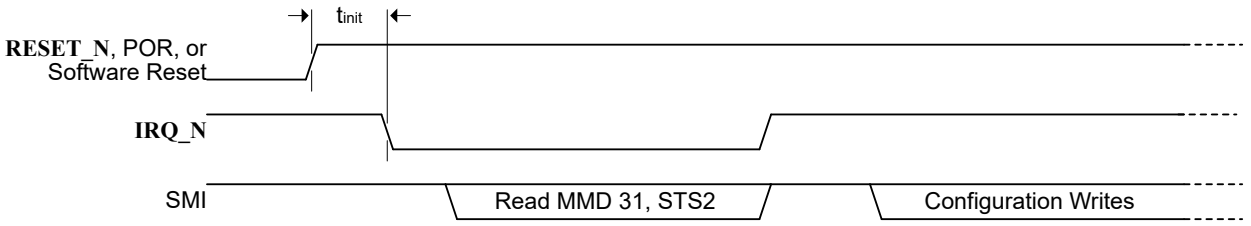
4.6. Initialization

When the device is in a reset state, the IRQ_N interrupt pin is high-impedance and will be pulled high through an external pull-up resistor to VDDP. Once all device reset sources are deasserted, the device will begin its internal initialization. The device will assert the Reset Complete (RESETC) bit in the Status 2 (STS2) register to indicate that it has completed its internal initialization and is ready for configuration. As the Reset Complete status is non-maskable, the IRQ_N pin will always be asserted and driven low following a device reset. The time required for the device to initialize once all reset sources are deasserted until the IRQ_N pin is asserted, t_{init}, is approximately 7 µs for product revision C2 and 900 µs for revision D0.

At the system level, the station host controller (STA) should respond to all assertions of the IRQ_N pin with a read of critical status registers through the Serial Management Interface (SMI), including

the Status 2 register. Upon reading of the Status 2 register, the pending Reset Complete status bit will be automatically cleared causing the IRQ_N pin to be released and pulled high again. The host controller may then continue to configure the device registers through the Serial Management Interface. See Figure 4-3 for an illustration of the device reset, initialization, and configuration process.

Figure 4-3. Initialization and Configuration Sequence



Related Links

STS2

Status 2 Register

Resets

4.7. Clock Manager

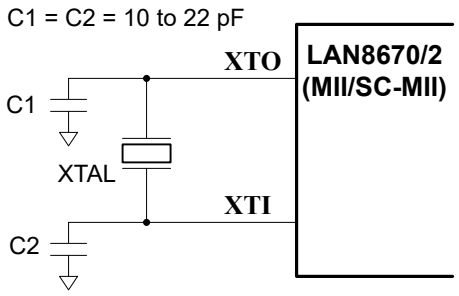
The Clock Manager generates the internal clocks from an external reference source. When using MII or SC-MII, the external source is applied to XTI/XTO. For RMII, the external source is applied to REFCLKIN.

Note: The pin XTI/REFCLKIN is used all configurations.

4.7.1. MII or SC-MII: Clock Source Applied to Crystal Pins (XTI/XTO)

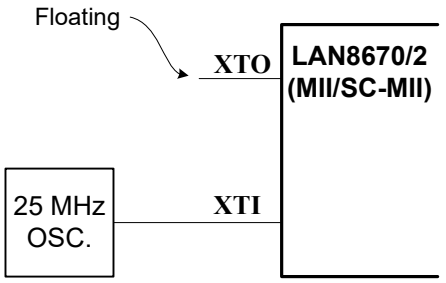
When using MII or SC-MII, most applications will connect a 25.0 MHz crystal to the XTI and XTO pins. Figure 4-4 depicts these pins and the external components required. The crystal should be in a fundamental, parallel resonant mode, with a frequency of 25.0 MHz.. Since the internal inverter/amplifier is operated in its linear region, external series resistors should not be used as they will lower the gain and could cause start-up problems. The device contains an internal ~1 MΩ resistance in parallel with the crystal amplifier to initiate oscillation, therefore an external resistance between XTO and XTI should not be used. Several factors must be considered when selecting a crystal including load capacitance, oscillator margin, cut, and operating temperature. Detailed specifications for the crystal can be found in the *Crystal Specifications* section and additional information be found in the *Crystal Oscillator Selection* section.

Figure 4-4. Crystal Input



For applications that do not require the full automotive temperature range, an external clock oscillator may be connected to the XTI pin in lieu of a crystal oscillator as shown in Figure 4-5. When used, the input clock must be between 1.8-3.3V amplitude. The clock source must be stable prior to the negation of reset and remain stable for proper operation. In addition, the XTO pin must be unconnected and floating with less than 10 pF stray capacitance. For details of oscillator requirements, refer to the section *Oscillator Clock Source - 25 MHz Oscillator*.

Figure 4-5. MII/SC-MII Clock Oscillator Input



Related Links

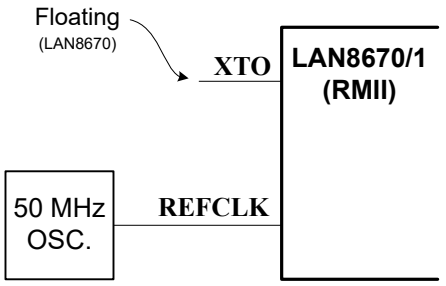
Crystal Oscillator Selection
Crystal Specifications
Oscillator Clock Source - 25 MHz Oscillator

4.7.2. Reference Clock (REFCLKIN)

The REFCLKIN pin is used to connect an external 50.0 MHz reference clock source for RMII operation. The input reference clock must be between 1.8-3.3V amplitude. The clock source must become stable after the assertion of reset and remain stable to begin proper operation. In addition, the LAN8670 XTO pin must be unconnected and floating.

For reference clock requirements refer to the section *RMII Clock Source - 50 MHz Oscillator*.

Figure 4-6. RMII Reference Clock Oscillator Input



Related Links

RMII Clock Source - 50 MHz Oscillator

4.8. Physical Layer Collision Avoidance (PLCA)

PLCA operates in conjunction with a CSMA/CD MAC to actively avoid collisions among half-duplex stations (known as PLCA *nodes*) allowing for greater network utilization. Each node on the network segment (i.e., collision domain) is assigned a unique *Local ID*. *Transmit opportunities* are then granted to each node in sequence based on their Local ID. The node configured as Local ID = 0 is known as the *PLCA coordinator*. The role of the PLCA coordinator is to transmit a periodic synchronizing BEACON onto the physical media. All other nodes are referred to as a *PLCA follower* as they follow the synchronization of the coordinator. Once the BEACON has been received on the segment, all nodes begin counting transmit opportunities beginning with zero. Nodes detect their

assigned transmit opportunity by counting the number of opportunities that have passed since the transmission of the BEACON by the PLCA coordinator. Each node may transmit when the number of transmit opportunities counted since the BEACON matches the Local ID assigned to the node. Within each transmit opportunity, the node assigned the current opportunity may either transmit a packet or yield. Once the node has transmitted a packet (or yielded), each node increments the transmit opportunity counter and the transmit opportunity goes to the next node. The first transmit opportunity of zero allows node with Local ID = 0 to transmit. Once a fixed number of transmit opportunities has been provided, the PLCA coordinator will transmit another BEACON starting the cycle over again. A BEACON followed by a fixed number of transmit opportunities is known as a *PLCA bus cycle*.

On multidrop topologies with multiple nodes connected to a shared media mixing segment, PLCA enables a fairness in opportunity to transmit such that one node cannot transmit more than one frame without each of the other nodes also being granted an opportunity to transmit. There are 2 exceptions that can be useful on multidrop segments where one or more nodes transmit more often than other nodes. PLCA allows individual nodes to be configured to transmit a burst of frames within a single transmit opportunity. The PHY can also assign individual nodes multiple transmit opportunities within the bus cycle.

PLCA is enabled by setting the PLCA Enable bit in the PLCA Control 0 (PLCA_CTRL0) register. The node Local ID is configured within the PLCA Local ID (ID) field of the PLCA Control 1 (PLCA_CTRL1) register and must be unique within the PLCA network segment to successfully avoid collisions. Additionally, the Local ID must be less than the number of transmit opportunities in each bus cycle in order to be granted a transmit opportunity (see the Node Count field of the PLCA Control 1 register). When the node is configured as the PLCA coordinator, then the number of transmit opportunities within each PLCA bus cycle (period between successive BEACON transmissions) is configured in the Node Count (NCNT) field of the PLCA Control 1 register.

The time for each transmit opportunity is configured within the PLCA Transmit Opportunity Timer (PLCA_TOTMR) register. The transmit opportunity timer must be set equal among all nodes in the PLCA collision domain to maintain synchronization among the nodes. The default transmit opportunity timer value, 3.2 µs, is appropriate for segments specified in IEEE 802.3 Clause 147 and should only be changed in special circumstances.

Important: The Transmit Opportunity timer must be configured identically across all nodes on the multidrop mixing segment.

CAUTION Improper configuration of the Transmit Opportunity timer may result in reduced network performance or collisions. Determination of the optimal Transmit Opportunity time requires knowledge of various delays of each of the vendor PHYs on the mixing segment and various physical layer propagation delay. It is recommended to leave this field at its default value unless a full evaluation of delays has been performed.

Tip: As collisions should not occur on a properly configured PLCA mixing segment, disabling collision detection is recommended when PLCA is enabled and active as it improves bus noise tolerance. See the *Transmit Collisions* and *PLCA Collision Detection* sections for more details.

When PLCA has been enabled on a node, the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register will indicate if the node is actively receiving a periodic PLCA BEACON. When the PST bit changes state, the PLCA Status Changed (PSTC) bit in the Status 1 (STS1) register will be set

and, optionally, may assert the IRQ_N pin. This may be useful for diagnosing a misbehaving PLCA network segment.

Related Links

PLCA Burst Mode
Multiple PLCA Transmit Opportunities
Transmit Collisions
PLCA Collision Detection
PLCA_CTRL0
PLCA Control 0 Register
PLCA_CTRL1
PLCA Control 1 Register
PLCA_TOTMR
PLCA Transmit Opportunity Timer Register
PLCA_STS
PLCA Status Register
STS1
Status 1 Register
STS1 - Rev D
Status 1 Register - Rev D

4.8.1. PLCA Burst Mode

Some applications, such as sensors or audio, may require the transmission of frequent small frames with a limited latency. As PLCA specifies only one transmit opportunity for each node in each bus cycle, these applications may experience significant latency when they are connected onto a multidrop mixing segment with applications that transmit large packets. For example, an audio application may require the transmission of eight stereo 16-bit audio samples as 64 byte packets every 167 µs with minimal latency. When another node on the segment transmits a 1500 byte packet it will occupy the channel for 1.2 ms. The audio application will therefore buffer seven audio packets during the time that the channel is occupied. With standard PLCA, the audio application will only be able to transmit one of its audio packets during the next PLCA bus cycle. The result is that each successive audio packet the audio application needs to transmit is delayed with increasing latency.

One solution to this problem is to allow specific nodes to transmit more than one packet during its transmit opportunity. This ability to transmit a burst of multiple packets allows the audio application in the above example to empty its buffers and transmit all audio packets that it has queued, preventing the latency of the audio packets to grow beyond a tolerable limit.

The ability to transmit packets in a burst is configurable individually for each node on the segment. The Maximum Burst Count (MAXBC) field in the PLCA Burst Mode (PLCA_BURST) register configures the maximum number of additional packets allowed to transmit in each of the node's transmit opportunities. This is in addition to the initial packet that may be transmitted by the node in its transmit opportunity. Additionally, the Burst Timer (BTMR) field configures the amount of time the node may transmit (COMMIT) to maintain a hold on its current transmit opportunity after transmitting a packet to allow the MAC to transmit an additional packet. Once this timer expires, the node will then yield the transmit opportunity to the next node.

Restriction: To prevent undesirable traffic shaping behavior, PLCA burst mode should not be used in conjunction with credit based traffic shaping.

Related Links

PLCA_BURST

PLCA Burst Mode Register

4.8.2. Multiple PLCA Transmit Opportunities

The PLCA burst mode allows a node to transmit multiple packets within its single transmit opportunity in each PLCA bus cycle. While transmitting a burst of packets in a single transmit opportunity bounds the maximum latency to the period of a PLCA bus cycle, the latency may be further reduced by allowing a node multiple transmit opportunities in each PLCA bus cycle. This allows the same node to transmit multiple frames evenly spread in time throughout the PLCA bus cycle. This is accomplished by assigning multiple Local IDs to the node thereby allowing it multiple transmit opportunities. When the transmit opportunity counter matches any one of the multiple Local IDs assigned to the node, the node may then transmit a packet or yield the transmit opportunity.

The PHY supports the assignment of up to eight additional transmit opportunities per PLCA bus cycle. The additional transmit opportunity Local IDs are configured in the ID1-ID8 fields of the PLCA Multiple ID 0-3 (MULTID0-MULTID3) registers.

The Clause 4 compliant MAC requires an inter-packet gap (IPG) of at least 9.6 µs (96 bits) following the transmission of one packet before it will transmit another packet. Should consecutive transmit opportunities be assigned to the same node, transmit opportunities following a packet transmission will not be used until after the inter-packet gap has expired. For best performance when assigning multiple transmit opportunities to the same node it is therefore recommended that they should be interleaved with transmit opportunities assigned to other nodes.

Related Links

MULTID0

PLCA Multiple ID 0 Register

MULTID1

PLCA Multiple ID 1 Register

MULTID2

PLCA Multiple ID 2 Register

MULTID3

PLCA Multiple ID 3 Register

4.8.3. PLCA Transmit Opportunity Skipping

PLCA transmit opportunity skipping is useful to limit the amount of data low-priority nodes may transmit onto the network. When transmit opportunity skipping is enabled, the PHY is configured to skip a number of PLCA transmit opportunities once a packet has been transmitted. The PHY will yield the skipped transmit opportunities and prevent the MAC from transmitting by asserting the MII CRS or RMII CRSDV pin. Once the specified number of transmit opportunities have been skipped, the PHY will re-enable normal PLCA operation of CRS/CRSDV and permit the MAC to transmit packets when its transmit opportunities occur.

PLCA transmit opportunity skipping is enabled by setting the PLCA Transmit Opportunity Skip Enable (TOSKPEN) bit in the PLCA Skip Control (PLCASKPCTL) register. The number of transmit opportunities to skip after transmitting a packet is configured in the PLCA Transmit Opportunity Skip (PLCATOSKP) register.

Restriction: To prevent undesirable traffic shaping behavior, PLCA transmit opportunity skipping should not be used in conjunction with credit based traffic shaping.

Related Links

PLCASKPCTL

PLCA Skip Control Register

PLCATOSKP

PLCA Transmit Opportunity Skip Register

4.8.4. Physical Layer Collision Avoidance (PLCA) Diagnostics

The PHY implements a number of features useful to the detection of PLCA misconfiguration on the network segment. These features include error status indications and event counters.

For revision C2 and earlier products, the PLCA error status indicators are located in the Status 1 (STS1) register. Each indication also has an associated interrupt mask bit in the Interrupt Mask 1 (IMSK1) register to enable an assertion of the interrupt on IRQ_N pin to the station host controller when the event is detected.

Revision D0 of the device implements the PLCA error status indicators in the OPEN Alliance standard PLCA Diagnostics (PLCA_DIAG) register. When one of these PLCA diagnostic bits is set, the PLCA Diagnostic (PLCADIAG) bit in the Status 1 (STS1 - Rev D0) register is set. The PLCA Diagnostic Mask (PLCADIAGM) bit in the Interrupt Mask 1 (IMSK1 - Rev D0) register may be written to '0' to enable an assertion of the interrupt on IRQ_N pin to the station host controller when the PLCADIAG status bit is set.

Each node of a PLCA segment must be assigned a unique Local ID to properly avoid collisions. The device has the ability to detect that another node is assigned the same Local ID by detecting the reception of a packet from the network during its assigned transmit opportunity. When this condition occurs, the Receive in Transmit Opportunity (RXINTO) status bit is set. Additionally, should a collision be detected while the device is transmitting in its assigned transmit opportunity, the Transmit Collision (TXCOL) status bit will be set.

Multiple nodes configured and acting as PLCA Coordinators also cause problems. Multiple Coordinators on the mixing segment will each transmit a BEACON according to its own PLCA bus cycle and timing. The result is that each Coordinator will receive BEACONs that it did not transmit. When configured as a PLCA Coordinator, it will set the Unexpected BEACON Received (UNEXPB) status bit to indicate the presence of another Coordinator on the network segment.

The PLCA Coordinator must be configured with the correct number of nodes on the segment to permit the proper number of transmit opportunities per bus cycle. If the Coordinator is configured to allow for too few transmit opportunities between BEACONs, Follower nodes may not have access to their assigned transmit opportunity. When the device is operating as a PLCA Follower, if it detects a BEACON before its assigned transmit opportunity occurs then the BEACON Received Before Transmit Opportunity (BCNBFTO) status bit is set to indicate that the configured PLCA bus cycle is too small to allow the Follower to transmit.

When configured as a PLCA Follower, the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register will be set as long as BEACONs are regularly being received from a Coordinator. If BEACONs are not received by the device it will continue incrementing its transmit opportunity counter. When the transmit opportunity counter reaches the maximum count of 255, it will then stop incrementing and a 13 ms timer is started. If no BEACON is received after the timer expires, the PLCA Status bit will be cleared. When the PLCA Status bit is zero, the device will revert to CSMA/CD operation with PLCA deactivated. Once a BEACON is received the device will set the PLCA Status bit and return to normal PLCA operation. Refer to Clause 148 of the *IEEE Std 802.3* specification for additional details. When the PLCA Status bit changes, the PLCA Status Changed (PSTC) bit in the Status 1 register is set and will assert the IRQ_N pin, if enabled in the Interrupt Mask 1 register.

The number of transmit opportunities in the PLCA bus cycle may be determined by reading the Maximum ID (MAXID) field of the PLCA Reconciliation Sublayer Status (PRSSTS) register. The MAXID field is updated at the end of each bus cycle. When read it will contain the number of transmit opportunities the PLCA coordinator allowed in the previous bus cycle.

Two event counters are implemented to aid the host controller in monitoring PLCA on the segment. These counters include a transmit opportunity counter and a BEACON counter. Each counter is enabled by setting the corresponding enable bit in the Counter Control (CTRCTRL) register. Writing a '1' to the Transmit Opportunity Counter Enable (TOCTRE) bit enables the transmit opportunity counter. The BEACON Counter Enable (BCNCTRE) bit enables the BEACON counter when set.

When enabled, the Transmit Opportunity Count High/Low (TOCNTH/TOCNTL) registers will contain the number of transmit opportunities the local PHY could have used to transmit since the last read. By polling the counter, the host controller can monitor that PLCA is active and that the PHY can transmit packets when needed.

Similarly, the BEACON Count High/Low (BCNCNTH/BCNCNTL) register contains the number of received BEACONs since the last read. The host controller can poll this counter to monitor the health of the PLCA Coordinator.

Related Links

STS1
Status 1 Register

IMSK1
Interrupt Mask 1 Register

STS1 - Rev D
Status 1 Register - Rev D

IMSK1 - Rev D
Interrupt Mask 1 Register - Rev D

PLCA_STS
PLCA Status Register

PLCA_DIAG - Rev D
PLCA Diagnostics Register - Rev D

PRSSTS
PLCA Reconciliation Sublayer Status

CTRCTRL
Counter Control Register

TOCNTH
Transmit Opportunity Count (High)

TOCNTL
Transmit Opportunity Count (Low)

BCNCNTH
BEACON Count (High)

BCNCNTL
BEACON Count (Low)

4.8.5. Transmit Collisions

By their very nature, transmitters on pure CSMA/CD networks (without PLCA) will at times collide at a rate dependent on the utilization of the network traffic on the mixing segment collision domain. As a result, many media access controllers (MACs) include collision counters so the station host controller can monitor the performance of the network segment. When PLCA is enabled the physical collisions of multiple transmitters are avoided. While PLCA prevents physical collisions on the physical media, as a part of normal operation the PLCA RS will at times assert a logical, or false, collision to the MAC to align the MAC's transmission with the PHY's transmit opportunity.

These PLCA logical collisions will be counted by a MAC collision counter and lead the host controller to the wrong conclusion about the state of collisions on the network segment. The PHY therefore contains an internal physical collision counter. The host controller can monitor the number of

physical collisions the PHY has encountered when transmitting packets onto the network by reading the Corrupted Transmit Count (CORTXCNT) in the 10BASE-T1S PCS Diagnostic 2 (T1SPCSDIAG2) register. Additionally, when the PHY detects a collision while transmitting the Transmit Collision Status (TXCOL) bit in the Status 1 (STS1) register is set. If the Transmit Collision Interrupt Mask (TXCOLM) is enabled in the Interrupt Mask 1 (IMSK1) register then the IRQ_N pin will assert. In a properly configured and operating PLCA mixing segment, no transmit collisions will be detected and the transmit collision counter will remain zero.

For devices of revision D0 and later, it is possible to disable the CORTXCNT physical collision detection counter as well as the signaling of collisions to the MAC via the MII or RMII. These settings are only available while a '1' is written into the Collision Detect Enable (CDEN) bin in the Collision Detector Control 0 (CDCTL0) register enabling the detection of physical collisions on the medium. These configuration options are controlled by the Collision Counting and MAC Forwarding Configuration (CCMFC) bit field of the CDCTL0 register and enables the device to be configured according to the IEEE default or the Open Alliance default settings. See Table 4-2 shows the collision counting and signaling options.

Table 4-2. Collision Counting and MAC Forwarding Configuration

CDEN	CCMFC[1]	CCMFC[0]	Comment
0	X	X	Collision Detection disabled
1	0	0	IEEE default: Collisions counted and forwarded to the MAC
1	X	1	OA default: Collisions counted and forwarded to the MAC when PLCA_Status ≠ OK Collisions neither counted nor forwarded to the MAC when PLCA_Status = OK
1	1	0	Collisions counted and forwarded to the MAC when PLCA_Status ≠ OK Collisions counted but *not* forwarded to the MAC when PLCA_Status = OK

Related Links

PLCA Collision Detection

T1SPCSDIAG2

10BASE-T1S PCS Diagnostic 2

STS1

Status 1 Register

IMSK1

Interrupt Mask 1 Register

STS1 - Rev D

Status 1 Register - Rev D

IMSK1 - Rev D

Interrupt Mask 1 Register - Rev D

CDCTL0 - Rev D

Collision Detector Control 0 Register - Rev D

4.9. Application Controlled Media Access (ACMA)

Physical Layer Collision Avoidance (PLCA) improves upon traditional CSMA/CD network utilization by eliminating collisions while also providing determinism for packet transmission. A customized media access method may be appropriate in systems requiring more control over latency or bandwidth allocation. The PHY provides Application Controlled Media Access (ACMA) as an alternative to PLCA or CSMA/CD which allows implementation of custom scheduled access to the medium for applications requiring a fixed, deterministic latency. This could be used to implement a time-division multiple access (TDMA) method that allocates a specific transmit time slot for each station on the shared medium. Such a system avoids collisions, while reserving fixed bandwidth for each station and guarantees access latency to provide deterministic network behavior. A system using ACMA can

even allow synchronization of the time slots across a network using the IEEE Std 802.1AS generalized Precision Time Protocol (gPTP).

The ACMA mode is enabled by setting the ACMA Enable (ACMAEN) bit in the ACMA Control (ACMACTL) register. The assertion level of the ACMA input is configured by the ACMA Polarity (ACMAPOL) bit in the Pin Control (PINCTRL) register.

Important: Only revision C2 of the LAN8672 has a dedicated pin for ACMA input. Refer to the *Pin Configuration* section of this document to ensure proper pin selection and configuration for the LAN8670 or LAN8671.

When enabled, the ACMA signal is used to control transmit access to the medium. If the ACMA input is not asserted, transmission from the MAC is held off by signaling carrier sense through the assertion of the MII CRS or RMII CRSDV pin. Only when the ACMA signal is asserted is the MAC allowed to transmit by negating CRS/CRSDV. If the MAC has a frame to send, it asserts TXEN and begins transmitting. The MAC can send multiple packets if the ACMA assertion time is long enough to permit it. Once transmission of a packet has started, the full packet will be transmitted regardless of the status of ACMA.

The timing of the ACMA signals depends on the bandwidth requirements and numbers of transmitters on the mixing segment. To work with the greatest variety of MACs, the minimum recommended ACMA enable pulse width is 10 µs. This ensures that the device will have more than the inter-packet gap of 9.6 µs to enable TXEN after release of carrier sense. The minimum period between consecutive time slots on the mixing segment must not be less than the time to transmit the largest Ethernet packet or sequence of packets plus 9.6 µs.

Note: Other stations on the network must not assert ACMA until the previous time slot has expired. Failure to meet this constraint may result in collisions on the network or the loss of ability to transmit within the assigned time slot.

Collisions will not occur on properly engineered and synchronized ACMA. However, to aid in development and debug, when ACMA is enabled the device will set the Unexpected Carrier Sense (UNCRS) status bit in the Status 1 (STS1) register if receive carrier is sensed from the network when the ACMA pin is asserted. If needed, IRQ_N can be asserted when this status bit is asserted; this is configured by writing a 0 into the UNCRSM bit of the IMSK1 register.

Related Links

ACMACTL
Application Controlled Media Access Control Register

PINCTRL
Pin Control Register

Pin Configuration

STS1
Status 1 Register

IMSK1
Interrupt Mask 1 Register

4.10. Credit Based Traffic Shaping

The PHY implements a hardware credit based traffic shaper (CBS) to control the station's transmit bandwidth. A hardware credit counter is used to enable and disable the ability to transmit packets onto the medium. The PHY decrements the credit counter during transmit and increments the counter when the PHY is receiving data or the medium is idle. When the credit counter is below the stop threshold, the PHY does not have enough credits to transmit. The PHY will then hold the MAC off from transmitting by asserting the MII CRS or RMII CRSDV pin. When the PHY is not transmitting, it will accumulate credits. Once the credit counter exceeds the start threshold, CRS/CRSDV will operate normally. Once the PHY allows the MAC to begin transmitting a packet, the entire packet will be transmitted even if the credit counter decrements below the stop threshold while it is transmitting.

The credit based traffic shaper is enabled by setting the CBS Enable (CBSEN) bit in the Credit Based Shaper Control (CBSCTRL) register. The credit based traffic shaper may be used with or without PLCA.

The transmit stop threshold is configurable in the Stop Threshold (STOPTHR) bit field in the Credit Based Shaper Stop Threshold High/Low (CBSSPTHH/CBSSPTHL) registers. The Start Threshold (STARTTHR) field in the Credit Based Shaper Start Threshold High/Low (CBSSTTHH/CBSSTTHL) registers is used to configure the transmit start threshold.

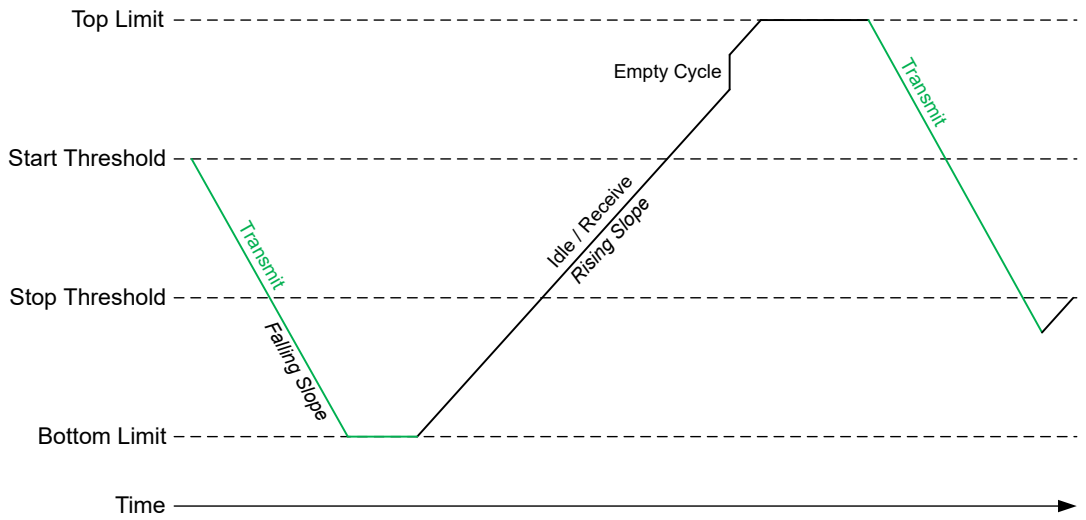
The Falling Slope (FALLSLP) field of the Credit Based Shaper Slope Control (CBSSLPCTL) register configures the rate at which the credit counter loses credits when transmitting. Similarly, the Rising Slope (RISESLP) field configures the rate at which the credit counter will accumulate credits when the medium is idle or the PHY is receiving data. When PLCA is enabled, credits may additionally be accumulated at an accelerated rate when no transmission is detected within each PLCA bus cycle. The rate at which credits are accumulated for each empty PLCA bus cycle is configured by the Empty Cycle Credits (ECCRDS) field of the Credit Based Shaper Control register.

The credit counter will saturate and stop accumulating credits when the limit set by the Top Limit (TOPLIMIT) field in the Credit Based Shaper Top Limit High/Low (CBSTPLMTH/CBSTPLMTL) registers is reached. Likewise, the credit counter will saturate and stop losing credits at the limit set by the Bottom Limit (BOTLIMIT) field in the Credit Based Shaper Bottom Limit High/Low (CBSBTLMTH/CBSBTLMTL) registers. This prevents the credit counter from incrementing or decrementing into an overflow condition. The saturation of the credit counter also prevents the PHY from delaying transmission of a packet too long or transmitting a burst of packets. For example, the PHY may lose a significant number of credits by transmitting a maximal size packet. If the credit counter were not limited by a lower bound, it may take a significant amount of time for the PHY to accumulate enough credits to transmit another packet. Similarly, if the PHY has not transmitted in a long time, it may accumulate too many credits allowing it to transmit multiple frames if the credit counter were not limited by an upper bound. By controlling the top and bottom limits of the credit counter, the credit based shaper may be configured to transmit at the desired rate.

For debug or monitoring purposes, the current value of the credit counter may be obtained by reading the Credit Counter (CREDITCTR) field of the Credit Based Shaper Counter High/Low (CBSCRCTRH/CBSCRCTRL) registers.

Restriction: To prevent undesirable traffic shaping behavior, the credit based shaper should not be used in conjunction with PLCA transmit opportunity skipping or with PLCA burst mode.

Figure 4-7. Credit Based Shaping Example



Related Links

CBSCTRL

Credit Based Shaper Control Register

CBSSTTHH

Credit Based Shaper Start Threshold (High) Register

CBSSTTHL

Credit Based Shaper Start Threshold (Low) Register

CBSSPTHH

Credit Based Shaper Stop Threshold (High) Register

CBSSPTHL

Credit Based Shaper Stop Threshold (Low) Register

CBSSLPCTL

Credit Based Shaper Slope Control Register

CBSTPLMTH

Credit Based Shaper Top Limit (High) Register

CBSTPLMTL

Credit Based Shaper Top Limit (Low) Register

CBSBTLMTH

Credit Based Shaper Bottom Limit (High) Register

CBSBTLMTL

Credit Based Shaper Bottom Limit (Low) Register

CBSCRCTRH

Credit Based Shaper Credit Counter (High) Register

CBSCRCTRL

Credit Based Shaper Credit Counter (Low) Register

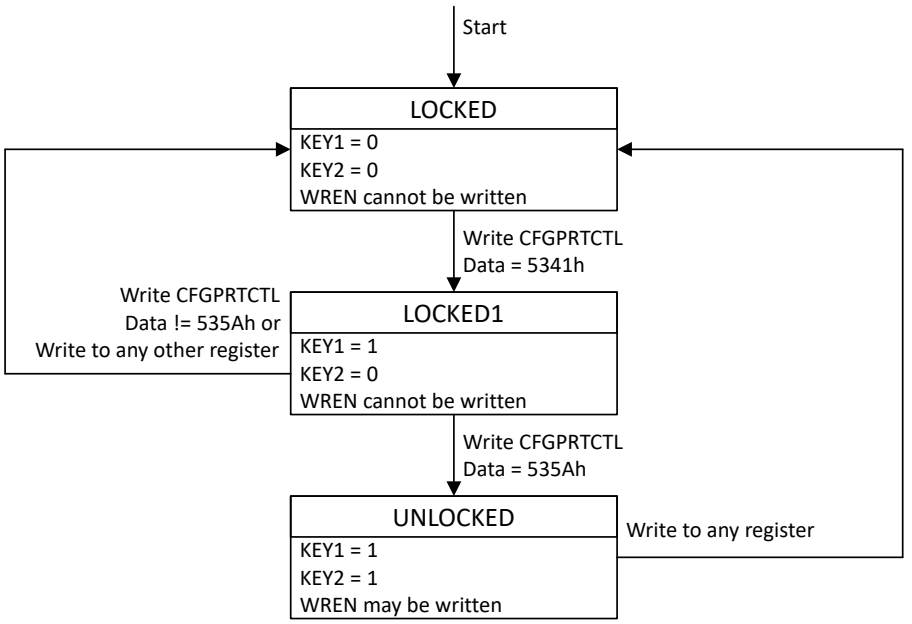
4.11. Configuration Protection

Once the PHY has been configured, writes to register bit fields by the station host controller are typically no longer necessary. However, should the host controller encounter a fault, it is possible that incorrect firmware execution may result in errant writes to PHY registers resulting in misconfiguration that could interfere with system-wide communication among other nodes on the bus. For this reason, the PHY includes a feature to prevent writes to all registers once configuration by the host controller is complete.

The Write Enable (WREN) bit in the Configuration Protection Control (CFGPRTCTL) register enables and disables (blocks) writes to the configuration registers. Following reset, the Write Enable bit is set indicating that configuration protection is inactive and writing to all register bit fields is enabled. Once the host controller has configured the PHY, it must unlock the CFGPRTCTL register as described below before it may write a '0' to the Write Enable bit to activate configuration protection and disable writing to all configuration register bit fields preventing changes to the configuration. When configuration protection is active, the only PHY registers that may be written and modified are the Clause 22 MMD Control (MMDCTRL) and MMD Address/Data (MMDAD) registers. These are used to indirectly access registers within the various memory mapped devices, including the Configuration Protection Control register.

By default, the Configuration Protection Control register is locked and the Write Enable bit cannot be modified. Changing the Write Enable bit requires the Configuration Protection Control register to be unlocked. Unlocking the Configuration Protection Control register requires writing two unique key values in sequence to the Configuration Protection Control register. The host controller must first write a value of 5341h to the Configuration Protection Control register. Once written, the Key #1 Accepted (KEY1) status bit will be set. The host controller must then write a value of 535Ah to the Configuration Protection Control register resulting in the Key #2 Accepted (KEY2) status bit being set. If any value other than 535Ah is written after the first key value has been accepted, the LOCKED state is re-entered, the Key #1 Accepted status bit will be cleared and the unlocking process must be restarted. Additionally, writing to any register other than the Configuration Protection Control will also result in the register being locked again with the Key #1 Accepted status bit cleared. It is allowed to read this register before writing the second key to assure that the first key has been accepted. When both key values have been written in the correct sequence and accepted as indicated by both the KEY1 Accepted and KEY2 Accepted status bits being set, the Configuration Protection Control register is unlocked and the host controller may then write and modify the Write Enable bit, enabling or disabling writes to all register bit fields. When the Configuration Protection Control register is unlocked, a write to *any* register will cause the Configuration Protection Control register to immediately become locked again, this includes a write to the CFGPRTCTL register. If another register was written to when the CFGPRTCTL register is unlocked, it will become locked again and the WREN bit will remain the same as before being unlocked. See Figure 4-8.

Figure 4-8. Configuration Protection Control Register Lock/Unlock State Diagram



Related Links

CFGPRTCTL

Configuration Protection Control

4.12. Time Synchronization

This section describes how to use the PHY in networks that use layer 2 clock synchronization based on PTP messages over Ethernet.

4.12.1. Introduction to IEEE 802.1AS / IEEE 1588

Many end applications that are run on a network require a common time base; these applications are often called time-aware. Input sensor data needs timestamping for processing and analysis; motor and brake controls must be synchronized to control machines; chimes and lights are coordinated for a better user experience. IEEE Std 1588 describes the PTP protocol, which is used to synchronize clocks across a network. PTPv2 is a feature rich standard that allows for many variations, not all of which are compatible. IEEE Std 802.1AS specifies a subset of PTP, a *PTP profile*, called generalized Precision Time Protocol (gPTP) which is increasingly used in embedded systems. gPTP uses only layer 2 (Ethernet) synchronization, which relies on the precise timestamping of specific packets used to distribute clock and delay information across a network.

In a time-aware network, any given network segment, including a 10BASE-T1S multidrop segment, has one clock source. This source can be any element on the segment or it can be a time-aware bridge, which is synchronized to the main system clock elsewhere on the network. The clock source periodically broadcasts the current system time using the PTP SYNC message and captures the exact time at which the message is transmitted. The timestamp for the SYNC message is then provided to the clock followers, either directly in the SYNC packet, or in a separate FOLLOWUP packet. Other time aware devices on the network segment capture the time that the SYNC message arrives and use that, along with the information from the FOLLOWUP message when needed, to adjust their local clocks to match that of the clock source. In a time aware system with known, fixed network delays, it is possible to achieve very precise clock synchronization using only these messages.

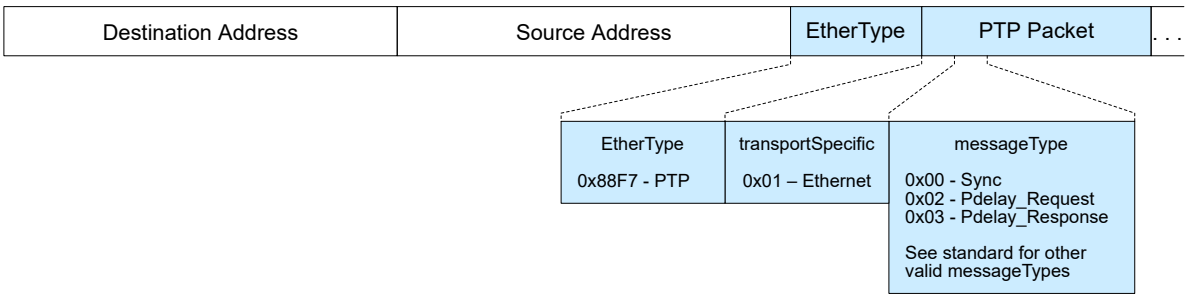
To account for network delays when they are not known, PTP includes peer delay message types, which are used in a similar manner to calculate the delay between the local clock source and each element on the segment. One of these messages, PDELAY_REQUEST requires precision

timestamping on egress from the network element and ingress to the local clock master, similar to that required on the SYNC message. The algorithm which calculates the delay between peers assumes that the delays are constant and symmetric; it can compensate for any fixed delay, including timestamping a packet at a fixed point later than the standard end of Start-of-Frame Delimiter (SFD).

4.12.1.1. PTP Message Format

PTP messages are transmitted in a standard Ethernet frame, which starts after the SFD with 6 bytes of Destination Address, and 6 bytes of source address. The next 2 bytes are the EtherType field, which indicates which protocol the payload represents. An EtherType field of 0x88F7 indicates that the packet is PTP over Ethernet. The next byte is fixed at 0x01 for PTP over Ethernet. The byte that follows is the PTP message type; the message types of interest are shown in Figure 4-9

Figure 4-9. Start of a PTP over Ethernet Frame



4.12.1.2. PTP and 10BASE-T1S

Effective time synchronization can be run over 10BASE-T1S networks. There are two issues that need to be considered during implementation.

- When using delay calculations, timestamps need to be taken where the delay is constant. The timestamp for packet transmission normally occurs at the end of the SFD on the MII/RMII interface. When the MAC delivers the packet to a 10BASE-T1S PHY, however, there is a variable delay through the PHY when PLCA is enabled. PLCA requires the PHY to delay transmission of a packet until the next PLCA transmit opportunity. To have a constant delay, the transmit timestamp needs to be taken after the PLCA. Considering the receive timestamp, the MAC will only be able to create a timestamp to the resolution of the clock for the inbound data signal from the PHY, which is 400 ns for MII. The solution to both of these problems is to use the signal on the MDI to determine when to timestamp. The remainder of this section will discuss features of the PHY which enable this type of timestamping.
- While 802.1AS clearly defines the Sync and PDelay methods for full-duplex Ethernet links, there is not yet a clear definition for a shared medium, like 10BASE-T1S when used with PLCA in multidrop mode. All of the message types above are currently defined as multicast. Software workarounds to existing PTP processing are required until the standards are adapted for multidrop segments. These workarounds are beyond the scope of this document.

4.12.2. Identifying PTP Packets for Timestamping

The PHY supports the implementation of PTP over Ethernet within the station's host controller by being able to detect the exact time of transmission and reception of PTP messages. This is done by examining the bytes of a packet that contain the EtherType and the first 2 bytes of the PTP header, and signaling when the correct pattern is detected.

To configure the desired pattern on transmitted packets, the most significant byte of the desired value is written into the Transmit Match Pattern High (TXMPATH) register and the lower two octets of the match value is written into the Transmit Match Pattern Low (TXMPATL) register. As an

example, to match on a SYNC message, the EtherType value of 0x88F7 and PTP header value of 0x10 creates a 24-bit match value of 0x88F710. The value 0x88 is written into TXMPATH and the value 0xF710 is written into TXMPATL.

Configuring the receive pattern matcher is done in a similar manner but using Receive Match Pattern High (RXMPATH) register and Receive Match Pattern Low (RXMPATL) register.

Pattern matching can be used to support time synchronization in two different ways. Pattern match output pins can be used on both transmitted and received packets. MAC Transmit Time Stamp works directly with certain MACs. These are described in the next sections.

Related Links

TXMPATH

Transmit Match Pattern (High) Register

TXMPATL

Transmit Match Pattern (Low) Register

RXMPATH

Receive Match Pattern (High) Register

RXMPATL

Receive Match Pattern (Low) Register

4.12.3. Pattern Match Output Pins

When an outbound packet matches the configured transmit match pattern, the device can assert the Transmit Packet Indication (TXPI) signal. Similarly, the Receive Packet Indication (RXPI) signal can be asserted when an inbound packet matches the configured receive match pattern. Alternatively, the Receive/Transmit Packet Indication (RXTXPI) signal can be asserted when an inbound packet *or* an outbound packet matches the respective patterns. That is, RXTXPI is essentially the logical OR of the TXPI and RXPI internal signals. The station host controller can then use the signals on these pins to generate a time stamp.

The GPIO0 Source Select bit in the Pin Control (PINCTRL) register can be used to select either of the pattern matching signals TXPI, RXPI, or RXTXPI. In addition, revision C2 of the LAN8672 has a dedicated pin for RXPI, and the LAN8670 provides the RXPI signal on a separate pin only when in SC-MII or RMII modes. The TXPI Polarity (TXPIPOL) bit configures whether a rising or falling edge is used on TXPI to indicate a transmit packet match to the host controller. The RXPI Polarity (RXPIPOL) provides the same functionality for a receive patch match. When GPIO0 is configured as RXTXPI, the RXTXPI polarity is configured using the TXPI Polarity (TXPIPOL) bit.

Once the transmit packet pattern matcher is configured, the transmit packet pattern matcher is enabled by setting the Transmit Packet Match Enable (TXME) bit in the Transmit Match Control (TXMCTL) register. When the device detects that a packet being transmitted matches, the TXPI signal will be asserted. Similarly, the receive packet pattern matcher is enabled by setting the Receive Packet Match Enable (RXME) bit in the Receive Match Control (RXMCTL) register.

The pattern match outputs are delayed relative to the end of the Start-of-Stream Delimiter (SSD) as it is present on the pins. This delay has a fixed amount through the analog and digital circuit paths of the device, and a jitter component. See the following table for details.

Figure 4-10. Delays from SSD to Pattern Match Output Pin

Description	Fixed Delay	Delay Jitter
Transmitter: End of SSD transmitted to TXPI asserted	18 080 ns	0 - 20 ns
Receiver: End of SSD received to RXPI asserted	24 080 ns	0 - 45 ns

Related Links

PINCTRL

Pin Control Register

TXMCTL

Transmit Match Control Register

RXMCTL

Receive Match Control Register

4.12.4. MAC Timestamping

Many MACs have special hardware dedicated to timestamping outbound and inbound packets. In this mode, the MAC assumes that the delay through the PHY is nearly constant. While PLCA has no impact on inbound packets, on transmitted packets, delay through the PLCA RS can range from 0, if the transmit packet arrives during the transmit opportunity, to as high as 39.6 µs, if the PLCA RS delay line is completely full. The PHY incorporates a unique feature to allow the MAC to transmit PTP frames through the PLCA-enabled PHY without incurring any PLCA delay.

MAC transmit timestamping support requires that the pattern matcher is programmed to match the desired outbound packet, usually PTP SYNC. When this feature is enabled, any time that an outbound packet is detected that matches the pattern and will encounter a delay in the PLCA RS, the PHY will emulate a collision to the MAC causing the MAC to terminate transmission of the current packet, producing a JAM signal back off to wait to retransmit. The PLCA algorithm will then assert carrier sense to hold off the MAC from attempting to retransmit the packet until the back-off has expired. When the next PLCA transmit opportunity has arrived, the PHY will begin to transmit COMMIT symbols onto the network to claim the transmit opportunity while releasing carrier sense to the MAC. Once carrier sense has been released, the MAC will wait for the mandatory 9.6 µs inter-packet gap delay and retransmit the packet. This time the packet will be transmitted directly through the PLCA RS to the network without delay, allowing the MAC to capture an accurate time stamp of the packet's departure to the network.

This mode of MAC timestamping support is enabled by setting the MAC Transmit Time Stamp Enable (MACTXTSE) bit in the Transmit Match Control (TXMCTL) Register. Pattern matching must be configured as above for the desired PTP message.

Note: When the PHY emulates a collision to the MAC, it may be possible that the beginning of the outbound packet has started being transmitted to the network. In this case, the PHY will continue to transmit a repeating '01' pattern until at least 64 bytes has been transmitted. The PHY will then terminate the fragment with an End-of-Stream Error Delimiter (ESDERR) to indicate to the receiver that the frame should be ignored.

Restriction: The MAC Transmit Time Stamp Enable (MACTXTSE) bit cannot be set at the same time that the Transmit Match Enable (TXME) bit is set. The device cannot provide transmit packet indication output to TXPI when the MAC Transmit Time Stamp feature is enabled.

Related Links

TXMCTL

Transmit Match Control Register

4.13. Sleep Mode - Rev C2

NOTICE The following section applies to devices of revision C2 and earlier. For newer devices, see the section *Sleep Mode - Rev D0*.

The PHY provides an ultra-low power (typically less than 140 µW) sleep mode based on the OPEN Alliance TC10 specifications. In this mode, it will release the INH pin to allow shutdown of most external power supplies. Only the uninterrupted supply VDDAU remains active to monitor and react to user selectable wake events. After a wake event, INH is asserted and the remaining power supplies are re-enabled. Since the INH pin can control power supplies shared with other devices, this feature allows for an entire node to enter a low power state, and be awakened by external events.

This section will describe

- how the INH pin can be used to control the shutdown of power supplies, including using a delay feature
- how to select what events will wake the device from sleep
- how to enter sleep mode, including how to configure activity timeouts
- how the device will behave upon wake and what actions are required

Related Links

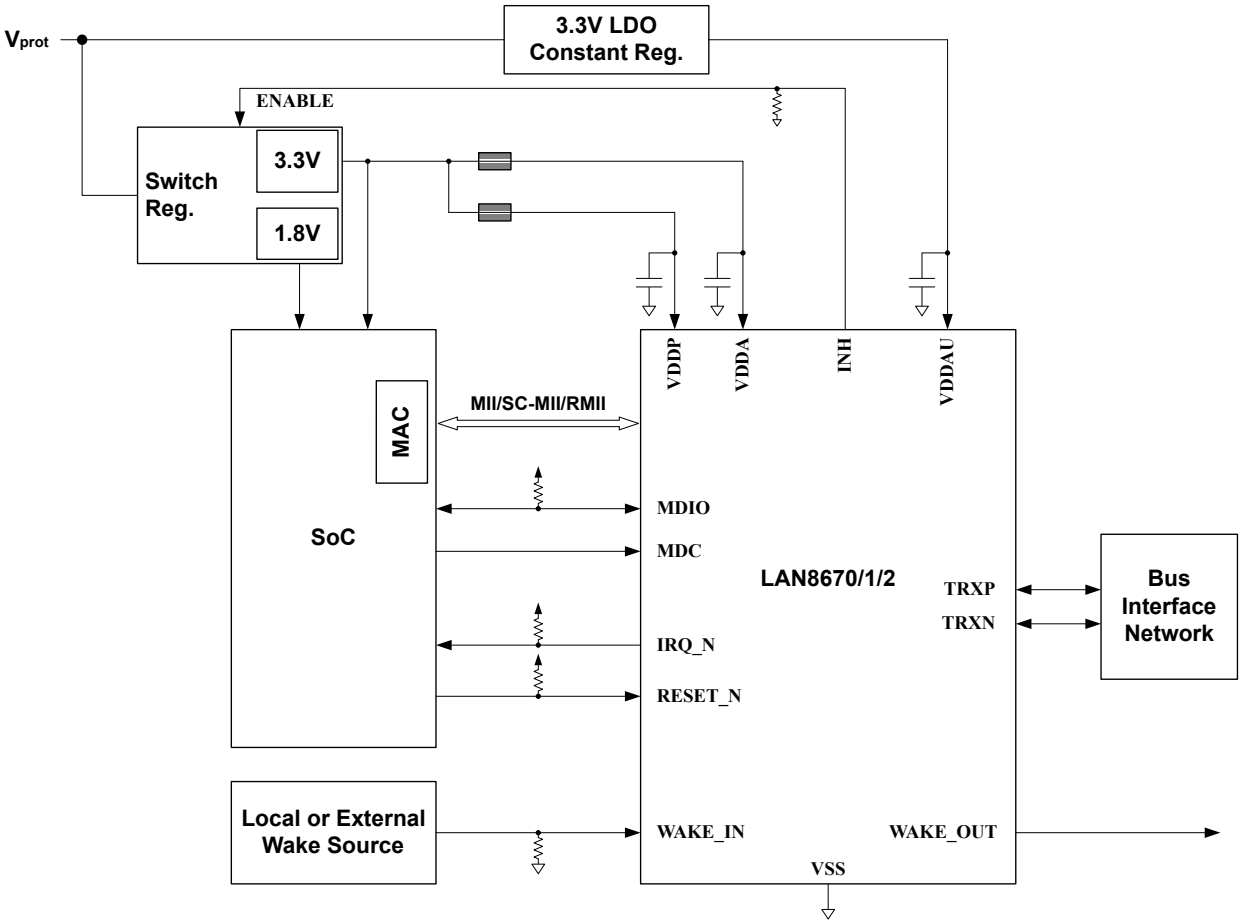
Sleep Mode - Rev D0

4.13.1. Sleep Mode and System Power Management

NOTICE This section applies to devices of revision C2 and earlier.

Figure 4-11 shows an example of how power should be supplied in a system that will use the low-power sleep mode of the device. In this diagram, VDDAU is provided by a constant supply, so that it is always enabled, even during sleep mode. On system power-up, once this supply is active, the INH pin will be asserted so that its active high output can drive the enable pins of the external switchable supplies for VDDA and VDDP.

Figure 4-11. Sleep Mode Example System

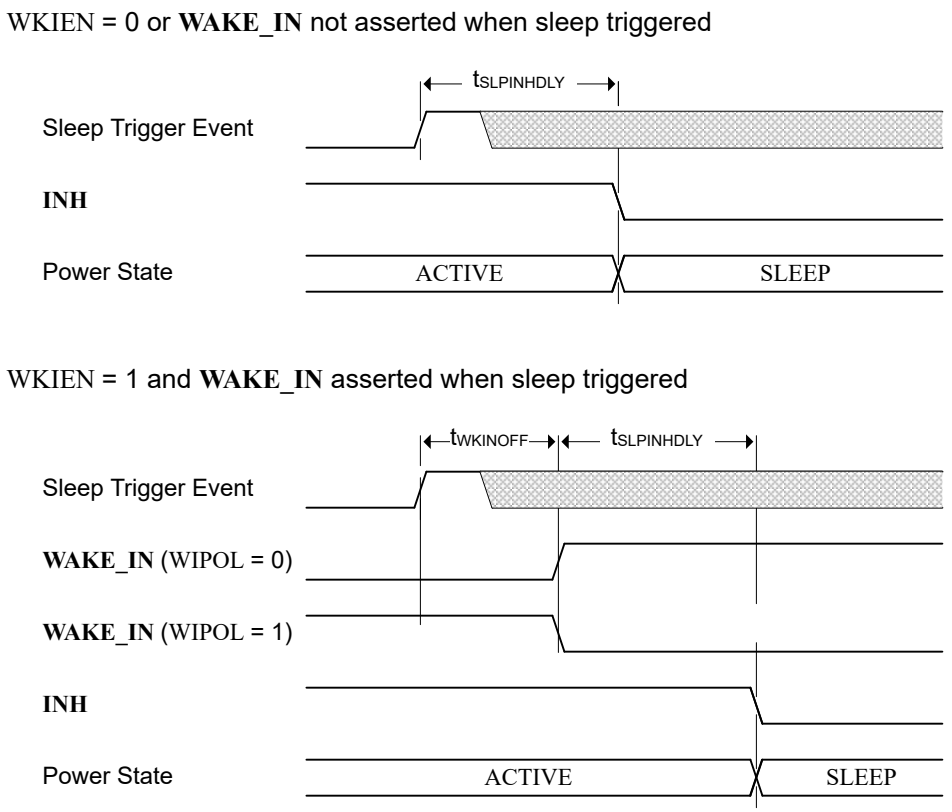


After the device enters sleep mode, the INH pin will enter a high-impedance state. The external resistor will pull the signal down to ground, which will then disable any voltage sources controlled by INH. This can be used to disable power to additional devices, including, when needed, the station host controller.

Important: Before entering SLEEP mode, the desired device wake configuration must be configured . It is recommended that this mode is configured immediately after a reset. Details can be found in the *Configuring Wake-up* section.

Some systems may require a delay between the trigger for the start of sleep mode and disable of the local power supplies, for example, to allow for other nodes on the mixing segment to go quiet. Delay timing is configured with the Sleep Inhibit Delay (SLPINHDLY) field of the Sleep Control 0 (SLPCTL0) register. If wake from the WAKE_IN pin is enabled (WKIEN=1), the WAKE_IN pin must be deasserted before the Sleep Inhibit Delay timer will be started. See Figure 4-12 for a diagram illustrating the timing from when SLEEP state is commanded until the INH pin is released and the SLEEP state is entered.

Figure 4-12. Sleep Timing



In sleep mode, a small amount of current is drawn from VDDAU to monitor for a wake condition. The wake condition can be a WAKE_IN pulse provided from another device, or a signal on the wire harness from another node on 10BASE-T1S network. After a wake condition is detected, INH is actively driven high, enabling the external power supplies, which should be fully powered within 1 ms of INH being driven high according to the OPEN Alliance *10BASE-T1S Sleep/Wake-Up Specification*. Once all power supplies are above their thresholds, the device will behave as if it had been reset by the RESET_N pin, and will assert IRQ_N to signal that the device is ready to be configured as described in the *Initialization* section.

Note:
Once the device enters sleep, the VDDA and VDDP power supplies **must** be powered down prior to a wake-up event.

Important: To achieve maximum power savings and allow TC10 power goals to be met when in the SLEEP state, all power supplies except for VDDAU must be powered down.

Related Links
Configuring Wake-up
Initialization
SLPCTL0
Sleep Control 0 Register

4.13.2. Configuring Wake-up

NOTICE This section applies to devices of revision C2 and earlier.

The sleep/wake module is powered by the externally protected continuous VDDAU supply and detects a wake condition when the device is in the SLEEP state. This module monitors activity energy on the MDI interface and/or wake pulses on the WAKE_IN pin to determine if the device has received wake-up signaling. Once wake-up signaling has been received and validated, this module will drive the INH pin high to the VDDAU supply to enable the external switched power supplies.

Prior to entering the SLEEP state, the host controller must configure the device to select one or both of these wake methods.

4.13.2.1. MDI Wake-up Activity Detection - Rev C2

NOTICE This section applies to product LAN8670/1/2 revision C2 and earlier.

In these versions, MDI wake detection was **not** designed to meet the OPEN Alliance *10BASE-T1S Sleep/Wake-up Specification*, version 1.0. Received energy that is of sufficient length that is detected either from other nodes transmitting onto the segment or from noise will trigger the device to wake when MDI wake-up is enabled. Partial networking is not supported.

The device may be configured to wake from activity on the MDI interface when in the SLEEP state. The device monitors activity energy on TRXP/TRXN. Continuous activity must be detected for a minimum amount of time to ensure that false positive wake events are not caused by impulse noise; this time is documented in the *Wake-up Signal Characteristics and Timing - Rev C2* section. Once a valid wake event is detected, the INH pin is driven high to the VDDAU supply to re-enable external power supplies and wake the system.

Wake from MDI is enabled by writing a '1' to the MDI Wake Enable (MDIWKEN) bit in the Sleep Control 0 (SLPCTL0) register prior to entering the SLEEP state.

Related Links

Wake-up Signal Characteristics and Timing - Rev C2

SLPCTL0

Sleep Control 0 Register

4.13.2.2. External Pin Wake-up

NOTICE This section applies to devices of revision C2 and earlier.

The device may be configured to wake from SLEEP when a valid pulse on the WAKE_IN/WAKE_IO pin, as specified by the OPEN Alliance *10BASE-T1S Sleep/Wake-Up Specification* is detected. After receipt of a valid signal, the INH pin is driven high to the VDDAU supply to re-enable external power supplies and wake the system. See Wake-up Signal Characteristics and Timing - Rev C2 for details.

Wake-up via the WAKE_IN/WAKE_IO pin is enabled by writing a '1' to the WAKE_IN Enable (WKINEN) bit in the Sleep Control 0 (SLPCTL0) register prior to entering the SLEEP state. The Wake In Polarity (WIPOL) bit in the Sleep Control 1 (SLPCTL1) register selects whether this signal is active high or low.

Restriction: Assertion of the WAKE_IN pin is only detectable when the device is in the SLEEP state. When awake and in ACTIVE state the device will not detect pulse assertions on the WAKE_IN pin.

Important: When wake from WAKE_IN is enabled, the device will not enter the SLEEP state while the WAKE_IN input is asserted. The WAKE_IN pin must be deasserted before the Sleep Inhibit Delay will occur followed by the INH pin being released and the SLEEP state entered. See the section *Sleep Mode and System Power Management* for more details.

Related Links

SLPCTL0

Sleep Control 0 Register

SLPCTL1

Sleep Control 1 Register

Sleep Mode and System Power Management

4.13.3. Entering Sleep Mode

NOTICE This section applies to devices of revision C2 and earlier.

After wake-up has been configured, the host controller may command the device to enter the SLEEP state. This is done by writing a '1' to the Sleep Enable (SLPEN) bit in the Sleep Control 0 (SLPCTL0) register. Alternatively the device may also be configured to enter SLEEP automatically upon expiration of an inactivity watchdog as detailed below.

Related Links

SLPCTL0

Sleep Control 0 Register

4.13.3.1. Inactivity Watchdog

NOTICE This section applies to devices of revision C2 and earlier.

The device includes an inactivity watchdog timer that can be used to automatically command the device into the SLEEP state. The inactivity watchdog can be used to allow the system to reduce its power consumption when no activity is present on the network. It can also be used to detect when the controller has malfunctions and is no longer managing the device; in this case, the watchdog can be used to force the device into the SLEEP state to prevent the malfunctioning node from consuming power on an inactive network segment.

The inactivity watchdog can be configured to trigger on inactivity of three sources: no receive packets from the network, no transmit packets from the MAC, and no SMI access by the controller. Each of these three inactivity sources may be enabled separately or together in any combination. Once enabled, the watchdog timer will be reset upon detected activity on any of the selected watchdog sources. When the watchdog expires, the Inactivity Watchdog Timeout (IWDTO) bit in the Status 2 (STS2) register will be set commanding the transition to the SLEEP state and initiating the Sleep Inhibit Delay timer. The Inactivity Watchdog Timeout Interrupt Mask (IWDTOM) bit in

the Interrupt Mask 2 (IMSK2) register should be set to assert the IRQ_N pin to immediately notify the host controller when the inactivity watchdog expiration occurs. Once the Inactivity Watchdog Timeout status bit is set, the controller may halt the pending SLEEP transition by clearing the Inactivity Watchdog Timeout status bit any time before the Sleep Inhibit Delay expires.

Before enabling the inactivity watchdog timer, the inactivity sources to be used for resetting the watchdog timer when activity occurs must be configured by setting the appropriate bits within the Port Management 2 (PRTMGMT2) register:

- Network packet receive inactivity - Media Interface Receive Watchdog Enable (MIRXWDEN)
- MAC packet transmit inactivity - Media Interface Transmit Watchdog Enable (MITXWDEN)
- SMI access inactivity - PHY Register Inactivity Watchdog Enable (PRIWDEN)

The 32-bit Inactivity Watchdog Timeout (TIMEOUT) field in the Inactivity Watchdog Timeout High/Low (IWDTOH/IWDTOL) registers configures how long the enabled inactivity sources must show no activity before the watchdog timer expires. The default setting for the Inactivity Watchdog Timeout yields an inactivity timeout of 2 seconds. When activity is detected on the inactivity sources, the watchdog timer is reset to the value in the TIMEOUT field. The watchdog timer then decrements every 200 ns. Should the watchdog timer decrement to zero, the Inactivity Watchdog Timer expires causing the Inactivity Watchdog Timeout (IWDTO) status bit to become set.

The watchdog is enabled by setting the Inactivity Watchdog Enable (IWDE) bit in the Control 1 (CTRL1) register after configuring the inactivity sources, the watchdog timeout, and enabling the Inactivity Watchdog Timeout Interrupt Mask.

Related Links

CTRL1
Control 1 Register

STS2
Status 2 Register

IMSK2
Interrupt Mask 2 Register

PRTMGMT2
Port Management 2

IWDTOH
Inactivity Watchdog Timeout (High)

IWDTOL
Inactivity Watchdog Timeout (Low)

SLPCTL0
Sleep Control 0 Register

4.13.4. Wake-up

NOTICE This section applies to devices of revision C2 and earlier.

After all of the power supplies of the device are above thresholds, whether a wake event has occurred or not, the device will be in a state similar to a power-on reset; this includes asserting IRQ_N to indicate that the device is ready for configuration. Unlike a power-on reset, upon wake the STATUS 2 (STS2) register will contain information about the wake event, and, if configured, wake forwarding will automatically send wake signals to additional devices. As after any reset, the device must be reconfigured, as described in the section *Initialization*.

The host controller can identify that the device was powered up from a wake event, by examining the Wake-up MDI (WKEMDI) and Wake-up WAKE_IN (WKEWI) status bits in the Status 2 (STS2) register indicating the source of the wake event. Once the device has awakened, it will continue to drive the INH pin high causing the ECU to remain awake until the controller initiates a new transition into the SLEEP state. The device may optionally be configured to forward a received wake event to other devices by driving a wake pulse on WAKE_OUT and/or generating a wake signal on the MDI. As the device configuration is reset to its default state upon wake-up, it must be reconfigured, including wake/sleep settings, prior to sleeping again.

Related Links

Initialization

STS2

Status 2 Register

4.13.4.1. MDI Wake Forwarding

NOTICE This section applies to devices of revision C2 and earlier.

The LAN8670/1/2 may be configured to generate activity signaling on the MDI upon wake from SLEEP due to a wake pulse on WAKE_IN. The wake signaling consists of a 1 ms transmission of differential Manchester encoded pseudo-random binary data. The device will not listen for activity on the network prior to transmitting the wake signaling.

MDI wake activity forwarding is enabled by setting the MDI Forward Enable (MDIFWDEN) bit of the Sleep Control 1 (SLPCTL1) register. Automatic forwarding of WAKE_IN wake events to the MDI must be configured prior to entering the SLEEP state.

Important: This MDI wake signaling does **not** meet the OPEN Alliance *10BASE-T1S Sleep/Wake-up Specification*, version 1.0. For a compliant signal, use Revision D0 or later.

Related Links

SLPCTL1

Sleep Control 1 Register

4.13.4.2. Wake Forwarding on the WAKE_OUT pin

NOTICE This section applies to devices of revision C2 and earlier.

The WAKE_OUT pin may be configured to generate a valid wake pulse upon wake from SLEEP . Enabling of WAKE_OUT pin forwarding is accomplished by setting the WAKE_OUT Forward Enable (WKOFWDEN) bit of the Sleep Control 1 (SLPCTL1) register prior to entering the SLEEP state. Automatic forwarding of wake events to the WAKE_OUT pin must be configured prior to entering the SLEEP state.

Tip: The WAKE_OUT pin is shared with RXCLK on the LAN8670 and can be used only if the device is configured for RMII operation.

Important: The WAKE_OUT pin operates from the VDDP power domain and therefore will only be asserted once the external VDDP supply has been powered.

Related Links

SLPCTL1

Sleep Control 1 Register

4.13.4.3. Manual Wake Assertion

NOTICE This section applies to devices of revision C2 and earlier.

Any time that the LAN8670/1/2 is powered up in the ACTIVE state, the host controller may request that the device generate wake-up event.

A manual wake forward event is activated by writing a '1' to the Manual Wake Forward (MWKFWD) bit in the Sleep Control 1 (SLPCTL1) register. Other bits in the same register will set the type of wake event and should be written appropriately. To trigger wake activity on the MDI, the MDI Wake Forward Enable (MDIWFWD) bit must be set. To trigger wake pulse on the WAKE_OUT pin, the WAKE_OUT Forward Enable (WKOFWDEN) bit must be set. Both modes may be triggered at the same time. If neither is set, no wake event is generated. Once the wake events have completed, the device will clear the MWKFWD bit, but the forwarding enable bits will hold their values.

Related Links

SLPCTL1

Sleep Control 1 Register

4.14. Sleep Mode - Rev D0

NOTICE This section applies to devices of revision D0 and later. For newer devices, see the section *Sleep Mode - Rev C2*.

The PHY provides an ultra-low power (typically less than 140 µW) sleep mode based on the OPEN Alliance TC10 specifications. In this mode, it will release the INH pin to allow shutdown of most external power supplies. Only the uninterrupted supply VDDAU remains active to monitor and react to user selectable wake events. After a wake event, INH is asserted and the remaining power supplies are re-enabled. Since the INH pin can control power supplies shared with other devices, this feature allows for an entire node to enter a low power state, and be awakened by external events.

This section will describe

- how the INH pin can be used to control the shutdown of power supplies, including using a delay feature
- how to select what events will wake the device from sleep
- how to enter sleep mode
- how the device will behave upon wake and what actions are required

Related Links

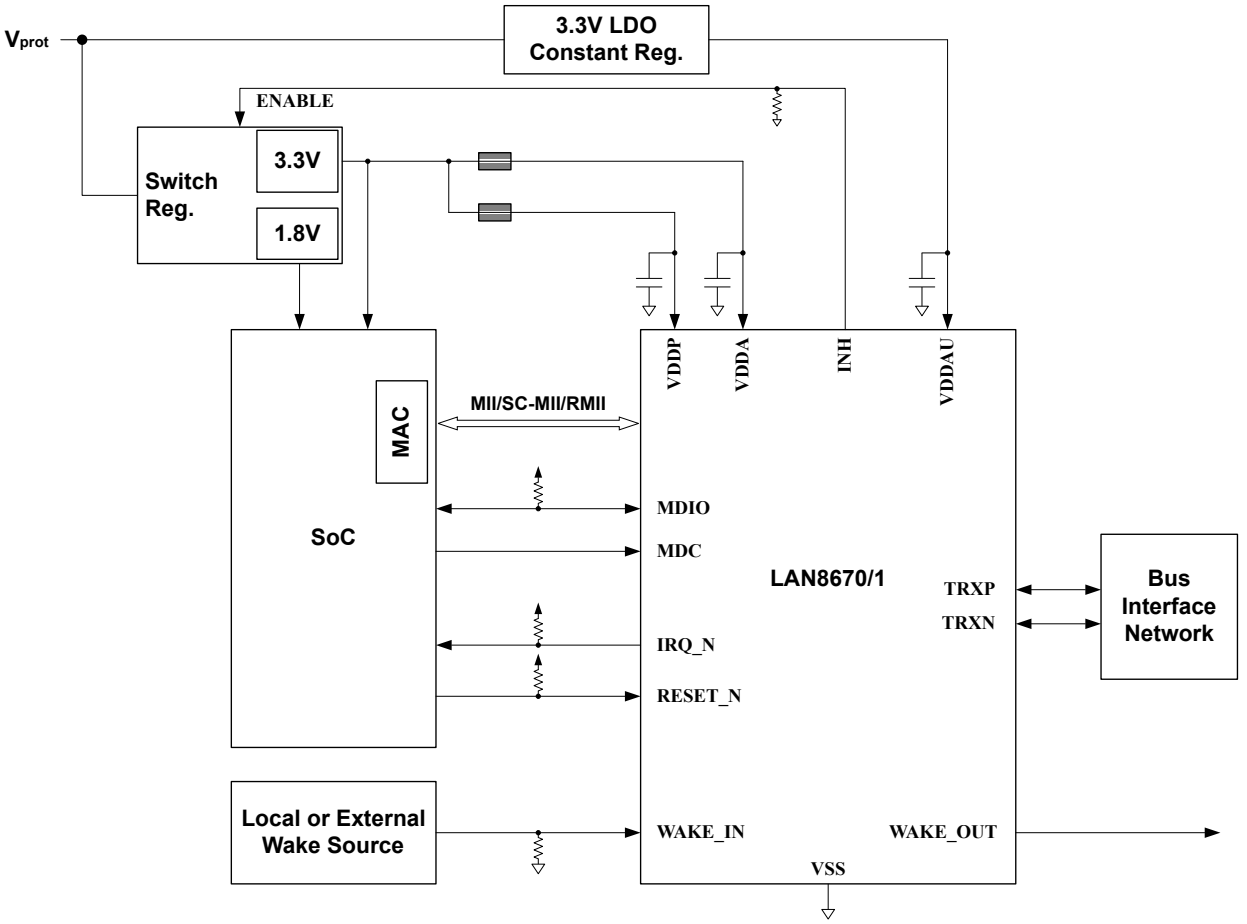
Sleep Mode - Rev C2

4.14.1. Sleep Mode and System Power Management

NOTICE This section applies to devices of revision D0 and later.

Figure 4-13 shows an example of how power should be supplied in a system that will use the low-power sleep mode of the device. In this diagram, VDDAU is provided by a constant supply, so that it is always enabled, even during sleep mode. On system power-up, once this supply is active, the INH pin will be asserted so that its active high output can drive the enable pins of the external switchable supplies for VDDA and VDDP.

Figure 4-13. Sleep Mode Example System

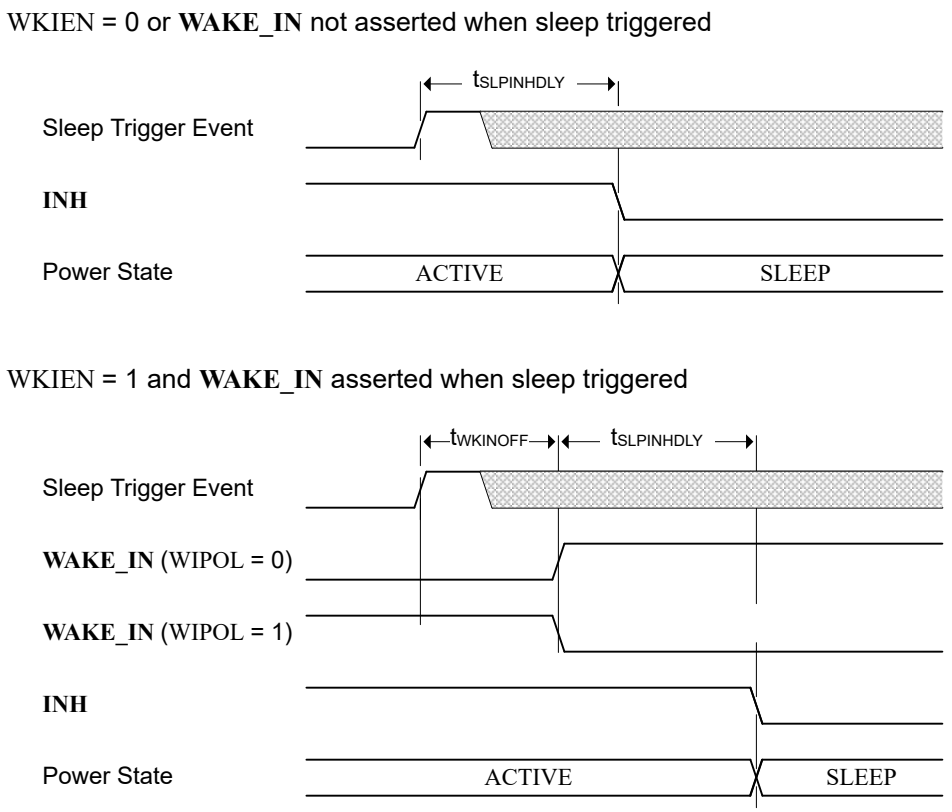


After the device enters sleep mode, the INH pin will enter a high-impedance state. The external resistor will pull the signal down to ground, which will then disable any voltage sources controlled by INH. This can be used to disable power to additional devices, including, when needed, the station host controller.

Important: Before entering SLEEP mode, the desired device wake configuration must be configured . It is recommended that this mode is configured immediately after a reset. Details can be found in the *Configuring Wake-up* section.

Some systems may require a delay between the trigger for the start of sleep mode and disable of the local power supplies, for example, to allow for other nodes on the mixing segment to go quiet. Delay timing is configured with the Sleep Inhibit Delay (SLPINHDLY) field of the Sleep Control 0 (SLPCTL0) register. If wake from the WAKE_IN pin is enabled (WKIEN=1), the WAKE_IN pin must be deasserted before the Sleep Inhibit Delay timer will be started. See Figure 4-14 for a diagram illustrating the timing from when SLEEP state is commanded until the INH pin is released and the SLEEP state is entered.

Figure 4-14. Sleep Timing



In sleep mode, a small amount of current is drawn from VDDAU to monitor for a wake condition. The wake condition can be a WAKE_IN pulse provided from another device, or a signal on the wire harness from another node on 10BASE-T1S network. After a wake condition is detected, INH is actively driven high, enabling the external power supplies, which should be fully powered within 1 ms of INH being driven high according to the OPEN Alliance *10BASE-T1S Sleep/Wake-Up Specification*. Once all power supplies are above their thresholds, the device will behave as if it had been reset by the RESET_N pin, and will assert IRQ_N to signal that the device is ready to be configured as described in the *Initialization* section.

Note:
The VDDA and VDDP power supplies are not required to be powered down prior to a wake-up event. In this case, the registers retain their values and the device does not need to be re-configured. However, if the VDDA and VDDP supplies are disabled, then the device must be re-initialized upon wake.

Important: To achieve maximum power savings and allow TC10 power goals to be met when in the SLEEP state, all power supplies except for VDDAU must be powered down.

Related Links
Configuring Wake-up
Initialization
SLPCTL0
Sleep Control 0 Register

4.14.2. Configuring Wake-up

NOTICE This section applies to devices of revision D0 and later.

The sleep/wake module is powered by the externally protected continuous VDDAU supply and detects a wake condition when the device is in the SLEEP state. This module monitors for a 625 kHz wake-up tone (WUT) on the MDI and/or wake pulses on the WAKE_IN/WAKE_IO pin to determine if the device has received wake-up signaling. Once wake-up signaling has been received and validated, this module will drive the INH pin high to the VDDAU supply to enable the external switched power supplies.

Prior to entering the SLEEP state, the host controller must configure the device to select one or both of these wake methods.

4.14.2.1. MDI Wake-up Tone Detection - Rev D0

NOTICE This section applies to devices of revision D0 and later.

In these revisions, MDI wake detection was designed to meet the OPEN Alliance *10BASE-T1S Sleep/Wake-up Specification*, version 1.0. Partial networking is supported.

The device may be configured to wake from a wake-up pulse (WUP) on the MDI interface when in the SLEEP state. The WUP consists of a preamble of six DME encoded 'T' symbols, 12 periods of a 625 kHz signal, and 24 to 26 DME encoded 'J' symbols. The device begins its wake sequence upon receiving the 625 kHz WUT. Once a valid wake event is detected, the INH pin is driven high to the VDDAU supply to re-enable external power supplies and wake the system. Detailed timing diagrams can be found in *Wake-up Signal Characteristics and Timing - Rev D0*

Wake from MDI is enabled by writing a '1' to the MDI Wake Enable (MDIWKEN) bit in the Sleep Control 0 (SLPCTL0) register prior to entering the SLEEP state.

Related Links
Wake-up Signal Characteristics and Timing - Rev D0
SLPCTL0 - Rev D
Sleep Control 0 Register - Rev D

4.14.2.2. External Pin Wake-up

NOTICE This section applies to devices of revision D0 and later.

The device may be configured to wake from SLEEP when a valid pulse on the WAKE_IN/WAKE_IO pin, as specified by the OPEN Alliance *10BASE-T1S Sleep/Wake-Up Specification* is detected. After receipt of

a valid signal, the INH pin is driven high to the VDDAU supply to re-enable external power supplies and wake the system. See Wake-up Signal Characteristics and Timing - Rev D0 for details.

Wake-up via the WAKE_IN/WAKE_IO pin is enabled by writing a '1' to the WAKE_IN Enable (WKINEN) bit in the Sleep Control 0 (SLPCTL0) register prior to entering the SLEEP state. The Wake In Polarity (WIPOL) bit in the Sleep Control 1 (SLPCTL1) register selects whether this signal is active high or low.

Note: Detection of a valid wake-up pulse on WAKE_IN or WAKE_IO after the sleep request and before the release of the INH pin will result in the sleep request being canceled. The device will remain in the active state.

Note: The WAKE_OUT pin may be disabled and combined with WAKE_IN as WAKE_IO.

Related Links

SLPCTL0 - Rev D

Sleep Control 0 Register - Rev D

SLPCTL1 - Rev D

Sleep Control 1 Register - Rev D

4.14.3. Entering Sleep Mode

NOTICE This section applies to devices of revision D0 and later.

After wake-up has been configured, the host controller may command the device to enter the SLEEP state. This is done by writing a '1' to the Low Power Request (LPREQ) bit in the Wake/Sleep Control (WS_CTRL) register.

Related Links

WS_CTRL

Wake Sleep Control Register

4.14.4. Wake-up

NOTICE This section applies to devices of revision D0 and later.

For the device to wake, it must receive a wake event and all of the power supplies of the device must be at or above operational levels. After wake, the device will be in a state similar to a power-on reset; this includes asserting IRQ_N to indicate that the device is ready for configuration. Unlike a power-on reset, upon wake the STATUS 2 (STS2) register will contain information about the wake event, and, if configured, wake forwarding will automatically send wake signals to additional devices. As after any reset, the device must be reconfigured, as described in the section *Initialization*.

The host controller can identify that the device was powered up from a wake event, by examining the Wake-up MDI (WKEMDI) and Wake-up WAKE_IN (WKEWI) status bits in the Status 2 (STS2) register indicating the source of the wake event. Once the device has awakened, it will continue to drive the INH pin high causing the ECU to remain awake until the controller initiates a new transition into the SLEEP state. The device may optionally be configured to forward a received wake event to other devices by driving a wake pulse on WAKE_OUT and/or generating a wake signal on the MDI. As the device configuration is reset to its default state upon wake-up, it must be reconfigured, including wake/sleep settings, prior to sleeping again.

Related Links
Initialization
STS2 - Rev D
Status 2 Register - Rev D

4.14.4.1. MDI Wake Forwarding

NOTICE This section applies to devices of revision D0 and later.

The LAN8670/1/2 may be configured to generate a WUP containing the 625 kHz wake-up tone on the MDI upon wake from SLEEP due to a wake pulse on WAKE_IN. MDI wake activity forwarding is enabled by setting the MDI Forward Enable (MDIFWDEN) bit of the Sleep Control 1 (SLPCTL1) register. Automatic forwarding of WAKE_IN wake events to the MDI must be configured prior to entering the SLEEP state.

Related Links
SLPCTL1 - Rev D
Sleep Control 1 Register - Rev D

4.14.4.2. Using a Pin for Wake Forwarding

NOTICE This section applies to devices of revision D0 and later.

When selected, wake forwarding will generate a valid wake pulse upon wake from SLEEP on either the WAKE_OUT pin or the WAKE_IN/WAKE_IO pin.

Wake forwarding is enabled by setting the Wake Forward Enable (WKOFWDEN) bit of the Sleep Control 1 (SLPCTL1) register prior to entering the SLEEP state. When enabling this feature, ensure that the desired output pin is selected as described below.

WAKE_OUT pin
WAKE_OUT is configured as a push-pull output. It cannot be connected to another output. This behavior is configured by default, or can be reconfigured by writing a '0' into the WAKE_IO Enable (WIOEN) bit of the Sleep Control 1 (SLPCTL1) register.

Tip: The WAKE_OUT pin is shared with RXCLK on the LAN8670 and can be used only if the device is configured for RMII operation.

Important: The WAKE_OUT pin operates from the VDDP power domain and therefore will only be asserted once the external VDDP supply has been powered.

WAKE_IN/WAKEIO pin
If the WAKE_OUT pin is not available or there is a need for multiple devices are to be connected as wake sources, the WAKE_IN/WAKE_IO pin can be configured to provide wake forwarding and it becomes an open-drain input/output. In this mode, the pin is still available as a wake input as described in the section *External Pin Wake-up*. When WAKE_IN/WAKE_IO is selected for wake forwarding, the WAKE_OUT pin will be unused and is connected internally to ground.

To select WAKE_IN/WAKE_IO as the output for wake forwarding write a '1' into the WAKE_IO Enable (WIOEN) bit of the Sleep Control 1 (SLPCTL1) register. The polarity of the both the detected and generated wake pulse is determined by the WAKE_IN Polarity (WIPOL) bit in the SLPCTL1 register.

Related Links

SLPCTL0 - Rev D

Sleep Control 0 Register - Rev D

SLPCTL1 - Rev D

Sleep Control 1 Register - Rev D

SLPCTL1 - Rev D

Sleep Control 1 Register - Rev D

External Pin Wake-up

4.14.4.3. Manual Wake Assertion

NOTICE This section applies to devices of revision D0 and later.

Any time that the LAN8670/1 is powered up in the ACTIVE state, the host controller may trigger a wake-up event to be sent to the network and/or additional devices.

This event can be configured to be a wake signal generated on the MDI (see *MDI Wake Forwarding*), a pulse on either WAKE_OUT or WAKE_IO (see *Using a Pin for Wake Forwarding*) or both.

Once configuration is completed, there are two ways to implement manual wake assertion:

- Using the OPEN Alliance WS_CTRL Register

  A wake forward event can be activated by writing a '1' to the Generate Low Power Mode Exit Request (LPEXIT) bit in the WS_CTRL register. Once the wake events have completed, the device will clear the LPEXIT bit.

- Using the SLPCTL1 Register for Backwards Compatibility

  A wake forward event can be activated by writing a '1' to the Manual Wake Forward (MWKFWD) bit in the Sleep Control 1 (SLPCTL1) register. Use a read-modify-write sequence to maintain the configured wake signaling. Once the wake events have completed, the device will clear the MWKFWD bit, but the forwarding enable bits will hold their values.

Related Links

WS_CTRL

Wake Sleep Control Register

SLPCTL1 - Rev D

Sleep Control 1 Register - Rev D

MDI Wake Forwarding

Using a Pin for Wake Forwarding

4.15. Topology Discovery - Rev D0

NOTICE This section applies to devices of revision D0 and later.

This device supports Topology Discovery according to the OPEN Alliance *10BASE-T1S Topology Discovery Specification*. Topology Discovery is a method to measure the signal propagation time between two nodes on the same 10BASE-T1S segment and, therefore, the relative distances and order of the nodes on the segment. If the speed of propagation through the medium is known, typically about 5 ns/m, the distance between the two nodes can be calculated.

Topology Discovery a system diagnostic, meaning that before the measurement can begin, a reference and a measured node must be determined and coordinated. During this time, all other nodes must avoid all transmissions. This includes disabling of PLCA to prevent transmission of BEACON symbols from interfering with the measurement. Furthermore, it is recommended to place the reference node on the physical end of the transmission line. This way, each measured node will have a unique signal propagation time relative to the reference node.

Topology Discovery works by the reference node transmitting a single pulse onto the network. The measured node detects this pulse and transmits a pulse in return. The reference node receives this returned pulse and transmits another pulse. This cycle of “bouncing” a pulse back and forth between the reference and measured nodes is repeated for a fixed, known time interval. The distance between the devices may then be calculated using the duration of the measurement, the number of pulses received and the internal delays of both nodes.

The polarity of the transmitted pulse is randomly varied each transmission cycle through the use of a scrambler. This is done to provide rejection of noise and To prevent a baseline wander on the line, a 1B/2B coding is applied to the output. This means that for every positive pulse sent, a negative pulse is sent in the cycle afterward and vice-versa.

Upon reception, the 2B pulse pair is internally deserialized into a single 1B pulse. A descrambler is used verify that the polarity of the incoming 1B pulse is as expected and correct. Prior to beginning an actual measurement, both descramblers must be trained by the transmissions from the other node. The first 60 pulses are therefore reserved for this synchronization and not counted as part of the measurement. If the scramblers and descramblers cannot be synchronized within this time, or if the polarity of an incoming pulse does not match the predicted polarity due to noise or error, then the measurement will result in a failure.

To activate Topology Discovery, a ‘1’ must be written into the Topology Discovery Enable (TDEN) bit in the Topology Discovery Control (TDCTL) register. If a ‘1’ is written into the Reference Node Select (REFN) bit in the TDCTL register, then the node is selected as the reference node. Otherwise, it will be treated as a measured node.

Topology discovery is performed in two steps. Only the final step determines number of pulses exchanged between the reference and measured nodes as previously described. First, however, the internal delay of the device must be measured. By measuring the internal delay, any variability in timing due to silicon process, temperature, and voltage may be removed increasing the accuracy of the measurement of the signal propagation time between the two nodes. The internal delay of a node is the delay between the first edge of a receiving pulse and the first edge of the corresponding pulse being transmitted by that same node. To measure the internal delay of a node, all other nodes must be configured so that they do not transmit anything onto the network including PLCA BEACONs. The node measuring its internal delay is then permitted to begin its delay measurement by enabling topology discovery and writing a ‘1’ into the Internal Delay Measurement Start (INTDLYSTRT) bit in the TDCTL register. Because only this one node is transmitting onto the network, the other nodes are able to listen in while this node’s internal delay is measured. Similar to the distance measurement, the device sends pulses onto the network. However, instead of waiting

for a response from another node, it listens to its *own* transmitted pulses to trigger the follow-up pulse. This is repeated for a fixed amount of time as configured in the Distance Measurement Duration (DISTMESDUR) field of the TDCTL register and the number of pulses is counted. The internal delay is calculated by dividing the duration of the measurement by the number of pulses counted.

The resulting internal delay count is contained in the Topology Discovery Internal Node Delay Result -Low (TDINTDLYRESL) and -High (TDINTDLYRESH) registers. In manual mode, this internal delay measurement must be communicated from the measured node back to the reference node in its Topology Discovery Measured Node Delay Measurement Result -Low (TDMNDLYRESL) and -High (TDMNDLYRESH) registers for it to calculate the signal propagation time between the two nodes. However, in automatic mode, the reference node acquires values in these registers by listening in while the measured node performs its internal delay count. In this case, the internal delay count of the measured node as observed by the reference node is automatically stored in the TDMNDLYRESL and TDMNDLYRESH registers.

The signal propagation time measurement is initiated with the reference node transmitting a single pulse onto the network. The measured node detects this pulse and transmits a return pulse. When the reference node receives this returned pulse it will respond by transmitting another pulse. This cycle is repeated for a fixed time interval defined in the Distance Measurement Duration (DISTMESDUR) field of the TDCTL register. When the Distance Measurement Done (DISTMESDN) bit in the Topology Discovery Status (TDSTS) register is set, the signal propagation time measurement phase has completed and the number of pulses received and counted by the reference node is stored in the Topology Discovery Distance Measurement Result -Low (TDDISTRESL) and -High (TDDISTRESH) registers. The signal propagation time between the two nodes may then be calculated using the duration of the measurement, the number of pulses received and the internal delays of both nodes. The resulting signal propagation time may be divided by the speed of propagation through the medium, if known, to derive the physical distance between the nodes to within a number of centimeters.

Additional Topology Discovery details may be found in the *Topology Discovery for 10BASE-T1S Systems* application note.

Related Links

TDCTL - Rev D

Topology Discovery Control Register - Rev D

TDSTS - Rev D

Topology Discovery Status Register - Rev D

TDADVCTRL - Rev D

Topology Discovery Advanced Control Register - Rev D

TDDISTRESH - Rev D

Topology Discovery Distance measurement Result Register (High) - Rev D

TDDISTRESL - Rev D

Topology Discovery Distance measurement Result Register (Low) - Rev D

TDINTDLYRESH - Rev D

Topology Discovery Internal Delay Result Register (High) - Rev D

TDINTDLYRESL - Rev D

Topology Discovery Internal Delay Result Register (Low) - Rev D

TDMNDLYRESH - Rev D

Topology Discovery Measured Node Delay measurement Result Register (High) - Rev D

TDMNDLYRESL - Rev D

Topology Discovery Measured Node Delay measurement Result Register (Low) - Rev D

TDMNMESDUR - Rev D

Topology Discovery Measured Node Measurement Duration Register - Rev D

4.16. Signal Quality Indicator (SQI) - Rev C2

NOTICE This section applies to devices of revision C2 and earlier. For newer devices, see the section *Sleep Mode - Rev D0*.

The channel Signal Quality Indication (SQI) provides an indication of channel quality between nodes on the network segment. This SQI implementation is designed to be compatible with version 1.1 of the OPEN Alliance *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs Specification*.

The SQI is determined by accumulating statistics on received data. When PLCA is used, a single node is selected by using the Transmit Opportunity ID (TOID) bit field of the SQI Configuration 0 (SQICFG0); the SQI is then computed from the data received only during that transmit opportunity. If the average SQI of the transmission line required, it is possible to set this field to '0xFF' to calculate the SQI for all nodes simultaneously. This calculates a weighted average of the complete data traffic on the line, the more a node transmits, the higher this node will be weighted. When PLCA is not enabled, this field should be set to '0xFF' to request that the SQI will be computed over all received data. Statistics are calculated on the selected data and the resulting quality index is stored in the SQI Value (SQIVAL) field of the SQI Status 0 (SQISTS0) register in eight levels (between '000' = worst value and '111' = best value).

During the accumulation of statistics, it is possible that an error could occur. Such an error is indicated by setting bits in two different registers: the SQI Error (SQIERR) bit in the SQI Status 0 (SQISTS0) register and the SQI status bit in the Status 1 (STS1) register. In addition, an SQI error can be selected to assert the IRQ_N pin by clearing the SQI Interrupt Mask (SQIM) bit in the Interrupt Mask 1 (IMSK1) register.

Important: When an SQI measurement error has been detected, receive statistic accumulation is halted and the SQI Enable bit must be written to '0' before starting another SQI measurement.

The SQI feature operates in one of two modes. Polling mode is used for taking a single measurement or when comparing performance between multiple channels. Threshold alert mode is used to monitor one TOID continuously and provide an interrupt should SQI drop below a limit. These modes are described in the following sections.

Programming Model - Polling

In polling mode, the host controller polls the device to identify when a new SQI estimation is available. Polling mode is selected by setting the SQI Interrupt Threshold (SQIINTTHR) field of the SQI Configuration 2 (SQICFG2) to 11111b, which disables interrupts.

CAUTION When writing to the configuration registers below, use read-modify-write operations to avoid accidental updates to reserved fields.

1. Configure the PLCA transmit opportunity of the node of interest into the Transmit Opportunity ID (TOID) bit field of the SQI Configuration 0 (SQICFG0) register. If not using PLCA, the value 0xFF should be used so that the SQI is computed from received packets from all nodes.
2. Ensure that the SQI Interrupt Threshold (SQIINTTHR) field of the SQI Configuration 2 (SQICFG2) register is at the default value of 11111b.
3. Set the SQI Enable (SQIEN) bit to '1' in the SQI Control (SQICTL) register to start SQI measurement.

4. The SQI statistical accumulation process has completed and an SQI computed once the SQI Valid (SQIVLD) bit is set. Periodically poll both the SQIVLD and SQIERR bit until one is set.
   - If the SQIVLD bit = '1', the measured SQI is returned in the SQI Value (SQIVAL) field.
   - Else if the SQIERR bit = '1', restart the measurement:
     i. Write a '0' to the SQI Enable bit to clear the error.
     ii. Write a '1' to the SQI Enable to restart.

Tip: The time required for the SQI statistical accumulation process to complete depends on the amount of data received from the node of interest and may therefore vary significantly. A polling rate of approximately once per second is recommended.

5. The SQI Valid status bit will be cleared when read and automatically set again once a new SQI value has been determined. The application may continue to monitor the SQI for the selected transmit opportunity by returning to step #3 above and polling for the SQI Valid bit to become set again.
6. To stop SQI measurements, write a '0' to clear the SQI Enable bit.

Programming Model - Threshold Alert Mode

In threshold alert mode, the device is configured to continually estimate the SQI and alert the host controller via an interrupt when the measured SQI falls below a specified threshold. When the SQI Interrupt Threshold is set to a value from 1 to 7, the device will assert the SQI status bit in the Status 1 (STS1) register any time the measured SQI is equal to or below the configured threshold. If the SQI Interrupt Mask (SQIM) bit is '0' in the Interrupt Mask 1 (IMSK1) register, the assertion of the SQI status bit will additionally generate an assertion on the IRQ_N pin.

CAUTION When writing to the configuration registers below, use read-modify-write operations to avoid accidental updates to reserved fields.

1. Configure the PLCA transmit opportunity of the node of interest into the Transmit Opportunity ID (TOID) bit field of the SQI Configuration 0 (SQICFG0) register. If not using PLCA, the value 0xFF should be used so that the SQI is computed from received packets from all nodes.
2. Configure the SQI Interrupt Threshold (SQIINTTHR) field of the SQI Configuration 2 (SQICFG2) register for the SQI threshold at which the SQI status bit will be asserted. For example, configuring SQIINTTHR to 00101b will result in the SQI status bit being asserted when an SQI of 4 or below is measured.
3. Write a '0' to the SQI Interrupt Mask (SQIM) bit of the Interrupt Mask 1 (IMSK1) register to enable the assertion of the IRQ_N pin when the SQI status bit is set.
4. Set the SQI Enable (SQIEN) bit to '1' in the SQI Control (SQICTL) register to enable SQI measurement.
5. When the IRQ_N pin is asserted, read the Status 1 (STS1) register.
   - If the SQIVLD bit = '1', the device measured an SQI of less than or equal to the configured threshold.
   - Else if the SQIERR bit = '1', restart the measurement:
     i. Write a '0' to the SQI Enable bit to clear the error.
     ii. Write a '1' to the SQI Enable to restart.
6. To stop SQI measurements, write a '0' to clear the SQI Enable bit.

Related Links

SQICTL
SQI Control Register

SQISTS0
SQI Status 0 Register

SQICFG0
SQI Configuration 0 Register

SQICFG2
SQI Configuration 2 Register

STS1
Status 1 Register

IMSK1
Interrupt Mask 1 Register

4.17. Dynamic Channel Quality - Signal Quality Indicator (DCQ SQI) - Rev D0

NOTICE This section applies to devices of revision D0 and later.

The Dynamic Channel Quality (DCQ) Signal Quality Indication (SQI) feature has been implemented according to version 2.1 of the OPEN Alliance *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs Specification*. The major advantage of this SQI method over the method used in earlier product revisions is that it returns a channel quality measurement much quicker and over a wider range.

Note: This DCQ SQI cannot be used at the same time as the non-DCQ SQI implemented previously. The SQI Enable (SQIEN) bit in the SQI Control (SQICTL) register must be '0' disabling the earlier non-SQI implementation.

The DCQ SQI is determined by accumulating jitter statistics on received data. Two ranges of SQI are generated. The three-bit DCQ SQI returns an eight-level value ranging from '000', worst value, and '111', best value, in the SQI field of the DCQ_SQI register. An enhanced range five-bit SQI Plus (SQI+) returns a 32-level value ranging from '00000', worst value, and '11111', best value, in the SQI Plus (SQIP) field of the DCQ_SQIP register. Both the 8-level SQI and 32-level SQI+ measurements are performed simultaneously and complete at the same time. The three bits of the 8-level SQI are identical to the most significant three bits of the 32-level SQI+; The 32-level SQI+ simply provides extra granularity.

When PLCA is used, a single node is selected by using the Transmit Opportunity ID (TOID) field of the DCQ Transmit Opportunity ID (DCQ_TOID) register. The DCQ SQI and SQI+ measurements are computed only from the data received during the specified transmit opportunity.

When PLCA is not enabled, the TOID field must be set to '0xFF' so the DCQ SQI and SQI+ will be computed from all data received regardless of PLCA Transmit Opportunity. In this case, the resulting SQI and SQI+ measurement is a weighted average of data transmitted from all other nodes on the mixing segment; the more packets a node transmits, the higher this node will be weighted.

The DCQ SQI and SQI+ measurements begin automatically upon writing a *new* value into the TOID field of the DCQ_TOID register. Upon completion the measurement, a '1' is written by hardware into the SQI Update (SQI_UPD) and SQI+ Update (SQIP_UPD) bits of the DCQ_SQI and DCQ_SQIP registers, respectively. The setting of the SQI_UPD bit indicates that the value in the corresponding three-bit SQI field is valid. Likewise, SQIP_UPD being set indicates that the value in the corresponding five-bit SQIP field is valid.

The SQI_UPD and SQIP_UPD bits are automatically cleared on read. Reading of SQI_UPD also results in a new measurement being triggered in addition to the clearing of the SQI_UPD status bit. Reading of the SQIP_UPD bit will not trigger a new measurement, although it will result in SQIP_UPD being cleared.

Tip: First read the 32-level DCQ SQI Plus register (DCQ_SQIP) to return the current SQIP_UPD status and SQIP value. If the SQIP_UPD status is set, then the returned 32-level SQIP value is valid. The SQIP_UPD status was cleared. Then, to restart a new measurement, read the eight-level DCQ SQI register (DCQ_SQI) to clear the SQI_UPD status bit and trigger new measurement for the eight-level SQI and 32-level SQI+.

When the DCQ SQI Update and DCQ SQI_ Update bits are set then the SQI bit in the Status 1 (STS1) register is set. The SQI Mask (SQIM) bit in the Interrupt Mask 1 (IMSK1) register may be written to '0' to enable an assertion of the interrupt on IRQ_N pin to the station host controller when the SQI status bit is set.

A new SQI measurement is also triggered upon writing a *new* value to the DCQ_TOID register. If the value of the TOID field is changed while a measurement is ongoing then the current measurement will be aborted and a new one started.

Programming Model - Polling

In polling mode, the host controller polls the SQIP_UPD bit in the DCQ_SQIP register to identify when new DCQ SQI and SQI+ measurement results are available.

1. Configure the PLCA transmit opportunity of the node of interest into the Transmit Opportunity ID (TOID) bit field of the DCQ_TOID register. If not using PLCA, the value 0xFF should be used so that the SQI is computed from received packets from all nodes.
2. Periodically poll the DCQ_SQIP register. The DCQ_SQIP and DCQ_SQI status bits will be set simultaneously. When the SQIP_UPD bit is set in the DCQ_SQIP register, the SQIP field returns the measured 32-level SQI+ result.

   Tip: The time required for the SQI statistical accumulation process to complete depends on the amount of data received from the node of interest and may therefore vary significantly. A polling rate of approximately once per second is recommended.

3. Read the DCQ_SQI register. The SQI_UPD bit should be set. When the SQI_UPD bit is set in the DCQ_SQI register, the SQI field contains the measured eight-level SQI result and may be used, if desired. Reading of the DCQ_SQI register clears the SQI_UPD bit and initiates a new measurement.
4. Continue polling in step 2, above.
5. A new measurement is also initiated by writing a new value to the DCQ_TOID register.

Programming Model - Interrupt

In interrupt mode, the host controller configures and initiates a DCQ SQI/SQI+ measurement then waits for an assertion of the interrupt on IRQ_N pin to the station host controller when the measurement is complete and results are available.

1. Write a '0' to the SQI Mask (SQIM) bit of the Interrupt Mask 1 registers. This will enable the assertion of the interrupt on IRQ_N pin to the station host controller when the measurement is complete

2. Configure the PLCA transmit opportunity of the node of interest into the Transmit Opportunity ID (TOID) bit field of the DCQ_TOID register. If not using PLCA, the value 0xFF should be used so that the DCQ SQI/SQI+ is computed from received packets from all nodes.
3. Wait for an assertion of the interrupt on IRQ_N pin.
4. Read the Status 1 (STS1) register. If the SQI bit is clear, process the other pending interrupts and continue waiting in step 3 above.

> **Tip:** The time required for the SQI statistical accumulation process to complete depends on the amount of data received from the node of interest and may therefore vary significantly. A polling rate of approximately once per second is recommended.

5. When the SQI bit of the Status 1 (STS1) register is set, read the DCQ_SQIP register. The DCQ_SQIP and DCQ_SQI status bits will be set simultaneously. When the SQIP_UPD bit is set in the DCQ_SQIP register, the SQIP field returns the measured 32-level SQI+ result.
6. Read the DCQ_SQI register. The SQI_UPD bit should be set. When the SQI_UPD bit is set in the DCQ_SQI register, the SQI field contains the measured eight-level SQI result and may be used, if desired. Reading of the DCQ_SQI register clears the SQI_UPD bit and initiates a new measurement.
7. Continue waiting for the new SQI/SQI+ measurement to complete by waiting for an interrupt in step 3, above.
8. A new measurement is also initiated by writing a new value to the DCQ_TOID register.

Related Links

DCQ_TOID - Rev D
Dynamic Channel Quality Transmit Opportunity ID Register - Rev D

DCQ_SQI - Rev D
Signal Quality Index Register - Rev D

DCQ_SQIP - Rev D
Signal Quality Index Plus Register - Rev D

SQICTL
SQI Control Register

STS1 - Rev D
Status 1 Register - Rev D

STS2 - Rev D
Status 2 Register - Rev D

4.17.1. SQI+ to BER Correlation

The Table 4-3 below shows the relations between SQI and Bit-Error-Rate (BER) according to the OPEN Alliance *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs* specification. The BER is calculated assuming white Gaussian noise with a bandwidth of 40 MHz.

Note: The following table is derived from characterized sames and is provided for informative purposed only.

Table 4-3. LAN8670/1 SQI+ to BER Correlation

SQIP Field Value		SQI+[2]	BER for AWG noise model (informative)[3]
Binary (*R*)[1]	Decimal		
00000111	0	3.13	
00001111	1	6.25	
00010111	2	9.38	BER > 10^{-2}
00011111	3	12.50	
00100111	4	15.63	
00101111	5	18.75	
00110111	6	21.88	
00111111	7	25.00	
01000111	8	28.13	
01001111	9	31.25	
01010111	10	38.38	
01011111	11	37.50	
01100111	12	40.63	
01101111	13	43.75	BER > 10^{-3}
01110111	14	46.88	
01111111	15	50.00	
10000111	16	53.13	BER > 10^{-4}
10001111	17	56.25	
10010111	18	59.38	
10011111	19	62.50	BER > 10^{-5}
10100111	20	65.63	
10101111	21	68.75	BER > 10^{-6}
10110111	22	71.88	
10111111	23	75.00	10^{-10} < BER < 10^{-6}
11000111	24	78.13	
11001111	25	81.25	BER < 10^{-10}
11010111	26	84.38	
11011111	27	87.50	BER < 10^{-13}
11100111	28	90.63	BER < 10^{-17}
11101111	29	93.75	
11110111	30	96.88	
11111111	31	100.00	

Notes:

1. The 5-bit SQIP field is left justified and '1' padded to represent an unsigned 8-bit fixed-point integer, *R*.
2. The SQI+ value ranges from zero to 100% and is computed by the formula $\mathrm{SQI+} = 100 \cdot (R + 1) / 256$. Refer to the OPEN Alliance *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs Specification* for more information.
3. Characterized on samples.

4.18. Cable Fault Diagnostics - Rev C2

NOTICE This section applies to devices of revision C2 and earlier. For newer devices, see the section *Harness Defect Detection - Rev D0*.

This product implements hardware to support basic cable fault diagnostics as specified in version 1.1 of OPEN Alliance *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs Specification*. Using these features, it is possible for a station host controller to determine various cable failures in a multidrop network. These failures include

- Both conductors open
- Both conductors shorted together
- Both conductors shorted to power or ground

Additional information, including the software algorithm recommended for the host controller, is available under NDA. When using the software algorithm to aid in the harness defect detection, the following failures may additionally be possible to detect under the correct circumstances:

- One conductors shorted to ground or a supply voltage
- One conductor open
- Incorrect wire termination

4.19. Harness Defect Detection (HDD) - Rev D0

NOTICE This section applies to devices of revision D0 and later.

The Harness Defect Detection feature has been implemented according to version 2.1 of the OPEN Alliance *Advanced Diagnostic Features for 10BASE-T1S Automotive Ethernet PHYs Specification*. Class 2 hard failure detection capabilities are provided as indicated in the Harness Defect Detection (HDD) field of the Advanced Diagnostic Features Capability (ADFCAP) register. Detectable Class 2 failure modes are outlined in Table 4-4.

Table 4-4. Class 2 Detectable Harness Defects

Description	Pass	Fail
Both wires open	R ≤ 2.5Ω	R ≥ 100 kΩ
Both wires shorted to ground or battery supply	R ≥ 100 kΩ	R ≤ 10Ω
Both wires shorted together	R ≥ 100 kΩ	R ≤ 10Ω
Single wire open or single termination lost	R ≤ 2.5Ω	R ≥ 100 kΩ

When the harness defect detection measurement is in process, all nodes on the mixing segment must be in a high-impedance receive state. Any transmissions will interfere with the process and lead to a measurement failure.

Programming Model - Polling

In polling mode, the host controller initiates the harness defect detection process then polls the START bit to identify when it is cleared indicating the process has completed.

1. Guarantee that all nodes on the mixing segment remain silent and in a high-impedance receive state. This is typically implemented as a special system diagnostic mode.
2. Configure the PMA for HDD diagnostic mode by writing a ‘1’ to the HDD Request (HDDREQ) bit of the HDD register.

3. Verify that the PMA is in the HDD diagnostic mode by reading a '0' from the HDD Ready (HDDRDY) bit of the HDD register.
4. Once HDD is ready, the harness defect detection process is started by setting the START bit.
5. Poll the HDD register to determine when the HDD process has completed and the device has cleared the START bit.
6. If the VALID bit returns '0', then an error has occurred during the HDD process.
7. If the VALID bit returns '1', it indicates that the result of the HDD process in the Short Open State (SHTOPNSTS) field contains a valid HDD result.
8. Write a '0' to the HDD Request bit to request the PMA to exit the HDD diagnostic mode and return to normal operation.
9. Verify that the PMA has returned to normal operation by reading a '0' from the HDD Ready bit.
10. Re-enable packet transmission and exit the special system diagnostic mode.

Programming Model - Interrupt

In interrupt mode, the host controller initiates the harness defect detection process then waits for an assertion of the interrupt on IRQ_N indicating that START bit was cleared and results are available.

1. Write a '0' to the Harness Defect Detection Done Mask (HDDDM) bit of the Interrupt Mask 1 registers. This will enable the assertion of the interrupt on IRQ_N pin to the station host controller when the process is complete and the device clears the START bit.
2. Guarantee that all nodes on the mixing segment remain silent and in a high-impedance receive state. This is typically implemented as a special system diagnostic mode.
3. Configure the PMA for HDD diagnostic mode by writing a '1' to the HDD Request (HDDREQ) bit of the HDD register.
4. Verify that the PMA is in the HDD diagnostic mode by reading a '0' from the HDD Ready (HDDRDY) bit of the HDD register.
5. Once HDD is ready, the harness defect detection process is started by setting the START bit.
6. Wait for an assertion of the interrupt on IRQ_N pin.
7. Read the Status 1 (STS1) register. If the HDDD bit is clear, process the other pending interrupts and continue waiting in step 6 above.
8. When the HDDD bit of the Status 1 register is set, read the HDD register.
9. If the VALID bit returns '0', then an error has occurred during the HDD process.
10. If the VALID bit returns '1', it indicates that the result of the HDD process in the Short Open State (SHTOPNSTS) field contains a valid HDD result.
11. Write a '0' to the HDD Request bit to request the PMA to exit the HDD diagnostic mode and return to normal operation.
12. Verify that the PMA has returned to normal operation by reading a '0' from the HDD Ready bit.
13. Re-enable packet transmission and exit the special system diagnostic mode.

Related Links

ADFCAP - Rev D

Advanced Diagnostic Features Capability - Rev D

HDD - Rev D

Harness Defect Detection - Rev D

4.20. Safety Notifications

The LAN8670/1/2 may be configured to perform temperature and voltage monitoring and alert the station host controller when operational parameters are at risk of being exceeded. This section describes the monitoring of power supplies and die junction temperature for safe operation within operational limits as well as network related system issues.

4.20.1. Under Voltage Detection

The LAN8670/1/2 is able to detect a brown-out condition on 3.3V power supply. Details for monitoring the power supply is contained in the following sections.

4.20.1.1. Under-Voltage Detection (3.3V Supply)

The device is able to detect a voltage source brown-out condition. The under-voltage condition is triggered when the VDDA or VDDAU supplies drop below a 3.05V (-7.5% nominal) threshold causing the assertion of the 3.3V supply Under-Voltage (UV33) status bit in the Status 2 (STS2) register. If the interrupt status is not masked via the 3.3V Under-Voltage Interrupt Mask (UV33M) bit in the Interrupt Mask 2 (IMSK2) register, the IRQ_N pin will assert. The 3.3V Under-Voltage status bit will not be cleared until the supply voltage rises above the minimum threshold.

To prevent false brown-out detection due to power supply noise, the supply voltage must remain below the minimum threshold for greater than 200 µs before the under-voltage condition will be triggered. The debounce time may be adjusted by configuring the 3.3V supply Under-Voltage Filter Time (UV33FTM) field of the Analog Control 5 (ANALOG5) register.

Related Links

STS2

Status 2 Register

IMSK2

Interrupt Mask 2 Register

ANALOG5

Analog Control 5

4.20.2. Over-Temperature Detection

A mechanism is provided within the device to detect when the die junction temperature exceeds a threshold. As shown in Table 4-5, there is a rising and falling die temperature threshold. The over-temperature condition is triggered when the rising temperature threshold is exceeded causing the assertion of the Over-Temperature Error (OT) status bit in the Status 2 (STS2) register. If the interrupt status is not masked via the Over-Temperature Error Interrupt Mask (OTM) bit in the Interrupt Mask 2 (IMSK2) register, the IRQ_N pin will assert. The Over-Temperature Error status bit will not be cleared until the die temperature falls below the falling temperature threshold.

Regardless of the state of the Over-Temperature Error status bit, the device disables this function when in the SLEEP power state and the IRQ_N pin will not be asserted.

Table 4-5. Over-Temperature Thresholds

Description	Symbol	Min	Max	Units
Die Junction Over-Temperature Threshold				
Rising Temperature	T_{wh}	135	154	°C
Falling Temperature	T_{wl}	121	139	°C

Note: This table contains characterization data from a limited number of representative devices. The values are measured values and are not guaranteed.

Related Links

STS2

Status 2 Register

IMSK2

Interrupt Mask 2 Register

4.20.3. Transmit Jabber

Network communication may become blocked if a device fails in such a mode as to become stuck in the transmit state continually driving the shared bus, i.e., “jabber”. To help guard against this failure mode the LAN8670/1/2 is designed with a transmit jabber watchdog. Should the PCS block remain in the transmit state for longer than 2 ms the jabber watchdog will trigger. When the transmit jabber watchdog triggers, the PCS will transmit special ESDERR End-of-Stream Error ESDJAB End-of-Stream Jabber Delimiter codes to the network followed by disabling the transmitter. Additionally, the Jabber Detection Status (JAB_DET) bit in the Clause 22 Basic Status (BASIC_STATUS) register will be set along with the Transmit Jabber Status (TXJAB) status bit in the Status 1 (STS1) register. If the Transmit Jabber Status interrupt status is not masked via the Transmit Jabber Interrupt Mask (TXJABM) bit in the Interrupt Mask 1 (IMSK1) register, the IRQ_N pin will assert.

Once a transmit jabber condition has been detected, the PCS will wait 16 ms before attempting another transmission. The transmit jabber watchdog is reset between packets transmitted with PLCA burst mode enabled.

Since a device terminates a jabber transmission with a special ESDJAB End-of-Stream Jabber Delimiter code, all receiving devices can detect when a remote device has jabbered. When the LAN8670/1/2 detects a remote transmit jabber error occurred on a remote device, the Remote Jabber Count (RMTJABCNT) field in the 10BASE-T1S PCS Diagnostic 1 (T1SPCSDIAG1) register will be incremented. In addition, the End-of-Stream Error Delimiter (ESDERR) status bit in the Status 1 (STS1) register will set. If enabled by clearing the End-of-Stream Error Delimiter Mask (ESDERRM) bit in the Interrupt Mask 1 (IMSK1) register, the IRQ_N pin will assert when a remote jabber condition has been detected.

Related Links

BASIC_STATUS

Basic Status

STS1

Status 1 Register

IMSK1

Interrupt Mask 1 Register

T1SPCSDIAG1

10BASE-T1S PCS Diagnostic 1

4.20.4. PLCA Notifications

The LAN8670/1/2 has the ability to detect the following PLCA error conditions and assert interrupts, if enabled. For details, please refer to the Physical Layer Collision Avoidance (PLCA) Diagnostics section.

Table 4-6. PLCA Notifications

Notification	Register.Bit	Description
PLCA Status	STS1.PSTC	PLCA Status Changed
PLCA Diagnostic	STS1.PLCADIAG PLCADIAG.RXINTO (Rev D and later)	PLCA Diagnostic Status Changed
Receive in TO	STS1.RXINTO (Rev C and earlier) PLCADIAG.RXINTO (Rev D and later)	Packet received in assigned transmit opportunity

Table 4-6. PLCA Notifications (continued)

Notification	Register.Bit	Description
Unexpected Beacon	STS1.UNEXPB (Rev C and earlier) PLCADIAG.UNEXPB (Rev D and later)	A Beacon was received from another device on the bus
Beacon before TO	STS1.BCNBFTO (Rev C and earlier) PLCADIAG.BCNBFTO (Rev D and later)	A Beacon was received before the local transmit opportunity occurred
Maximum TO	PRSSTS.MAXID	Number of transmit opportunities in the last PLCA cycle
TO Counter	TOCNTH/TOCNTL	Number of assigned transmit opportunities that have occurred
Beacon Counter	BCNCNTH/BCNCNTL	Number of received Beacons (PLCA cycles)

Related Links

Physical Layer Collision Avoidance (PLCA) Diagnostics

PLCA_DIAG - Rev D

PLCA Diagnostics Register - Rev D

STS1

Status 1 Register

STS1 - Rev D

Status 1 Register - Rev D

PRSSTS

PLCA Reconciliation Sublayer Status

TOCNTH

Transmit Opportunity Count (High)

TOCNTL

Transmit Opportunity Count (Low)

BCNCNTH

BEACON Count (High)

BCNCNTL

BEACON Count (Low)

4.21. Link Status Overview - Rev D0

NOTICE Link status is a feature only available for devices of revision D0 and later.

Link status is an indicator that the network media is active and other stations are connected to the physical media and available for communication. Traditionally, a positive link status is set once a pair of stations at each end of a full duplex point-to-point link segment have trained their equalizers and established two-way communication. When this occurs, the Link Status (LNKSTS) bit of the Basic Status register is set.

For a half-duplex mixing segment, however, there is no equivalent concept of link status specified. Stations connected to a multidrop media make no announcement of their presence and there is no automatic way to detect them. This limitation may introduce challenges when using existing full duplex Ethernet driver architectures with 10BASE-T1S should they require knowledge of media availability. The device therefore includes features to create a surrogate link status indication. Several options are available and presented here.

Related Links

BASIC_STATUS

Basic Status

4.21.1. Link Status Modes

The link status mode is configured by writing to the Link Status Configuration (LSCFG) field of the Link Status Control (LSCTL) register. The field selects the operating conditions which link status changes state.

When the conditions selected for link are met, then link will indicate true immediately. However, once the conditions for link are no longer met, a loss of link will not be indicated until after a false link timer has expired. This time defaults to 25 ms, but may be increased up to 1000 ms by configuring the Link Status Timer (LSTMR) field.

Related Links

LSCTL - Rev D

Link Status Control - Rev D

4.21.1.1. Fixed

When configured for fixed link status operation, the LNKSTS bit will always read as '0'. This will indicate a negative link status to the Ethernet driver, regardless of the local station being configured, connected to the physical media, or remote stations being available for communication. This reflects the lack of an actual link between devices in half-duplex mixing segments as exists between two devices that have successfully completed training in a full-duplex point-to-point segment

4.21.1.2. Firmware Semaphore

This mode is useful for Ethernet driver architectures utilizing two separate threads where one thread performs configuration and management of the device, and the second thread controls Ethernet packet data transfer. The thread responsible for the transfer of data will only function once link status is true indicating that the local device is fully configured and there are other stations available for communication on the media.

When operating in this mode, the LNKSTS bit will reflect the state of the Link Status Semaphore (LSSEM) bit. By default, LSSEM is '0' resulting in a false link indication at the LNKSTS bit. Once the driver management thread has configured the local device, it may set the LSSEM bit to '1' resulting in a true link indication at the LNKSTS bit. The driver data thread monitoring link status can then know that local station is ready for data transfer.

Link status may conversely at any time be changed to false by clearing the LSSEM bit resulting a loss of link indication and halting the driver data thread from transferring packets.

Note, however, that in this mode of operation, link status will not indicate the availability of remote stations on the media for communication.

4.21.1.3. PLCA Status

When PLCA is enabled, this mode will set link status to true when a PLCA beacons are regularly being received and the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register is set. Link status will indicate false once beacons are no longer detected and PLCA status becomes false.

For PLCA followers, this mode will indicate the presence of at least a coordinator on the bus and available for communication. PLCA coordinators, however, cannot detect follower nodes being available for communication.

4.21.1.4. Activity

This mode of link indication intends to extend the PLCA Status mode above and eliminate the limitations that the coordinator cannot detect the presence of follower nodes being available for communication. For PLCA followers, link will indicate true when PLCA beacons are regularly being received as in the PLCA Status mode above. However, when configured as a PLCA coordinator, link will indicate true once a packet has been received from a follower on the segment.

This mode requires a follower node to first indicate link by detecting PLCA beacons. Once the follower transmits a packet, the coordinator will then indicate link as well. As such, packets must be regularly received by the coordinator to maintain an indication of link.

4.21.2. Hardware Link Status Indication

Link indication is available by reading the Link Status (LNKSTS) bit of the Basic Status register. Sometimes, especially during the prototype phase, it may be useful to have a real-time indication of link output to a pin. This may be used to control an LED, or for signaling link status in real time input to a station microcontroller.

The enabling and configuration of link status output pin is accomplished by writing to the Link Status Pin Select (LSPSEL) field.

Note: When a pin is configured as link status output, it overrides any other pin mux configuration.

Related Links

LSCTL - Rev D

Link Status Control - Rev D

5. Register Descriptions

This chapter describes the various device registers, which are categorized as follows:

- SMI Basic Control and Status Registers (Clause 22)
- PMA/PMD Registers (MMD 1)
- PCS Registers (MMD 3)
- Miscellaneous Registers (MMD 31)

For details on register bit attribute notation, refer to the section *Register Bit Types*.

Related Links

Register Bit Types

5.1. SMI Basic Control and Status Registers

The section describes the various SMI Control and Status Registers (CSRs). The SMI CSRs follow the IEEE 802.3 (Clause 22.2.4) management register set. All functionality and bit definitions comply with these standards.

Important: RESERVED address space must not be written to except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	BASIC_CONTROL	15:8	SW_RESET	LOOPBACK	SPD_SEL[0]	AUTONEGEN	PD	ISOLATE	REAUTONEG	DUPLEXMD
		7:0	COLTST	SPD_SEL[1]						
0x01	BASIC_STATUS	15:8	100BT4A	100BTXFDA	100BTXHDA	10BTFDA	10BTHDA	100BT2FDA	100BT2HDA	EXTSTS
		7:0		MFPRESUPA	AUTONEGC	RMTFLTD	AUTONEGA	LNKSTS	JABDET	EXTCAPA
0x01	BASIC_STATUS - Rev D	15:8	100BT4A	100BTXFDA	100BTXHDA	10BTFDA	10BTHDA	100BT2FDA	100BT2HDA	EXTSTS
		7:0		MFPRESUPA	AUTONEGC	RMTFLTD	AUTONEGA	LNKSTS	JABDET	EXTCAPA
0x02	PHY_ID1	15:8	OUI[2:9]							
		7:0	OUI[10:17]							
0x03	PHY_ID2	15:8	OUI[18:23]						MODEL[5:4]	
		7:0	MODEL[3:0]				REV[3:0]			
0x05 ... 0x0C	Reserved									
0x0D	MMDCTRL	15:8	FNCTN[1:0]							
		7:0				DEVAD[4:0]				
0x0E	MMDAD	15:8	ADR_DATA[15:8]							
		7:0	ADR_DATA[7:0]							
0x10 ... 0x11	Reserved									
0x12	STRAP_CTRL0	15:8								MITYP[1]
		7:0	MITYP[0]	PKGTYP[1:0]		SMIADR[4:0]				

5.1.1. Basic Control

Name: BASIC_CONTROL
Address: 0x00

Clause 22 Basic Control Register

Bit	15	14	13	12	11	10	9	8
	SW_RESET	LOOPBACK	SPD_SEL[0]	AUTONEGEN	PD	ISOLATE	REAUTONEG	DUPLEXMD
Access	R/W SC	R/W	RO	RO	R/W	R/W	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COLTST	SPD_SEL[1]						
Access	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – SW_RESET PHY Soft Reset
Writing a '1' to this bit will initiate a software reset of the PHY. A software reset will restore all PHY registers to their default state, except for those fields identified as "NASR".
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal operation
1	PHY software reset

Bit 14 – LOOPBACK Near-End Loopback
When set, this bit enables a near-end loopback. When enabled, transmit data (TXD) pins from the MAC will be looped back onto the receive data (RXD) pins to the MAC. In this mode, no signal is transmitted onto the network media.

Important: PLCA must be disabled or configured as the PLCA Coordinator (Local ID = 0) when the near-end loopback mode is enabled.

Value	Description
0	Normal operation
1	Enable near-end loopback mode

Bit 13 – SPD_SEL[0] PHY Speed Select
Together with SPD_SEL[1], sets the network communication speed.
Note: Only 10 Mbit/s is supported. This bit is always '0'.

Value	Description
00	10 Mbit/s
01	100 Mbit/s
10	1000 Mbit/s
11	Reserved

Bit 12 – AUTONEGEN Auto-Negotiation Enable
Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Disable auto-negotiate process
1	Enable auto-negotiate process

Bit 11 – PD Power Down

Setting this bit will power down the PMA leaving the remainder of the device functional.

Note: This bit is the same as the Low Power Enable bit in the 10BASE-T1S PMA Control register.

Value	Description
0	Normal operation
1	PMA is powered down

Bit 10 – ISOLATE Electrical isolation of the PHY from MII/RMII

When this bit is set, the PHY will electrically isolate its data paths from the MII/RMII .

Value	Description
0	Normal operation (PHY is not electrically isolated from MII/RMII)
1	Electrical isolation of PHY from MII/RMII

Bit 9 – REAUTONEG Restart Auto-Negotiation

Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Normal operation
1	Restart auto-negotiate process

Bit 8 – DUPLEXMD Duplex Mode

This bit configures the PHY for full-duplex or half-duplex network communication.

Note: Only half duplex operation is supported. This bit is always '0'.

Value	Description
0	Half duplex
1	Full duplex

Bit 7 – COLTST Collision Test

When the Near-End Loopback is enabled (LOOPBACK), setting this bit will allow the COL pin to be tested. When the Collision Test is enabled, asserting TXEN will cause the COL output to go high within 512 bit times. Negating TXEN will cause the COL output to go low within 4 bit times. The Collision Test should only be enabled when Near-End Loopback is enabled.

Value	Description
0	Normal operation. Collision test is disabled.
1	Enable collision test

Bit 6 – SPD_SEL[1] PHY Speed Select

See description for SPD_SEL[0] for details.

Note: Only 10 Mbit/s operation is supported. This bit is always '0'.

5.1.2. Basic Status

Name: BASIC_STATUS
Address: 0x01

Clause 22 Basic Status Register

Bit	15	14	13	12	11	10	9	8
	100BT4A	100BTXFDA	100BTXHDA	10BTFDA	10BTHDA	100BT2FDA	100BT2HDA	EXTSTS
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
		MFPRESUPA	AUTONEGC	RMTFLTD	AUTONEGA	LNKSTS	JABDET	EXTCAPA
Access	RO	RO	RO	RO	RO	RO	RC	RO
Reset	0	0	0	0	0	1	0	1

Bit 15 – 100BT4A 100BASE-T4 Ability
Note: 100BASE-T4 operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T4
1	PHY able to operate at 100BASE-T4

Bit 14 – 100BTXFDA 100BASE-TX Full Duplex Ability
Note: 100BASE-TX full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to perform full duplex 100BASE-TX
1	PHY able to perform full duplex 100BASE-TX

Bit 13 – 100BTXHDA 100BASE-TX Half Duplex Ability
Note: 100BASE-TX half duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to perform half duplex 100BASE-TX
1	PHY able to perform half duplex 100BASE-TX

Bit 12 – 10BTFDA 10BASE-T Full Duplex Ability
Note: Full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 10 Mbit/s in full duplex
1	PHY able to operate at 10 Mbit/s in full duplex

Bit 11 – 10BTHDA 10BASE-T Half Duplex Ability
Note: Half duplex operation is supported. This bit is always '1'.

Value	Description
0	PHY not able to operate at 10 Mbit/s in half duplex
1	PHY able to operate at 10 Mbit/s in half duplex

Bit 10 – 100BT2FDA 100BASE-T2 Full Duplex Ability
Note: 100BASE-T2 full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T2 in full duplex

Value	Description
1	PHY able to operate at 100BASE-T2 in full duplex

Bit 9 – 100BT2HDA 100BASE-T2 Half Duplex Ability

Note: 100BASE-T2 half duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T2 in half duplex
1	PHY able to operate at 100BASE-T2 in half duplex

Bit 8 – EXTSTS Extended status information ability

Note: Extended status information is not available. This bit is always '0'.

Value	Description
0	No extended status information in register 0x0F
1	Extended status information in register 0x0F

Bit 6 – MFPRESUPA Management Frame Preamble Suppression Ability

Note: Management frame preamble suppression is not supported. This bit is always '0'.

Value	Description
0	PHY will not accept management frames with preamble suppressed
1	PHY will accept management frames with preamble suppressed

Bit 5 – AUTONEGC Auto-Negotiation Complete

Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Auto-negotiation process has not completed
1	Auto-negotiation process has completed

Bit 4 – RMTFLTD Remote Fault Detection

Note: Remote fault detection is not supported. This bit is always '0'.

Value	Description
0	No remote fault condition detected
1	Remote fault condition detected

Bit 3 – AUTONEGA Auto-Negotiation Ability

Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	PHY is not able to perform auto-negotiation
1	PHY is able to perform auto-negotiation

Bit 2 – LNKSTS Link Status

Note: Link status indication is not supported. This bit is always '1'.

Value	Description
0	Network link is down
1	Network link is up

Bit 1 – JABDET Jabber Detection Status

This bit is set on detection of a jabber condition.

Value	Description
0	No jabber condition detected
1	Jabber condition detected

Bit 0 – EXTCAPA Extended Capabilities Ability

Note: Extended capabilities registers are supported. This bit is always ‘1’.

Value	Description
0	Extended capabilities registers not supported. Basic capabilities registers only.
1	Extended capabilities registers supported in addition to basic capabilities registers.

5.1.3. Basic Status - Rev D

Name: BASIC_STATUS - Rev D
Address: 0x01

Clause 22 Basic Status Register

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	100BT4A	100BTXFDA	100BTXHDA	10BTFDA	10BTHDA	100BT2FDA	100BT2HDA	EXTSTS
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
		MFPRESUPA	AUTONEGC	RMTFLTD	AUTONEGA	LNKSTS	JABDET	EXTCAPA
Access	RO	RO	RO	RO	RO	RO	RC	RO
Reset	0	0	0	0	0	0	0	1

Bit 15 – 100BT4A 100BASE-T4 Ability
Note: 100BASE-T4 operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T4
1	PHY able to operate at 100BASE-T4

Bit 14 – 100BTXFDA 100BASE-TX Full Duplex Ability
Note: 100BASE-TX full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to perform full duplex 100BASE-TX
1	PHY able to perform full duplex 100BASE-TX

Bit 13 – 100BTXHDA 100BASE-TX Half Duplex Ability
Note: 100BASE-TX half duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to perform half duplex 100BASE-TX
1	PHY able to perform half duplex 100BASE-TX

Bit 12 – 10BTFDA 10BASE-T Full Duplex Ability
Note: Full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 10 Mbit/s in full duplex
1	PHY able to operate at 10 Mbit/s in full duplex

Bit 11 – 10BTHDA 10BASE-T Half Duplex Ability
Note: Half duplex operation is supported. This bit is always '1'.

Value	Description
0	PHY not able to operate at 10 Mbit/s in half duplex
1	PHY able to operate at 10 Mbit/s in half duplex

Bit 10 – 100BT2FDA 100BASE-T2 Full Duplex Ability
Note: 100BASE-T2 full duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T2 in full duplex
1	PHY able to operate at 100BASE-T2 in full duplex

Bit 9 – 100BT2HDA 100BASE-T2 Half Duplex Ability

Note: 100BASE-T2 half duplex operation is not supported. This bit is always '0'.

Value	Description
0	PHY not able to operate at 100BASE-T2 in half duplex
1	PHY able to operate at 100BASE-T2 in half duplex

Bit 8 – EXTSTS Extended status information ability

Note: Extended status information is not available. This bit is always '0'.

Value	Description
0	No extended status information in register 0x0F
1	Extended status information in register 0x0F

Bit 6 – MFPRESUPA Management Frame Preamble Suppression Ability

Note: Management frame preamble suppression is not supported. This bit is always '0'.

Value	Description
0	PHY will not accept management frames with preamble suppressed
1	PHY will accept management frames with preamble suppressed

Bit 5 – AUTONEGC Auto-Negotiation Complete

Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	Auto-negotiation process has not completed
1	Auto-negotiation process has completed

Bit 4 – RMTFLTD Remote Fault Detection

Note: Remote fault detection is not supported. This bit is always '0'.

Value	Description
0	No remote fault condition detected
1	Remote fault condition detected

Bit 3 – AUTONEGA Auto-Negotiation Ability

Note: Auto-negotiation is not supported. This bit is always '0'.

Value	Description
0	PHY is not able to perform auto-negotiation
1	PHY is able to perform auto-negotiation

Bit 2 – LNKSTS Link Status

For revision D0 devices and later, this bit indicates a real-time link status.

Value	Description
0	Network link is down
1	Network link is up

Bit 1 – JABDET Jabber Detection Status

This bit is set on detection of a jabber condition.

Value	Description
0	No jabber condition detected

Value	Description
1	Jabber condition detected

Bit 0 – EXTCAPA Extended Capabilities Ability

Note: Extended capabilities registers are supported. This bit is always '1'.

Value	Description
0	Extended capabilities registers not supported. Basic capabilities registers only.
1	Extended capabilities registers supported in addition to basic capabilities registers.

5.1.4. PHY Identifier 1 Register

Name: PHY_ID1
Address: 0x02

This register contains the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22. Ethernet devices read this register to determine the upper three bytes of the Ethernet MAC address. The two least significant bits of the OUI are always 0 due to legacy compatibility, these two bits are not stored in this nor the following register. The OUI in both registers is stored in bit-reverse order, meaning the most significant bit (MSB) is stored in the register bit offset 0. The OUI is stored in little-endian format, meaning the most significant byte is stored in the following register. When combining these two data formats, the resulting data in the registers is saved as 0x03E000. Left shifting by two bits, results in the value of 0x0F8000, which corresponds to an OUI of 00:80:0F.

Bit	15	14	13	12	11	10	9	8
	OUI[2:9]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUI[10:17]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	1	1	1

Bits 15:8 – OUI[2:9] Organizationally Unique Identifier
This field contains the 3rd through the 10th bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22.

Bits 7:0 – OUI[10:17] Organizationally Unique Identifier
This field contains the 11th through the 18th bits of the Organizationally Unique Identifier (OUI) as specified in IEEE Std 802.3 Clause 22.

5.1.5. PHY Identifier 2 Register

Name: PHY_ID2
Address: 0x03

Bit	15	14	13	12	11	10	9	8
	OUI[18:23]						MODEL[5:4]	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	MODEL[3:0]				REV[3:0]			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	1	1	0	x	x	x	x

Bits 15:10 – OUI[18:23] Organizationally Unique Identifier
This field contains the 19th through the 24th bits of the Organizationally Unique Identifier (OUI). See register PHY_ID1 for complete OUI details

Bits 9:4 – MODEL[5:0] Manufacturer's Model Number
Six-bit manufacturer's model / product identification number

Value	Description
010110	LAN8670/1/2

Bits 3:0 – REV[3:0] Manufacturer's Revision Number
Four-bit manufacturer's silicon revision identification number
Note: The default value of the this field varies dependent on the silicon revision number.

Value	Description
0000	Silicon revision 0
0010	Silicon revision 2
0100	Silicon revision 4
0101	Silicon revision 5 (Rev C2 default)
0110	Silicon revision 6 (Rev D0 default)

5.1.6. MMD Access Control Register

Name: MMDCTRL
Address: 0x0D

Bit	15	14	13	12	11	10	9	8
	FNCTN[1:0]							
Access	R/W	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
				DEVAD[4:0]				
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:14 – FNCTN[1:0] MMD Function
This field specifies the action to be performed when reading or writing the MMD Access Address/ Data register.

Value	Description
00	Address
01	Data - No post increment
10	Data - Post increment on reads and writes
11	Data - Post increment on writes only

Bits 4:0 – DEVAD[4:0] Device Address
Address of the MDIO Manageable Device to access.

Value	Description
00001	PMA/PMD
00011	PCS
11111	Vendor Specific 2
Others	Reserved - do not access

5.1.7. MMD Access Address/Data Register

Name: MMDAD
Address: 0x0E

Bit	15	14	13	12	11	10	9	8
	ADR_DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADR_DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – ADR_DATA[15:0] MMD Address / Data
Functionality depends on the MMD Function (FNCTN) bits in the MMD Access Control (MMDCTRL) register as specified in IEEE Std 802.3 Annex 22D:

- `00b` = Writing this field sets the offset of the register within the MMD to access
- `01b`, `10b`, `11b` = When written, the contents are written into the MMD register
- `01b`, `10b`, `11b` = When read, the contents from the MMD register are returned

Related Links
MMDCTRL
MMD Access Control Register

5.1.8. Strap Control 0 Register

Name: STRAP_CTRL0
Address: 0x12

This register reports the device packet type and the status of the external strap pins, as captured at power-on.

Important: For proper device operation, do not change the value of any bits in this register.

Bit	15	14	13	12	11	10	9	8
								MITYP[1]
Access	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	x

Bit	7	6	5	4	3	2	1	0
	MITYP[0]	PKGTYP[1:0]		SMIADR[4:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	x	x	x	x	x	x	x	x

Bits 8:7 – MITYP[1:0] Media Interface Type - LAN8670 only
In the LAN8670, this field indicates the media interface type as defined by state of the MODE[1:0] configuration strap pins at reset.
Note: This bit field is undetermined in the LAN8671 and LAN8672.

Value	Description
00b	Invalid external strap setting
01b	RMII MODE[1:0] = 10b
10b	MII MODE[1:0] = 01b
11b	Single Clock MII (SC-MII) MODE[1:0] = 11b

Bits 6:5 – PKGTYP[1:0] Package Type
This field indicates the product and package type.

Value	Description
00b	Invalid
01b	32-pin LAN8670
10b	24-pin LAN8671 with RMII interface
11b	36-pin LAN8672 (Revision C2, only) with MII interface

Bits 4:0 – SMIADR[4:0] Serial Management Interface Address
This field indicates the SMI address as defined by the PHYAD[] configuration strap pins at reset.

Value	Description
xxxxxb	Serial Management Interface Address: LAN8670/2
0xxxxb	Serial Management Interface Address: LAN8671

Related Links
Configuration Straps

5.2. PMA/PMD Registers

The PMA/PMD registers are located at MDIO Manageable Device (MMD) address 0x01.

Important: RESERVED address space must not be written to except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x11	Reserved									
0x12	T1PMAPMDEXTA	15:8								
		7:0					T1SABL	T1LABL		
0x14 ... 0x0833	Reserved									
0x0834	T1PMAPMDCTL	15:8								
		7:0					TYPSEL[3:0]			
0x0836 ... 0x08F8	Reserved									
0x08F9	T1SPMACTL	15:8	RST	TXD			LPE	MDE		
		7:0								LBE
0x08F9	T1SPMACTL - Rev D	15:8	RST	TXD			LPE	MDE		
		7:0								LBE
0x08FA	T1SPMASTS	15:8			LBA		LPA	MDA	RXFA	
		7:0							RXFD	
0x08FB	T1STSTCTL	15:8	TSTCTL[2:0]							
		7:0								

5.2.1. BASE-T1 PMA/PMD Extended Ability

Name: T1PMAPMDEXTA
Address: 0x0012

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					T1SABL	T1LABL		
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	0	0

Bit 3 – T1SABL 10BASE-T1S Ability
This bit indicates the ability of the PHY to support 10BASE-T1S.
Note: 10BASE-T1S operation is supported. This bit always reads 1.

Value	Description
0	PMA/PMD is not able to perform 10BASE-T1S operation
1	PMA/PMD is able to perform 10BASE-T1S operation

Bit 2 – T1LABL 10BASE-T1L Ability
This bit indicates the ability of the PHY to support 10BASE-T1L.
Note: 10BASE-T1L operation is not supported. This bit always reads 0.

Value	Description
0	PMA/PMD is not able to perform 10BASE-T1L operation
1	PMA/PMD is able to perform 10BASE-T1L operation

5.2.2. BASE-T1 PMA/PMD Control

Name: T1PMAPMDCTL
Address: 0x0834

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					TYPSEL[3:0]			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	1	1

Bits 3:0 – TYPSEL[3:0] Type Selection
This field sets the PMA/PMD mode of operation.
Note: Only 10BASE-T1S operation is supported. This field always reads `0011b`.

Value	Description
`0000b`	100BASE-T1
`0001b`	1000BASE-T1
`0010b`	10BASE-T1L
`0011b`	10BASE-T1S
`01xxb`	Reserved
`1xxxb`	Reserved

5.2.3. 10BASE-T1S PMA Control

Name: T1SPMACTL
Address: 0x08F9

Bit	15	14	13	12	11	10	9	8
	RST	TXD			LPE	MDE		
Access	R/W SC	R/W	RO	RO	R/W	R/W	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								LBE
Access	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – RST PMA Reset
Setting this bit will reset the device PMA.
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal Operation
1	PMA Reset

Bit 14 – TXD Transmit Disable
The PMA transmit path is disabled when this bit is set. This bit must be clear for normal operation.

Value	Description
0	Normal operation
1	Transmit disable

Bit 11 – LPE Low Power Enable
Setting this bit will power down the PMA.
Note: This bit has the same effect as the Power Down bit in the Clause 22 BASIC_CONTROL register.

Value	Description
0	Normal operation
1	Place PMA into low-power mode

Bit 10 – MDE Multidrop Enable
When set, this bit will enable multidrop operation on a mixing segment.
Note: This bit has no effect on the operation of the device.

Value	Description
0	Disable mixing segment operation (point-to-point mode)
1	Enable PMA multidrop (mixing segment) operation

Bit 0 – LBE PMA Loopback Enable
This bit will enable the PMA loopback test mode when set. Data received from the MAC via the media interface will be passed through the PCS scrambler/descrambler, 4B/5B encoder/decoder, and the PMA differential Manchester encoder/decoder and returned back to the MAC.

Important: PLCA must be disabled or configured as the PLCA Coordinator (Local ID = 0) when the PMA loopback mode is enabled.

Value	Description
0	Disable PMA loopback mode
1	Enable PMA loopback mode

5.2.4. 10BASE-T1S PMA Control - Rev D

Name: T1SPMACTL - Rev D
Address: 0x08F9

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	RST	TXD			LPE	MDE		
Access	R/W SC	R/W	RO	RO	R/W	RO	RO	RO
Reset	0	0	0	0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
								LBE
Access	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – RST PMA Reset
Setting this bit will reset the device PMA.
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal Operation
1	PMA Reset

Bit 14 – TXD Transmit Disable
The PMA transmit path is disabled when this bit is set. This bit must be clear for normal operation.

Value	Description
0	Normal operation
1	Transmit disable

Bit 11 – LPE Low Power Enable
Setting this bit will power down the PMA.
Note: This bit has the same effect as the Power Down bit in the Clause 22 BASIC_CONTROL register.

Value	Description
0	Normal operation
1	Place PMA into low-power mode

Bit 10 – MDE Multidrop Mode
When set, this bit will enable multidrop operation on a mixing segment.
Note: This bit has no effect on the operation of the device.

Value	Description
0	Mixing segment operation disabled (point-to-point mode)
1	PMA multidrop (mixing segment) operation enabled

Bit 0 – LBE PMA Loopback Enable
This bit will enable the PMA loopback test mode when set. Data received from the MAC via the media interface will be passed through the PCS scrambler/descrambler, 4B/5B encoder/decoder, and the PMA differential Manchester encoder/decoder and returned back to the MAC.

Important: PLCA must be disabled or configured as the PLCA Coordinator (Local ID = 0) when the PMA loopback mode is enabled.

Value	Description
0	Disable PMA loopback mode
1	Enable PMA loopback mode

5.2.5. 10BASE-T1S PMA Status

Name: T1SPMASTS
Address: 0x08FA

Bit	15	14	13	12	11	10	9	8
			LBA		LPA	MDA	RXFA	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	1	0	1	1	0	0

Bit	7	6	5	4	3	2	1	0
							RXFD	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 13 – LBA PMA Loopback Ability
This bit indicates that the device has PMA loopback ability.
Note: PMA loopback is supported. This bit always reads as 1.

Value	Description
0	PHY does not support PMA loopback mode
1	PHY supports PMA loopback mode

Bit 11 – LPA Low Power Ability
This bit is set to indicate that the device PMA supports a low power state.
Note: PMA low power mode is supported. This bit always reads as 1.

Value	Description
0	PMA does not have low power ability
1	PMA has low power ability

Bit 10 – MDA Multidrop Ability
This bit is set to indicate that the device supports multidrop operation on a mixing segment.
Note: Multidrop mixing segment operation is supported. This bit always reads as 1.

Value	Description
0	PMA does not support mixing segment operation (point-to-point only)
1	PMA supports multidrop (mixing segment) operation

Bit 9 – RXFA Receive Fault Ability
This bit indicates the ability of the device to detect a fault on the PMA receive path.
Note: The device is unable to detect a PMA receive path fault. This bit always reads as 0.

Value	Description
0	PHY does not have the ability to detect PMA faults
1	PHY has the ability to detect faults in the PMA receive path

Bit 1 – RXFD Receive Fault Detection
This bit will be set when the PMA has detected a fault on the receive path.
Note: The device PMA does not support PMA receive fault detection. This bit always reads 0.

Value	Description
0	No PMA fault detected
1	PMA fault condition detected

5.2.6. 10BASE-T1S Test Mode Control

Name: T1STSTCTL
Address: 0x08FB

Bit	15	14	13	12	11	10	9	8
	TSTCTL[2:0]							
Access	R/W	R/W	R/W	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:13 – TSTCTL[2:0] Test Mode Control
This field configures and enables the various IEEE specified test modes. For a description of the test modes, refer to Clause 147.5.2 of the IEEE Std 802.3-2022.

Value	Description
000	Normal (non-test) operation
001	Test mode 1 - Transmitter output voltage, timing jitter
010	Test mode 2 - Transmitter output droop
011	Test mode 3 - Transmitter PSD mask
100	Test mode 4 - Transmitter high impedance mode
101	Reserved
11x	Reserved

5.3. PCS Registers

The PCS registers are located at MDIO Manageable Device (MMD) address 0x03.

Important: RESERVED address space must not be written to except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x08F2	Reserved									
0x08F3	T1SPCSCTL	15:8	RST	LBE						DUPLEX
		7:0								
0x08F4	T1SPCSSTS	15:8								
		7:0	FAULT							
0x08F5	T1SPCSDIAG1	15:8	RMTJABCNT[15:8]							
		7:0	RMTJABCNT[7:0]							
0x08F6	T1SPCSDIAG2	15:8	CORTXCNT[15:8]							
		7:0	CORTXCNT[7:0]							

5.3.1. 10BASE-T1S PCS Control

Name: T1SPCSCTL
Address: 0x08F3

Bit	15	14	13	12	11	10	9	8
	RST	LBE						DUPLEX
Access	R/W SC	R/W	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – RST PCS Reset
When this bit is set, the PCS 4B5B encoder/decoder, scrambler/descrambler, and frame encoder/decoder blocks will be reset.
Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal Operation
1	PCS reset

Bit 14 – LBE PCS Loopback Enable
When this bit is set, data from the MAC will be passed through the PHY to the PCS and returned back to the MAC. This tests the full path from the MAC media interface through the PCS scrambler/descrambler and 4B/5B encoder/decoder.

Important: PLCA must be disabled when the PCS loopback mode is enabled.

Value	Description
0	Disable PCS loopback mode
1	Enable PCS loopback mode

Bit 8 – DUPLEX Duplex Mode
Note: Only half-duplex operation is supported. This bit is always 1.

Value	Description
0	Full-duplex operation
1	Half-duplex operation

5.3.2. 10BASE-T1S PCS Status

Name: T1SPCSSTS
Address: 0x08F4

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FAULT							
Access	RC	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 7 – FAULT PCS Fault Indication

This bit will be set when the PCS has detected a fault condition on the receive or transmit path.

Note: This bit always reads '0' as there are no detectable PCS faults.

Value	Description
0	No PCS fault detected
1	PCS fault condition detected

5.3.3. 10BASE-T1S PCS Diagnostic 1

Name: T1SPCSDIAG1
Address: 0x08F5

Bit	15	14	13	12	11	10	9	8
	RMTJABCNT[15:8]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RMTJABCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RMTJABCNT[15:0] Remote Jabber Count
Field counting the number of remote jabber events (ESDJAB) received since the last read of the register. This field will saturate at 0xFFFF.

5.3.4. 10BASE-T1S PCS Diagnostic 2

Name: T1SPCSDIAG2
Address: 0x08F6

Bit	15	14	13	12	11	10	9	8
	CORTXCNT[15:8]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CORTXCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CORTXCNT[15:0] Corrupted Transmit Count
Field containing the number of times a locally initiated transmission resulted in a corrupted signal at the MDI. Corruption during transmission would typically be due to collisions on the physical layer. This field is self-clearing when read. This field will saturate at 0xFFFF.

5.4. Miscellaneous Registers

The miscellaneous registers are located at MDIO Manageable Device (MMD) address 0x1F.

Important: RESERVED address space must not be written to except when specifically directed to by Microchip. Failure to heed this warning may result in adverse operation and unexpected results.

Important: When writing to registers containing RESERVED bit fields, use a read-modify-write operation to avoid accidental modifications to RESERVED bit fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00 ... 0x0E	Reserved									
0x0F	CFGPRTCTL	15:8	KEY2	KEY1						
		7:0								WREN
0x10	CTRL1	15:8								
		7:0					IWDE	BCAEN	DIGLBE	
0x10	CTRL1 - Rev D	15:8								
		7:0						BCAEN	DIGLBE	
0x11	PINCTRL	15:8	GPIO0SS[1:0]							
		7:0	TXPIPOL[1:0]		RXPIPOL[1:0]				ACMAPOL[1:0]	
0x12	LSCTL - Rev D	15:8	LSPSEL[2:0]			LSCFG[1:0]		LSTMR[1:0]		
		7:0								LSSEM
0x14 ... 0x17	Reserved									
0x18	STS1	15:8				SQI	PSTC	TXCOL	TXJAB	TSSI
		7:0	EMPCYC	RXINTO	UNEXPB	BCNBFTO	UNCRS	PLCASYM	ESDERR	DEC5B
0x18	STS1 - Rev D	15:8	SLPFAIL	TDD	LNKSTSC	SQI	PSTC	TXCOL	TXJAB	TSSI
		7:0	EMPCYC		HDDD	PLCADIAG	UNCRS	PLCASYM	ESDERR	DEC5B
0x19	STS2	15:8					RESETC	WKEMDI	WKEWI	UV33
		7:0		OT	IWDTO					
0x19	STS2 - Rev D	15:8					RESETC	WKEMDI	WKEWI	UV33
		7:0		OT						
0x1A	STS3	15:8								
		7:0	ERRTOID[7:0]							
0x1C	IMSK1	15:8				SQIM	PSTCM	TXCOLM	TXJABM	TSSIM
		7:0	EMPCYCM	RXINTOM	UNEXPBM	BCNBFTOM	UNCRSM	PLCASYMM	ESDERRM	DEC5BM
0x1C	IMSK1 - Rev D	15:8	SLPFAILM	TDDM	LNKSTSC	SQIM	PSTCM	TXCOLM	TXJABM	TSSIM
		7:0	EMPCYCM		HDDDM	PLCADIAGM	UNCRSM	PLCASYMM	ESDERRM	DEC5BM
0x1D	IMSK2	15:8					RESETCM	WKEMDIM	WKEWIM	UV33M
		7:0		OTM	IWDTOM					
0x1D	IMSK2 - Rev D	15:8					RESETCM	WKEMDIM	WKEWIM	UV33M
		7:0		OTM						
0x1F	Reserved									
0x20	CTRCTRL	15:8								
		7:0							TOCTRE	BCNCTRE
0x22 ... 0x23	Reserved									
0x24	TOCNTH	15:8	TOCNT[31:24]							
		7:0	TOCNT[23:16]							
0x25	TOCNTL	15:8	TOCNT[15:8]							
		7:0	TOCNT[7:0]							

Miscellaneous Registers (continued)

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x26	BCNCNTH	15:8	BCNCNT[31:24]							
		7:0	BCNCNT[23:16]							
0x27	BCNCNTL	15:8	BCNCNT[15:8]							
		7:0	BCNCNT[7:0]							
0x29 ... 0x2F	Reserved									
0x30	MULTID0	15:8	ID1[7:0]							
		7:0	ID2[7:0]							
0x31	MULTID1	15:8	ID3[7:0]							
		7:0	ID4[7:0]							
0x32	MULTID2	15:8	ID5[7:0]							
		7:0	ID6[7:0]							
0x33	MULTID3	15:8	ID7[7:0]							
		7:0	ID8[7:0]							
0x35	PRSCTL1	15:8						FBEN		
		7:0								
0x35	PRSCTL1 - Rev D	15:8						FBEN		
		7:0								
0x36	PRSSTS	15:8	MAXID[7:0]							
		7:0								
0x38 ... 0x3C	Reserved									
0x3D	PRTMGMT2	15:8			MIRXWDEN	PRIWDEN	MITXWDEN			
		7:0								
0x3D	PRTMGMT2 - Rev D	15:8								
		7:0								
0x3E	IWDTOH	15:8	TIMEOUT[31:24]							
		7:0	TIMEOUT[23:16]							
0x3E	IWDTOH - Rev D	15:8								
		7:0								
0x3F	IWDTOL	15:8	TIMEOUT[15:8]							
		7:0	TIMEOUT[7:0]							
0x3F	IWDTOL - Rev D	15:8								
		7:0								
0x40	TXMCTL	15:8								
		7:0	TXPMDET					MACTXTSE	TXME	
0x41	TXMPATH	15:8								
		7:0	TXMPAT[23:16]							
0x42	TXMPATL	15:8	TXMPAT[15:8]							
		7:0	TXMPAT[7:0]							
0x44 ... 0x48	Reserved									
0x49	TXMDLY	15:8	TXMDLYEN					TXMPKTDLY[10:8]		
		7:0	TXMPKTDLY[7:0]							
0x4B ... 0x4F	Reserved									
0x50	RXMCTL	15:8								
		7:0		RXPMDET					RXME	
0x51	RXMPATH	15:8								
		7:0	RXMPAT[23:16]							
0x52	RXMPATL	15:8	RXMPAT[15:8]							
		7:0	RXMPAT[7:0]							
0x54 ... 0x58	Reserved									
0x59	RXMDLY	15:8	RXMDLYEN					RXMPKTDLY[10:8]		
		7:0	RXMPKTDLY[7:0]							

Miscellaneous Registers (continued)

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x5B ... 0x5F	Reserved									
0x60	CBSSPTHH	15:8								
		7:0					STOPTHR[19:16]			
0x61	CBSSPTHL	15:8	STOPTHR[15:8]							
		7:0	STOPTHR[7:0]							
0x62	CBSSTTHH	15:8								
		7:0					STARTTHR[19:16]			
0x63	CBSSTTHL	15:8	STARTTHR[15:8]							
		7:0	STARTTHR[7:0]							
0x64	CBSSLPCTL	15:8	FALLSLP[6:0]							
		7:0	RISESLP[6:0]							
0x65	CBSTPLMTH	15:8								
		7:0					TOPLIMIT[19:16]			
0x66	CBSTPLMTL	15:8	TOPLIMIT[15:8]							
		7:0	TOPLIMIT[7:0]							
0x67	CBSBTLMTH	15:8								
		7:0					BOTLIMIT[19:16]			
0x68	CBSBTLMTL	15:8	BOTLIMIT[15:8]							
		7:0	BOTLIMIT[7:0]							
0x69	CBSCRCTRH	15:8								
		7:0					CREDITCTR[19:16]			
0x6A	CBSCRCTRL	15:8	CREDITCTR[15:8]							
		7:0	CREDITCTR[7:0]							
0x6B	CBSCTRL	15:8								ECCRDS[7]
		7:0	ECCRDS[6:0]							CBSEN
0x6D ... 0x6F	Reserved									
0x70	PLCASKPCTL	15:8								
		7:0							TOSKPEN	
0x71	PLCATOSKP	15:8								
		7:0	TOSKPNUM[7:0]							
0x73	Reserved									
0x74	ACMACTL	15:8								
		7:0								ACMAEN
0x76 ... 0x7F	Reserved									
0x80	SLPCTL0	15:8	SLPEN	WKINEN	MDIWKEN	SLPINHDLY[1:0]				
		7:0		SLPCAL[3:0]						
0x80	SLPCTL0 - Rev D	15:8	WKINEN	MDIWKEN	SLPINHDLY[1:0]					
		7:0								
0x81	SLPCTL1	15:8								
		7:0	WOPOL		WIPOL			MWKFWD	WKOFWDEN	MDIFWDEN
0x81	SLPCTL1 - Rev D	15:8	WIOEN							
		7:0			WIPOL			WKOREQ	WKOFWDEN	MDIFWDEN
0x83 ... 0x86	Reserved									
0x87	CDCTL0	15:8	CDEN							
		7:0								
0x87	CDCTL0 - Rev D	15:8	CDEN					CCMFC[1:0]		
		7:0								
0x89 ... 0x9F	Reserved									
0xA0	SQICTL	15:8	SQIRST	SQIEN						
		7:0								

Miscellaneous Registers (continued)

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xA0	SQICTL - Rev D	15:8								
		7:0								
0xA1	SQISTS0	15:8								
		7:0	SQIERR	SQIVLD	SQIVAL[2:0]			SQIERRC[2:0]		
0xA1	SQISTS0 - Rev D	15:8								
		7:0								
0xA3 ... 0xA9	Reserved									
0xAA	SQICFG0	15:8					TOID[7:4]			
		7:0	TOID[3:0]							
0xAA	SQICFG0 - Rev D	15:8								
		7:0								
0xAC	SQICFG2	15:8				SQIINTTHR[4:0]				
		7:0								
0xAC	SQICFG2 - Rev D	15:8								
		7:0								
0xAE ... 0xCA	Reserved									
0xCB	PADCTRL3	15:8	PDRV4[1:0]		PDRV3[1:0]		PDRV2[1:0]		PDRV1[1:0]	
		7:0								
0xCD ... 0xD4	Reserved									
0xD5	ANALOG5	15:8	UV33FTM[7:0]							
		7:0								
0xD7 ... 0xC9FF	Reserved									
0xCA00	MIDVER	15:8	IDM[7:0]							
		7:0	VER[7:0]							
0xCA00	MIDVER - Rev D	15:8	IDM[7:0]							
		7:0	VER[7:0]							
0xCA01	PLCA_CTRL0	15:8	EN	RST						
		7:0								
0xCA02	PLCA_CTRL1	15:8	NCNT[7:0]							
		7:0	ID[7:0]							
0xCA03	PLCA_STS	15:8	PST							
		7:0								
0xCA04	PLCA_TOTMR	15:8								
		7:0	TOTMR[7:0]							
0xCA05	PLCA_BURST	15:8	MAXBC[7:0]							
		7:0	BTMR[7:0]							
0xCA06	PLCA_DIAG - Rev D	15:8								
		7:0						RXINTO	UNEXPB	BCNBFTO
0xCA08 ... 0xCBFF	Reserved									
0xCC00	ADFCAP - Rev D	15:8						HDD[2:0]		
		7:0				SQIP[3:0]				SQI
0xCC01	HDD - Rev D	15:8	HDDREQ	HDDRDY	START					
		7:0						VALID	SHTOPNSTS[1:0]	
0xCC02	DCQ_TOID - Rev D	15:8								
		7:0	TOID[7:0]							
0xCC03	DCQ_SQI - Rev D	15:8	SQI_UPD							
		7:0						SQI[2:0]		
0xCC04	DCQ_SQIP - Rev D	15:8	SQIP_UDP							
		7:0	SQIP[7:3]							

Miscellaneous Registers (continued)

Address	Name	Bit Pos.	7	6	5	4	3	2	1	0
0xCC06 ... 0xCDFF	Reserved									
0xCE00	TDCTL - Rev D	15:8	TDEN	REFN	INTDLYSTRT	DISTMESDUR[3:0]				DISTMESSTR
		7:0	AUTOSTR							
0xCE01	TDSTS - Rev D	15:8	INTDLYDN	INTDLYERR	DISTMESDN	DISTMESERR	AUTOERR			
		7:0								
0xCE02	TDDISTRESL - Rev D	15:8	DISTRESL[15:8]							
		7:0	DISTRESL[7:0]							
0xCE03	TDDISTRESH - Rev D	15:8	DISTRESH[15:8]							
		7:0	DISTRESH[7:0]							
0xCE04	TDINTDLYRESL - Rev D	15:8	INTDLYRESL[15:8]							
		7:0	INTDLYRESL[7:0]							
0xCE05	TDINTDLYRESH - Rev D	15:8	INTDLYRESH[15:8]							
		7:0	INTDLYRESH[7:0]							
0xCE06	TDMNDLYRESL - Rev D	15:8	MNDLYRESL[15:8]							
		7:0	MNDLYRESL[7:0]							
0xCE07	TDMNDLYRESH - Rev D	15:8	MNDLYRESH[15:8]							
		7:0	MNDLYRESH[7:0]							
0xCE08	TDMNMESDUR - Rev D	15:8	MNDLYDUR[3:0]							
		7:0								
0xCE0A ... 0xCEFF	Reserved									
0xCF00	TDADVCTRL - Rev D	15:8	DMTODIS							
		7:0								
0xCF02 ... 0xCFFF	Reserved									
0xD000	WS_STS - Rev D	15:8	LPCAP	LPFAIL						
		7:0								
0xD001	WS_CTRL	15:8	LPREQ	LPEXIT						
		7:0								

5.4.1. Configuration Protection Control

Name: CFGPRTCTL
Address: 0x000F

Bit	15	14	13	12	11	10	9	8
	KEY2	KEY1						
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								WREN
Access	RO	RO	RO	RO	RO	RO	RO	
Reset	0	0	0	0	0	0	0	1

Bit 15 – KEY2 Key #2 Accepted

This bit is set when Key #2 (535Ah) has been successfully written to this register after Key #1.
Note: This bit is cleared on write to any other bit field in this register.

Value	Description
0	Key #2 has not been successfully written after Key #1
1	Key #2 has been successfully written after Key #1

Bit 14 – KEY1 Key #1 Accepted

This bit is set when Key #1 (5341h) has been successfully written to this register.
Note: This bit is cleared on write of any other value is to this register, except Key #2.

Value	Description
0	Key #1 has not been successfully written
1	Key #1 has been successfully written

Bit 0 – WREN Configuration Write Enable

When this bit is clear, writes to register bit fields are disabled to protect against accidental configuration changes. Writable bit fields may be written when this bit is set.
Note: This bit may only be written once both Key #1 and Key #2 have been successfully written in the correct sequence and fields KEY1 and KEY2 are both set.

Note: Writes to Clause 22 MMD Control (MMDCTRL) and MMD Address/Data (MMDAD) registers are not blocked when this bit is clear as they are needed to write to this CFGPRTCTL register.

Value	Description
0	Writes to register bit fields disabled (Protected mode)
1	Writes to register bit fields enabled (Normal operation)

5.4.2. Control 1 Register

Name: CTRL1
Address: 0x0010

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	RO	RO	RO	RO	R/W	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					IWDE	BCAEN	DIGLBE	
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0

Bit 3 – IWDE Inactivity Watchdog Enable
When set, this bit enables the (MII/SC-MII/RMII/SMI) inactivity watchdog.

Value	Description
0	Inactivity watchdog disabled
1	Inactivity watchdog enabled

Bit 2 – BCAEN Broadcast Address Enable
When set, this the PHY will respond to SMI address 0x00 in addition to the address configured by the PHYADn configuration straps.

Value	Description
0	PHY will ignore SMI accesses to address 0x00.
1	PHY will respond to SMI accesses to address 0x00.

Bit 1 – DIGLBE Digital Loopback Enable
Enables a digital loopback from the differential Manchester encoder to the decoder.

Value	Description
0	Normal operation
1	Digital loopback enabled

5.4.3. Control 1 Register - Rev D

Name: CTRL1 - Rev D
Address: 0x0010

This register is only valid for devices of Revision D0 and later.

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	RO	RO	RO	RO	R/W	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						BCAEN	DIGLBE	
Access	RO	RO	RO	RO	RO	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0

Bit 2 – BCAEN Broadcast Address Enable
When set, this the PHY will respond to SMI address 0x00 in addition to the address configured by the PHYADn configuration straps.

Value	Description
0	PHY will ignore SMI accesses to address 0x00.
1	PHY will respond to SMI accesses to address 0x00.

Bit 1 – DIGLBE Digital Loopback Enable
Enables a digital loopback from the differential Manchester encoder to the decoder.

Value	Description
0	Normal operation
1	Digital loopback enabled

5.4.4. Pin Control Register

Name: PINCTRL
Address: 0x0011

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	GPIO0SS[1:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXPIPOL[1:0]		RXPIPOL[1:0]				ACMAPOL[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:14 – GPIO0SS[1:0] GPIO0 Signal Select
This field configures the GPIO0 signal select. The valid configurations and restrictions for each device and operating mode are shown in Table 5-1.

Table 5-1. GPIO0 Signal Select Restrictions

		LAN8670			LAN8671	LAN8672[1]
GPIO0SS	Signal	MII	SC-MII	RMII	RMII	MII
00	RXPI	✓	Reserved	Reserved	✓	Reserved
01	TXPI	✓	✓	✓	✓	✓
10	RXTXPI	✓	✓	✓	✓	✓
11	ACMA	✓	Reserved	Reserved	✓	Reserved

Note:
1. LAN8672 Revision C2, only.

Value	Description
00	Receive packet indication output pulse (RXPI)
01	Transmit packet indication output pulse (TXPI)
10	Receive/Transmit packet indication output pulse (RXTXPI)
11	Application Controlled Media Access input (ACMA)

Bits 7:6 – TXPIPOL[1:0] TXPI Polarity
This field configures the TXPI pin output polarity on a transmit packet indication. Additionally, when GPIO0 is configured as RXTXPI output, this field will configure the output polarity of RXTXPI on indication of a receive *or* transmit packet.

Value	Description
00	Transmit packet indication on rising edge of 200 ns positive pulse (pin is idle low)
01	Transmit packet indication on falling edge of 200 ns negative pulse (pin is idle high)
10	Undefined
11	Undefined

Bits 5:4 – RXPIPOL[1:0] RXPI Polarity
This field configures the RXPI pin output polarity on a receive packet indication.

Value	Description
00	Receive packet indication on rising edge of 200 ns positive pulse (pin is idle low)
01	Receive packet indication on falling edge of 200 ns negative pulse (pin is idle high)
10	Undefined
11	Undefined

Bits 1:0 – ACMAPOL[1:0] ACMA Polarity

This field configures the polarity of the ACMA pin that enables the PHY to transmit.

Value	Description
00	The PHY will be allowed to transmit when the ACMA pin is asserted high.
01	The PHY will be allowed to transmit when the ACMA pin is asserted low.
10	Undefined
11	Undefined

5.4.5. Link Status Control - Rev D

Name: LSCTL - Rev D
Address: 0x0012

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	LSPSEL[2:0]			LSCFG[1:0]		LSTMR[1:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								LSSEM
Access	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:13 – LSPSEL[2:0] Link Status Pin Select
When enabled, this field controls which pin is driven to reflect the link status state.

Value	Description
000	Disabled; Link status is not output to a pin.
001	LAN8671 pin 17 (WAKE_OUT)
010	LAN8670 pin 9 (GPIO0) LAN8671 pin 7 (GPIO0) This overrides the GPIO0SS settings in the PINCTRL register
011	LAN8670 pin 11 (TXER/ACMA)
others	Reserved

Bits 12:11 – LSCFG[1:0] Link Status Configuration
This field configures the link status behavior.

Value	Description
00	**Fixed** - Link Status is always zero indicating “no link” (default)
01	**PLCA Status** - When PLCA is enabled, link status reflects PLCA status.
10	**Semaphore** - Link status is controlled by the value written into the LSSEM bit.
11	**Activity** - When PLCA is enabled and the node is configured as a PLCA follower, link status will be set when PLCA BEACONs are actively detected. When configured as a PLCA coordinator, link status will be set when a packet has been received from another device on the mixing segment.

Bits 10:9 – LSTMR[1:0] Link Status Timer
This field configured the time for link status to return to false once link goes away.

Value	Description
00	15 ms
01	100 ms
10	500 ms
11	1000 ms

Bit 0 – LSSEM Link Status Semaphore
When link status is set to “semaphore” mode, LSCFG =10b, *Semaphore*, the value written to this bit controls the state of the IEEE Link Status bit as well as the output state of the Link Status pin, if enabled.

Value	Description
0	Link status is set to false

Value	Description
1	Link status is set to true

5.4.6. Status 1 Register

Name: STS1
Address: 0x0018

Bit	15	14	13	12	11	10	9	8
				SQI	PSTC	TXCOL	TXJAB	TSSI
Access	RO	RO	RO	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EMPCYC	RXINTO	UNEXPB	BCNBFTO	UNCRS	PLCASYM	ESDERR	DEC5B
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit 12 – SQI Signal Quality Indication Status
This bit is set to indicate an SQI status change.

Value	Description
0	SQI status has not changed.
1	SQI status has changed.

Bit 11 – PSTC PLCA Status Changed
This bit is set to indicate that the PLCA Status (PST) bit has changed within the PLCA Status (PLCA_STS) register.

Value	Description
0	PLCA Status has not changed.
1	PLCA Status has changed.

Bit 10 – TXCOL Transmit Collision Status
Physical collision on the network was detected. This does not include logical collisions due to normal operation of PLCA.

Value	Description
0	No collision detected during transmit
1	Collision detected during transmit

Bit 9 – TXJAB Transmit Jabber Status
This bit indicates the occurrence of a transmit jabber condition. A jabber condition occurs when the PHY detects that the PCS has remained in the transmit state longer than 2 ms. When a jabber condition is detected, the transmitter is disabled for the duration of 16 ms.

Value	Description
0	No transmit jabber detected
1	Transmit jabber detected

Bit 8 – TSSI Time Synchronization Service Interface Status
This bit is set when the TSSI has indicated the transmission or reception of an Ethernet packet.

Value	Description
0	No transmitted or received frames indicated
1	A transmitted or received frame has been indicated

Bit 7 – EMPCYC PLCA Empty Cycle Status

This bit indicates the detection of an empty PLCA bus cycle. An empty bus cycle occurs when the node detects no transmissions in any of the possible transmit opportunities between two successive BEACONs.

Value	Description
0	An empty PLCA cycle has not been detected
1	An empty PLCA cycle has been detected

Bit 6 – RXINTO Receive in Transmit Opportunity

This bit indicates the detection of another node transmitting in this node's local assigned transmit opportunity. This could indicate multiple nodes being assigned the same Local ID.

Value	Description
0	Another node has not been detected transmitting in this node's TO
1	Another node has been detected transmitting in this node's TO

Bit 5 – UNEXPB Unexpected BEACON Received

When configured as the PLCA coordinator in charge of transmitting the periodic coordinating BEACONs, this bit indicates the detection of an unexpected BEACON on the segment. This condition may be due to the configuration of multiple PLCA coordinators on the segment.

Value	Description
0	Another node on the segment has not been detected transmitting a BEACON
1	Another node on the segment has been detected transmitting a BEACON

Bit 4 – BCNBFTO BEACON Received Before Transmit Opportunity

This bit indicates the detection of a BEACON before the node's assigned transmit opportunity. This condition could indicate the configuration of multiple PLCA coordinators on the segment. Other conditions that may cause this to occur include a PLCA coordinator with an incorrectly configured maximum node count resulting in a PLCA cycle that is too short, or a PLCA Local ID that is configured beyond the PLCA cycle.

Value	Description
0	A BEACON has not been detected before local transmit opportunity
1	A BEACON was detected before local transmit opportunity

Bit 3 – UNCRS Unexpected Carrier Sense

When operating in ACMA mode, this bit will indicate carrier sense during this PHY's transmit slot when ACMA is asserted.

Value	Description
0	No Carrier has been sensed during PHY's ACMA time slot
1	Carrier has been sensed during PHY's ACMA time slot

Bit 2 – PLCASYM PLCA Symbols Detected

This bit indicates the detection of PLCA BEACON symbols when PLCA is not enabled. This condition may indicate the local node is operating with PLCA disabled on a segment with PLCA enabled nodes.

Value	Description
0	PLCA BEACON symbols have not been detected from the network with PLCA disabled
1	PLCA BEACON symbols have been detected from the network with PLCA with disabled

Bit 1 – ESDERR End-of-Stream Delimiter Error

This bit indicates the reception of an End-of-Stream Delimiter Error (ESDERR) or End-of-Stream Jabber (ESDJAB) symbol.

Value	Description
0	ESD error has not been detected
1	ESD error has been detected

Bit 0 – DEC5B 5B Decode Error

This bit indicates the 5B decoder encountered an unknown or reserved 5B codeword that could not be decoded.

Value	Description
0	5B decoder error has not occurred
1	5B decode error has occurred

5.4.7. Status 1 Register - Rev D

Name: STS1 - Rev D
Address: 0x0018

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	SLPFAIL	TDD	LNKSTSC	SQI	PSTC	TXCOL	TXJAB	TSSI
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EMPCYC		HDDD	PLCADIAG	UNCRS	PLCASYM	ESDERR	DEC5B
Access	RC	RO	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit 15 – SLPFAIL Sleep Fail Status
This bit is set to indicate a failure to enter low-power sleep state.

Value	Description
0	Sleep mode has not failed.
1	Sleep mode failure detected.

Bit 14 – TDD Topology Discovery Done Status
This bit is set to indicate that Topology Discovery process has finished.

Value	Description
0	Topology Discovery has not completed.
1	Topology Discovery has completed.

Bit 13 – LNKSTSC Link Status Change
This bit is set to indicate that the Links Status has changed.

Value	Description
0	Link status has not changed.
1	Link status has changed.

Bit 12 – SQI Signal Quality Indication Status
This bit is set to indicate an SQI status change.

Value	Description
0	SQI status has not changed.
1	SQI status has changed.

Bit 11 – PSTC PLCA Status Changed
This bit is set to indicate that the PLCA Status (PST) bit has changed within the PLCA Status (PLCA_STS) register.

Value	Description
0	PLCA Status has not changed.
1	PLCA Status has changed.

Bit 10 – TXCOL Transmit Collision Status
Physical collision on the network was detected. This does not include logical collisions due to normal operation of PLCA.

Value	Description
0	No collision detected during transmit
1	Collision detected during transmit

Bit 9 – TXJAB Transmit Jabber Status

This bit indicates the occurrence of a transmit jabber condition. A jabber condition occurs when the PHY detects that the PCS has remained in the transmit state longer than 2 ms. When a jabber condition is detected, the transmitter is disabled for the duration of 16 ms.

Value	Description
0	No transmit jabber detected
1	Transmit jabber detected

Bit 8 – TSSI Time Synchronization Service Interface Status

This bit is set when the TSSI has indicated the transmission or reception of an Ethernet packet.

Value	Description
0	No transmitted or received frames indicated
1	A transmitted or received frame has been indicated

Bit 7 – EMPCYC PLCA Empty Cycle Status

This bit indicates the detection of an empty PLCA bus cycle. An empty bus cycle occurs when the node detects no transmissions in any of the possible transmit opportunities between two successive BEACONs.

Value	Description
0	An empty PLCA cycle has not been detected
1	An empty PLCA cycle has been detected

Bit 5 – HDDD Harness Defect Detection Done

This bit indicates that the harness defect detection process has finished.

Value	Description
0	Harness Defect Detection has not finished.
1	Harness Defect Detection is done.

Bit 4 – PLCADIAG PLCA Diagnostics Interrupt

This bit is triggered upon a PLCA diagnostic change.

Value	Description
0	No PLCA diagnostic interrupt is present.
1	PLCA diagnostic interrupt has occurred.

Bit 3 – UNCRS Unexpected Carrier Sense

When operating in ACMA mode, this bit will indicate carrier sense during this PHY's transmit slot when ACMA is asserted.

Value	Description
0	No Carrier has been sensed during PHY's ACMA time slot
1	Carrier has been sensed during PHY's ACMA time slot

Bit 2 – PLCASYM PLCA Symbols Detected

This bit indicates the detection of PLCA BEACON symbols when PLCA is not enabled. This condition may indicate the local node is operating with PLCA disabled on a segment with PLCA enabled nodes.

Value	Description
0	PLCA BEACON symbols have not been detected from the network with PLCA disabled

Value	Description
1	PLCA BEACON symbols have been detected from the network with PLCA with disabled

Bit 1 – ESDERR End-of-Stream Delimiter Error

This bit indicates the reception of an End-of-Stream Delimiter Error (ESDERR) or End-of-Stream Jabber (ESDJAB) symbol.

Value	Description
0	ESD error has not been detected
1	ESD error has been detected

Bit 0 – DEC5B 5B Decode Error

This bit indicates the 5B decoder encountered an unknown or reserved 5B codeword that could not be decoded.

Value	Description
0	5B decoder error has not occurred
1	5B decode error has occurred

5.4.8. Status 2 Register

Name: STS2
Address: 0x0019

Bit	15	14	13	12	11	10	9	8
					RESETC	WKEMDI	WKEWI	UV33
Access	RO	RO	RO	RO	RC	RC	RC	RC
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
		OT	IWDTO					
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit 11 – RESETC Reset Complete Status
This bit is asserted upon completion of a reset due to power-on, assertion of the RESET_N pin, or setting of the SW_RESET bit.

Value	Description
0	Reset has not occurred
1	Reset has occurred

Bit 10 – WKEMDI MDI Wake-up Status
This indicates wake-up from MDI energy.

Value	Description
0	Wake from MDI has not occurred
1	Wake from MDI has occurred

Bit 9 – WKEWI WAKE_IN Wake-up Status
This indicates wake-up from WAKE_IN pin.

Value	Description
0	Wake from WAKE_IN has not occurred
1	Wake from WAKE_IN has occurred

Bit 8 – UV33 3.3V supply Under-Voltage Status
Set when an under-voltage condition has been detected on the 3.3V supply.

Value	Description
0	3.3V supply under-voltage condition has not been detected
1	3.3V supply under-voltage condition has been detected

Bit 6 – OT Over-Temperature Error Status

Value	Description
0	No over-temperature error detected
1	Over-temperature error detected

Bit 5 – IWDTO Inactivity Watchdog Timeout Status
This bit is set to indicate a timeout of the inactivity watchdog has occurred.

Value	Description
0	Inactivity watchdog timer has not expired
1	Inactivity watchdog timer has expired

5.4.9. Status 2 Register - Rev D

Name: STS2 - Rev D
Address: 0x0019

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
					RESETC	WKEMDI	WKEWI	UV33
Access	RO	RO	RO	RO	RC	RC	RC	RC
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
		OT						
Access	RC	RC	RO	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit 11 – RESETC Reset Complete Status
This bit is asserted upon completion of a reset due to power-on, assertion of the RESET_N pin, or setting of the SW_RESET bit.

Value	Description
0	Reset has not occurred
1	Reset has occurred

Bit 10 – WKEMDI MDI Wake-up Status
This indicates wake-up from MDI energy.

Value	Description
0	Wake from MDI has not occurred
1	Wake from MDI has occurred

Bit 9 – WKEWI WAKE_IN Wake-up Status
This indicates wake-up from WAKE_IN pin.

Value	Description
0	Wake from WAKE_IN has not occurred
1	Wake from WAKE_IN has occurred

Bit 8 – UV33 3.3V supply Under-Voltage Status
Set when an under-voltage condition has been detected on the 3.3V supply.

Value	Description
0	3.3V supply under-voltage condition has not been detected
1	3.3V supply under-voltage condition has been detected

Bit 6 – OT Over-Temperature Error Status

Value	Description
0	No over-temperature error detected
1	Over-temperature error detected

5.4.10. Status 3 Register

Name: STS3
Address: 0x001A

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ERRTOID[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – ERRTOID[7:0] PLCA Error Transmit Opportunity ID
This field captures the local PLCA current transmit opportunity counter ID when any unmasked interrupt status bit in the Status 1 register is set.
Note: This field is only accurate if one unmasked interrupt status bit is set in the Status 1 register. If multiple interrupt status bits are set, then this field represents the transmit opportunity for only the most recent interrupt status bit.

5.4.11. Interrupt Mask 1 Register

Name: IMSK1
Address: 0x001C

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
				SQIM	PSTCM	TXCOLM	TXJABM	TSSIM
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	EMPCYCM	RXINTOM	UNEXPBM	BCNBFTOM	UNCRSM	PLCASYMM	ESDERRM	DEC5BM
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 12 – SQIM Signal Quality Indication Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Signal Quality Indication (SQI) status bit is set.

Value	Description
0	SQI status interrupt enabled.
1	SQI status interrupt disabled.

Bit 11 – PSTCM PLCA Status Changed Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Status Changed (PSTC) status bit is set.

Value	Description
0	PLCA status change interrupt enabled.
1	PLCA status change interrupt disabled.

Bit 10 – TXCOLM Transmit Collision Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Transmit Collision (TXCOL) status bit is set.

Value	Description
0	Transmit collision interrupt enabled
1	Transmit collision interrupt disabled

Bit 9 – TXJABM Transmit Jabber Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Transmit Jabber (TXJAB) status bit is set.

Value	Description
0	Transmit jabber interrupt enabled
1	Transmit jabber interrupt disabled

Bit 8 – TSSIM Time Synchronization Service Interface Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Time Synchronization Service Interface (TSSI) status bit is set.

Value	Description
0	TSSI interrupt enabled
1	TSSI interrupt disabled

Bit 7 – EMPCYCM PLCA Empty Cycle Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Empty Cycle (EMPCYC) status bit is set.

Value	Description
0	PLCA empty cycle interrupt enabled
1	PLCA empty cycle interrupt disabled

Bit 6 – RXINTOM Receive in Transmit Opportunity Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Receive in Transmit Opportunity (RXINTO) status bit is set.

Value	Description
0	Receive in transmit opportunity interrupt enabled
1	Receive in transmit opportunity interrupt disabled

Bit 5 – UNEXPBM Unexpected BEACON Received Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Unexpected BEACON Received (UNEXPB) status bit is set.

Value	Description
0	Unexpected BEACON received interrupt enabled
1	Unexpected BEACON received interrupt disabled

Bit 4 – BCNBFTOM BEACON Received Before Transmit Opportunity Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the BEACON Received Before Transmit Opportunity (BCNBFTO) status bit is set.

Value	Description
0	BEACON received before transmit opportunity interrupt enabled
1	BEACON received before transmit opportunity interrupt disabled

Bit 3 – UNCRSM Unexpected Carrier Sense Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Unexpected Carrier Sense (UNCRS) status bit is set.

Value	Description
0	Unexpected carrier sense interrupt enabled
1	Unexpected carrier sense interrupt disabled

Bit 2 – PLCASYMM PLCA Symbols Detected Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Symbols Detected (PLCASYM) status bit is set.

Value	Description
0	PLCA BEACON symbols detected interrupt enabled
1	PLCA BEACON symbols detected interrupt disabled

Bit 1 – ESDERRM End-of-Stream Delimiter Error Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the End-of-Stream Delimiter Error (ESDERR) status bit is set.

Value	Description
0	ESD error interrupt enabled
1	ESD error interrupt disabled

Bit 0 – DEC5BM 5B Decode Error Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the 5B Decoder Error (DEC5B) status is set.

Value	Description
0	5B decode error interrupt enabled
1	5B decode error interrupt disabled

5.4.12. Interrupt Mask 1 Register - Rev D

Name: IMSK1 - Rev D
Address: 0x001C

This register is only valid for devices of Revision D0 and later.

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	SLPFAILM	TDDM	LNKSTSC	SQIM	PSTCM	TXCOLM	TXJABM	TSSIM
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	EMPCYCM		HDDDM	PLCADIAGM	UNCRSM	PLCASYMM	ESDERRM	DEC5BM
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 15 – SLPFAILM Sleep Fail Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Sleep Fail (SLPFAIL) status bit is set.

Value	Description
0	Sleep Fail interrupt enabled
1	Sleep Fail interrupt disabled

Bit 14 – TDDM Topology Discovery Done Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Topology Discovery Done (TDD) status bit is set.

Value	Description
0	Topology Discovery Done interrupt enabled
1	Topology Discovery Done interrupt disabled

Bit 13 – LNKSTSC Link Status Changed Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Link Status Changes (LNKSTSC) status bit is set.

Value	Description
0	Link Status Changed interrupt enabled
1	Link Status Changed interrupt disabled

Bit 12 – SQIM Signal Quality Indication Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the Signal Quality Indication (SQI) status bit is set.

Value	Description
0	SQI status interrupt enabled.
1	SQI status interrupt disabled.

Bit 11 – PSTCM PLCA Status Changed Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Status Changed (PSTC) status bit is set.

Value	Description
0	PLCA status change interrupt enabled.
1	PLCA status change interrupt disabled.

Bit 10 – TXCOLM Transmit Collision Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Transmit Collision (TXCOL) status bit is set.

Value	Description
0	Transmit collision interrupt enabled
1	Transmit collision interrupt disabled

Bit 9 – TXJABM Transmit Jabber Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Transmit Jabber (TXJAB) status bit is set.

Value	Description
0	Transmit jabber interrupt enabled
1	Transmit jabber interrupt disabled

Bit 8 – TSSIM Time Synchronization Service Interface Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Time Synchronization Service Interface (TSSI) status bit is set.

Value	Description
0	TSSI interrupt enabled
1	TSSI interrupt disabled

Bit 7 – EMPCYCM PLCA Empty Cycle Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Empty Cycle (EMPCYC) status bit is set.

Value	Description
0	PLCA empty cycle interrupt enabled
1	PLCA empty cycle interrupt disabled

Bit 5 – HDDDM Harness Defect Detection Done Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Harness Defect Detection Done (HDDD) status bit is set.

Value	Description
0	Harness Defect Detection Done interrupt enabled
1	Harness Defect Detection Done interrupt disabled

Bit 4 – PLCADIAGM PLCA Diagnostics Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Diagnostics (PLCADIAG) status bit is set.

Value	Description
0	PLCA Diagnostics interrupt enabled
1	PLCA Diagnostics interrupt disabled

Bit 3 – UNCRSM Unexpected Carrier Sense Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Unexpected Carrier Sense (UNCRS) status bit is set.

Value	Description
0	Unexpected carrier sense interrupt enabled
1	Unexpected carrier sense interrupt disabled

Bit 2 – PLCASYMM PLCA Symbols Detected Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the PLCA Symbols Detected (PLCASYM) status bit is set.

Value	Description
0	PLCA BEACON symbols detected interrupt enabled
1	PLCA BEACON symbols detected interrupt disabled

Bit 1 – ESDERRM End-of-Stream Delimiter Error Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the End-of-Stream Delimiter Error (ESDERR) status bit is set.

Value	Description
0	ESD error interrupt enabled
1	ESD error interrupt disabled

Bit 0 – DEC5BM 5B Decode Error Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the 5B Decoder Error (DEC5B) status is set.

Value	Description
0	5B decode error interrupt enabled
1	5B decode error interrupt disabled

5.4.13. Interrupt Mask 2 Register

Name: IMSK2
Address: 0x001D

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
					RESETCM	WKEMDIM	WKEWIM	UV33M
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	1

Bit	7	6	5	4	3	2	1	0
		OTM	IWDTOM					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 11 – RESETCM Reset Complete Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the device reset has been completed.

Value	Description
0	Reset complete interrupt enabled
1	Reset complete interrupt disabled

Bit 10 – WKEMDIM MDI Wake-up Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the MDI Wake-up (WKEMDI) status bit is set.

Value	Description
0	MDI wake-up interrupt enabled
1	MDI wake-up interrupt disabled

Bit 9 – WKEWIM WAKE_IN Wake-up Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the WAKE_IN Wake-up (WKEWI) status bit is set.

Value	Description
0	WAKE_IN wake-up interrupt enabled
1	WAKE_IN wake-up interrupt disabled

Bit 8 – UV33M 3.3V supply Under-Voltage Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the 3.3V supply Under-Voltage (UV33) status bit is set.

Value	Description
0	3.3V supply under-voltage interrupt enabled
1	3.3V supply under-voltage interrupt disabled

Bit 6 – OTM Over-Temperature Error Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Over-Temperature Error (OT) status bit is set.

Value	Description
0	Over-temperature error interrupt enabled
1	Over-temperature error interrupt disabled

Bit 5 – IWDTOM Inactivity Watchdog Timeout Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Inactivity Watchdog Timeout (IWDTO) status bit is set.

Value	Description
0	Inactivity watchdog timeout interrupt enabled
1	Inactivity watchdog timeout interrupt disabled

5.4.14. Interrupt Mask 2 Register - Rev D

Name: IMSK2 - Rev D
Address: 0x001D

This register is only valid for devices of Revision D0 and later.

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
					RESETCM	WKEMDIM	WKEWIM	UV33M
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	0	0	1

Bit	7	6	5	4	3	2	1	0
		OTM						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 11 – RESETCM Reset Complete Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the device reset has been completed.

Value	Description
0	Reset complete interrupt enabled
1	Reset complete interrupt disabled

Bit 10 – WKEMDIM MDI Wake-up Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the MDI Wake-up (WKEMDI) status bit is set.

Value	Description
0	MDI wake-up interrupt enabled
1	MDI wake-up interrupt disabled

Bit 9 – WKEWIM WAKE_IN Wake-up Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the WAKE_IN Wake-up (WKEWI) status bit is set.

Value	Description
0	WAKE_IN wake-up interrupt enabled
1	WAKE_IN wake-up interrupt disabled

Bit 8 – UV33M 3.3V supply Under-Voltage Interrupt Mask
When clear, this bit will enable assertion of the IRQ_N pin when the 3.3V supply Under-Voltage (UV33) status bit is set.

Value	Description
0	3.3V supply under-voltage interrupt enabled
1	3.3V supply under-voltage interrupt disabled

Bit 6 – OTM Over-Temperature Error Interrupt Mask

When clear, this bit will enable assertion of the IRQ_N pin when the Over-Temperature Error (OT) status bit is set.

Value	Description
0	Over-temperature error interrupt enabled
1	Over-temperature error interrupt disabled

5.4.15. Counter Control Register

Name: CTRCTRL
Address: 0x0020

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							TOCTRE	BCNCTRE
Access	RO	RO	RO	RO	RO	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 1 – TOCTRE Transmit Opportunity Counter Enable
Enables and disables the PLCA transmit opportunity counter in the Transmit Opportunity Count (High) and Transmit Opportunity Count (Low) registers.

Value	Description
0	PLCA transmit opportunity counter is disabled
1	PLCA transmit opportunity counter is enabled

Bit 0 – BCNCTRE PLCA BEACON Counter Enable
Enables and disables the PLCA BEACON counter in BEACON Count (High) and BEACON Count (Low) registers.

Value	Description
0	PLCA BEACON counter is disabled
1	PLCA BEACON counter is enabled

5.4.16. Transmit Opportunity Count (High)

Name: TOCNTH
Address: 0x0024

Bit	15	14	13	12	11	10	9	8
	TOCNT[31:24]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOCNT[23:16]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TOCNT[31:16] Transmit Opportunity Count

This field maintains the upper 16 bits of the 32-bit count of the number of PLCA transmit opportunities the device may have utilized since the previous read.

Note: When this register is read, the contents of the 32-bit transmit opportunity counter will be latched into the high and low counter register pair. The high counter register will be updated prior to be driven to the station management entity host controller.

Note: The 32-bit counter will be reset when the contents are latched into the high and low counter register pair.

5.4.17. Transmit Opportunity Count (Low)

Name: TOCNTL
Address: 0x0025

Bit	15	14	13	12	11	10	9	8
	TOCNT[15:8]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TOCNT[15:0] Transmit Opportunity Count
This field maintains the lower 16 bits of the 32-bit count of the number of PLCA transmit opportunities the device may have utilized since the previous read.
Note: The contents of this register will be latched upon reading of the Transmit Opportunity Count (High) register.

5.4.18. BEACON Count (High)

Name: BCNCNTH
Address: 0x0026

Bit	15	14	13	12	11	10	9	8
	BCNCNT[31:24]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BCNCNT[23:16]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BCNCNT[31:16] Beacon Count

This field maintains the upper 16 bits of the 32-bit counter of PLCA beacons received or transmitted since the previous read.

Note: When this register is read, the contents of the 32-bit beacon counter will be latched into the high and low counter register pair. The high counter register will be updated prior to be driven to the station management entity host controller.

Note: The 32-bit beacon counter will be reset when the contents are latched into the high and low counter register pair.

5.4.19. BEACON Count (Low)

Name: BCNCNTL
Address: 0x0027

Bit	15	14	13	12	11	10	9	8
	BCNCNT[15:8]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BCNCNT[7:0]							
Access	RC	RC	RC	RC	RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BCNCNT[15:0] Beacon Count

This field maintains the lower 16 bits of the 32-bit counter of PLCA beacons received or transmitted since the previous read.

Note: The contents of this register will be latched upon reading of the BEACON Count (High) register.

5.4.20. PLCA Multiple ID 0 Register

Name: MULTID0
Address: 0x0030

Bit	15	14	13	12	11	10	9	8
	ID1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ID2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ID1[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

Bits 7:0 – ID2[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

5.4.21. PLCA Multiple ID 1 Register

Name: MULTID1
Address: 0x0031

Bit	15	14	13	12	11	10	9	8
	ID3[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ID4[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ID3[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

Bits 7:0 – ID4[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

5.4.22. PLCA Multiple ID 2 Register

Name: MULTID2
Address: 0x0032

Bit	15	14	13	12	11	10	9	8
	ID5[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ID6[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ID5[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

Bits 7:0 – ID6[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

5.4.23. PLCA Multiple ID 3 Register

Name: MULTID3
Address: 0x0033

Bit	15	14	13	12	11	10	9	8
	ID7[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ID8[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – ID7[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

Bits 7:0 – ID8[7:0]

When this field is neither 0x00 or 0xFF and PLCA is enabled, the node will transmit when its transmit opportunity counter equals the value in this field.

Value	Description
0x00, 0xFF	Value ignored
0x01-0xFE	Additional LocalID (transmit opportunity) assigned to node

5.4.24. PLCA Reconciliation Sublayer Control 1

Name: PRSCTL1
Address: 0x0035

Bit	15	14	13	12	11	10	9	8
						FBEN		
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	1	1	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 10 – FBEN Fallback Enable

By default this bit is set enabling the device to fall back to pure CSMA/CD operation when PLCA Beacons have not been received as specified in Clause 148. In some conditions, the user may wish to write this bit to '0' disabling this fallback to CSMA/CD and remaining in PLCA mode at the risk of the device not being able to transmit until PLCA Beacons are again received.

⚠ WARNING Clearing this bit and disabling the CSMA/CD fall back from PLCA will result in the device not transmitting packets onto the network when PLCA Beacons are not present. The controller should monitor the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register and the PLCA Status Changed (PSTC) bit in the Status 1 (STS1) register for indication of this condition and taking action appropriate for the application.

Value	Description
0	CSMA/CD fallback operation is disabled
1	Device will fall back to pure CSMA/CD operation when the PLCA Beacon coordinator disappears according to Clause 148. (default)

5.4.25. PLCA Reconciliation Sublayer Control 1 - Rev D

Name: PRSCTL1 - Rev D
Address: 0x0035

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
						FBEN		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	0	0	0	1	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 10 – FBEN Fallback Enable
By default this bit is set enabling the device to fall back to pure CSMA/CD operation when PLCA Beacons have not been received as specified in Clause 148. In some conditions, the user may wish to write this bit to '0' disabling this fallback to CSMA/CD and remaining in PLCA mode at the risk of the device not being able to transmit until PLCA Beacons are again received.

WARNING Clearing this bit and disabling the CSMA/CD fall back from PLCA will result in the device not transmitting packets onto the network when PLCA Beacons are not present. The controller should monitor the PLCA Status (PST) bit in the PLCA Status (PLCA_STS) register and the PLCA Status Changed (PSTC) bit in the Status 1 (STS1) register for indication of this condition and taking action appropriate for the application.

Value	Description
0	CSMA/CD fallback operation is disabled
1	Device will fall back to pure CSMA/CD operation when the PLCA Beacon coordinator disappears according to Clause 148. (default)

5.4.26. PLCA Reconciliation Sublayer Status

Name: PRSSTS
Address: 0x0036

Bit	15	14	13	12	11	10	9	8
	MAXID[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – MAXID[7:0] Maximum ID

This field contains the maximum PLCA transmit opportunity ID count in the previous PLCA bus cycle. By monitoring this field, the PLCA follower station applications may detect the number of transmit opportunities the PLCA coordinator allows between BEACONs.

5.4.27. Port Management 2

Name: PRTMGMT2
Address: 0x003D

Bit	15	14	13	12	11	10	9	8
			MIRXWDEN	PRIWDEN	MITXWDEN			
Access	RO	RO	R/W	R/W	R/W	RO	RO	RO
Reset	-	-	1	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 13 – MIRXWDEN Media Interface Receive Watchdog Enable
When set, packets received from the network and output through the MII/RMII/SC-MII will reset the inactivity watchdog timer.

Value	Description
0	Media interface receive inactivity watchdog disabled
1	Media interface receive watchdog enabled

Bit 12 – PRIWDEN PHY Register Inactivity Watchdog Enable
When set, SMI accesses by the station host controller will reset the inactivity watchdog timer.

Value	Description
0	PHY register access inactivity watchdog disabled
1	PHY register access inactivity watchdog enabled

Bit 11 – MITXWDEN Media Interface Transmit Watchdog Enable
When set, packets received from the MII/RMII/SC-MII and output on the network will reset the inactivity watchdog timer.

Value	Description
0	Media interface transmit inactivity watchdog disabled
1	Media interface transmit inactivity watchdog enabled

5.4.28. Port Management 2 - Rev D

Name: PRTMGMT2 - Rev D
Address: 0x003D

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	-	-	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

5.4.29. Inactivity Watchdog Timeout (High)

Name: IWDTOH
Address: 0x003E

Bit	15	14	13	12	11	10	9	8
	TIMEOUT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIMEOUT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	0	0	0

Bits 15:0 – TIMEOUT[31:16] Inactivity Watchdog Timeout
This field configures the upper 16 bits of the 32-bit MII/SC-MII/RMII/SMI inactivity watchdog timeout in increments of 200 ns.
Note: The default value of 0x00989680 results in a timeout of 2 seconds.

5.4.30. Inactivity Watchdog Timeout (High) - Rev D

Name: IWDTOH - Rev D
Address: 0x003E

This register is deprecated for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

5.4.31. Inactivity Watchdog Timeout (Low)

Name: IWDTOL
Address: 0x003F

Bit	15	14	13	12	11	10	9	8
	TIMEOUT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	0	1	1	0

Bit	7	6	5	4	3	2	1	0
	TIMEOUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bits 15:0 – TIMEOUT[15:0] Inactivity Watchdog Timeout
This field configures the lower 16 bits of the 32-bit MII/SC-MII/RMII/SMI inactivity watchdog timeout in increments of 200 ns.
Note: The default value of 0x00989680 results in a timeout of 2 seconds.

5.4.32. Inactivity Watchdog Timeout (Low) - Rev D

Name: IWDTOL - Rev D
Address: 0x003F

This register is deprecated for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

5.4.33. Transmit Match Control Register

Name: TXMCTL
Address: 0x0040

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXPMDET					MACTXTSE	TXME	
Access	RC	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – TXPMDET Transmit Packet Match Detected

Value	Description
0	A matching packet has not been transmitted
1	A matching packet has been transmitted

Bit 2 – MACTXTSE MAC Transmit Time Stamp Enable
When enabled, transmitted packets will be compared. When a match is detected, a logical collision will be asserted to the MAC delaying transmission until the next PLCA transmit opportunity.
Note: This bit cannot be enabled at the same time as the TXME bit.

Value	Description
0	Transmit MAC gPTP disabled. Normal operation.
1	Transmit MAC gPTP enabled. Matching transmit packets will delay transmission until the next PLCA transmit opportunity.

Bit 1 – TXME Transmit Match Enable
When enabled, transmit packets will be compared. When a match is detected, the TXPI pin will be asserted as configured.
Note: This bit cannot be enabled at the same time as the MACTXTSE bit.

Value	Description
0	Transmitted packets are not compared. Normal operation.
1	Transmitted packets will be compared and TXPI asserted on a match.

5.4.34. Transmit Match Pattern (High) Register

Name: TXMPATH
Address: 0x0041

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXMPAT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	0	0

Bits 7:0 – TXMPAT[23:16] Transmit Match Pattern (High)
Upper 8 bits of the 24-bit transmit match pattern.

5.4.35. Transmit Match Pattern (Low) Register

Name: TXMPATL
Address: 0x0042

Bit	15	14	13	12	11	10	9	8
	TXMPAT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	TXMPAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

Bits 15:0 – TXMPAT[15:0] Transmit Match Pattern (Low)
Lower 16 bits of the 24-bit transmit match pattern.

5.4.36. Transmit Matched Packet Delay Register

Name: TXMDLY
Address: 0x0049

Bit	15	14	13	12	11	10	9	8
	TXMDLYEN					TXMPKTDLY[10:8]		
Access	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TXMPKTDLY[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – TXMDLYEN Transmit Matched Packet Delay Measurement Enable
When set, this bit enables the measurement of matched transmit packet delays through the PHY.

Value	Description
0	Transmit packet delay measurement is disabled
1	Transmit packet delay measurement is enabled

Bits 10:0 – TXMPKTDLY[10:0] Transmit Matched Packet Delay
This field contains the delay of the previously matched transmit packet through the PHY. The delay is measured from the assertion of TXEN to the end of the transmission of the first SSD symbol ('H") of the packet preamble onto the line in units of 40 ns. When PLCA is enabled, the measured delay includes the delay of the packet through the PLCA elastic buffer.

Value	Description
0x000	0 ns
0x001	40 ns
...	...
0x7FF	81.880 µs

5.4.37. Receive Match Control Register

Name: RXMCTL
Address: 0x0050

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RXPMDET					RXME	
Access	R/W	RC	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 6 – RXPMDET Receive Packet Match Detected

Value	Description
0	A matching packet has not been received
1	A matching packet has been received

Bit 1 – RXME Receive Packet Match Enable

When enabled, receive packets will be compared. When a match is detected, RXPI pin will be asserted as configured.

Value	Description
0	Received packets are not compared. Normal operation.
1	Received packets will be compared and RXPI asserted on a match.

5.4.38. Receive Match Pattern (High) Register

Name: RXMPATH
Address: 0x0051

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RXMPAT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	0	0

Bits 7:0 – RXMPAT[23:16] Receive Match Pattern (High)
Upper 8 bits of the 24-bit receive match pattern.

5.4.39. Receive Match Pattern (Low) Register

Name: RXMPATL
Address: 0x0052

Bit	15	14	13	12	11	10	9	8
	RXMPAT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	RXMPAT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

Bits 15:0 – RXMPAT[15:0] Receive Match Pattern (Low)
Lower 16 bits of the 24-bit receive match pattern.

5.4.40. Receive Matched Packet Delay Register

Name: RXMDLY
Address: 0x0059

Bit	15	14	13	12	11	10	9	8
	RXMDLYEN					RXMPKTDLY[10:8]		
Access	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RXMPKTDLY[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – RXMDLYEN Receive Matched Packet Delay Measurement Enable
When set, this bit enables the measurement of matched receive packet delays through the PHY.

Value	Description
0	Receive packet delay measurement is disabled
1	Receive packet delay measurement is enabled

Bits 10:0 – RXMPKTDLY[10:0] Receive Matched Packet Delay
This field contains the delay of the previously matched receive packet through the PHY. The delay is measured from detection of the first SSD symbol ('H") of the packet preamble on the line to the assertion of Receive Data Valid at the media interface. The delay in this field is represented in units of 10 ns with an uncertainly of 10 ns.

Value	Description
0x000	0 ns
0x001	10 ns
0x010	20 ns
...	...
0x7FF	20.470 µs

5.4.41. Credit Based Shaper Stop Threshold (High) Register

Name: CBSSPTHH
Address: 0x0060

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					STOPTHR[19:16]			
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 3:0 – STOPTHR[19:16] Stop Threshold (High)
Upper 4 bits of the 20-bit credit stop threshold value. Once the credit counter drops below this threshold the device will assert CRS to hold off the MAC from transmitting.

5.4.42. Credit Based Shaper Stop Threshold (Low) Register

Name: CBSSPTHL
Address: 0x0061

Bit	15	14	13	12	11	10	9	8
	STOPTHR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	1	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	STOPTHR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	0	0

Bits 15:0 – STOPTHR[15:0] Stop Threshold (Low)
Lower 16 bits of the 20-bit credit stop threshold value. Once the credit counter drops below this threshold the device will assert CRS to hold off the MAC from transmitting.

5.4.43. Credit Based Shaper Start Threshold (High) Register

Name: CBSSTTHH
Address: 0x0062

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					STARTTHR[19:16]			
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 3:0 – STARTTHR[19:16] Start Threshold (High)
Upper 4 bits of the 20-bit credit start threshold value. Once the credit counter accumulates above this threshold the device will negate CRS to allow the MAC to transmit.

5.4.44. Credit Based Shaper Start Threshold (Low) Register

Name: CBSSTTHL
Address: 0x0063

Bit	15	14	13	12	11	10	9	8
	STARTTHR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	1	1	0	0	1	1

Bit	7	6	5	4	3	2	1	0
	STARTTHR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	1	0	0	0

Bits 15:0 – STARTTHR[15:0] Start Threshold (Low)
Lower 16 bits of the 20-bit credit start threshold value. Once the credit counter accumulates above this threshold the device will negate CRS to allow the MAC to transmit.

5.4.45. Credit Based Shaper Slope Control Register

Name: CBSSLPCTL
Address: 0x0064

Bit	15	14	13	12	11	10	9	8
	FALLSLP[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
	RISESLP[6:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	0

Bits 15:9 – FALLSLP[6:0] Falling Slope
Sets the rate at which credits are reduced when transmitting. Each time the PHY transmits the number of bytes configured by this parameter, the credit count will be decremented by one, until the bottom limit is reached.

Bits 8:1 – RISESLP[7:0] Rising Slope
Sets the rate at which credits are increased when receiving or idle. The PHY will count the number of received bytes or 800 ms periods of idle time. When the receive/idle byte count reaches the value in this parameter, the receive/idle byte count will be reset to 0 and the credit count will be incremented by one, until the top limit is reached.

5.4.46. Credit Based Shaper Top Limit (High) Register

Name: CBSTPLMTH
Address: 0x0065

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					TOPLIMIT[19:16]			
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 3:0 – TOPLIMIT[19:16] Credit Top Limit (High)
Upper 4 bits of the 20-bit credit top limit threshold value. The credit counter will saturate at this value once it has been incremented to this limit.

5.4.47. Credit Based Shaper Top Limit (Low) Register

Name: CBSTPLMTL
Address: 0x0066

Bit	15	14	13	12	11	10	9	8
	TOPLIMIT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
	TOPLIMIT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

Bits 15:0 – TOPLIMIT[15:0] Credit Top Limit (Low)
Lower 16 bits of the 20-bit credit top limit threshold value. The credit counter will saturate at this value once it has incremented to this limit.

5.4.48. Credit Based Shaper Bottom Limit (High) Register

Name: CBSBTLMTH
Address: 0x0067

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					BOTLIMIT[19:16]			
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 3:0 – BOTLIMIT[19:16] Credit Bottom Limit (High)
Upper 4 bits of the 20-bit credit bottom limit threshold value. The credit counter will saturate at this value once it has been decremented to this limit.

5.4.49. Credit Based Shaper Bottom Limit (Low) Register

Name: CBSBTLMTL
Address: 0x0068

Bit	15	14	13	12	11	10	9	8
	BOTLIMIT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BOTLIMIT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – BOTLIMIT[15:0] Credit Bottom Limit (Low)
Lower 16 bits of the 20-bit credit bottom limit threshold value. The credit counter will saturate at this value once it has been decremented to this limit.

5.4.50. Credit Based Shaper Credit Counter (High) Register

Name: CBSCRCTRH
Address: 0x0069

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					CREDITCTR[19:16]			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 3:0 – CREDITCTR[19:16] Credit Counter (High)
Upper 4 bits of the 20-bit credit counter.

5.4.51. Credit Based Shaper Credit Counter (Low) Register

Name: CBSCRCTRL
Address: 0x006A

Bit	15	14	13	12	11	10	9	8
	CREDITCTR[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CREDITCTR[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CREDITCTR[15:0] Credit Counter (Low)
Lower 16 bits of the 20-bit credit counter.

5.4.52. Credit Based Shaper Control Register

Name: CBSCTRL
Address: 0x006B

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
								ECCRDS[7]
Access	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
	ECCRDS[6:0]							CBSEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1	1	1	0	0

Bits 8:1 – ECCRDS[7:0] Empty Cycle Credits
Sets the number of additional credits added on detection of an empty PLCA bus cycle.

Bit 0 – CBSEN Credit Based Shaper Enable

Value	Description
0	Hardware credit based traffic shaping is disabled
1	Hardware credit based traffic shaping is enabled

5.4.53. PLCA Skip Control Register

Name: PLCASKPCTL
Address: 0x0070

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
							TOSKPEN	
Access	RO	RO	RO	RO	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 1 – TOSKPEN PLCA Transmit Opportunity Skip Enable
When enabled, the device will assert CRS for a number of its assigned PLCA transmit opportunities after transmitting a packet to delay the MAC from transmitting another packet. The number of transmit opportunities skipped before allowing the MAC to transmit is configured in the PLCA Cycle Skip register.

Value	Description
0	Transmit opportunity skipping is disabled.
1	Transmit opportunity skipping is enabled.

Related Links
PLCATOSKP
PLCA Transmit Opportunity Skip Register

5.4.54. PLCA Transmit Opportunity Skip Register

Name: PLCATOSKP
Address: 0x0071

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOSKPNUM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – TOSKPNUM[7:0] Transmit Opportunity Skip Number
Configures the number of assigned transmit opportunities to skip after transmitting a packet.

Related Links
PLCASKPCTL
PLCA Skip Control Register

5.4.55. Application Controlled Media Access Control Register

Name: ACMACTL
Address: 0x0074

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								ACMAEN
Access	RO	RO	RO	RO	RO	R/W	RC	R/W
Reset	0	0	0	0	0	0	0	0

Bit 0 – ACMAEN ACMA Enable
When enabled, the PHY will only allow the MAC to transmit a packet when the ACMA pin is asserted.

Value	Description
0	ACMA operation is disabled.
1	ACMA operation is enabled.

5.4.56. Sleep Control 0 Register

Name: SLPCTL0
Address: 0x0080

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	SLPEN	WKINEN	MDIWKEN	SLPINHDLY[1:0]				
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	1	1

Bit	7	6	5	4	3	2	1	0
		SLPCAL[3:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – SLPEN Sleep Enable
When set, the device stops driving the INH pin high, releasing it to high-impedance, and enters deep sleep mode. When released, if no other device is driving the INH electrical node, an external resistor will pull the node low disabling system switched power supplies.

Value	Description
0	Normal operation
1	Sleep

Bit 14 – WKINEN WAKE_IN Wake-up Enable
When set, enables wake-up from sleep mode upon detection of a pulse on the WAKE_IN pin.

Value	Description
0	Disable wake-up by input pulse on WAKE_IN
1	Enable wake-up by input pulse on WAKE_IN

Bit 13 – MDIWKEN MDI Wake-up Enable
When set, enables wake-up from sleep mode upon detection of activity at the MDI.

Value	Description
0	Disable wake-up from MDI activity detection
1	Enable wake-up from MDI activity detection

Bits 12:11 – SLPINHDLY[1:0] Sleep Inhibit Delay
This field configures the delay from when sleep is first commanded to when the power supply Inhibit (INH) pin becomes high-impedance and the sleep state is entered. This delay is used to allow all nodes on a mixing segment time to go quiet before powering down.

Value	Description
00	0 ms delay
01	50 ms delay
10	100 ms delay
11	200 ms delay

Bits 6:3 – SLPCAL[3:0] Sleep Calibration

Factory use only. Must always be written as 0000.

Value	Description
0000	Only valid value for write
Others	Invalid on write. Ignore on read.

5.4.57. Sleep Control 0 Register - Rev D

Name: SLPCTL0 - Rev D
Address: 0x0080

This register is only valid for devices of Revision D0 and later.

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	WKINEN	MDIWKEN	SLPINHDLY[1:0]					
Access	R/W	R/W	R/W	R/W	RO	RO	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	0	0	0	0

Bit 15 – WKINEN WAKE_IN Wake-up Enable
When set, enables wake-up from sleep mode upon detection of a pulse on the WAKE_IN/WAKE_IO pin.

Value	Description
0	Disable wake-up by input pulse on WAKE_IN/WAKE_IO
1	Enable wake-up by input pulse on WAKE_IN/WAKE_IO

Bit 14 – MDIWKEN MDI Wake-up Enable
When set, enables wake-up from sleep mode upon detection of Wake-Up Tone (WUT) at the MDI.

Value	Description
0	Disable wake-up from MDI Wake-Up Tone detection
1	Enable wake-up from MDI Wake-Up Tone detection

Bits 13:12 – SLPINHDLY[1:0] Sleep Inhibit Delay
This field configures the delay from when sleep is first commanded to when the power supply Inhibit (INH) pin becomes high-impedance and the sleep state is entered. This delay is used to allow all nodes on a mixing segment time to go quiet before powering down.

Value	Description
00	0 ms delay
01	5.2 ms delay
10	10.4 ms delay
11	55.7 ms delay

5.4.58. Sleep Control 1 Register

Name: SLPCTL1
Address: 0x0081

> **Important:** When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WOPOL		WIPOL			MWKFWD	WKOFWDEN	MDIFWDEN
Access	R/W	R/W	R/W	RO	R/W	R/W SC	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – WOPOL WAKE_OUT Polarity
This bit configures the polarity of the 90 µs output wake pulse generated on the WAKE_OUT pin.
Note: Only wake from HIGH pulses on WAKE_OUT is supported.

> **Restriction:** While this bit defaults to '0', it must always be written to '1' when writing to other bits in this register.

Value	Description
0	Reserved
1	Device will output an active HIGH pulse on the WAKE_OUT pin.

Bit 5 – WIPOL WAKE_IN Polarity
This bit configures the polarity of the pulse on the WAKE_IN pin that will wake the device from sleep.

Value	Description
0	Device will wake from an active LOW pulse on WAKE_IN pin.
1	Device will wake from an active HIGH pulse on WAKE_IN pin.

Bit 2 – MWKFWD Manual Wake Forward
When set, this bit will trigger a wake forwarding event. The device will generate a wake-up pulse on WAKE_OUT if forwarding of wake events to WAKE_OUT is enabled by WAKE_OUT Forward Enable (WKOFWDEN) bit. Wake activity signaling will be generated to the MDI if forwarding of wake events to MDI is enabled by MDI Wake Forward Enable (MDIFWDEN) bit.
Note: This bit is self-cleared by hardware once the wake output events have completed.

Value	Description
0	No wake out signaling (normal operation)
1	Generate wake out signaling to WAKE_OUT and/or MDI

Bit 1 – WKOFWDEN WAKE_OUT Forward Enable
Enable the generation of a WAKE_OUT pulse when a wake indication is detected by MDI activity or assertion of the WAKE_IN pin.

Value	Description
0	Disable generation of a pulse on WAKE_OUT on wake-up
1	Enable generation of a pulse on WAKE_OUT on wake-up

Bit 0 – MDIFWDEN MDI Forward Enable

This bit will enable the generation of activity signaling on the MDI when a wake indication is detected by the assertion of the WAKE_IN pin.

Value	Description
0	Disable generation MDI wake signaling upon wake-up from WAKE_IN
1	Enable generation MDI wake signaling upon wake-up from WAKE_IN

5.4.59. Sleep Control 1 Register - Rev D

Name: SLPCTL1 - Rev D
Address: 0x0081

This register is only valid for devices of Revision D0 and later.

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	WIOEN							
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	R/W
Reset	0	1	0	1	0	0	1	0

Bit	7	6	5	4	3	2	1	0
			WIPOL			WKOREQ	WKOFWDEN	MDIFWDEN
Access	R/W	R/W	R/W	RO	RO	R/W SC	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 15 – WIOEN WAKE_IO Enable
When set, this bit configures the WAKE_IN pin to be combined with the WAKE_OUT as WAKE_IO. The WAKE_OUT pin is not used in this mode.

Value	Description
0	WAKE_IN and WAKE_OUT are separate pins.
1	WAKE_IO is enabled as a combined WAKE_IN and WAKE_OUT. The WAKE_OUT pin is not used.

Bit 5 – WIPOL WAKE_IN Polarity
This bit configures the polarity of the pulse on the WAKE_IN pin that will wake the device from sleep. While WAKE_IO is active, this bit configures the wake input and wake output mode.

Value	Description
0	Device will wake from an active LOW pulse on WAKE_IN pin. WAKE_IO will trigger upon active LOW pulse, will output an active LOW wake output.
1	Device will wake from an active HIGH pulse on WAKE_IN pin. WAKE_IO will trigger upon active HIGH pulse, will output an active HIGH wake output.

Bit 2 – WKOREQ WAKE_OUT Request
Writing a '1' to this bit will cause the device will generate a wake-up pulse on WAKE_OUT, or, when enabled, WAKE_IO pin.
Note: This bit is self clearing.

Value	Description
0	No wake-up pulse signaling (normal operation)
1	Generate a wake-up pulse on WAKE_OUT/WAKE_IO

Bit 1 – WKOFWDEN Wake Forward Enable
Enable the generation of a WAKE_OUT pulse when a wake indication is detected by MDI activity or assertion of the WAKE_IN pin.

Value	Description
0	Disable generation of a pulse on WAKE_OUT on wake-up

Value	Description
1	Enable generation of a pulse on WAKE_OUT on wake-up

Bit 0 – MDIFWDEN MDI Forward Enable

This bit will enable the generation of activity signaling on the MDI when a wake indication is detected by the assertion of the WAKE_IN pin.

Value	Description
0	Disable generation MDI wake signaling upon wake-up from WAKE_IN
1	Enable generation MDI wake signaling upon wake-up from WAKE_IN

5.4.60. Collision Detector Control 0 Register

Name: CDCTL0
Address: 0x0087

Bit	15	14	13	12	11	10	9	8
	CDEN							
Access	R/W	R/W	R/W	R/W	RO	RO	RO	R/W
Reset	1	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	1	1

Bit 15 – CDEN Collision Detect Enable
When set, this bit enables the detection of collisions on the physical medium when transmitting.

Tip: No physical collisions will occur when all nodes in a mixing segment are properly configured for PLCA operation. As a result, for improved performance in high noise environments where false collisions may be detected leading to dropped packets, it is recommended that the user write this bit to a '0' to disable collision detection when PLCA is enabled. When collision detection is disabled, the PLCA reconciliation sublayer will still assert *logical collisions* to the MAC as part of normal operation.

Important: When writing to this bit, use a read-modify-write operation to avoid accidental modifications to RESERVED fields.

Value	Description
0	Collision detection is disabled
1	Collision detection is enabled (default)

5.4.61. Collision Detector Control 0 Register - Rev D

Name: CDCTL0 - Rev D
Address: 0x0087

This register is only valid for devices of Revision D0 and later.

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	CDEN					CCMFC[1:0]		
Access	R/W	R/W	R/W	R/W	RO	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	1	1

Bit 15 – CDEN Collision Detect Enable
When set, this bit enables the detection of collisions on the physical medium when transmitting.

Value	Description
0	Collision detection is disabled
1	Collision detection is enabled (default)

Bits 10:9 – CCMFC[1:0] Collision Counting and MAC Forwarding Control
When CDEN is '0' this field configures how detected collisions are counted within the device and forwarded to the MAC through the MII or RMII.
This field has **no effect** when CDEN is '0' as collision detection is disabled.

Value	Description
00	IEEE default: Collisions counted and forwarded to the MAC
x1	OA default: Collisions counted and forwarded to the MAC when PLCA_Status ≠ OK Collisions neither counted nor forwarded to the MAC when PLCA_Status = OK
10	Collisions counted and forwarded to the MAC when PLCA_Status ≠ OK Collisions counted but *not* forwarded to the MAC when PLCA_Status = OK

5.4.62. SQI Control Register

Name: SQICTL
Address: 0x00A0

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	SQIRST	SQIEN						
Access	R/W SC	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	1	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – SQIRST SQI Reset
Setting this bit will reset the SQI block. This bit is self-clearing.

Value	Description
0	Normal Operation
1	SQI block is reset

Bit 14 – SQIEN SQI Enable
This bit enables the SQI measurement process when set.

Value	Description
0	SQI is disabled
1	SQI is enabled

5.4.63. SQI Control Register - Rev D

Name: SQICTL - Rev D
Address: 0x00A0

This register is deprecated for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	R/W	RO	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	1	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

5.4.64. SQI Status 0 Register

Name: SQISTS0
Address: 0x00A1

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SQIERR	SQIVLD	SQIVAL[2:0]			SQIERRC[2:0]		
Access	RO	RC	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 7 – SQIERR SQI ERR
This bit will be set when an error has occurred during the SQI statistic accumulation period.

Value	Description
0	No error detected during SQI measurement
1	Error has been detected during SQI measurement

Bit 6 – SQIVLD SQI Valid
This bit is set when the SQI measurement is valid and may be read from SQIVAL.

Value	Description
0	SQI estimation is not complete or valid
1	SQI estimation is complete and valid

Bits 5:3 – SQIVAL[2:0] SQI Value
This field contains the measured SQI Value.

Value	Description
000	SNR ≤ ~5 dB (Worst SQI) BER ≥ ~3.8E-02
001	~5 dB ≤ SNR ≤ ~10 dB ~3.8E-02 ≥ BER ≥ ~7.8E-4
010	~10 dB ≤ SNR ≤ ~12 dB ~7.8E-4 ≥ BER ≥ ~3.4E-5
011	~12 dB ≤ SNR ≤ ~14 dB ~3.4E-5 ≥ BER ≥ ~2.7E-7
100	~14 dB ≤ SNR ≤ ~16 dB ~2.7E-7 ≥ BER ≥ ~1.4E-10
101	~16 dB ≤ SNR ≤ ~17 dB ~1.4E-10 ≥ BER ≥ ~7.2E-13
110	~17 dB ≤ SNR ≤ ~18 dB ~7.2E-13 ≥ BER ≥ ~9.9E-16
111	SNR ≥ ~18 dB (Best SQI) BER ≤ ~9.9E-16

Bits 2:0 – SQIERRC[2:0] SQI Error Code
This field returns the SQI Error code when the SQIERR bit is set indicating an error condition occurred during the SQI statistic accumulation period.

Value	Description
000	No error / events
001	Low threshold > Maximum limitation
010	High threshold > Maximum limitation
011	Low threshold < Minimum limitation
100	High threshold < Minimum limitation
101	Low threshold > High threshold
Others	Undefined

5.4.65. SQI Status 0 Register - Rev D

Name: SQISTS0 - Rev D
Address: 0x00A1

This register is deprecated for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

5.4.66. SQI Configuration 0 Register

Name: SQICFG0
Address: 0x00AA

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
					TOID[7:4]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOID[3:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

Bits 11:4 – TOID[7:0] Transmit Opportunity ID
This field configures the PLCA transmit opportunity ID for which to measure the SQI. This is used to measure the SQI for a specific node on a PLCA enabled segment. A value of 0xFF will result in the SQI being measured over packets received from all nodes.

5.4.67. SQI Configuration 0 Register - Rev D

Name: SQICFG0 - Rev D
Address: 0x00AA

This register is deprecated for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

5.4.68. SQI Configuration 2 Register

Name: SQICFG2
Address: 0x00AC

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
				SQIINTTHR[4:0]				
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 12:8 – SQIINTTHR[4:0] SQI Interrupt Threshold

This field configures the upper threshold for asserting a SQI interrupt. When set to 0x1F, the SQI interrupt is disabled.

When set to a value other than 0x1F, The SQI interrupt will be triggered at any time the computed SQI Value (SQIVAL) is less than or equal to the configured threshold. This may be used to trigger an interrupt at any time the SQI of a specific PLCA node falls below a desired level.

Value	Description
x1F	SQI threshold interrupt disabled
1	SQI threshold interrupt when SQIVAL ≤ 1
2	SQI threshold interrupt when SQIVAL ≤ 2
3	SQI threshold interrupt when SQIVAL ≤ 3
4	SQI threshold interrupt when SQIVAL ≤ 4
5	SQI threshold interrupt when SQIVAL ≤ 5
6	SQI threshold interrupt when SQIVAL ≤ 6
7	SQI threshold interrupt when SQIVAL ≤ 7
others	Invalid

5.4.69. SQI Configuration 2 Register - Rev D

Name: SQICFG2 - Rev D
Address: 0x00AC

This register is deprecated for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

5.4.70. Pad Control 3 Register

Name: PADCTRL3
Address: 0x00CB

Important: When writing to this register, use a read-modify-write operation to avoid accidental modifications to RESERVED fields. Failure to use a read-modify-write operation may result in adverse operation and unexpected results.

Bit	15	14	13	12	11	10	9	8
	PDRV4[1:0]		PDRV3[1:0]		PDRV2[1:0]		PDRV1[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
Access	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	1

Bits 15:14 – PDRV4[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 4.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

Bits 13:12 – PDRV3[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 3.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

Bits 11:10 – PDRV2[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 2.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive
11	High current drive (default)

Bits 9:8 – PDRV1[1:0] Digital Output Pad Drive Strength
This field configures the output pad drive strength for pin group 1.

Value	Description
00	Low current drive
01	Medium-low current drive
10	Medium-high current drive

Value	Description
11	High current drive (default)

Related Links

Output Drive Strength Control

5.4.71. Analog Control 5

Name: ANALOG5
Address: 0x00D5

Bit	15	14	13	12	11	10	9	8
	UV33FTM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	1	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – UV33FTM[7:0] Voltage Ready Time

This field configures the 3.3V VDDA and VDDAU supply under-voltage filter in increments of 10 µs. The voltage must fall below the under-voltage threshold for longer than the time configured in this field before the 3.3V under-voltage condition will be triggered.

Value	Description
00h	0 µs
01h	10 µs
02h	20 µs
...	...
14h	200 µs (default)
...	...
FFh	2.55 ms

5.4.72. OPEN Alliance Map ID and Version Register

Name: MIDVER
Address: 0xCA00

Bit	15	14	13	12	11	10	9	8
	IDM[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
	VER[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	0	0	0	0

Bits 15:8 – IDM[7:0] Register Map ID
This field uniquely identifies the OPEN Alliance address space for register mapping.

Value	Description
0x0A	OPEN Alliance register map

Bits 7:0 – VER[7:0] Register Map Version
This field specifies the register map version. The version number is represented in binary-coded-decimal.

Tip: This device conforms to the OPEN Alliance *10BASE-T1S PLCA Management Registers Specification*, version 1.1 although this field indicates conformity to version 1.0. The only difference between the two specifications is the default value of the Transmit Opportunity Timer (TOTMR) bit field. Version 1.0 of the register map specifies a default TOTMR value of 24 whereas this device implements a default TOTMR value of 32 conforming to Clause 30 of the *IEEE Std 802.3* specification. This discontinuity was resolved with *10BASE-T1S PLCA Management Registers Specification*, version 1.1.

Value	Description
0x10	OPEN Alliance register map version 1.0

5.4.73. OPEN Alliance Map ID and Version Register - Rev D

Name: MIDVER - Rev D
Address: 0xCA00

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	IDM[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
	VER[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	1	0	0	1	0

Bits 15:8 – IDM[7:0] Register Map ID
This field uniquely identifies the OPEN Alliance address space for register mapping.

Value	Description
0x0A	OPEN Alliance register map

Bits 7:0 – VER[7:0] Register Map Version
This field specifies the register map version. The version number is represented in binary-coded-decimal.

Tip: This device conforms to the OPEN Alliance *10BASE-T1S PLCA Management Registers Specification*, version 1.2.

Value	Description
0x12	OPEN Alliance register map version 1.2

5.4.74. PLCA Control 0 Register

Name: PLCA_CTRL0
Address: 0xCA01

Bit	15	14	13	12	11	10	9	8
	EN	RST						
Access	R/W	R/W SC	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – EN PLCA Enable

Setting this bit will enable Physical Layer Collision Avoidance. When this bit is clear, the PHY will operate in pure CSMA/CD mode.

Note: When PLCA is enabled on a properly configured mixing segment, no collisions should occur on the physical layer. It is therefore recommended to disable physical layer collision detection to achieve a higher level of noise tolerance.

Value	Description
0	The PLCA reconciliation sublayer is disabled and the PHY operates in normal CSMA/CD mode without the performance enhancements of PLCA.
1	The Physical Layer Collision Avoidance (PLCA) reconciliation sublayer functionality is enabled.

Bit 14 – RST PLCA Reset

Writing '1' to this bit will result in a reset of the PLCA reconciliation sublayer.

Note: This bit is self-clearing. When setting this bit, do not set other bits in this register.

Value	Description
0	Normal operation
1	PLCA reconciliation sublayer is reset

5.4.75. PLCA Control 1 Register

Name: PLCA_CTRL1
Address: 0xCA02

Bit	15	14	13	12	11	10	9	8
	NCNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	0	0	0

Bit	7	6	5	4	3	2	1	0
	ID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 15:8 – NCNT[7:0] Node Count

This field configures the maximum number of nodes supported on the multidrop network. Proper operation requires that this field be set to at least the number of nodes that may exist on the network. The number of transmit opportunities in a given PLCA cycle.
Valid range: 0x01-0xFF
Note: This field must be configured correctly on the node with ID=0 (Controller). Nodes configured with ID other than zero (Followers) ignore this field.

Bits 7:0 – ID[7:0] PLCA Local ID

This field configures the node's PLCA Local ID and the transmit opportunity within the PLCA cycle which it will transmit. A value of zero configures the node as the PLCA coordinator responsible for the periodic transmission of the PLCA BEACON and the number of transmit opportunities available per PLCA bus cycle. When set to 0xFF, the PLCA operation will be disabled and the node will revert to CSMA/CD.
Up to eight additional transmit opportunities may be configured in the PLCA Multiple ID 0-3 (MULTID0-MULTID3) registers.
Note: This parameter shall be configured unique across the multidrop network to ensure proper collision-free operation.

Value	Description
0	PLCA Coordinator node Local ID
1-0xFE	PLCA Follower node Local ID
0xFF	PLCA Disabled

Related Links

MULTID0
PLCA Multiple ID 0 Register
MULTID1
PLCA Multiple ID 1 Register
MULTID2
PLCA Multiple ID 2 Register
MULTID3
PLCA Multiple ID 3 Register

5.4.76. PLCA Status Register

Name: PLCA_STS
Address: 0xCA03

Bit	15	14	13	12	11	10	9	8
	PST							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – PST PLCA Status

This field indicates that the PLCA reconciliation sublayer is active and a BEACON is being regularly transmitted or received.

Value	Description
0	The PLCA reconciliation sublayer is not regularly receiving or transmitting the BEACON
1	The PLCA reconciliation sublayer is regularly receiving or transmitting the BEACON

5.4.77. PLCA Transmit Opportunity Timer Register

Name: PLCA_TOTMR
Address: 0xCA04

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOTMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bits 7:0 – TOTMR[7:0] PLCA Transmit Opportunity Timer
Configures the PLCA Transmit Opportunity time allowed for each node to begin transmitting and capture the carrier sense for all nodes on the network. The time is represented in increments of 100 ns (i.e., 1 BT). This field defaults to 32 bit times (3.2 µs) according to the *IEEE Std 802.3-2022* specification (Clause 30.16.1.1.5), and the OPEN Alliance *10BASE-T1S PLCA Management Registers Specification*, Version 1.2.

Important: This field must be configured identically across all nodes on the multidrop mixing segment.

CAUTION Improper configuration of Transmit Opportunity timer may result in reduced network performance or collisions. Determination of the optimal Transmit Opportunity time requires knowledge of various delays of each of the vendor PHYs on the mixing segment and various physical layer propagation delay. It is recommended to leave this field at its default value unless a full evaluation of delays has been performed.

Note: Due to discrepancies in the default value for this register between Version 1.0 of the OPEN Alliance *10BASE-T1S PLCA Management Registers Specification* for this field and Clause 30.16.1.1.5 of the *IEEE Std 802.3-2022* specification, it is recommended that this field always be configured to the desired value for all Microchip and non-Microchip devices on the network.

5.4.78. PLCA Burst Mode Register

Name: PLCA_BURST
Address: 0xCA05

Bit	15	14	13	12	11	10	9	8
	MAXBC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BTMR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bits 15:8 – MAXBC[7:0] Maximum Burst Count

This field configures the maximum number of additional frames that the node may transmit in a single transmit opportunity. When set to 0, the PLCA burst mode is disabled and only one frame will be transmitted per transmit opportunity.

Value	Description
0	Burst mode disabled. Only one frame will be transmitted per Transmit Opportunity.
1-0xFF	Number of additional frames that may be transmitted in a burst.

Bits 7:0 – BTMR[7:0] Burst Timer

When burst mode is enabled, this field configures the amount of time allowed following the transmission of a frame which the node will continue to transmit and hold the multidrop network waiting for the MAC to transmit an additional frame. Should the timer expire before the MAC transmits an additional frame, or if the maximum number of frames allowed to be transmitted in a single burst has been exceeded, the node will stop transmitting and yield the network to the next transmit opportunity.

The time is represented in increments of 100 ns (i.e., 1 BT).

Note: The minimum value should be equal to the MAC inter-frame gap (IFG) plus margin for the latency between the MAC and PHY.

5.4.79. PLCA Diagnostics Register - Rev D

Name: PLCA_DIAG - Rev D
Address: 0xCA06

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						RXINTO	UNEXPB	BCNBFTO
Access	RO	RO	RO	RO	RO	R/W1C	R/W1C	R/W1C
Reset	0	0	0	0	0	0	0	0

Bit 2 – RXINTO Receive in Transmit Opportunity
This bit indicates the detection of another node transmitting in this node's local assigned transmit opportunity. This could indicate multiple nodes being assigned the same Local ID.

Value	Description
0	Another node has not been detected transmitting in this node's TO
1	Another node has been detected transmitting in this node's TO

Bit 1 – UNEXPB Unexpected Beacon received
When configured as the PLCA coordinator in charge of transmitting the periodic coordinating BEACONs, this bit indicates the detection of an unexpected BEACON on the segment. This condition may be due to the configuration of multiple PLCA coordinators on the segment.

Value	Description
0	Another node on the segment has not been detected transmitting a BEACON
1	Another node on the segment has been detected transmitting a BEACON

Bit 0 – BCNBFTO Beacon received Before Transmit Opportunity
This bit indicates the detection of a BEACON before the node's assigned transmit opportunity. This condition could indicate the configuration of multiple PLCA coordinators on the segment. Other conditions that may cause this to occur include a PLCA coordinator with an incorrectly configured maximum node count resulting in a PLCA cycle that is too short, or a PLCA Local ID that is configured beyond the PLCA cycle.

Value	Description
0	A BEACON has not been detected before local transmit opportunity
1	A BEACON was detected before local transmit opportunity

5.4.80. Advanced Diagnostic Features Capability - Rev D

Name: ADFCAP - Rev D
Address: 0xCC00

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
						HDD[2:0]		
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	1	0

Bit	7	6	5	4	3	2	1	0
				SQIP[3:0]				SQI
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	1	0	1	1

Bits 10:8 – HDD[2:0] Harness Defect Detection Capability
The PHY supports Class 2 harness defect detection.

Value	Description
000	HDD not supported
001	HDD Class 1 is supported
010	HDD Class 2 is supported
011	HDD Class 3 is supported
100	HDD Class 4 is supported
others	Reserved

Bits 4:1 – SQIP[3:0] SQI+ Capability
The PHY supports SQI+ with 32 levels (5 bits).

Value	Description
0000	SQI+ not supported
0001	Reserved
0010	Reserved
0011	SQI+ supported using 8 levels (3 bits)
0100	SQI+ supported using 16 levels (4 bits)
0101	SQI+ supported using 32 levels (5 bits)
0110	SQI+ supported using 64 levels (6 bits)
0111	SQI+ supported using 128 levels (7 bits)
1000	SQI+ supported using 256 levels (8 bits)
others	Reserved

Bit 0 – SQI SQI Capability
The PHY supports SQI with 8 levels (3 bits).

Value	Description
0	SQI not supported
1	SQI supported using 8 levels (3 bits)

5.4.81. Harness Defect Detection - Rev D

Name: HDD - Rev D
Address: 0xCC01

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	HDDREQ	HDDRDY	START					
Access	R/W	RO	R/W SC	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						VALID	SHTOPNSTS[1:0]	
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – HDDREQ HDD Request
Setting this bit requests the PMA to enter the HDD diagnostic mode. When the PMA has successfully entered the HDD diagnostic mode, the HDDRDY bit will be set. Similarly, writing a '0' to this bit will return the PMA to normal operation and will be verified by the HDDRDY returning '0'.

Value	Description
0	PMA in normal mode - HDD not requested
1	Request PMA to enter the HDD diagnostic mode

Bit 14 – HDDRDY HDD Ready
When this bit is set it indicates that the PMA is in the HDD diagnostic mode. When clear, the PMA is in normal mode. This bit is used to feed back the current state of the PMA as controlled by the HDDREQ bit.

Value	Description
0	PMA in normal mode - HDD is not ready
1	PMA is in HDD diagnostic mode - HDD is ready

Bit 13 – START Start HDD measurement
Writing a '1' to this bit will start the HDD measurement process. Once set, it will automatically be cleared to '0' once the process has completed. Upon completion, if there is no error, the VALID bit will be set.

Value	Description
0	HDD measurement not in progress
1	HDD measurement in progress

Bit 2 – VALID Valid HDD Measurement Results
When this bit is set, the value in the SHTOPNSTS field is valid and may be read. This bit is cleared when the measurement process is started by setting the START bit.

Value	Description
0	Measurement not valid
1	Measurement results are valid

Bits 1:0 – SHTOPNSTS[1:0] Short Open State
This field returns the open/short state of the cable harness.

Value	Description
00	No fault detected

Value	Description
01	Fault detected - Open or missing termination(s)
10	Fault detected - Short or extra termination(s)
11	Fault detected - type undetermined

5.4.82. Dynamic Channel Quality Transmit Opportunity ID Register - Rev D

Name: DCQ_TOID - Rev D
Address: 0xCC02

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TOID[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 7:0 – TOID[7:0] Transmit Opportunity ID
Transmit Opportunity for which the SQI or SQI+ is calculated. A new DCQ SQI/SQI+ measurement will be initiated when a new value is written into this field.

5.4.83. Signal Quality Index Register - Rev D

Name: DCQ_SQI - Rev D
Address: 0xCC03

This register contains the 8-level DCQ SQI status and result. It is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	SQI_UPD							
Access	RC	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						SQI[2:0]		
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – SQI_UPD Signal Quality Index Update
This bit indicates whether the eight-level DCQ SQI has been updated since the last read.
Note: Reading of this status bit when set results in the device automatically clearing it. This action **will** trigger a new DCQ SQI/SQI+ measurement. A new measurement may also be triggered by writing a new value into the TOID field of the DCQ_TOID register.

Value	Description
0	SQI has not been updated since last read
1	SQI has been updated since last read

Bits 2:0 – SQI[2:0] Signal Quality Index
When the SQI_UPD bit is set, this field contains the current eight-level SQI result. This field is equivalent to the most-significant three bits of the SQIP field of the DCQ_SQIP register.

5.4.84. Signal Quality Index Plus Register - Rev D

Name: DCQ_SQIP - Rev D
Address: 0xCC04

This register contains the 32-level DCQ SQI+ status and result. It is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	SQIP_UDP							
Access	RC	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SQIP[7:3]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	1	1	1

Bit 15 – SQIP_UDP DCQ Advanced SQI Update

This bit indicates whether the advanced 32-level SQI+ has been updated since the last read.
Note: Reading of this status bit when set results in the device automatically clearing it. This does **not**, however, trigger a new DCQ SQI/SQI+ measurement. A new measurement is triggered when the SQI_UPD bit is automatically cleared by reading the DCQ_SQI register or by writing a new value to the TOID field of the DCQ_TOID register.

Value	Description
0	SQI+ has not been updated since last read
1	SQI+ has been updated since last read

Bits 7:3 – SQIP[7:3] DCQ Advanced SQI Result

When the SQIP_UDP bit is set, this field contains the current 32-level SQI+ result.

5.4.85. Topology Discovery Control Register - Rev D

Name: TDCTL - Rev D
Address: 0xCE00

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	TDEN	REFN	INTDLYSTRT	DISTMESDUR[3:0]				DISTMESSTR
Access	R/W	R/W	R/W SC	R/W	R/W	R/W	R/W	R/W SC
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AUTOSTR							
Access	R/W SC	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – TDEN Topology Discovery Enable
This bit enables the Topology Discovery mode when set.

Value	Description
0	Device is in Normal Operation.
1	Device is in Topology Discovery mode.

Bit 14 – REFN Reference Node selection
This bit set whether this node is a reference or measured node.

Value	Description
0	Device is a measured node.
1	Device is a reference node.

Bit 13 – INTDLYSTRT Internal Delay Measurement Start
Writing a '1' to this bit starts the internal delay measurement of the node.
Note: This bit is self clearing.

Bits 12:9 – DISTMESDUR[3:0] Distance Measurement Duration
Sets the duration of the distance measurement in ms.

Bit 8 – DISTMESSTR Distance Measurement Start
Writing a '1' to this bit starts the distance measurement with the current settings.
Note: This bit is self clearing.

Bit 7 – AUTOSTR Automatic Mode Start
Writing a '1' to this bit starts the automatic mode.
Note: This bit is self clearing.

5.4.86. Topology Discovery Status Register - Rev D

Name: TDSTS - Rev D
Address: 0xCE01

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	INTDLYDN	INTDLYERR	DISTMESDN	DISTMESERR	AUTOERR			
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – INTDLYDN Internal Delay Measurement Done
This bit whether the internal delay measurement has finished.

Value	Description
0	Internal delay measurement not done.
1	Internal delay measurement finished successfully.

Bit 14 – INTDLYERR Internal Delay Measurement Error
This bit whether the internal delay measurement has encountered an error.

Value	Description
0	Internal delay measurement has not encountered an error.
1	Internal delay measurement has encountered an error.

Bit 13 – DISTMESDN Distance Measurement Done
This bit whether the distance measurement has finished.

Value	Description
0	Distance measurement not done.
1	Distance measurement finished successfully.

Bit 12 – DISTMESERR Distance Measurement Error
This bit whether the distance measurement has encountered an error.

Value	Description
0	Distance measurement has not encountered an error.
1	Distance measurement has encountered an error.

Bit 11 – AUTOERR Automatic Measurement Error
This bit whether the automatic measurement has encountered an error.

Value	Description
0	Automatic measurement has not encountered an error.
1	Automatic measurement has encountered an error.

5.4.87. Topology Discovery Distance measurement Result Register (Low) - Rev D

Name: TDDISTRESL - Rev D
Address: 0xCE02

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	DISTRESL[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DISTRESL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DISTRESL[15:0] Distance measurement Result (Low)
This field contains the lower 16 bits of the distance measurement result value.

5.4.88. Topology Discovery Distance measurement Result Register (High) - Rev D

Name: TDDISTRESH - Rev D
Address: 0xCE03

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	DISTRESH[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DISTRESH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DISTRESH[15:0] Distance measurement Result (High)
This field contains the upper 16 bits of the distance measurement result value.

5.4.89. Topology Discovery Internal Delay Result Register (Low) - Rev D

Name: TDINTDLYRESL - Rev D
Address: 0xCE04

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	INTDLYRESL[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTDLYRESL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTDLYRESL[15:0] Internal Delay measurement Result (Low)
This field contains the lower 16 bits of the internal delay measurement result value.

5.4.90. Topology Discovery Internal Delay Result Register (High) - Rev D

Name: TDINTDLYRESH - Rev D
Address: 0xCE05

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	INTDLYRESH[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	INTDLYRESH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – INTDLYRESH[15:0] Internal Delay measurement Result (High)
This field contains the upper 16 bits of the internal delay measurement result value.

5.4.91. Topology Discovery Measured Node Delay measurement Result Register (Low) - Rev D

Name: TDMNDLYRESL - Rev D
Address: 0xCE06

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	MNDLYRESL[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MNDLYRESL[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MNDLYRESL[15:0] Measured Node Delay measurement Result (Low)
This field contains the lower 16 bits of the internal delay measurement of the measured node for which the current distance measurement is being conducted.

5.4.92. Topology Discovery Measured Node Delay measurement Result Register (High) - Rev D

Name: TDMNDLYRESH - Rev D
Address: 0xCE07

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	MNDLYRESH[15:8]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MNDLYRESH[7:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – MNDLYRESH[15:0] Measured Node Delay measurement Result (High)
This field contains the upper 16 bits of the internal delay measurement of the measured node for which the current distance measurement is being conducted.

5.4.93. Topology Discovery Measured Node Measurement Duration Register - Rev D

Name: TDMNMESDUR - Rev D
Address: 0xCE08

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	MNDLYDUR[3:0]							
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bits 15:12 – MNDLYDUR[3:0] Measured Node Delay Duration
This field contains the duration of the internal delay measurement that was conducted in the current measured node.

5.4.94. Topology Discovery Advanced Control Register - Rev D

Name: TDADVCTRL - Rev D
Address: 0xCF00

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	DMTODIS							
Access	RW	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – DMTODIS Distance Measurement Timeout Disable
Disables the distance measurement timer timeout (optional by OA).
This disable should only be set if Firmware implements a TD timeout or for debug purpose.

Value	Description
0	Distance measurement timer timeout enabled.
1	Distance measurement timer timeout disabled.

5.4.95. Wake Sleep Status Register - Rev D

Name: WS_STS - Rev D
Address: 0xD000

This register is only valid for devices of Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	LPCAP	LPFAIL						
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – LPCAP Low Power Capability
This bit indicates whether the device is capable of a low power mode.

Value	Description
0	Client is not capable of power management.
1	Client is capable of lower power mode.

Bit 14 – LPFAIL Low Power Fail
Low power entry request status. This bit is cleared when a request to transition to LOW POWER is received.

5.4.96. Wake Sleep Control Register

Name: WS_CTRL
Address: 0xD001

This register is only present in Revision D0 and later.

Bit	15	14	13	12	11	10	9	8
	LPREQ	LPEXIT						
Access	R/W SC	R/W SC	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit 15 – LPREQ Low Power Mode Request
Request a transition to low power mode on this device.
Note: This bit is self clearing.

Bit 14 – LPEXIT Generate Low Power Mode Exit Request
Signal other devices to wake from sleep according configured in the SLPCTRL1 register. One wake event will be generated on each enabled interface.
Note: This bit will clear itself when wake event generation is complete.

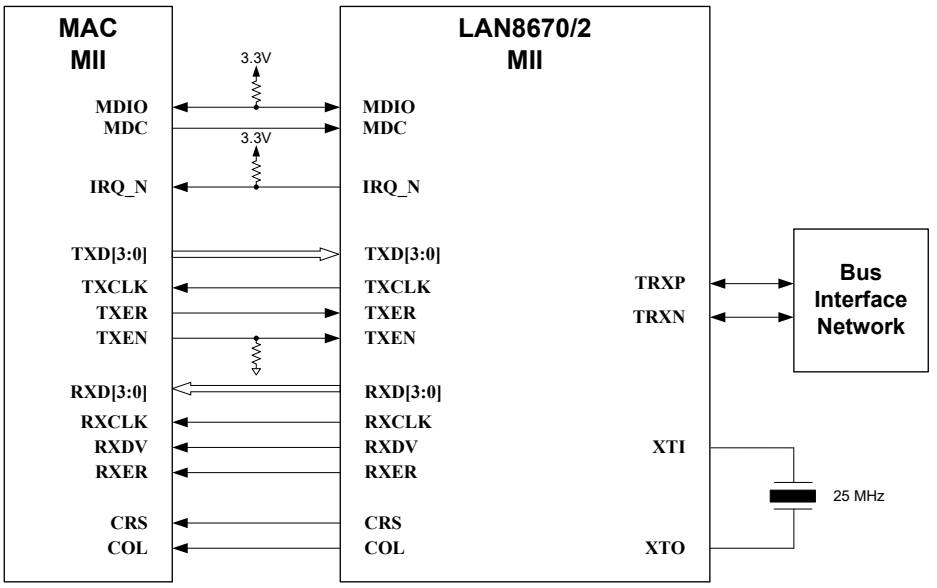
Value	Description
0	Do not generate a wake event (normal operation)
1	Generate a wake event on each interface enabled in SLPCTRL1.

6. Application Information

6.1. MII Connectivity

Figure 6-1 illustrates device connectivity in MII mode.

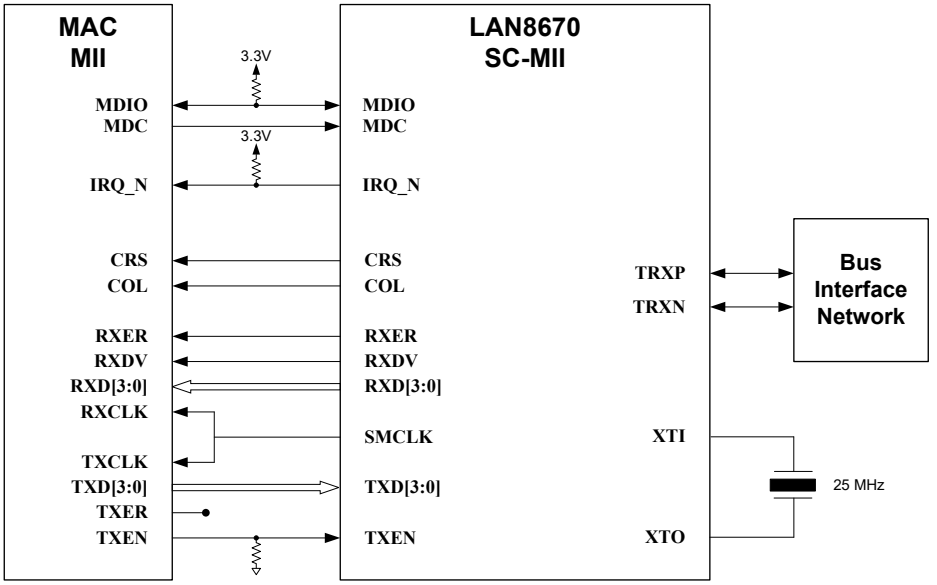
Figure 6-1. MII Connectivity



6.1.1. Single Clock MII Connectivity

Figure 6-2 illustrates device connectivity in SC-MII mode.

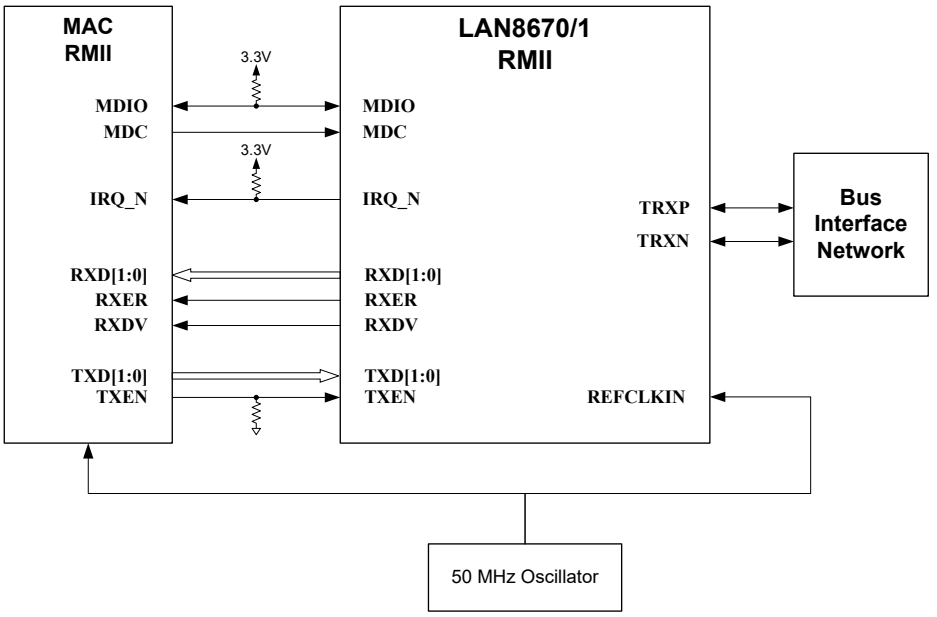
Figure 6-2. Single Clock MII Connectivity



6.2. RMII Connectivity with Reference Clock

The figure below illustrates device connectivity in RMII mode with a 50 MHz reference clock.

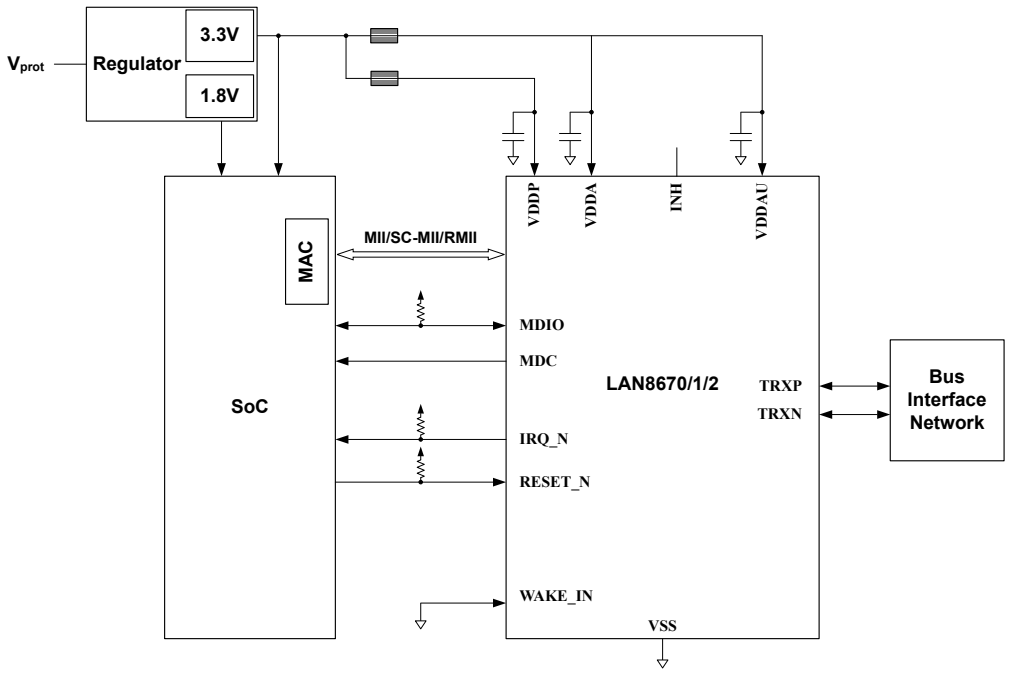
Figure 6-3. RMII Connectivity with Reference Clock



6.3. System Configuration without Sleep Mode

Device connectivity without sleep mode is illustrated in the following figure. A configuration with sleep mode can be found in the *Sleep Mode and System Power Management* section.

Figure 6-4. Example System without Sleep Mode



Related Links

Sleep Mode and System Power Management

6.4. Power Connectivity

This section describes the typical power configuration for the LAN8670/1/2 devices with the power supply architecture and recommended decoupling.

For simple architectures, the LAN8670/1/2 requires only a single 3.3V power supply if no low power sleep state with wake-up mechanism is required. If the application requires a low power sleep state and wake-up, then an additional uninterrupted, continuous 3.3V power supply ($3.3V_{cont}$) must be connected to VDDAU to power the internal wake-up circuitry. See Figure 6-6. When a sleep power state is not required, a continuous 3.3V power supply is not necessary and VDDAU is therefore connected to the same switched power supply ($3.3V_{sw}$) as VDDA as illustrated in Figure 6-5.

When a continuous 3.3V supply is used to implement a low power sleep state, the VDDA supply pin must never exceed the VDDAU supply pin by more than 0.5V. One approach to satisfying this power sequencing requirement is to connect a Schottky diode between the power supplies to prevent VDDA from exceeding VDDAU by more than a forward-biased voltage drop. The Schottky diode must be sized appropriately if used; the forward voltage drop must be less than 0.5V when the diode conducts current when VDDA exceeds VDDAU. See Figure 6-6 and Figure 6-8.

Proper decoupling of the LAN8670/1/2 power distribution network is a prerequisite for stable operation and best EMC performance. Low ESR 0.1 µF and 0.01 µF decoupling capacitors are placed at each power pin of the device for localized decoupling. These decoupling capacitors should be located as close as possible to the pin to minimize parasitic inductance and maximize their effectiveness. This is typically done by placing the decoupling capacitors on the opposite side of the board from the device directly under the pin and connecting them to the exposed pad. Priority is always given to the placement of the smaller 0.01 µF decoupling capacitor closer to the corresponding pin rather than the larger 0.1 µF capacitor. Each decoupling capacitor is ideally connected to the power plane through two vias to minimize interconnection inductance. Decoupling capacitors should not share vias.

In addition to the decoupling capacitors at each pin, a bulk capacitor, typically 10 µF, is placed near the LAN8670/1/2 in the direction of the power supply that will be supplying current. The bulk capacitors serve to provide low frequency energy that is outside the supply's response time.

EMI sensitive applications requiring increased noise performance, may optionally add ferrite beads such as the Würth 742792640 to create localized power islands around the device for the VDDA, VDDAU, and VDDP supplies as illustrated in Figure 6-7 and Figure 6-8. When a ferrite bead is used, it should have a resistance of around 300Ω at 100 MHz. Additionally, the ferrite bead must have a DC current rating of at least twice the maximum supply current of the corresponding power pins to supply power and avoid core saturation and degradation in performance. During the prototype phase, it is recommended to include the option for adding ferrite beads should the need arise to improve noise immunity.

Depending on the properties of the ferrite bead, its combination with the small decoupling capacitors may cause resonant noise amplification at certain frequencies, leading to an undesired amplification of noise in the system and resulting in increased electromagnetic radiation and noise coupling in form of amplitude noise and jitter. Since the ferrite bead selection is highly dependent on the noise in the system, which varies from design to design, the large bulk capacitor, typically 10 µF, is recommended to be placed on the device side of the ferrite bead. When ferrite beads are used, a 10 µF bulk capacitor on the supply side of the ferrite bead is not necessary. See Figure 6-7 and Figure 6-8.

Ideally, the board stackup will contain a large power plane layer next to a ground plane layer. The capacitance between the power and ground planes serve to provide high frequency, low inductance decoupling. When local power islands are used, the islands should be smaller planes underneath the LAN8670/1/2, again adjacent to a ground plane to provide high-frequency capacitive decoupling. The use of power tracks is discouraged but, if used, should be as short and wide as possible to minimize sheet resistance and current dependent voltage ripple at the power distribution to the pins.

Important:
The exposed ground pad (ePAD) of the package serves as the primary ground connection of the device and must be adequately connected to the PCB ground plane through an array of vias as specified in the *Packaging Information* section.

The analog pins (WAKE_IN, WAKE_IO, TRXP, TRXN, XTI/REFCLKIN, and XTO) pins must never be driven to more than the VDDAU supply. Furthermore, all other digital pins must never be driven to more than the VDDP supply. These requirements are applicable during power-up and power-down, as well as during normal operating conditions.

Figure 6-5. LAN8670/1/2 Minimal Power Connectivity without Sleep

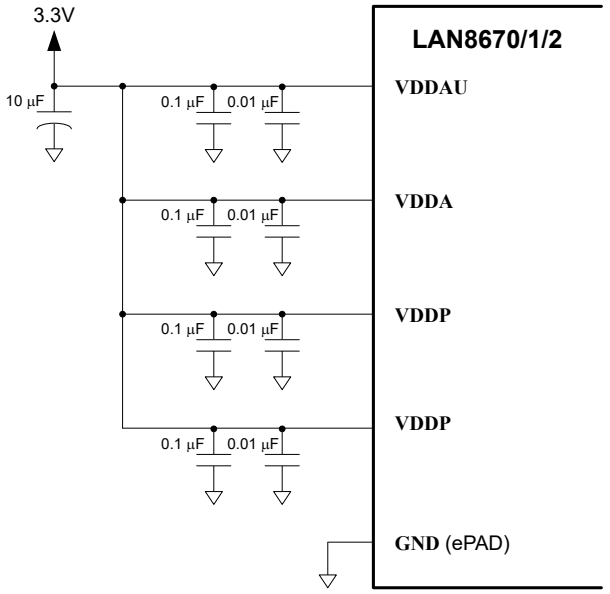


Figure 6-6. LAN8670/1/2 Minimal Power Connectivity with Sleep

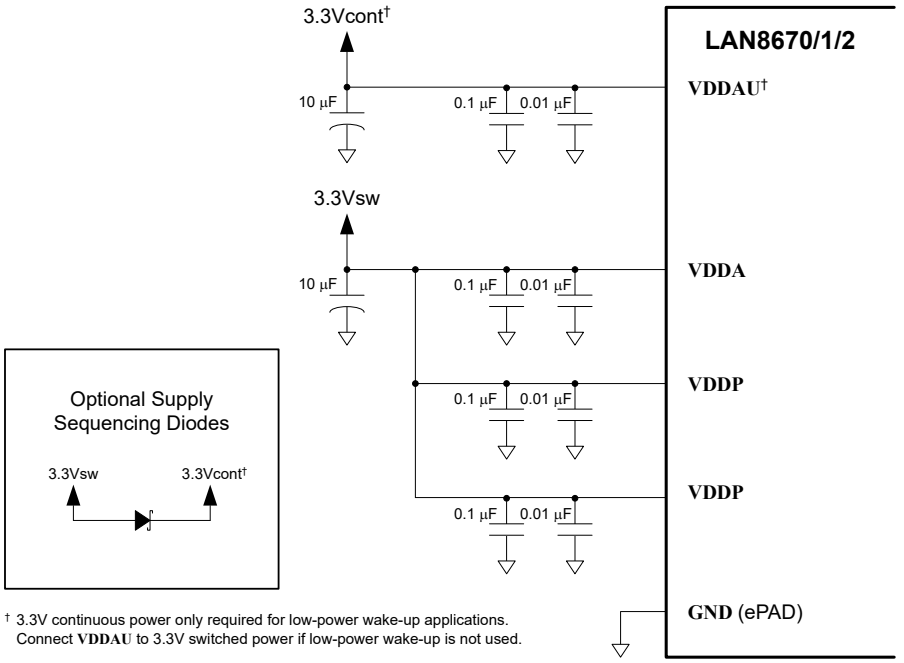


Figure 6-7. LAN8670/1/2 Localized Power Island Connectivity without Sleep

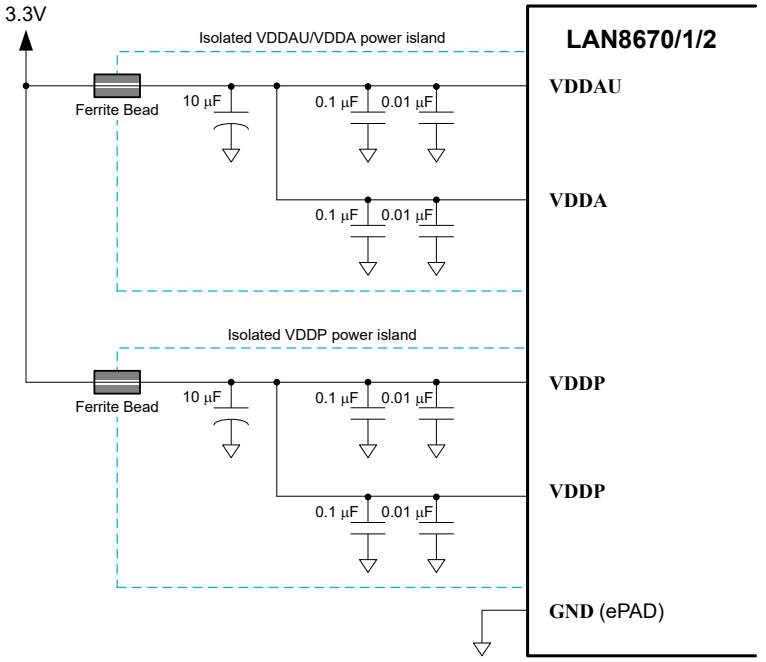
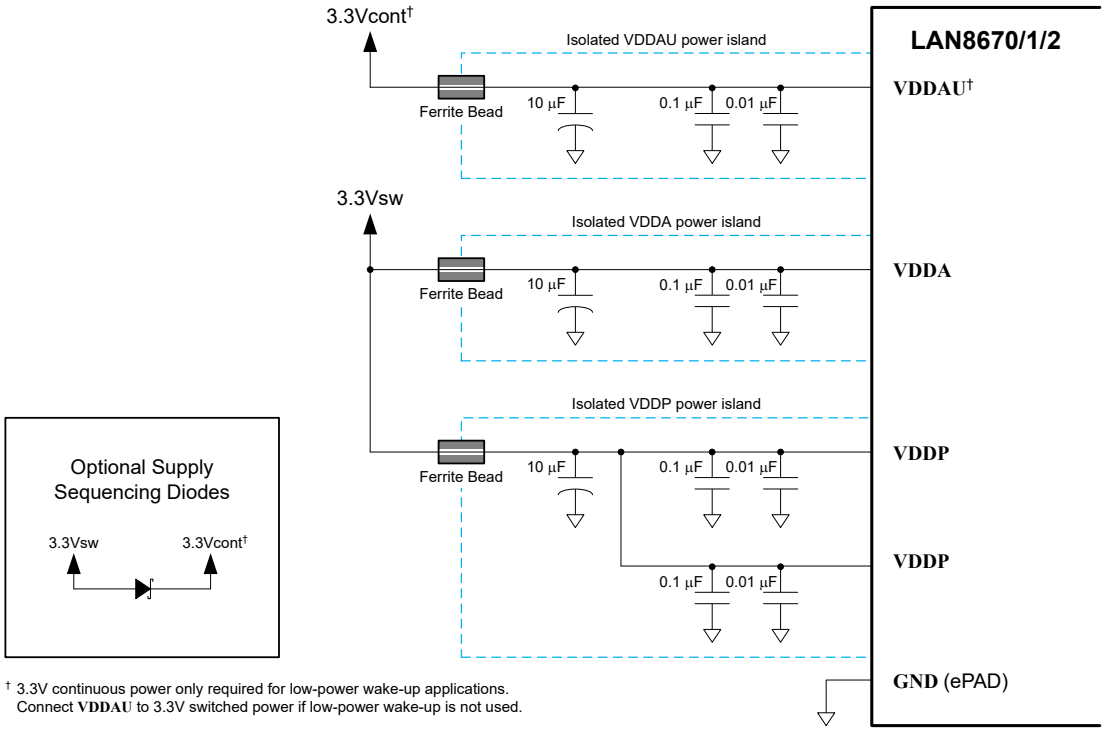


Figure 6-8. LAN8670/1/2 Localized Power Island Connectivity with Sleep



† 3.3V continuous power only required for low-power wake-up applications. Connect **VDDAU** to 3.3V switched power if low-power wake-up is not used.

Related Links

Packaging Information

6.5. Electromagnetic Compatibility (EMC) Considerations

The latest recommendations for schematic design and PCB layout to achieve optimal EMC performance for the LAN8670/1/2 can be found in the *LAN86xx Bus Interface Network (BIN) Reference Design Application Note AN1718*.

Related Links

Reference Documents

6.5.1. Output Drive Strength Control

The LAN8670/1/2 digital outputs are configurable to one of four drive strengths. By changing the digital output impedance in combination with the output load, the rise and fall time of driven output signals may be adjusted to meet timing requirements while reducing the sharp transitions and ringing that can be a source of unwanted radiated emissions. The pin output drive strength is configurable in groups based on their application as defined in the table below. The output drive level for each pin group is configured within the Pad Control 3 (PADCTRL3) register. The output drive currents are specified in the *DC Specifications* section.

Table 6-1. Digital Output Drive Pin Groups

Pin Name	Pin Number		
	LAN8670	LAN8671	LAN8672[1]
Pin Group 1 - Application			
GPIO0	9	7	10
TXCLK/RXPI	12	—	—
RXPI	—	—	14
IRQ_N	22	16	24
WAKE_OUT	—	17	27
Pin Group 2 - Serial Management Interface			
MDIO	14	10	16
Pin Group 3 - MII/SC-MII			
COL	2	—	2
CRS	15	—	17
RXCLK/SMCLK/WAKE_OUT	17	—	—
RXCLK	—	—	19
RXD2	23	—	25
RXD3	24	—	26
TXCLK	—	—	3
Pin Group 4 - MII/SC-MII/RMII			
RXD0	16	11	18
RXD1	19	12	21
RXDV/CRSDV	20	—	—
CRSDV	—	14	—
RXDV	—	—	22
RXER	21	15	23

Note:

1. LAN8672 Revision C2, only.

Related Links

PADCTRL3

Pad Control 3 Register

DC Specifications (other than 10BASE-T1S PMA)

6.5.2. PLCA Collision Detection

When nodes in a mixing segment are properly configured for PLCA operation there will be no physical collisions. However, under certain conditions, including mixing segments with significant inherent noise due to reflections, and systems under high electromagnetic stress, false collisions may be detected. The false detection of late collisions will result in the transmitting node dropping the packet. As packets are typically received correctly in these conditions, it is recommended to disable collision detection at any time that PLCA is enabled and active. Collision detection is disabled by writing a zero to the Collision Detect Enable (CDEN) bit in the Collision Detector Control 0 (CDCTL0) register.

Note: Collision detection **must** be enabled when the node is operating purely CSMA/CD when PLCA is disabled or inactive. For revision D0 and later products, collision detection may be configured to automatically enable and disable based upon the state of the PLCA Status indication. Please refer to the section *Transmit Collisions* for details.

Related Links

Transmit Collisions

6.6. Crystal Oscillator Selection

Oscillator margin is a measure of the stability of an oscillator circuit, and is defined in Equation 6-1 as the ratio of the oscillator's negative resistance (R_{NEG}) to the crystal's ESR (R_{ESR}).

Equation 6-1. Crystal Oscillator Margin Measurement

$$\text{Margin} = \frac{|R_{\text{NEG}}|}{R_{\text{ESR}}} = \frac{|R_{\text{VAR}}| + R_{\text{ESR}}}{R_{\text{ESR}}}$$

The negative resistance can be measured by placing a variable resistor (R_{VAR}) in series with the crystal and finding the largest resistor value where the crystal still starts up properly. This point would be just below where the oscillator does not start-up or where the start-up time is excessively long. Ideally, oscillator margin should be greater than 10, and should be at least 5. Smaller oscillator margin can affect the ability of the oscillator to start up.

The load capacitance, C_L, which is specified when ordering the crystal, is calculated from the capacitance on each leg of the crystal, C_x, combined with the stray capacitance, C_{stray}, which is contributed by PCB traces and chip pins. $C_{stray}$is usually in the range of 2 pF to 5 pF. The clock circuit requires that both crystal pins have matching C_x. C_L can then be calculated from

Equation 6-2. Crystal Load Capacitance

$$\mathrm{C_L} = \frac{1}{2}\mathrm{C_x} + \mathrm{C_{stray}}$$

Larger capacitors also have a negative effect on oscillator margin. It is recommended that a crystal utilizing matching parallel load capacitors be used for the crystal input/output signals (XTI/XTO). The transconductance gain (g_m) of the internal inverting amplifier is nominally 18.2 mS.

The crystal cut and tolerance value listed in the *Crystal Specifications* section are typical values and may be changed to suit differing system requirements. Higher ESR values (than those listed in *Crystal Specifications*) run the risk of having start-up problems and should be thoroughly tested before being used. Contact the crystal manufacturer for more information.

Related Links
Crystal Specifications

6.7. Reference Schematics

The schematics on the following pages contain example reference implementations of the LAN8670/1/2.

The bus interface network, or BIN, not shown, is composed of the discrete analog components that interface the device TRXP/TRXN pins to the bus connector. Design of the BIN is largely dependent upon specific application requirements, but at a minimum must include a series 100 nF coupling capacitor on each of the TRXP and TRXN pins. Additional bus interface network details are contained in a separate *LAN86xx Bus Interface Network (BIN) Reference Design Application Note AN1718*.

Figure 6-9. LAN8670 MII Reference Schematic (No Sleep/Wake)

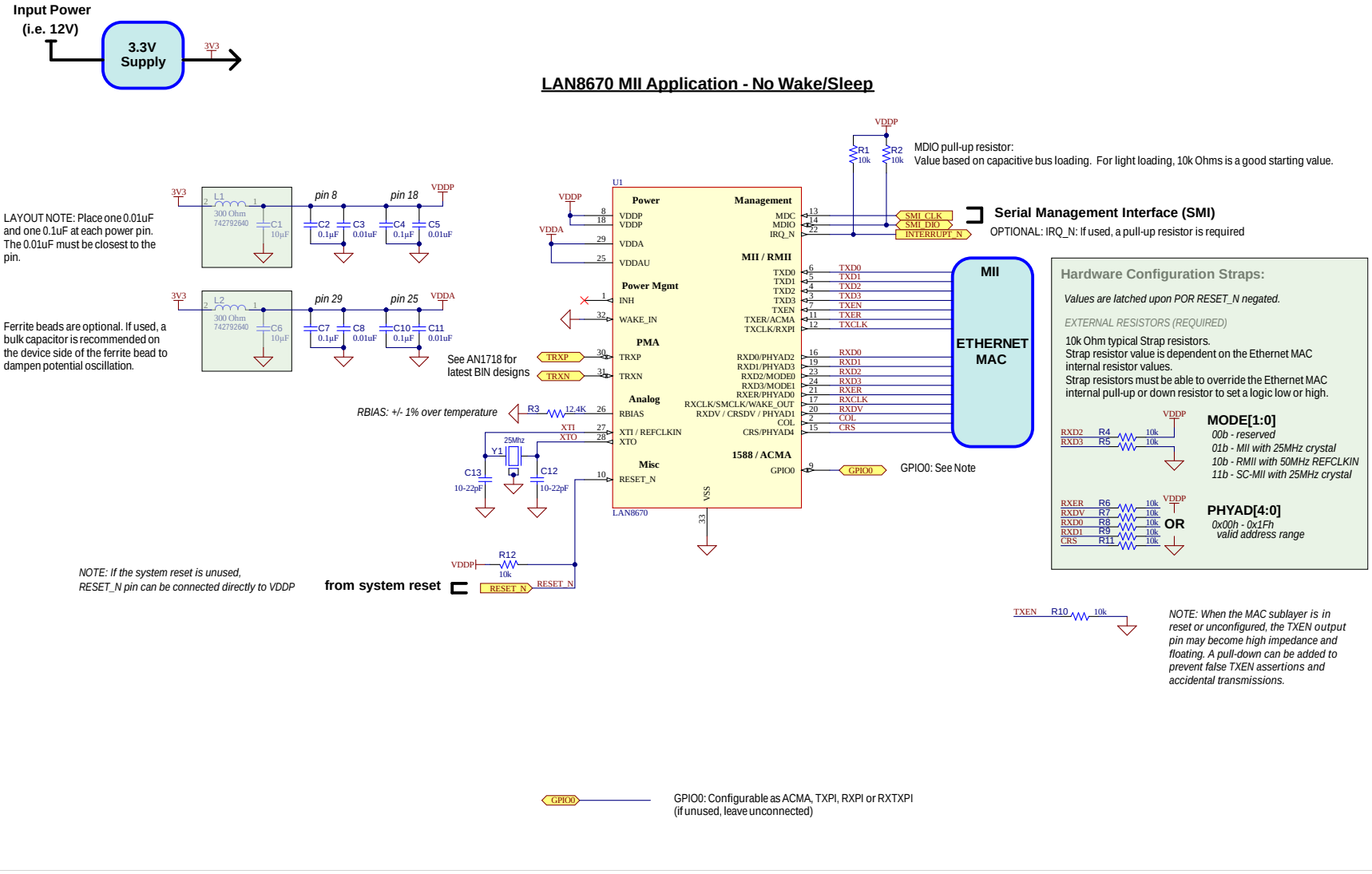


Figure 6-10. LAN8670 MII Reference Schematic (With Sleep/Wake)

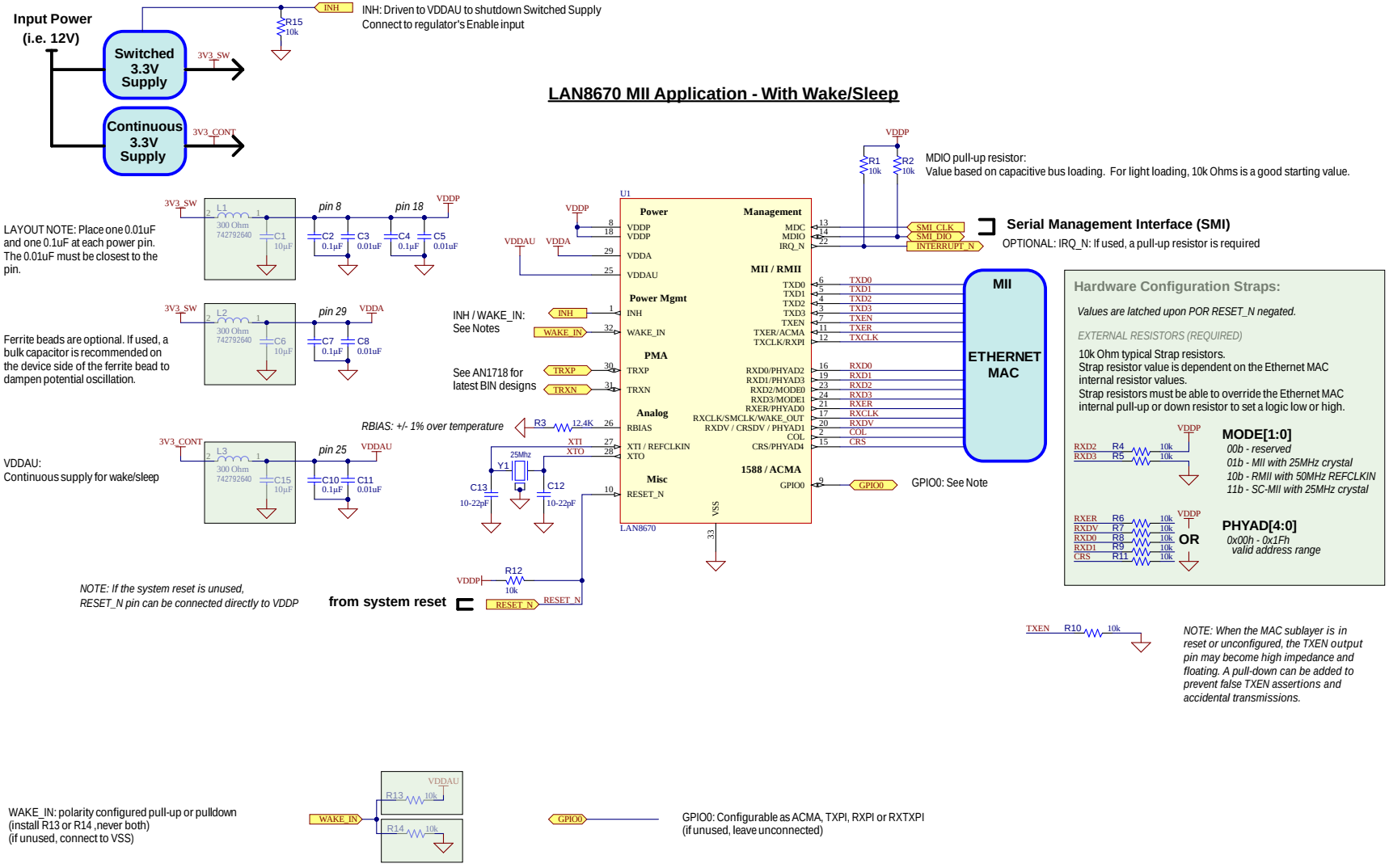


Figure 6-11. LAN8670 SC-MII Reference Schematic (No Sleep/Wake)

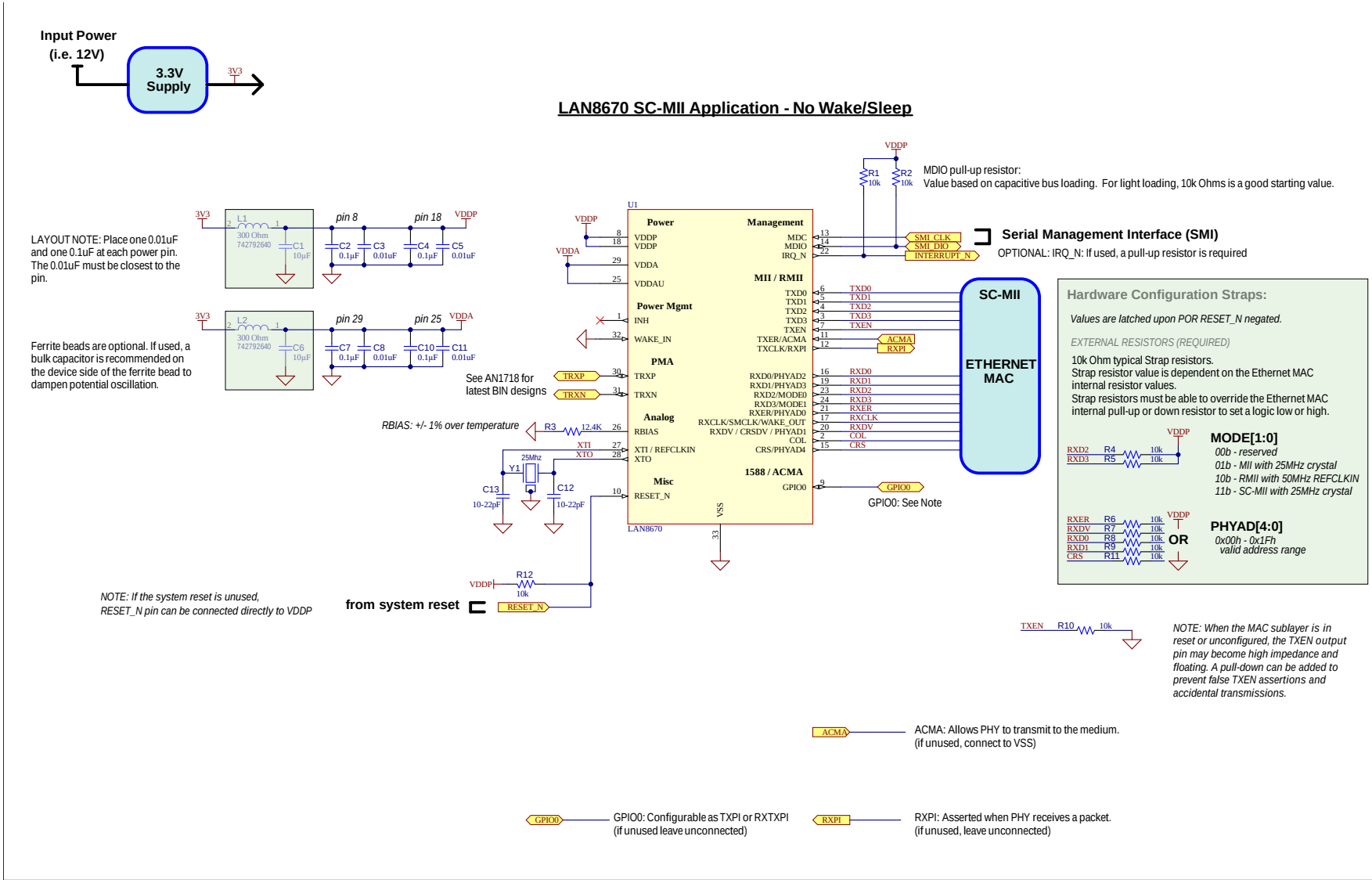


Figure 6-12. LAN8670 SC-MII Reference Schematic (With Sleep/Wake)

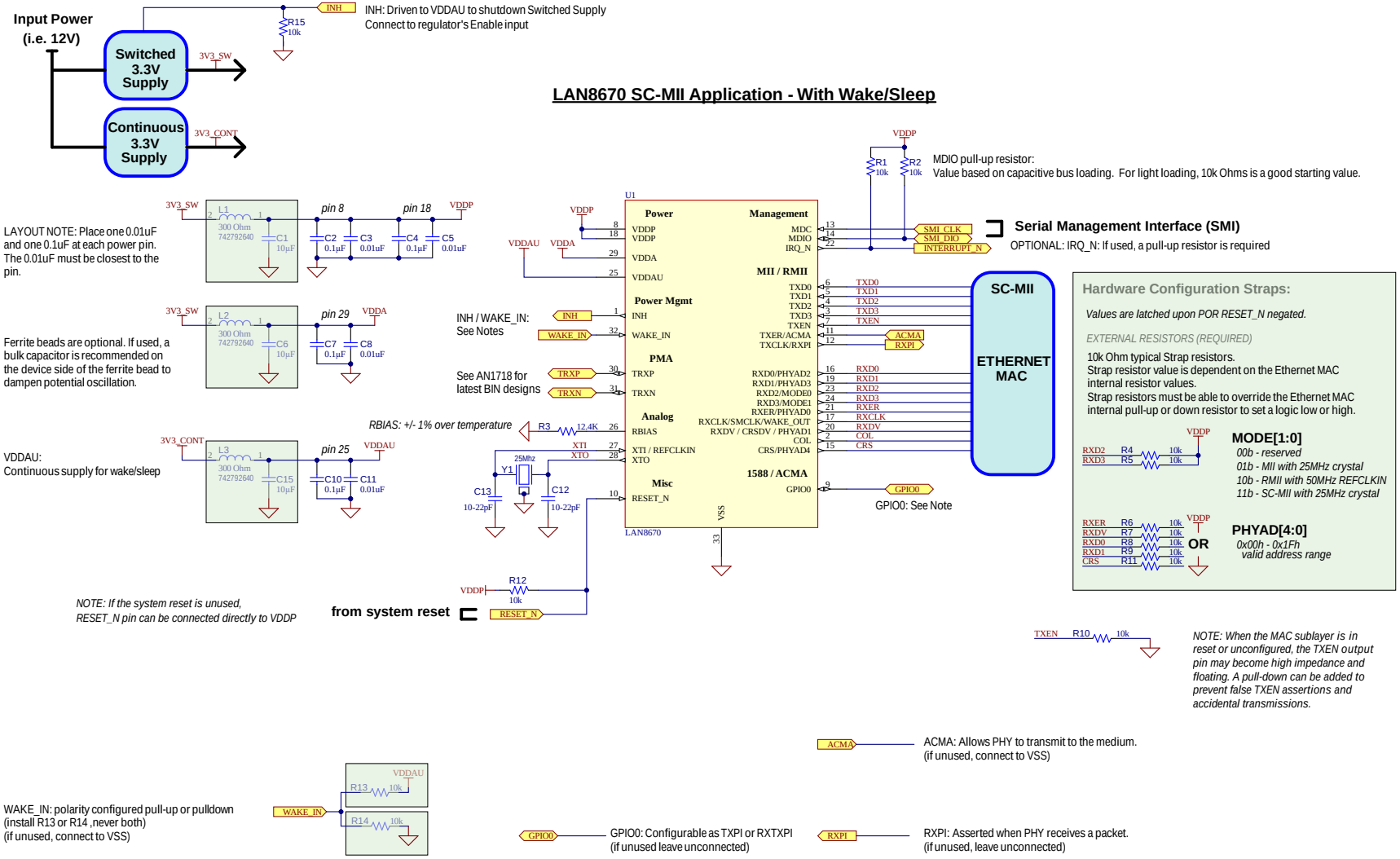


Figure 6-13. LAN8670 RMII Reference Schematic (No Sleep/Wake)

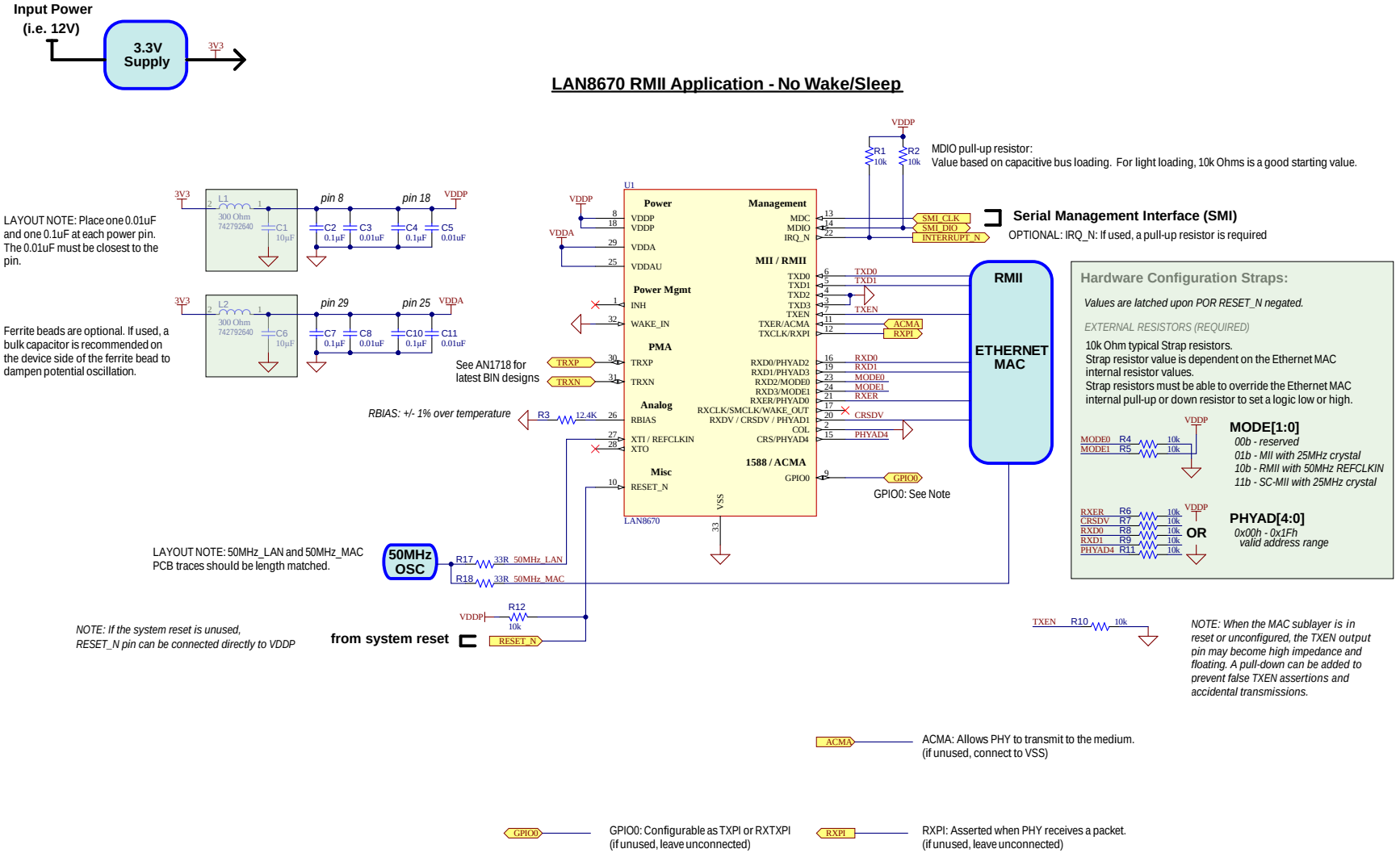


Figure 6-14. LAN8670 RMII Reference Schematic (With Sleep/Wake)

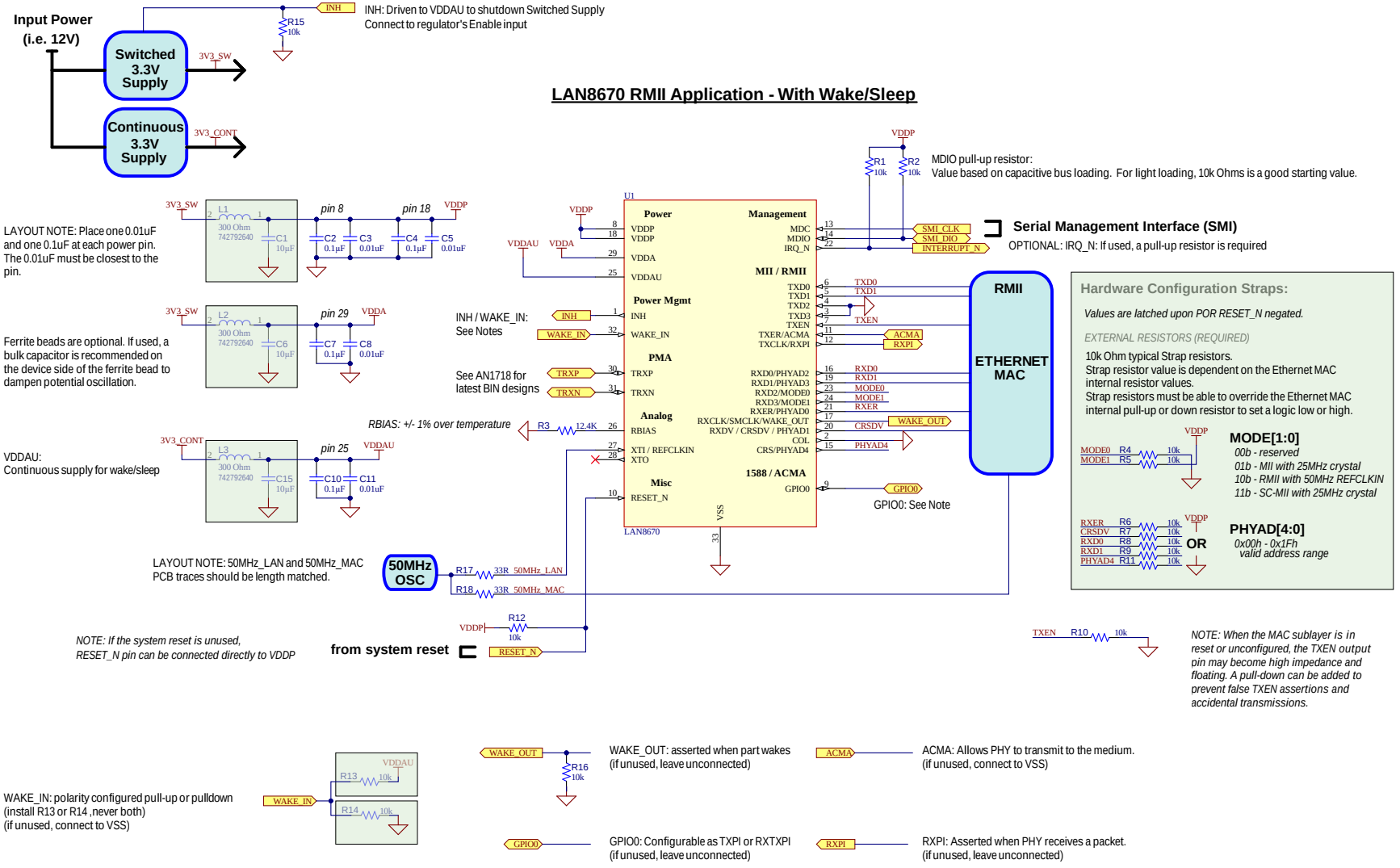


Figure 6-15. LAN8671 RMII Reference Schematic (No Sleep/Wake)

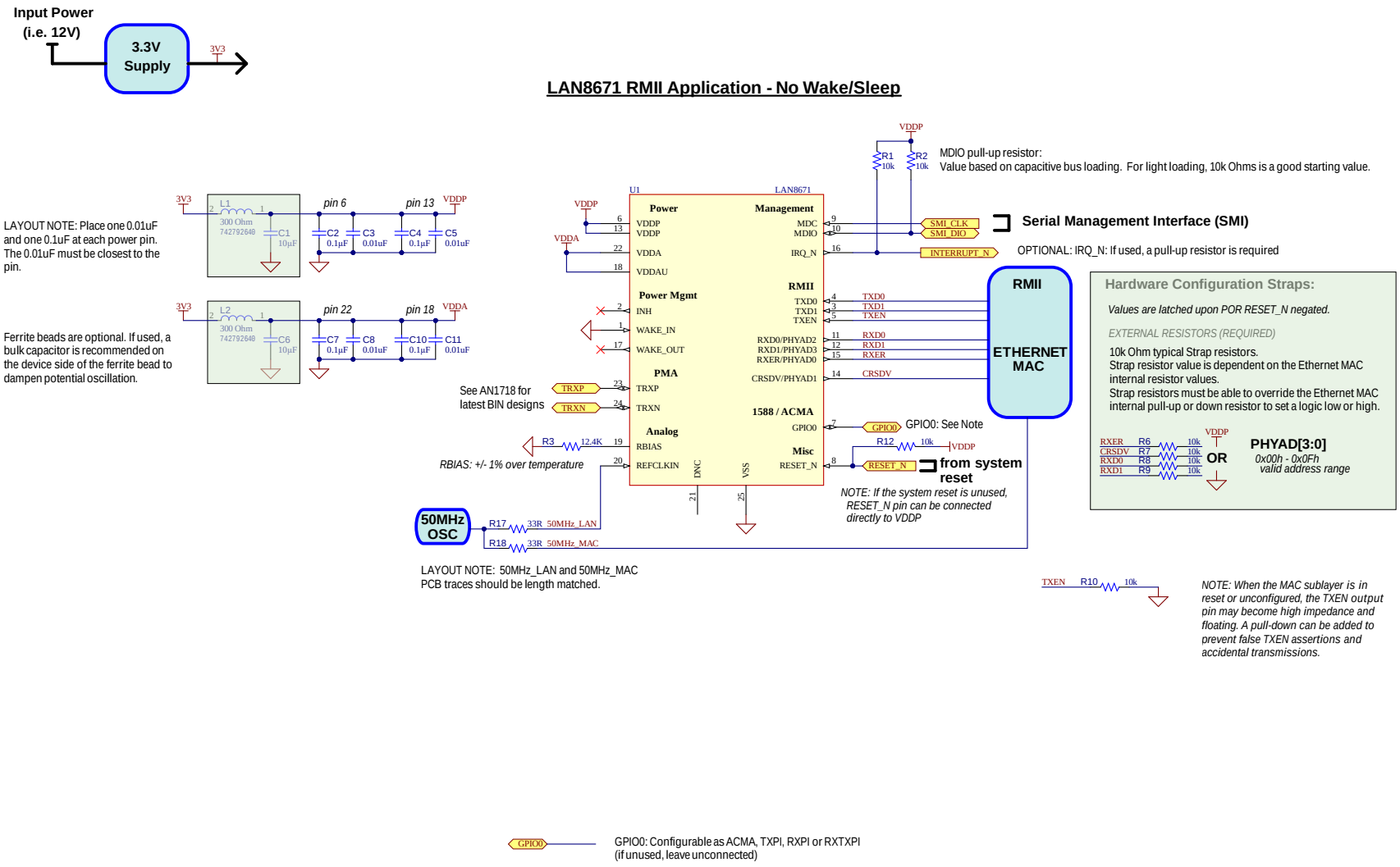


Figure 6-16. LAN8671 RMII Reference Schematic (With Sleep/Wake)

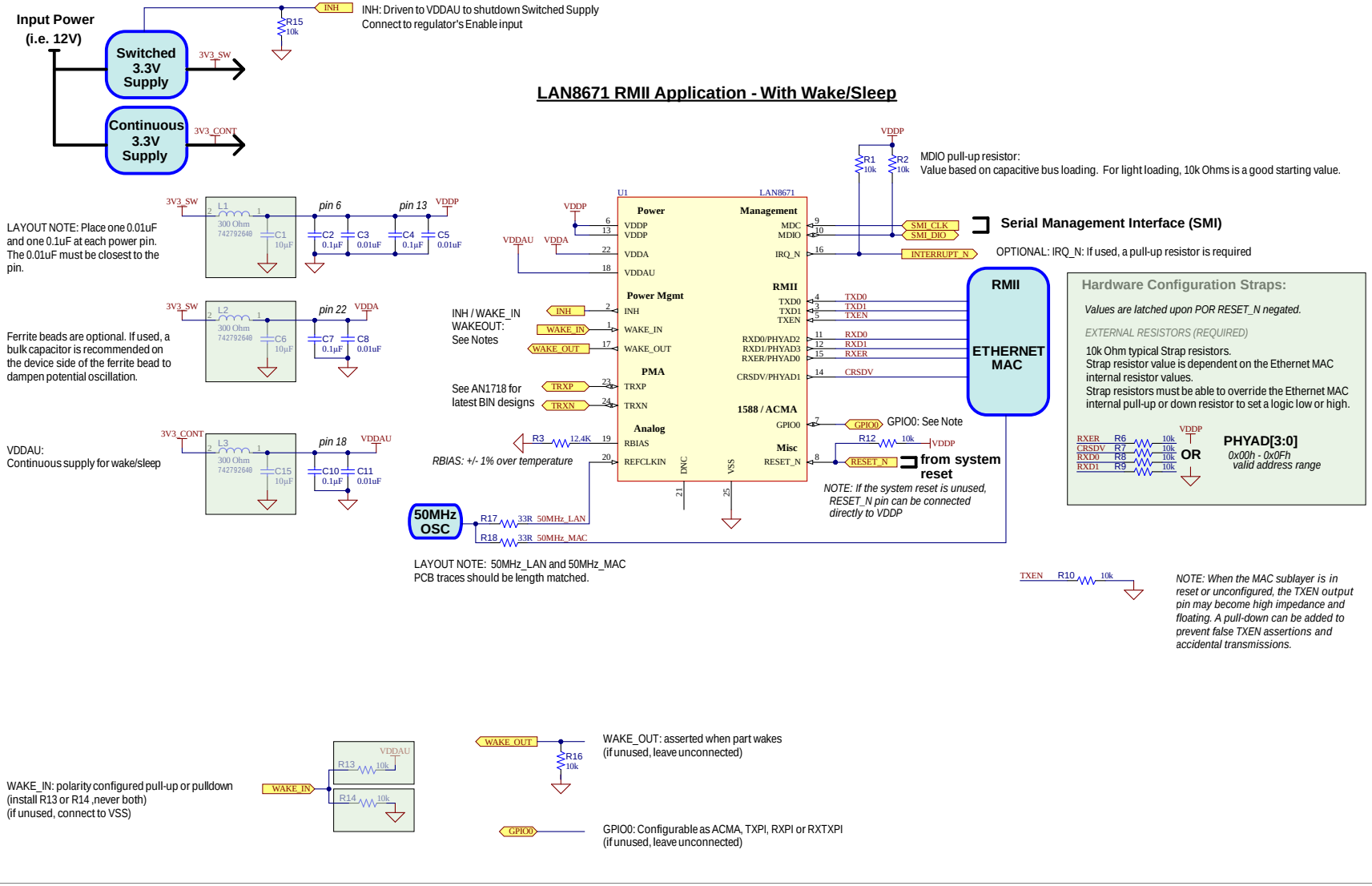


Figure 6-17. LAN8672 MII Reference Schematic (No Sleep/Wake)

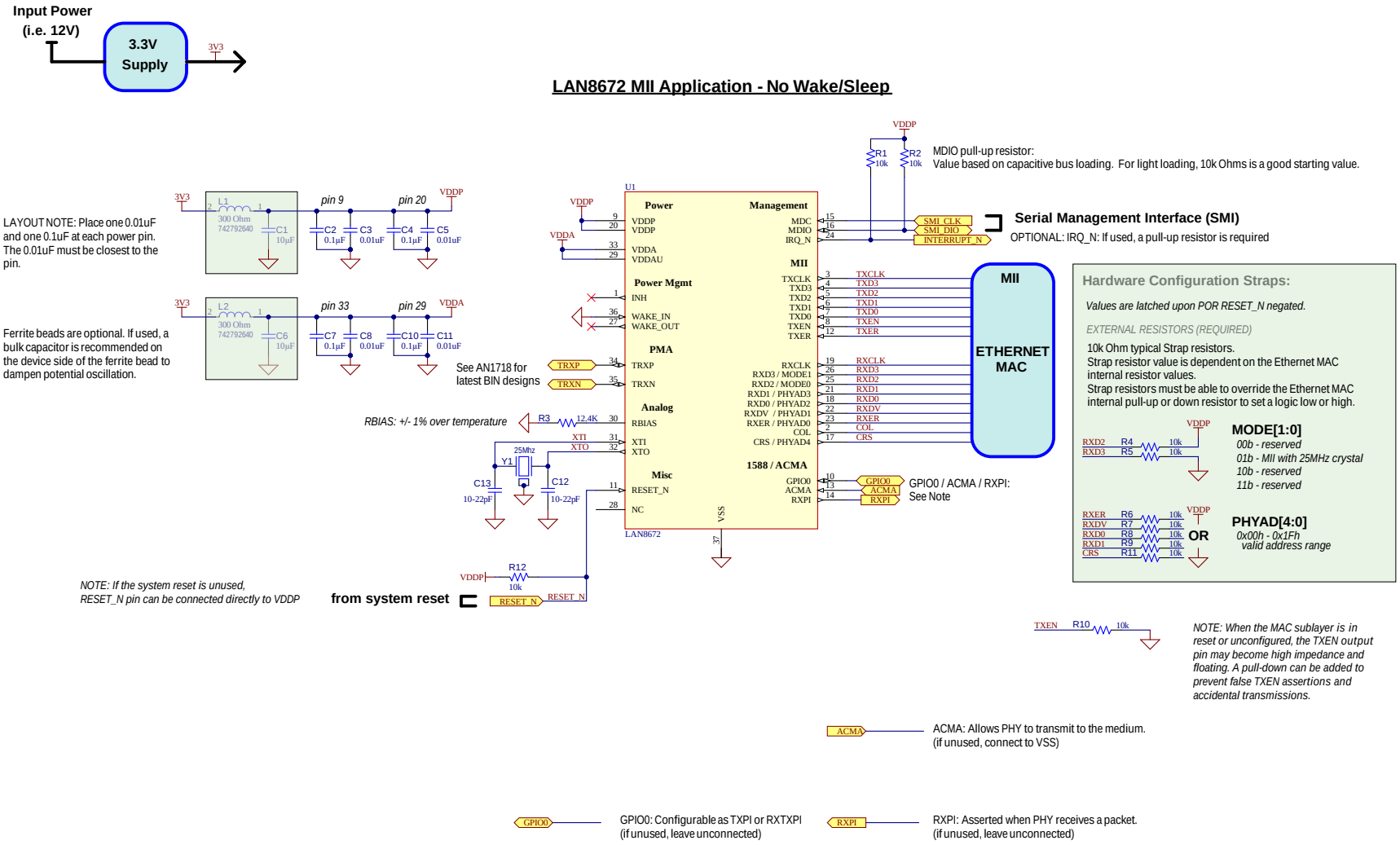
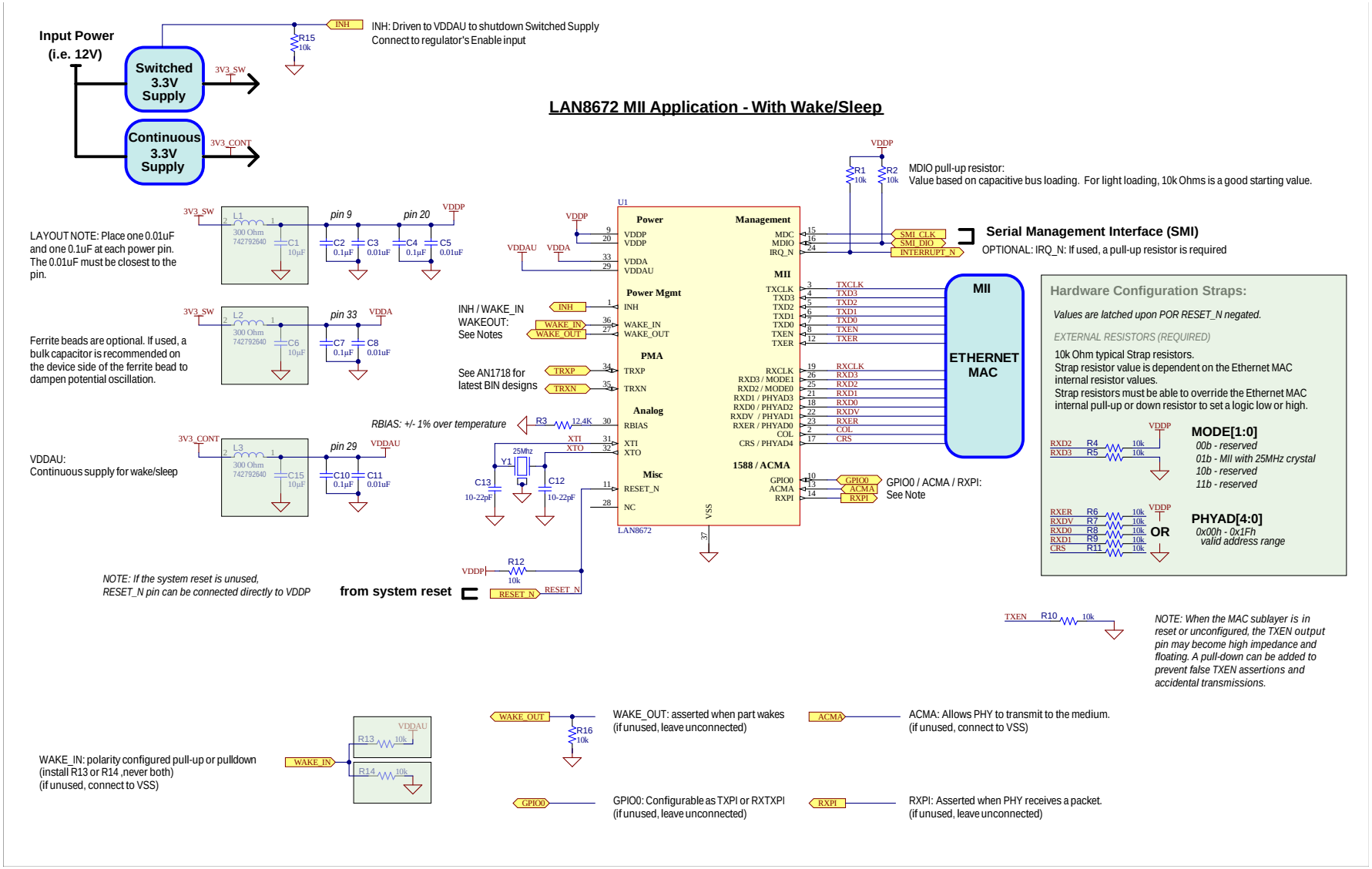


Figure 6-18. LAN8672 MII Reference Schematic (With Sleep/Wake)



7. Operational Characteristics

7.1. Absolute Maximum Ratings

Stresses exceeding those listed in this section could cause permanent damage to the device. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at any condition exceeding those indicated in *Operating Conditions*, *DC Specifications*, or any other applicable section of this specification is not implied.

Attention: Exposure at or above these limits may damage the device.

Table 7-1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Power Supply Voltage:					Note 1
Digital I/O (VDDP)		-0.5	3.9	V	
Analog (VDDA)		-0.5	3.9	V	
Continuous (VDDAU)		-0.5	3.9	V	
Voltage applied to pins:					
TRXP, TRXN	$V_{TRXP/N}$	-27	42	V	
TRXP/TRXN (differential)	V_{DIFF}	-32	32	V	
XTI/REFCLKIN, RBIAS		-0.5	VDDA + 0.5	V	Note 2
WAKE_IN		-0.5	VDDAU+ 0.5	V	Note 2
All other pins		-0.5	VDDP + 0.5	V	Note 2
Junction Temperature Under Bias	T_J	-40	150	°C	
Storage Temperature	T_{stg}	-55	150	°C	
Lead Temperature Range	Refer to JEDEC Spec. J-STD-020				
ESD Human Body Model		-8	+8	kV	Note 3
ESD Charge Device Model		-1	+1	kV	AEC-Q100-011

Notes:

1. When powering this device from laboratory or system power supplies, it is important that the absolute maximum ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.
2. Voltage applied to pins must remain below 3.9V.
3. Test specification following JESD22-A114/AEC-Q100-002: (1.5 kΩ/100 pF)

7.2. Operating Conditions

Proper operation of the device is guaranteed only within the ranges specified in this section.

Table 7-2. Operating Conditions

Description	Symbol	Min	Max	Units	Notes
Power Supply Voltage:					
Digital I/O (VDDP)		3.135	3.465	V	
Continuous (VDDAU)		3.135	3.465	V	
Analog (VDDA)		3.135	3.465	V	Note 1
Maximum Input Voltage:					
XTI/REFCLKIN, RBIAS		-0.3	VDDA + 0.3	V	
WAKE_IN		-0.3	VDDAU + 0.3	V	
All other pins		-0.3	VDDP + 0.3	V	
Power Supply Ramp Rate		300		µs/V	
Ambient Operating Temperature (Still Air)	T_A	-40	+125	°C	Note 2

Notes:

1. The VDDA pin shall never exceed the VDDAU pin by more than 0.5 V. This requirement applies to power-up, power-down, and normal operation.
2. Junction temperature shall never exceed 135 °C.

7.3. Power Consumption

All parameters tested unless otherwise noted.

Table 7-3. Current Consumption and Power Dissipation LAN8670/1/2 (Rev C2)

Supply	Current			Power			Notes
	Typical	Maximum	Units	Typical	Maximum	Units	
Sleep							
VDDAU	40	56	µA	132	194	µW	Notes 1, 2
Normal operation							
VDDAU	570		µA				Note 3
VDDA	34	41	mA				Note 3
VDDP	4		mA				Note 4
Power				129	149	mW	Note 5

Notes:

1. Current for sleep mode is only for VDDAU. All other power pins are assumed to be unpowered.
2. Maximum sleep power calculated for VDDAU = 3.465V
3. Continuous transmission.
4. Typical VDDP current when receiving data. Current is lower in other modes.
5. Maximum power occurs during continuous transmission with all power supplies at 3.465V

Table 7-4. Current Consumption and Power Dissipation LAN8670/1 (Rev D0)

Supply	Current			Power			Notes
	Typical	Maximum	Units	Typical	Maximum	Units	
Sleep							
VDDAU	40	56	µA	132	194	µW	Notes 1, 2
Normal operation							
VDDAU	570		µA				Note 3
VDDA	40	45	mA				Note 3
VDDP	4		mA				Note 4
Power				147	175	mW	Note 5

Notes:

1. Current for sleep mode is only for VDDAU. All other power pins are assumed to be unpowered.
2. Maximum sleep power calculated for VDDAU = 3.465V
3. Continuous transmission.
4. Typical VDDP current when receiving data. Current is lower in other modes.
5. Maximum power occurs during continuous transmission with all power supplies at 3.465V

7.4. Package Thermal Specifications

Note: Thermal parameters are measured or estimated for devices in a multi-layer 2S2P PCB per JESD51.

Table 7-5. LAN8670 Package Thermal Parameters (32-VQFN)

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	43	°C/W	Still air
Junction-to-Top-of-Package	Ψ_{JT}	0.6	°C/W	Still air
Junction-to-Case	Θ_{JC}	7.6	°C/W	

Table 7-6. LAN8671 Package Thermal Parameters (24-VQFN)

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	54	°C/W	Still air
Junction-to-Top-of-Package	Ψ_{JT}	0.9	°C/W	Still air
Junction-to-Case	Θ_{JC}	8.3	°C/W	

Table 7-7. LAN8672 Revision C2 Package Thermal Parameters (36-VQFN)

Parameter	Symbol	Value	Units	Notes
Junction-to-Ambient	Θ_{JA}	35	°C/W	Still air
Junction-to-Top-of-Package	Ψ_{JT}	0.4	°C/W	Still air
Junction-to-Case	Θ_{JC}	5.0	°C/W	

7.5. DC Specifications (other than 10BASE-T1S PMA)

All parameters are tested unless otherwise noted.

Table 7-8. DC Electrical Characteristics (other than 10BASE-T1S PMA)

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
VIS-VDDP Type Input Buffers						
Low-Level Input Voltage	V_{IL}			0.8	V	
High-Level Input Voltage	V_{IH}	2.0			V	
Input Hysteresis	ΔV_{hys}	18		170	mV	Note 1
Input Leakage	I_L	-10		10	µA	V_{IN} = VSS or VDDP
Input Capacitance	C_{IN}			3	pF	Note2
VI-VDDAU Type Input Buffers						
Low-Level Input Voltage	V_{IL}			0.8	V	
High-Level Input Voltage	V_{IH}	2.0			V	
Input Leakage	I_L	-10		10	µA	V_{IN} = VSS or VDDAU
Input Capacitance	C_{IN}			3	pF	Note2
VO-VDDP Type Output Buffers						
Low-Level Output	V_{OL}			0.4	V	Note 3
	I_{OL-L}	-0.6			mA	Low drive
	I_{OL-ML}	-1.7			mA	Medium-low drive
	I_{OL-MH}	-2.8			mA	Medium-high drive
	I_{OL-H}	-4.0			mA	High drive
High-Level Output	V_{OH}	VDDP-0.4			V	Note 4
	I_{OH-L}	0.45			mA	Low drive
	I_{OH-ML}	1.2			mA	Medium-low drive
	I_{OH-MH}	2.0			mA	Medium-high drive
	I_{OH-H}	2.9			mA	High drive
VODL-VDDP Type Output Buffers						
Low-Level Output	V_{OL}			0.4	V	Note 3
	I_{OL-L}	-0.6			mA	Low drive
	I_{OL-ML}	-1.7			mA	Medium-low drive
	I_{OL-MH}	-2.8			mA	Medium-high drive
	I_{OL-H}	-4.0			mA	High drive
VOH-VDDP Type Output Buffers						
Low-Level Output	V_{OL}			0.4	V	Note 3
	I_{OL-L}	-1.3			mA	Low drive
	I_{OL-ML}	-2.7			mA	Medium-low drive
	I_{OL-MH}	-4.0			mA	Medium-high drive
	I_{OL-H}	-5.3			mA	High drive

Notes:

1. Characterized on samples
2. Design parameter, not tested
3. I_{OL} is configurable to four levels of sink current.
4. I_{OH} is configurable to four levels of source current.

Table 7-8. DC Electrical Characteristics (other than 10BASE-T1S PMA) (continued)

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
High-Level Output	V_{OH}	VDDP-0.4			V	Note 4
	I_{OH-L}	1.0			mA	Low drive
	I_{OH-ML}	2.0			mA	Medium-low drive
	I_{OH-MH}	2.8			mA	Medium-high drive
	I_{OH-H}	3.5			mA	High drive
VODH-VDDAU Type Output Buffers						
High-Level Output	V_{OH}	VDDAU-0.4			V	
	I_{OH}	1.7			mA	
ICLK Type Input Buffer						RMII REFCLK
Low-Level Input Voltage	V_{IL}			0.7	V	
High-Level Input Voltage	V_{IH}	1.1			V	
Input Leakage	I_L	-10		10	µA	
Input Capacitance	C_{IN}			3	pF	Note 2

Notes:

1. Characterized on samples
2. Design parameter, not tested
3. I_{OL} is configurable to four levels of sink current.
4. I_{OH} is configurable to four levels of source current.

7.6. AC Specifications

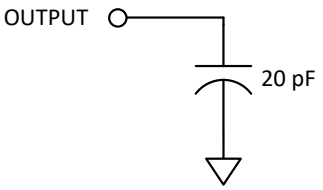
This section details the various AC timing specifications of the device. All parameters are tested unless otherwise noted.

Note: The Ethernet TRXP/TRXN pin timing adheres to *IEEE Std 802.3-2022*. Refer to Clause 147 of the *IEEE Std 802.3-2022* specification for detailed Ethernet timing information.

7.6.1. Equivalent Test Load

Output timing specifications assume a 20 pF equivalent test load, unless otherwise noted, as illustrated below.

Figure 7-1. Output Equivalent Test Load



7.6.2. General Signals and Clocks

Table 7-9. AC Electrical Characteristics (other than Ethernet PMA)

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
VO-VDDP Type Output Buffers						
Output Rise Time (10% to 90%)	t_r		23		ns	Low drive
			8		ns	Medium-low drive
			5		ns	Medium-high drive
			3		ns	High drive
Output Fall Time (90% to 10%)	t_f		23		ns	Low drive
			8		ns	Medium-low drive
			5		ns	Medium-high drive
			3		ns	High drive
VODL-VDDP Type Output Buffers						
Output Fall Time (90% to 10%)	t_f		23		ns	Low drive
			7		ns	Medium-low drive
			5		ns	Medium-high drive
			3		ns	High drive
VOH-VDDP Type Output Buffers						
Output Rise Time (10% to 90%)	t_r		10		ns	Low drive
			5		ns	Medium-low drive
			4		ns	Medium-high drive
			3		ns	High drive
Output Fall Time (90% to 10%)	t_f		10		ns	Low drive
			5		ns	Medium-low drive
			4		ns	Medium-high drive
			3		ns	High drive

Table 7-9. AC Electrical Characteristics (other than Ethernet PMA) (continued)

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
VODH-VDDAU Type Output Buffers						
Output Rise Time (10% to 90%)	t_r		27		ns	

7.6.3. Power-On Configuration Strap Timing

The timing diagram below illustrates the configuration strap timing requirements, in relation to power-on, for applications where RESET_N is not used at power-on. The operational level (V_{opp}) for the external power supply is defined as the minimum operational supply voltage as detailed in the Operating Conditions section.

Figure 7-2. Power-On Configuration Strap Timing

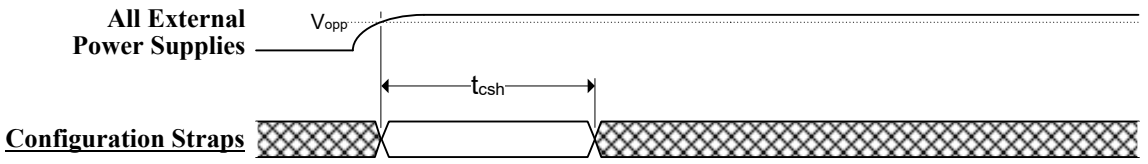


Table 7-10. Power-On Configuration Strap Timing

Description	Symbol	Min	Typ	Max	Units	Additional Information
Configuration strap hold after external power supply at operational level	t_{csh}	4			ms	Note 1
Note: 1. Design parameter, not tested						

7.6.4. RESET_N Configuration Strap Timing

The following diagram illustrates the RESET_N timing requirements and its relation to the configuration straps. Assertion of RESET_N is not a requirement. However, if used, it must be asserted for the minimum period specified.

Figure 7-3. RESET_N Configuration Strap Timing

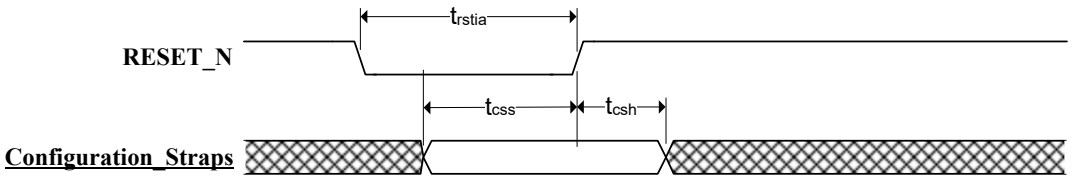


Table 7-11. RESET_N Configuration Strap Timing

Description	Symbol	Min	Typ	Max	Units
RESET_N input assertion time	t_{rstia}	5			µs
Configuration strap setup before RESET_N negation	t_{css}	200			ns
Configuration strap hold after RESET_N negation	t_{csh}	10			ns

7.6.5. Power Sequence Timing

Power supplies must adhere to the following rules:

- The VDDA supply must never be powered without VDDAU also powered.
- The VDDA supply must never exceed the VDDAU supply by more than 0.5 V.
- There is no power-up sequencing requirement, however all power supplies must reach operational levels within the time periods specified in Table 7-12.
- There is no power-down sequencing or timing requirement for VDDP relative to VDDA, however VDDA must not be powered for an extended period of time without VDDP also at operational levels.
- Following initial power-on, or if a power supply brownout occurs (i.e., either of the VDDA or VDDP supplies drops below operational limits), an internal power-on reset will be performed once all power supplies reach operational levels. Refer to the section Power-On Configuration Strap Timing for power-on reset requirements.
- Do not drive input signals without power supplied to the device.

Attention: Violation of these specifications may damage the device.

Figure 7-4. Power Sequence Timing

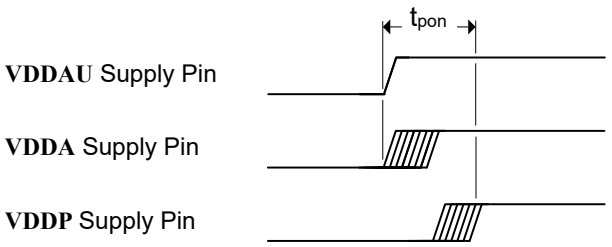


Table 7-12. Power Sequence Timing

Description	Symbol	Min	Typ	Max	Units	Additional Information
VDDP supply turn-on time relative to VDDA	t_{pon}	0		5	ms	Note 1

Note:
1. Design parameter, not tested.

Related Links

Power-On Configuration Strap Timing

7.6.6. MII/SC-MII Timing

This section specifies the MII/SC-MII transmit and receive timing. Note that timing was designed for system load between 5 pF and 20 pF.

Figure 7-5. MII/SC-MII Transmit Timing

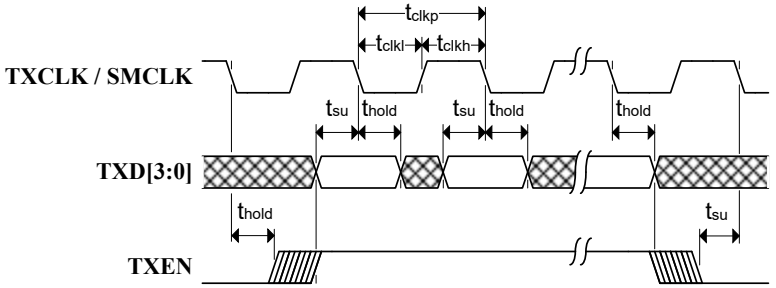


Table 7-13. MII/SC-MII Transmit Timing

Description	Symbol	Min	Typ	Max	Units	Additional Information
TXCLK/SMCLK period	t_{clkp}		400		ns	Note 1
TXCLK/SMCLK high time	t_{clkh}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns	Note 1
TXCLK/SMCLK low time	t_{clkl}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns	Note 1
TXD[3:0], TXEN setup time to falling edge of TXCLK/SMCLK	t_{su}	26.0			ns	
TXD[3:0], TXEN hold time after falling edge of TXCLK/SMCLK	t_{hold}	0			ns	

Note:
1. Design parameter, not tested

Figure 7-6. MII/SC-MII Receive Timing

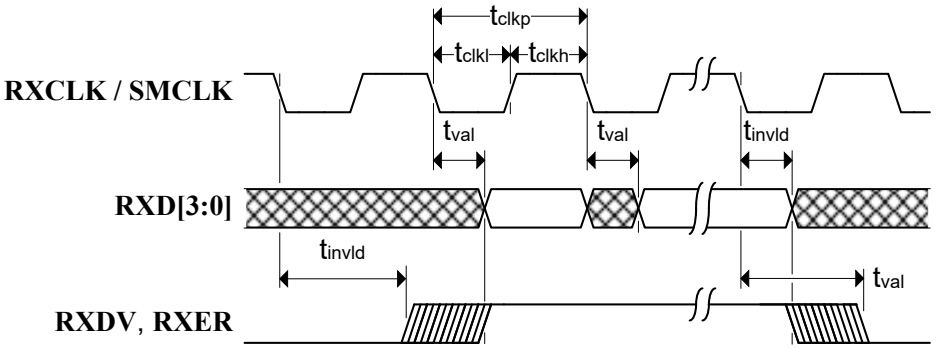


Table 7-14. MII/SC-MII Receive Timing

Description	Symbol	Min	Typ	Max	Units	Additional Information
RXCLK/SMCLK period	t_{clkp}		400		ns	Note 1
RXCLK/SMCLK high time	t_{clkh}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns	Note 1
RXCLK/SMCLK low time	t_{clkl}	t_{clkp} * 0.4		t_{clkp} * 0.6	ns	Note 1
RXD[3:0], RXDV, RXER output valid from falling edge of RXCLK/SMCLK	t_{val}			28.0	ns	
RXD[3:0], RXDV, RXER output invalid from falling edge of RXCLK/SMCLK	t_{invld}	10.0			ns	

Note:
1. Design parameter, not tested

7.6.7. RMII Timing

This section specifies the RMII interface transmit and receive timing.

In this mode, a 50 MHz clock must be input on the REFCLKIN pin. Refer to the *RMII Clock Source - 50 MHz Oscillator* section for additional clock details.

Note: The CRSDV pin performs both carrier sense and data valid functions. CRSDV is asserted asynchronously on detection of carrier due to the criteria relevant to the operating mode. If the PHY has additional bits to be presented on RXD[1:0] following the initial negation of CRSDV, then the device will assert CRSDV on cycles of REFCLKIN which present the second di-bit of each nibble and negate CRSDV on cycles of REFCLKIN which present the first di-bit of a nibble. For additional information, refer to the *RMII Specification*.

Figure 7-7. RMII Timing

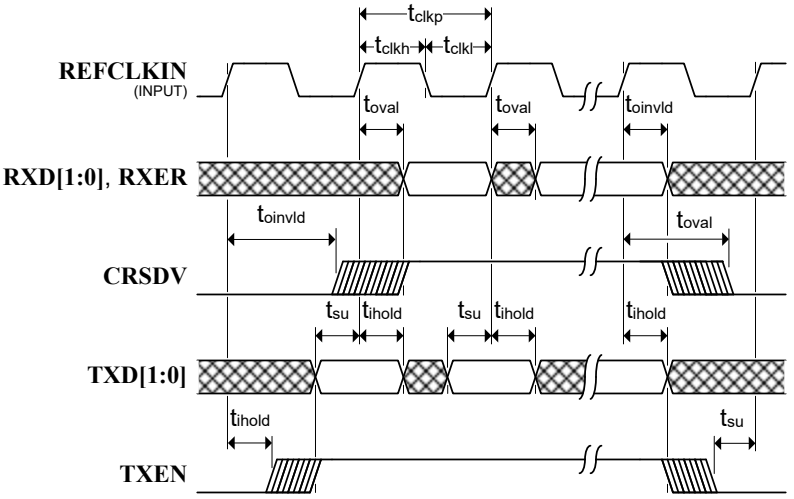


Table 7-15. RMII Timing

Description	Symbol	Min	Typ	Max	Units	Additional Information
REFCLKIN period	t_{clkp}		20		ns	Note 1
REFCLKIN high time	t_{clkh}	t_{clkp} * 0.45		t_{clkp} * 0.55	ns	Note 1, 2
REFCLKIN low time	t_{clkl}	t_{clkp} * 0.45		t_{clkp} * 0.55	ns	Notes 1, 2
RXD[1:0], RXER, CRSDV output valid from rising edge of REFCLKIN	t_{oval}			12	ns	
RXD[1:0], RXER, CRSDV output invalid from rising edge of REFCLKIN	t_{oinvld}	3.0			ns	
TXD[1:0], TXEN setup time to rising edge of REFCLKIN	t_{su}	4.0			ns	
TXD[1:0], TXEN hold time after rising edge of REFCLKIN	t_{ihold}	1.5			ns	

Notes:
1. Design parameter, not tested.
2. 1.8V 50 MHz clock input on REFCLKIN

Note: Timing was designed for system load between 5 pF and 20 pF.

Related Links

RMII Clock Source - 50 MHz Oscillator

7.6.8. SMI Timing

This section specifies the serial management interface timing of the device.

Figure 7-8. SMI Timing

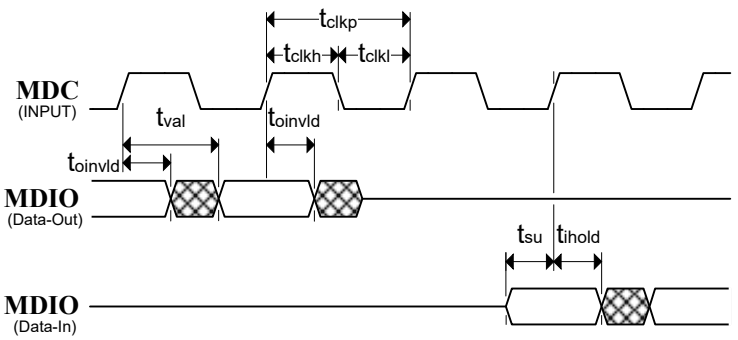


Table 7-16. SMI Timing

Description	Symbol	Min	Typ	Max	Units
MDC period	t_{clkp}	250			ns
MDC high time	t_{clkh}	t_{clkp} * 0.4			ns
MDC low time	t_{clkl}	t_{clkp} * 0.4			ns
MDIO (read from PHY) output valid from rising edge of MDC	t_{val}			130	ns
MDIO (read from PHY) output invalid from rising edge of MDC	t_{oinvld}	0			ns
MDIO (write to PHY) setup time to rising edge of MDC	t_{su}	10			ns
MDIO (write to PHY) input hold time after rising edge of MDC	t_{ihold}	10			ns

7.6.9. 10BASE-T1S PMA Electrical Characteristics

This section contains electrical characteristics of the TRXP/TRXN pins to enable the design of 10BASE-T1S devices compliant to IEEE Std 802.3-2022 Clause 147.

7.6.9.1. 10BASE-T1S PMA Transmitter Characteristics

Table 7-17. 10BASE-T1S PMA Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
Differential driver output	V_{od}	0.8	1.0	1.2	V_{pp}	Figure 7-9
Cycle-to-cycle jitter	$t_{j(c-c)}$		0.65	1.2	ns	Note 1 Figure 7-9
Rise time, Fall time (20%-80%)	t_{rtx}, t_{ftx}	7.9		14.75	ns	Note 1 Figure 7-10
Droop		0		13	%	Note 1 Figure 7-9

Note:
1. C = Characterized on samples

Figure 7-9. Differential Output Test Fixture

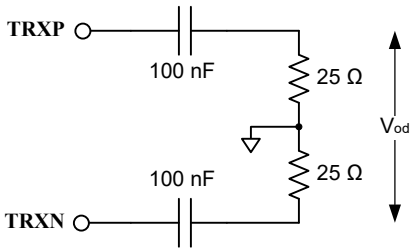
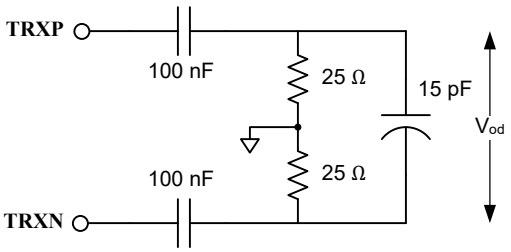
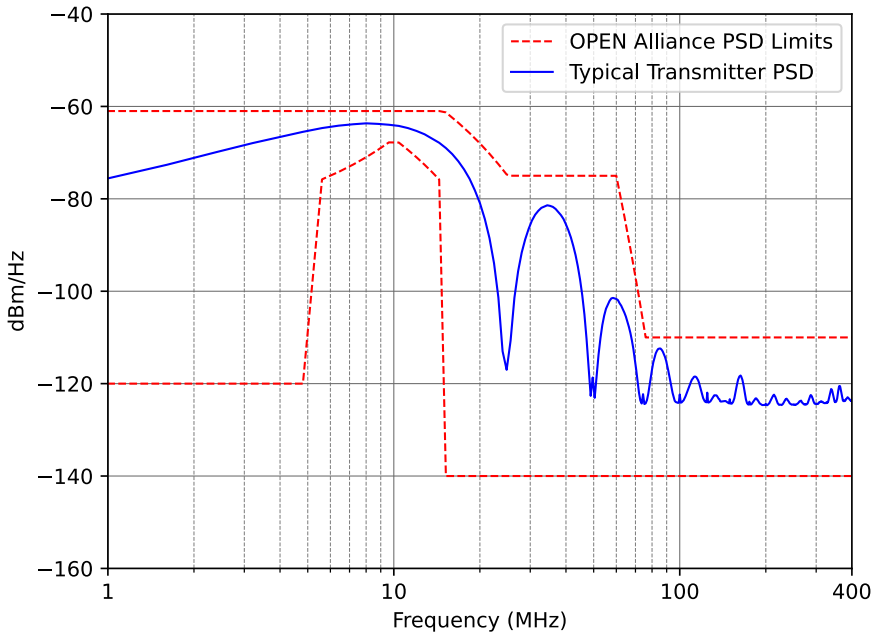


Figure 7-10. Transmitter Output Rise/Fall Test Fixture



Power spectral density was measured in a multidrop configuration (50 Ω termination) as shown in Figure 7-9 with the transmitter in the IEEE Transmitter PSD mask test mode 3. The upper and lower limits shown are as proposed by the OPEN Alliance *10BASE-T1S System Implementation Specification*, Version 1.0.

Figure 7-11. Transmitter Power Spectral Density (Typical)



Topology Discovery - Rev D0

The following section describes the Topology Discovery timing and behavior for devices using silicon revision D0 and later.

Figure 7-12. Topology Discovery Signal Characteristics - Rev D0

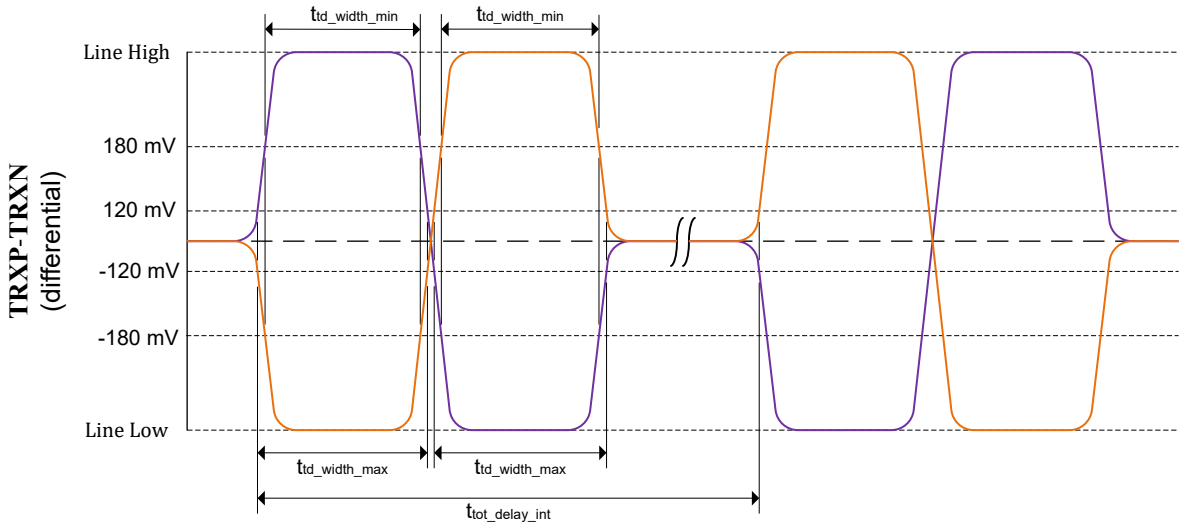


Table 7-18. Signal Characteristics during Topology Discovery - Rev D0

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
Topology Discovery Pulse width Maximum	$t_{td\_width\_max}$	40	80	91	ns	Note 1
Topology Discovery Pulse width Minimum	$t_{td\_width\_min}$	77	84	92	ns	Note 1
Internal loopback delay	$t_{tot\_delay\_int}$	125	170	260	ns	Note 1

Note:
1. C = Characterized on samples

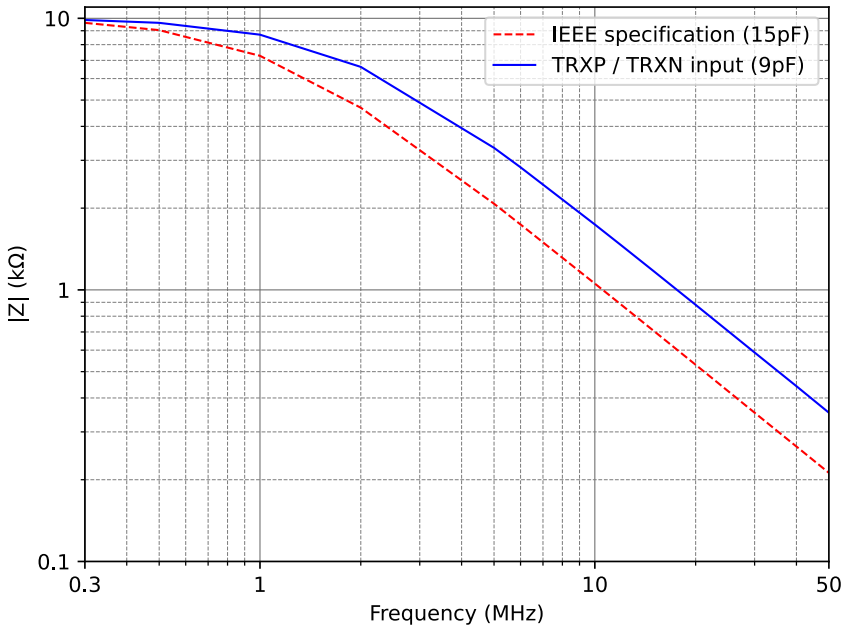
7.6.9.2. 10BASE-T1S PMA Receiver Characteristics

Table 7-19. 10BASE-T1S PMA Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Additional Information
Receiver differential sensitivity	V_{th}		0		mV	
Single-ended Input Resistance	R_{SE}		5.4	6	kΩ	Note 1
Differential Input Resistance	R_{DIFF}		14.5		kΩ	Note 1
Differential input Capacitance	C_{DIFF}	6.5		8.5	pF	20 MHz Note 1
Common Mode Voltage Range	V_{CM}	-30		+30	V_{pp}	2 MHz Note 1

Note:
1. C = Characterized on samples

Figure 7-13. Differential Input Impedance (Typical)



7.6.10. Wake-up Signal Characteristics and Timing - Rev C2

Note: This section describes the timing and behavior for LAN8670/1 revision C2 and earlier.

The following diagram illustrates the behavior and timing characteristics as the device wakes from sleep.

Figure 7-14. Wake Signal Timing (Rev C2)

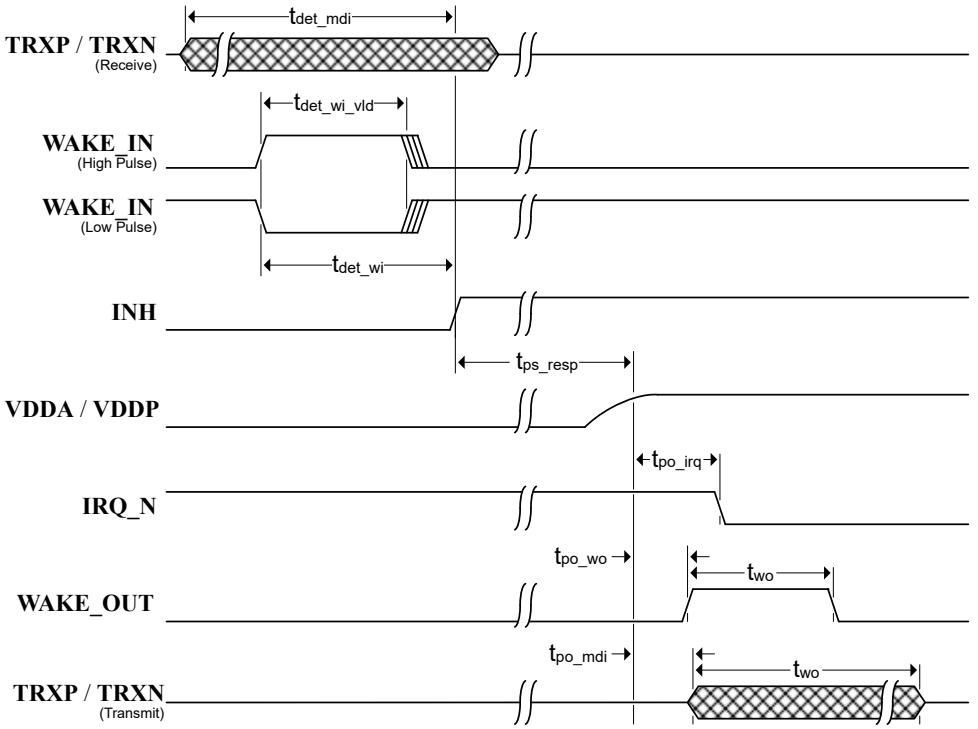


Table 7-20. 10BASE-T1S PMA Receiver Wake Signal Characteristics (Rev C2)

Description	Symbol	Min	Typ	Max	Units	Additional Information
MDI wake response time	t_{det_mdi}	250		450	µs	Note 1
MDI wake signal threshold	V_{thresh_mdi}	100		700	mV_{pp}	Note 2

Notes:

1. The device will not wake if the signal duration is less than or equal to the minimum value of t_{det_mdi}. It will wake if the signal duration is greater than or equal to the maximum value of t_{det_mdi}. The behavior is undefined for signal duration between these limits.
2. The device will not wake if the signal amplitude is less than or equal to the minimum V_{thresh_mdi}. It will wake if the signal amplitude is greater than or equal to the maximum value V_{thresh_mdi}. The behavior is undefined for amplitudes between these limits.

Table 7-21. WAKE_IN Signal Characteristics (Rev C2)

Description	Symbol	Min	Typ	Max	Units	Additional Information
WAKE_IN response time	t_{det_wi}		33	40	µs	Note 1
WAKE_IN detection time	$t_{det\_wi\_vld}$	15	22	40	µs	Notes 2, 3

Notes:

1. Measured from WAKE_IN active edge to INH assertion.
2. The device will not wake if the signal duration is less than or equal to the minimum value of t_{det_wi}. It will wake if the signal duration is greater than or equal to the maximum value of t_{det_wi}. The behavior is undefined for signal duration between these limits.
3. The WAKE_IN pin is a standard VI-VDDAU type input buffer. See the section DC Electrical Characteristics (other than 10BASE-T1S PMA) for details.

Table 7-22. Wake Signal Time (Rev C2)

Description	Symbol	Min	Typ	Max	Units	Additional Information
IRQ_N assertion time after all power supplies valid	t_{po_irq}		6.6		µs	
MDI wake forward signaling activity start after all power supplies valid	t_{po_mdi}		2		µs	
WAKE_OUT wake forward assertion time after all power supplies valid	t_{po_wo}		1.8		µs	
WAKE_OUT pulse width	t_{wo}		90		µs	
MDI wake signaling time	t_{wk_mdi}		1		ms	
Power supply response time	t_{ps_resp}	Application Specific				Notes 1, 2

Notes:

1. The power supply response time is the length of time from the power supplies being enabled by INH being driven high to the time the VDDP and VDDA supplies are high enough to release the internal power-on reset circuits. This time is dependent upon the implementation of the external power supply circuits and therefore is implementation specific.
2. The VDDP and VDDA supplies **must** be disabled after entering sleep mode prior to a wake event.

Related Links

DC Specifications (other than 10BASE-T1S PMA)

7.6.11. Wake-up Signal Characteristics and Timing - Rev D0

Note: This section describes the timing and behavior for LAN8670/1 revision D0.

The following diagram illustrates the timing characteristics as the device wakes from sleep.

Figure 7-15. Wake Signal Timing (Rev D0)

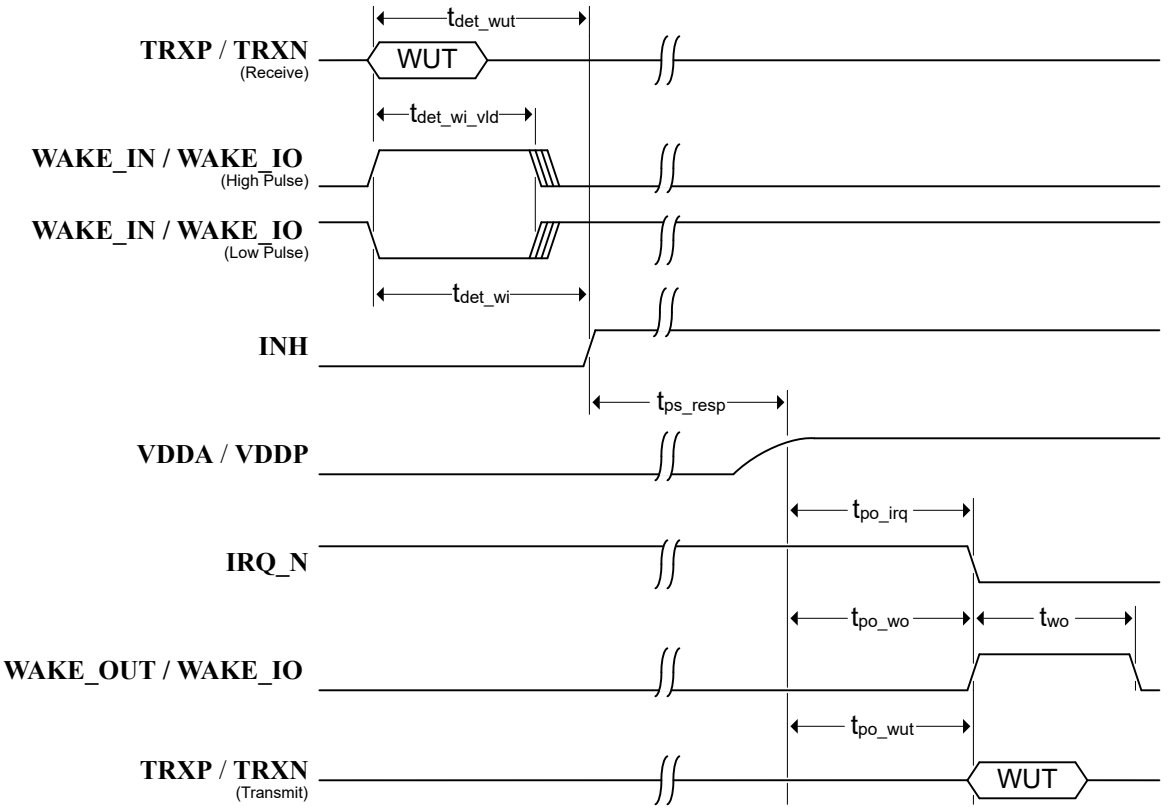


Table 7-23. 10BASE-T1S PMA Receiver Wake Signal Characteristics

Description	Symbol	Min	Typ	Max	Units	Additional Information
MDI wake-up tone (WUT) response time	t_{det_wut}	30		45	µs	Note 1
MDI wake-up tone (WUT) signal threshold	V_{thresh_wut}	100		750	mV_{pp}	Note 2

Notes:

1. Measured from the start of 625 kHz tone to INH assertion.
2. The device will not wake if the WUT signal amplitude is less than or equal to the minimum V_{thresh_wut}. It will wake if the signal amplitude is greater than or equal to the maximum value V_{thresh_wut}. The behavior is undefined for amplitudes between these limits.

Table 7-24. WAKE_IN / WAKE_IO Input Signal Characteristics

Description	Symbol	Min	Typ	Max	Units	Additional Information
WAKE_IN / WAKE_IO response time	t_{det_wi}		39	45	µs	Note 1
WAKE_IN / WAKE_IO detection time	$t_{det\_wi\_vld}$	15	23	40	µs	Notes 2, 3

Notes:

1. Measured from WAKE_IN active edge to INH assertion.
2. The device will not wake if the signal duration is less than or equal to the minimum value of $t_{det\_wi\_vld}$. It will wake if the signal duration is greater than or equal to the maximum value of $t_{det\_wi\_vld}$. The behavior is undefined for signal duration between these limits.
3. The WAKE_IN pin is a standard VI-VDDAU type input buffer. See the section *DC Electrical Characteristics (other than 10BASE-T1S PMA)* for details.

Table 7-25. Wake Signal Time

Description	Symbol	Min	Typ	Max	Units	Additional Information
IRQ_N assertion time after all power supplies valid	t_{po_irq}		900		µs	
MDI wake-up tone (WUT) forward signaling activity start after all power supplies valid	t_{po_wut}		900		µs	Note 1
WAKE_OUT / WAKE_IO wake forward assertion time after all power supplies valid	t_{po_wo}		900		µs	
WAKE_OUT / WAKE_IO pulse width	t_{wo}		90		µs	
Power supply response time	t_{ps_resp}	Application Specific				Notes 2, 3

Notes:

1. The WUT forwarding latency will depend on PLCA or other network traffic.
2. The power supply response time is the length of time from the power supplies being enabled by INH being driven high to the time the VDDP and VDDA supplies are high enough to release the internal power-on reset circuits. This time is dependent upon the implementation of the external power supply circuits and therefore is implementation specific.
3. The VDDP and VDDA supplies are not required to be disabled after entering sleep mode prior to a wake event. However, if the supplies are disabled then the device must be re-configured upon wake.

7.7. Clock Circuit

For MII and SC-MII operation, the LAN8670 and LAN8672 require a 25 MHz clock source, either a crystal or single-ended clock oscillator. For RMII operation, the LAN8670 and LAN8671 require a 50 MHz single-ended clock oscillator. In all cases, the clock source must be ± 100 ppm or better tolerance.

7.7.1. MII/SC-MII

7.7.1.1. Crystal Specifications

In MII and SC-MII modes, a 25 MHz crystal can be placed between XTO and XTI. This crystal should meet the requirements in Table 7-26 below.

Table 7-26. Recommended Crystal Specifications

Parameter	Min	Typ	Max	Units	Notes
Crystal Cut		AT (typical)			
Crystal Oscillation Mode		Fundamental			
Crystal Calibration Mode		Parallel Resonant Mode			
Frequency		25.000		MHz	
Tolerance			±100	ppm	Note 1, 2
Recommended Maximum Shunt Capacitance			6	pF	
Recommended Load Capacitance		10-22		pF	Note 3
Drive Level		50		µW	
Recommended Maximum Equivalent Series Resistance (ESR)			100	Ω	
XTI/XTO Pin Capacitance		2		pF	Note 4

Notes:

1. The total deviation for the transmitter clock frequency is specified by IEEE Std 802.3-2022 Clause 147 as ±100 ppm.
2. This parameter must include increased variation over the expected operational lifetime of the application (aging), temperature, and load capacitance.
3. Load capacitance per crystal terminal. The terminals should each see the same load.
4. This number includes the pad, the bond wire and the lead frame. Printed circuit board trace capacitance is not included in this value. The XTI/XTO pin and PCB trace capacitance values are required to accurately calculate the value of the two external load capacitors. These two external load capacitors determine the accuracy of the 25.000 MHz frequency.

7.7.1.2. Oscillator Clock Source - 25 MHz Oscillator

In MII/SC-MII mode, a 25 MHz single-ended clock oscillator input with a nominal 1.8V or 3.3V clock signal may be driven onto XTI instead of using a crystal resonator. This clock must meet the requirements in the following table.

Note: When operating the MII/SC-MII interface with an oscillator clock source, only industrial grade Ambient Operating Temperatures (T_A -40°C to +85°C) are guaranteed, refer to the Operating Conditions section.

Table 7-27. MII/SC-MII Oscillator Timing Requirements

Parameter	Min	Typ	Max	Units	Notes
XTI frequency		25		MHz	
XTI Frequency Stability			±100	ppm	Including aging
XTI Duty Cycle	45		55	%	
XTI Jitter			840	ps	peak-to-peak (not RMS)
XTI rise/fall time			1.5	ns	

Note: The XTO pin must be left unconnected and XTI driven with a nominal 1.8-3.3V clock signal.

7.7.2. RMII Clock Source - 50 MHz Oscillator

In RMII mode, a 50 MHz single-ended clock oscillator input with a nominal 1.8-3.3V clock signal must be driven onto REFCLKIN. This clock must meet the requirements in the following table.

Table 7-28. RMII REFCLKIN Timing Requirements

Parameter	Min	Typ	Max	Units	Notes
REFCLKIN frequency		50		MHz	
REFCLKIN Frequency Stability			±100	ppm	Including aging
REFCLKIN Duty Cycle	45		55	%	
REFCLKIN Jitter			840	ps	peak-to-peak (not RMS)

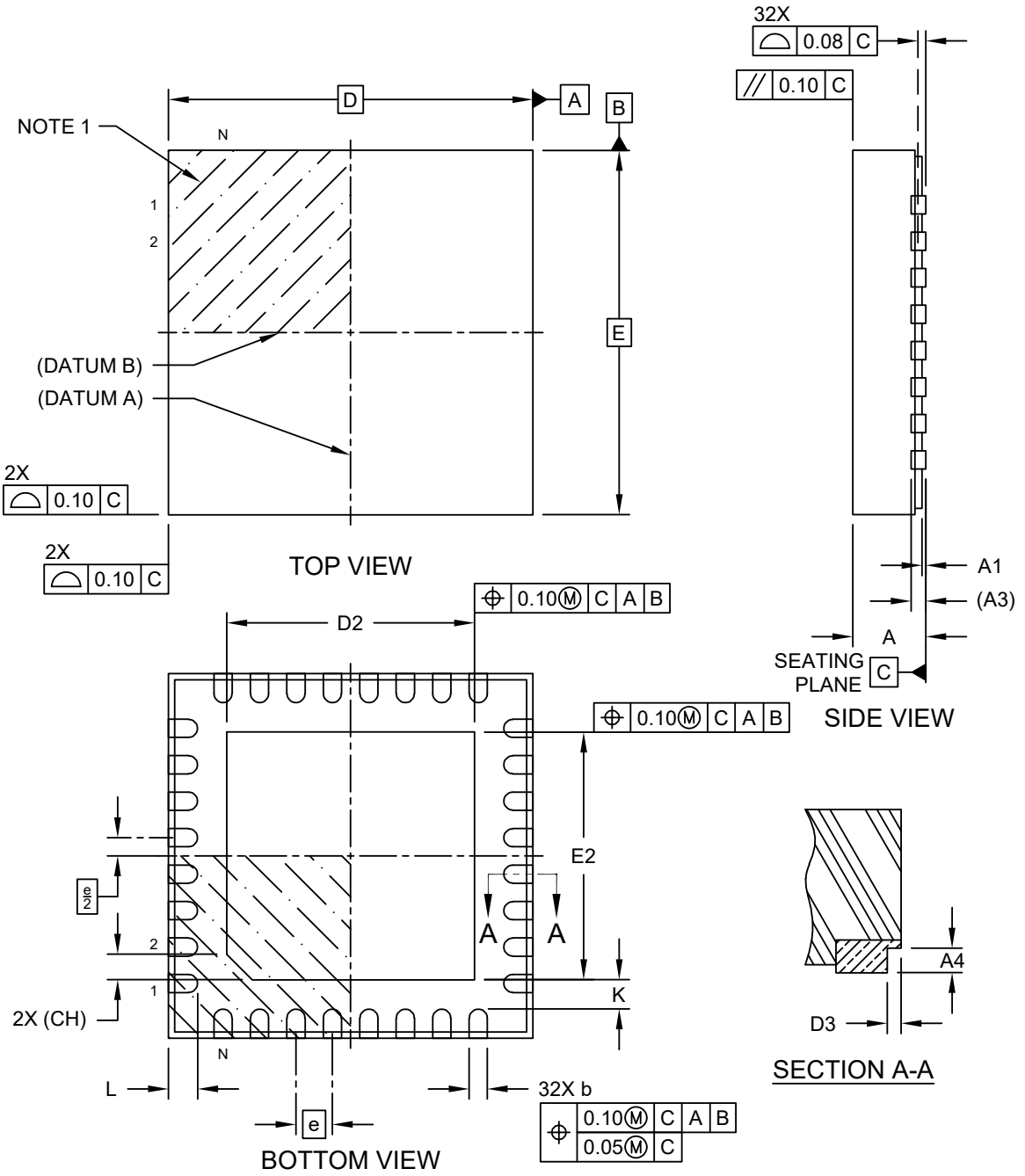
Note: On the LAN8670, XTO should be left unconnected and REFCLKIN (XTI) driven with a nominal 1.8-3.3V clock signal.

8. Packaging Information

8.1. 32-VQFN (LAN8670 Only)

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN]
With 3.4 mm Exposed Pad and Stepped Wettable Flanks

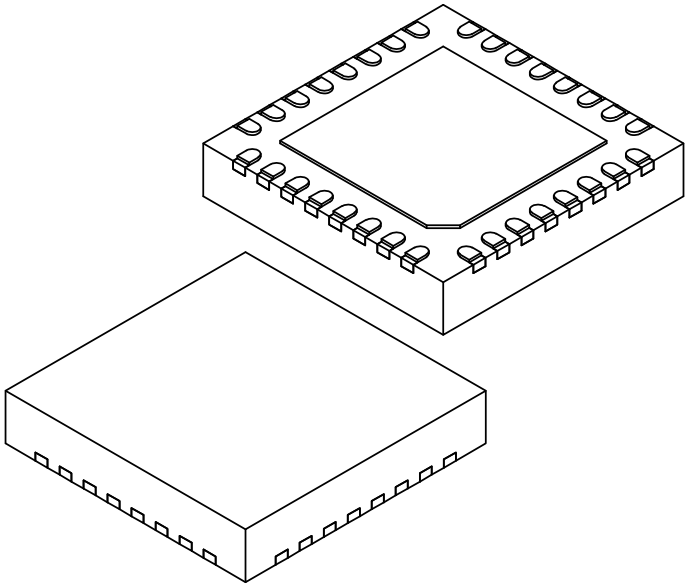
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.30	3.40	3.50
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.30	3.40	3.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-
Exposed Pad Corner Chamfer	CH		0.35 REF	
Step Height	A4	0.10	-	0.19
Step Length	D3	0.035	0.060	0.085

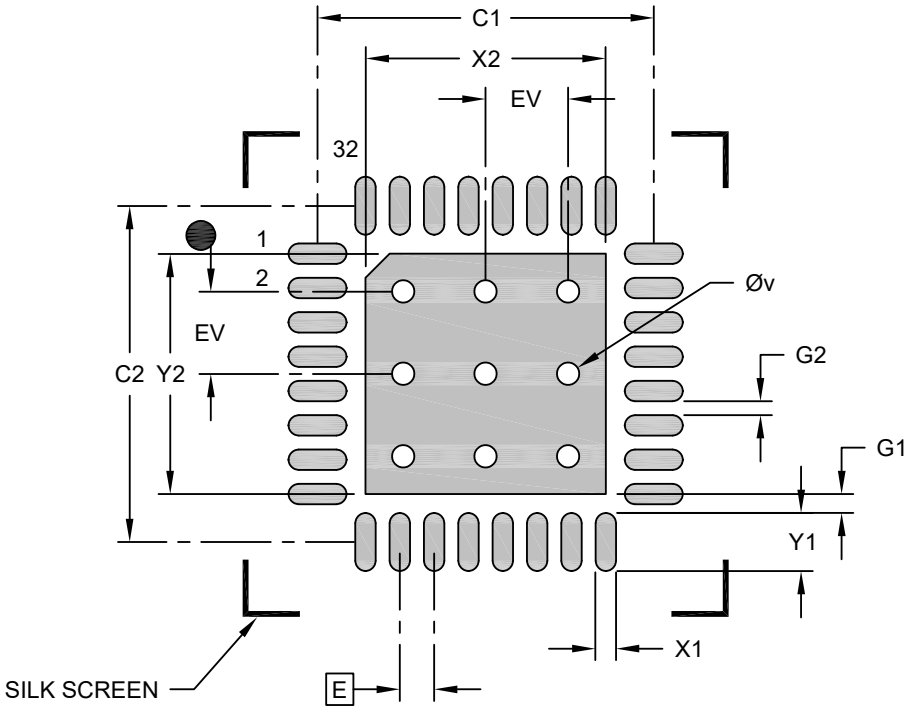
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-500 Rev B Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (LMX) - 5x5x1.0 mm Body [VQFN] With 3.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.50
Center Pad Length	Y2			3.50
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (32)	X1			0.30
Contact Pad Length (32)	Y1			0.85
Contact Pad to Center Pad (32)	G1	0.20		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

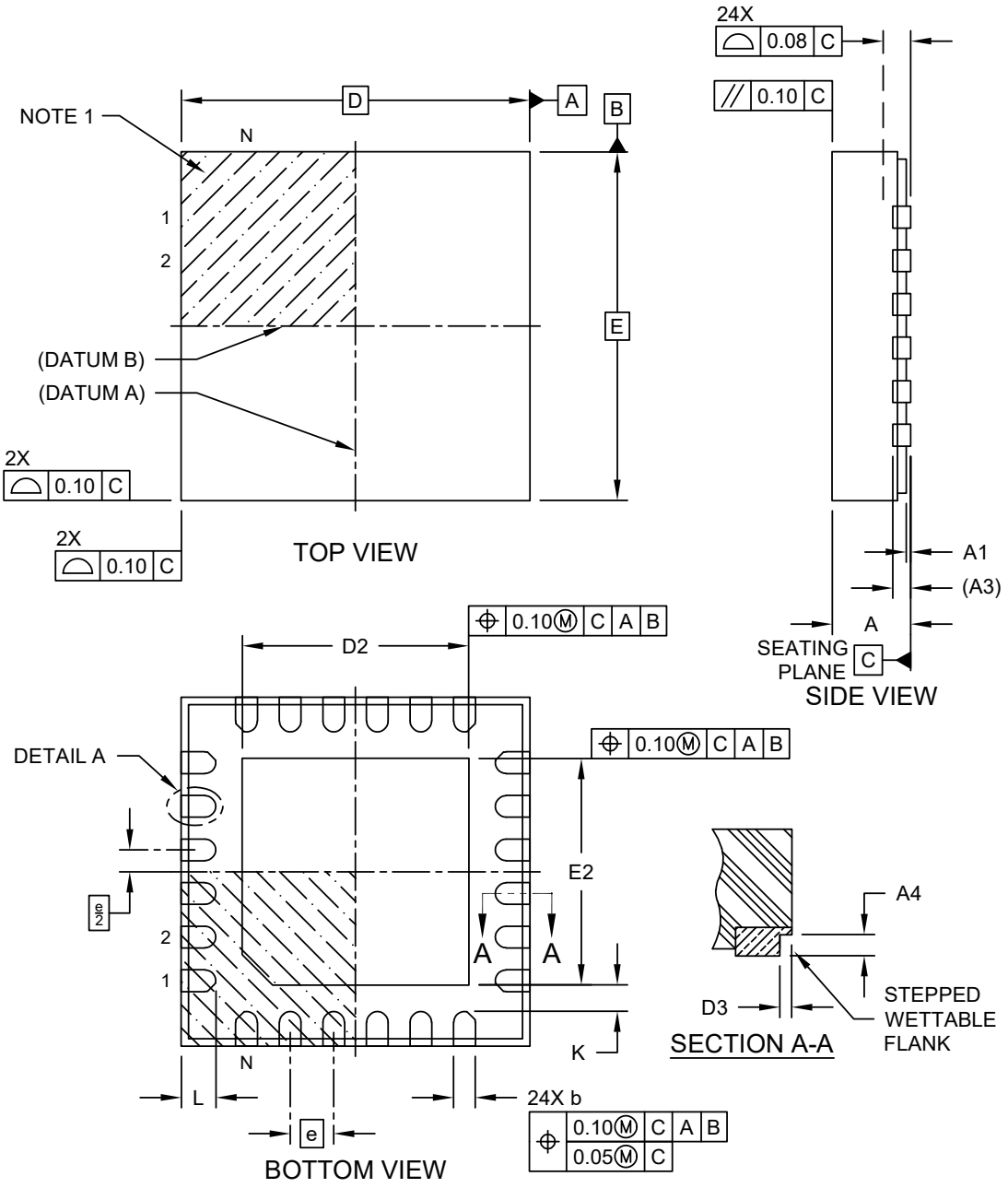
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2500 Rev B

8.2. 24-VQFN (LAN8671 Only)

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

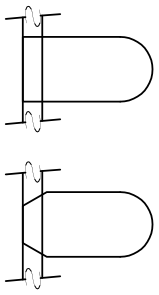
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



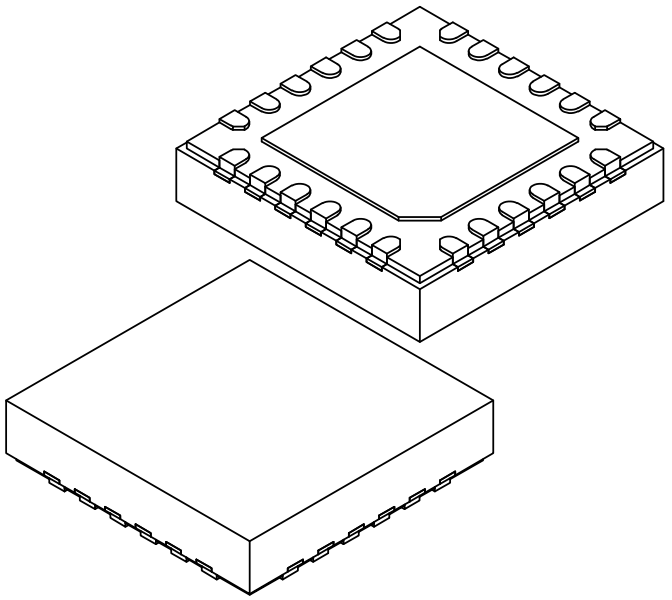
Microchip Technology Drawing C04-21483 Rev B Sheet 1 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		24	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.50	2.60	2.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

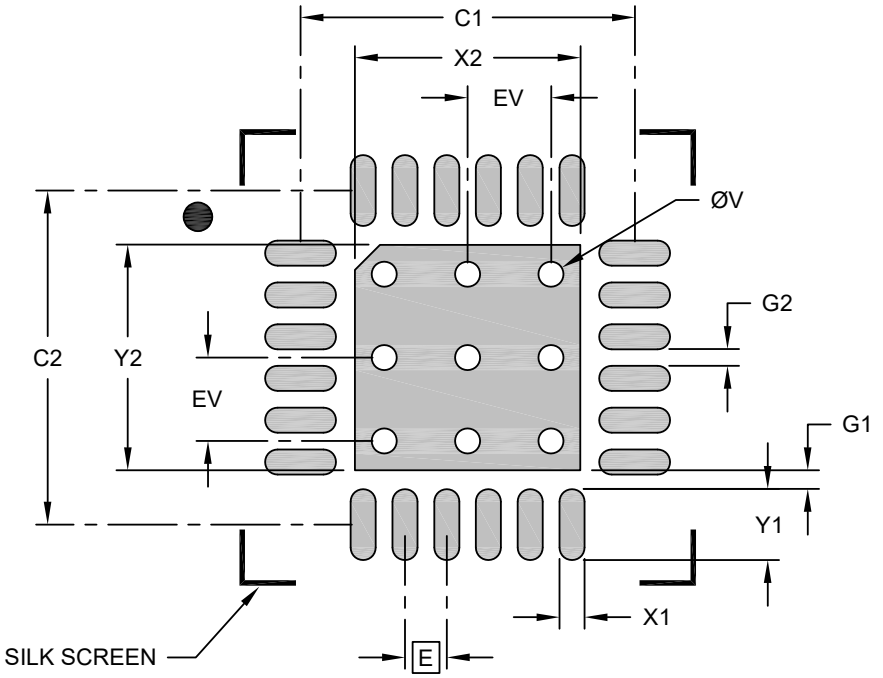
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21483 Rev B Sheet 2 of 2

24-Lead Very Thin Plastic Quad Flat, No Lead Package (U3B) - 4x4 mm Body [VQFN] With 2.6mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZCY

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.70
Optional Center Pad Length	Y2			2.70
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X24)	X1			0.30
Contact Pad Length (X24)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.23		
Contact Pad to Contact Pad (20)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

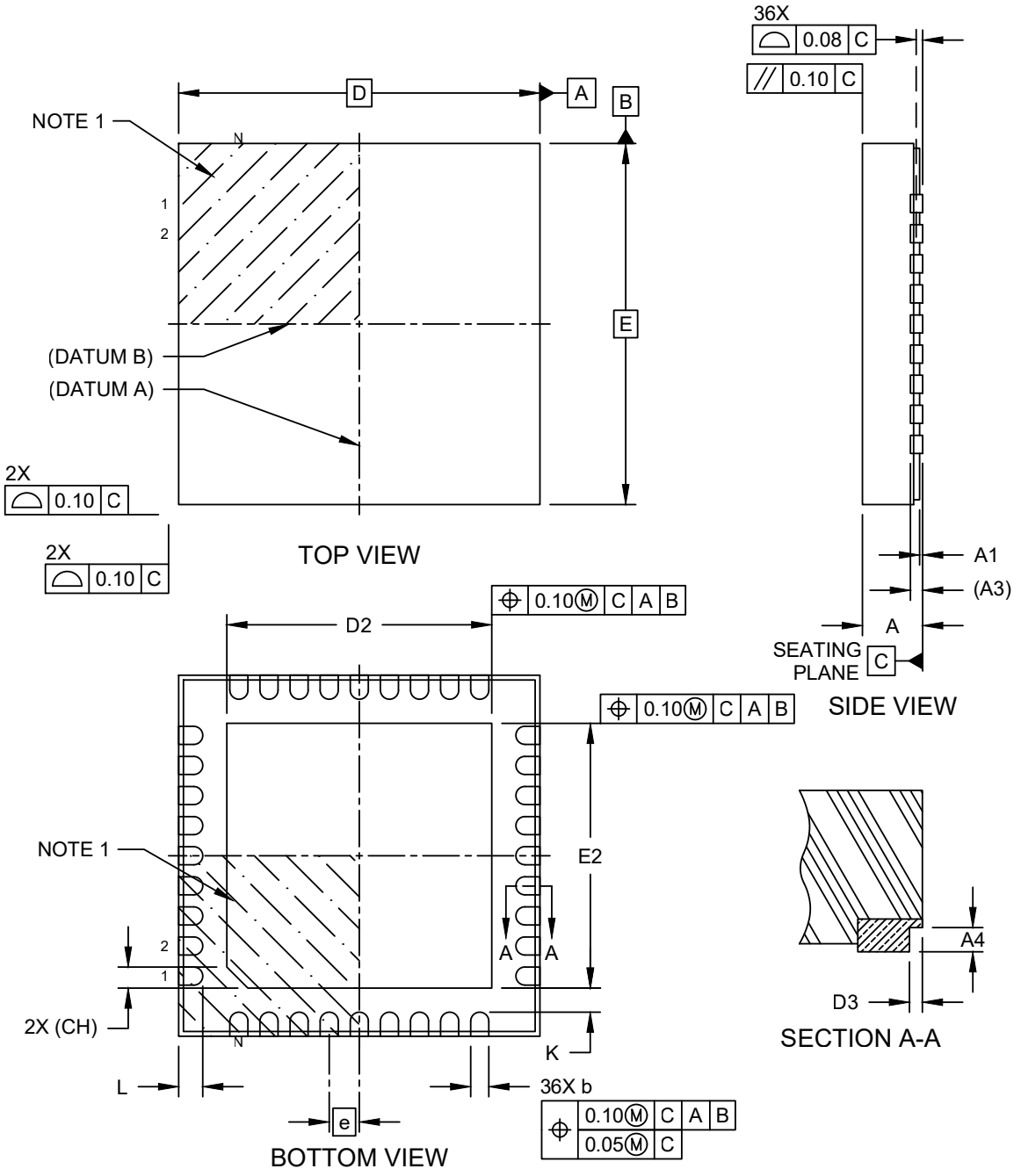
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23483 Rev B

8.3. 36-VQFN (LAN8672 Revision C2 Only)

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

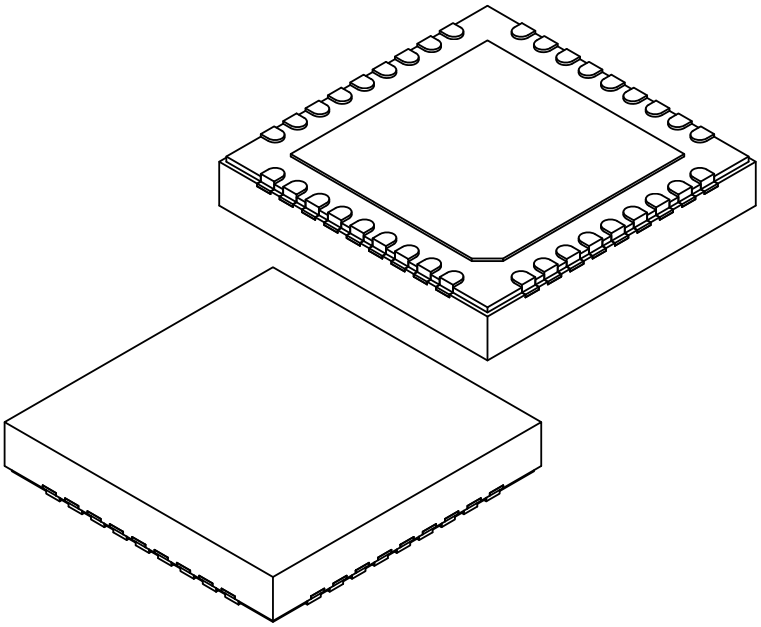
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-00501 Rev C Sheet 1 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	4.30	4.40	4.50
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	4.30	4.40	4.50
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.40	-	-
Exposed Pad Corner Chamfer	CH		0.35 REF	
Step Height	A4	0.10	-	0.19
Step Length	D3	0.035	0.060	0.085

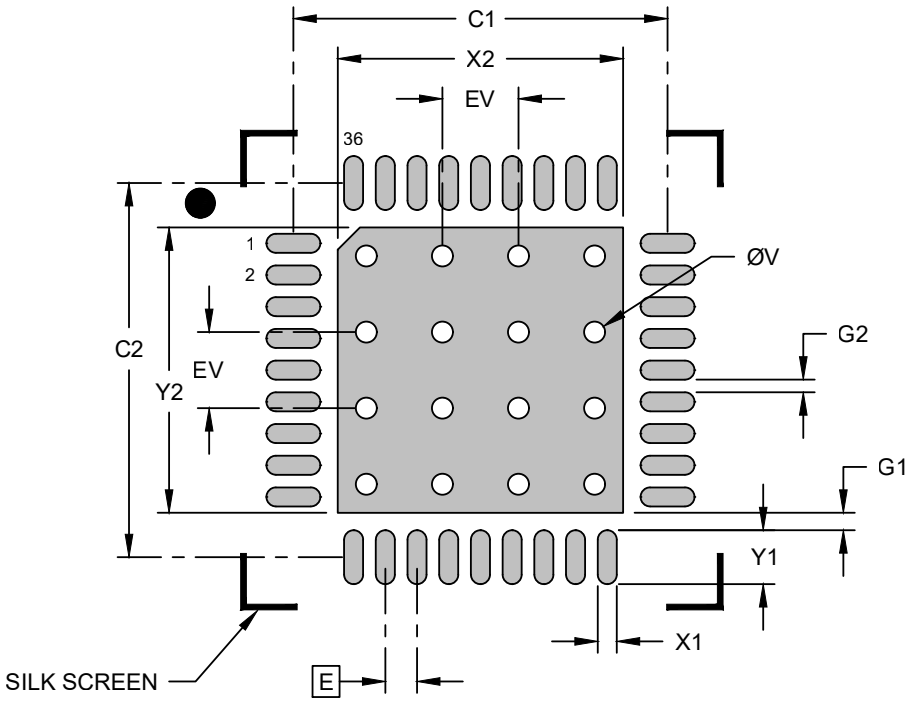
Notes:

1. The Pin 1 visual index feature may vary, but it must be located within the hatched area.
2. The package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
   REF: Reference Dimension, usually without tolerance, is for information purposes only.

Microchip Technology Drawing C04-00501 Rev C Sheet 2 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (LNX) - 6x6x1.0 mm Body [VQFN] With 4.4 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			4.50
Center Pad Length	Y2			4.50
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.85
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. The theoretically exact value is shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during the reflow process.

Microchip Technology Drawing C04-02501 Rev C

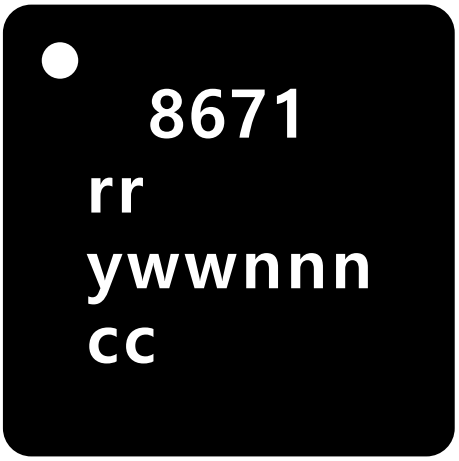
9. Package Marking Information

Figure 9-1. LAN8670 Top Mark

Legend:

LAN8670	Device Identifier
rr	Product Revision Code
yy	last two digits of Assembly Year
ww	Assembly Work Week
nnn	Tracking Number
cc	Country of Origin Abbreviation (optional)
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Figure 9-2. LAN8671 Top Mark



Legend:

8671	Device Identifier (LAN8671)
rr	Product Revision Code
y	last digit of Assembly Year
ww	Assembly Work Week
nnn	Tracking Number
cc	Country of Origin Abbreviation (optional)
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Figure 9-3. LAN8672 Revision C2 Top Mark

Legend:		
	LAN8672	Device Identifier
	rr	Product Revision Code
	yy	last two digits of Assembly Year
	ww	Assembly Work Week
	nnn	Tracking Number
	cc	Country of Origin Abbreviation (optional)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Product Identification System

To order or obtain information, for example, on pricing or delivery, contact Microchip: https://www.microchip.com/en-us/about/contact-us.

PART NO.	XX	[X](1)	-	X	/	XXX	[XXX]
Device	Product Revision	Tape and Reel Option		Temperature Grade		Package Type	Automotive Code

Device:	LAN8670 10BASE-T1S Ethernet PHY Transceiver, MII/SC-MII/RMII LAN8671 10BASE-T1S Ethernet PHY Transceiver, RMII LAN8672 (Revision C2, only) 10BASE-T1S Ethernet PHY Transceiver, MII	
Product Revision:	xx	Two character code specifying product revision
Tape and Reel Option:	Blank	Standard packaging (tray)
	T	Tape and Reel(1)
Temperature Grade:	E	-40ºC to +125ºC Extended range
Package Type:	LMX	32-pin VQFN (LAN8670 only)
	U3B	24-pin VQFN (LAN8671 only)
	LNX	36-pin VQFN (LAN8672 Revision C2, only)
Automotive Code:	Vxx	Optional three character code with "V" prefix specifying automotive product

- LAN8670D0-E/LMXVAO - 10BASE-T1S Ethernet PHY Transceiver, MII/SC-MII/RMII, Revision D0, Standard tray packaging, 32-VQFN package, -40ºC to +125ºC, automotive
- LAN8671D0-E/U3BVAO - 10BASE-T1S Ethernet PHY Transceiver, RMII, Revision D0, Standard tray packaging, 24-VQFN package, -40ºC to +125ºC, automotive
- LAN8670D0T-E/LMX - 10BASE-T1S Ethernet PHY Transceiver, MII/SC-MII/RMII, Revision D0, Tape and Reel packaging, 32-VQFN package, -40ºC to +125ºC
- LAN8670C2-E/LMXVAO - 10BASE-T1S Ethernet PHY Transceiver, MII/SC-MII/RMII, Revision C2, Standard tray packaging, 32-VQFN package, -40ºC to +125ºC, automotive
- LAN8671C2-E/U3BVAO - 10BASE-T1S Ethernet PHY Transceiver, RMII, Revision C2, Standard tray packaging, 24-VQFN package, -40ºC to +125ºC, automotive
- LAN8672C2-E/LNX - 10BASE-T1S Ethernet PHY Transceiver, MII, Revision C2, Standard tray packaging, 36-VQFN package, -40ºC to +125ºC
- LAN8670C2T-E/LMX - 10BASE-T1S Ethernet PHY Transceiver, MII/SC-MII/RMII, Revision C2, Tape and Reel packaging, 32-VQFN package, -40ºC to +125ºC

Note:

1. Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Data Sheet Revision History

Table 11-1. Data Sheet Revision History

Revision Level & Date	Section/Figure/Entry	Correction
DS60001573K (Oct-2025)		
	4.13	Updated sleep description for Rev D
	4.15	Added SQI for Rev D
	4.17	Added Topology Discovery for Rev D
	4.19	Added Link Status Overview for Rev D
	5.1, 5.4	Added various registers for Rev D
	7.6.9.1	Added PMA Transmitter Characteristics for Topology Discovery in Rev D
	7.6.11	Added Wake-up Signal Characteristics and Timing Rev D
	7.6.7	Reduce RMII t_{oval} maximum from 16 ns to 12 ns
DS60001573J (Mar-2025)	1.1	Added SSD (Start-of-Stream Delimiter)
		Corrected alphabetical order of entries
	1.4	Updated reference documents
		Corrected links to reference documents
	2.1	Updated reference to IEEE 802.3
		Added reference to RMII patent number
	2.3	Clarified power supply isolation when sleep mode is not required
	3.4	Clarified behavior of pins during reset
	3.5.1	Clarified MODE strap pin requirements for LAN8670 and LAN8672 (Datasheet Clarification d6)
	4.7.2	Clarified section to show that REFCLKIN is not required prior to reset, only after reset for device to function
	4.8	Corrected register name and bit name
	4.8.5 to 4.16.4	Moved section 4.8.5 Transmit Collisions to 4.16.4
	Fig. 4-10	Corrected direction of MDC line
	4.12.3, Fig. 4-9,	Correct start of delay measurement for PTP timestamping
	4.14	Clarified that SQI can be taken over all received data
	4.15	Added info about cable fault diagnostics algorithm.
	5.1.3, 5.1.4	Reworded OUI description
	5.1, 5.2, 5.3, 5.4	Modified wording for reserved register access
	5.1.7	Explained bitfield MITYP is only valid for LAN8670 (Datasheet Clarification d7), plus minor wording changes to improve clarity.
	5.4.8	Fixed a typo incorrectly stating the wrong voltage
	PLCA Reconciliation Sublayer Control 1 Register	Removed Register
	PLCA Reconciliation Sublayer Status Register	Removed Register
	PLCA Cycle Skip Register	Removed Register
	Credit Based Shaper Slope Control Register (5.4.33)	Corrected width of bit-fields

Table 11-1. Data Sheet Revision History (continued)

Revision Level & Date	Section/Figure/Entry	Correction
	Sleep Control 1 Register (5.4.45)	Removed bits 3 and 4, which were erroneously included
	6.6	Added PLCA Collision Detection
	Fig. 6-9 - 6-18	Updated figures to show that the schematic is not dependent on silicon revision
	7.1	Remove reference to IBEE CAN EMC ratings
DS60001573H (Dec-2023)		Update for silicon revision 5 (product revision C2)
	6.4	Clarify Power Connectivity
	3.4, 4.7.2, 7.1, 7.2, 7.5, 7.6.7, 7.7.2	Clarify REFCLKIN 1.8V/3.3V support and duty cycle range
	3.4, 3.5	Clarify need for configuration strap pull-up/down resistors
DS60001573G (Jul-2023)	All	Update for silicon revision 4 (product revision C1)
DS60001573F (Jun-2023)	All	Update for silicon revision 4 (product revision C1)
DS60001573C (Jun-2021)	3	Separating unused pins that are internally connected (DNC) from those which are internally unconnected (NC)
	7.5	Updated VIS-VDDP input hysteresis; VO-VDDP, VOH-VDDP output high level drive currents; ICLK input voltage limits
	7.6.2	Updated typical rise/fall times
	7.6.6	Updated MII TXD/TXEN setup time
	7.6.7	Updated RMII RXD/RXER/CRSDV output valid time
	7.7	Updated 10BASE-T1S PMA Electrical Characteristics
	7.1	Updated ESD Machine Model rating
	4.7	Added initialization and configuration sequence
	4.9.2	Added PLCA diagnostics
	6.6	Added reference schematics
	All	Various editorial changes
DS60001573B (Feb-2021)	All	Updated Release for RevB1
DS60001573A (Aug-2019)	All	Initial Release

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