XC9572 In-System Programmable CPLD

December 4, 1998 (Version 3.0)

Product Specification

Features

- 7.5 ns pin-to-pin logic delays on all pins
- f_{CNT} to 125 MHz
- 72 macrocells with 1,600 usable gates
- Up to 72 user I/O pins
- 5 V in-system programmable (ISP)
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
  - 90 product terms drive any or all of 18 macrocells within Function Block
  - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slew rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs
- 3.3 V or 5 V I/O capability
- Advanced CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 44-pin PLCC, 84-pin PLCC, 100-pin PQFP and 100-pin TQFP packages

Description

The XC9572 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of four 36V18 Function Blocks, providing 1,600 usable gates with propagation delays of 7.5 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC9572 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

I_{CC} (mA) =

MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 mA/MHz) f

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC9572 device.

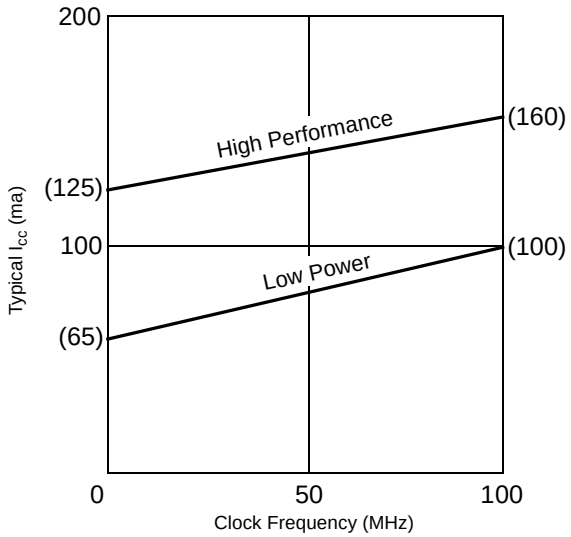


Figure 1: Typical I_{CC} vs. Frequency for XC9572

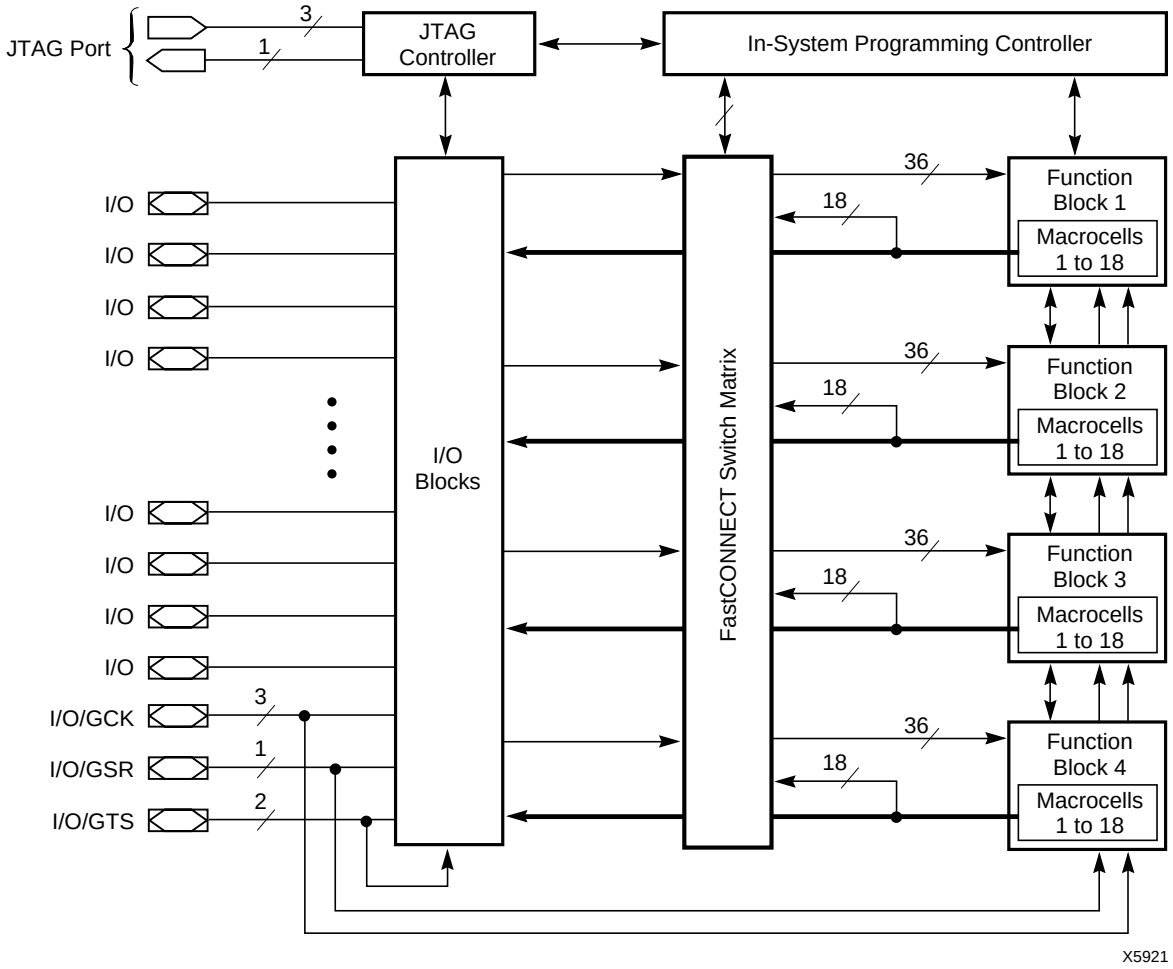


Figure 2: XC9572 Architecture

Note: Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 s @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operation Conditions[1]

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	V_{CCINT} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V

Note: 1. Numbers in parenthesis are for industrial temperature range versions.

Endurance Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles	10,000	-	Cycles

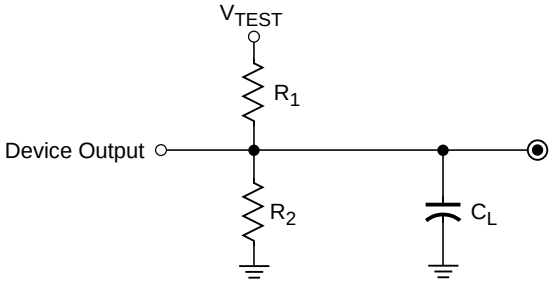
DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	Output high voltage for 3.3 V operation	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	Output low voltage for 5 V operation	I_{OL} = 24 mA V_{CC} = Min		0.5	V
	Output low voltage for 3.3 V operation	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
I_{IH}	I/O high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}		±10.0	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	65 (Typ)		ma

AC Characteristics

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		7.5		10.0		15.0	ns
t_{SU}	I/O setup time before GCK	4.5		6.0		8.0		ns
t_{H}	I/O hold time after GCK	0.0		0.0		0.0		ns
t_{CO}	GCK to output valid		4.5		6.0		8.0	ns
f_{CNT}[1]	16-bit counter frequency	125.0		111.1		95.2		MHz
f_{SYSTEM} [2]	Multiple FB internal operating frequency	83.3		66.7		55.6		MHz
t_{PSU}	I/O setup time before p-term clock input	0.5		2.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	4.0		4.0		4.0		ns
t_{PCO}	P-term clock to output valid		8.5		10.0		12.0	ns
t_{OE}	GTS to output valid		5.5		6.0		11.0	ns
t_{OD}	GTS to output disable		5.5		6.0		11.0	ns
t_{POE}	Product term OE to output enabled		9.5		10.0		14.0	ns
t_{POD}	Product term OE to output disabled		9.5		10.0		14.0	ns
t_{WLH}	GCK pulse width (High or Low)	4.0		4.5		5.5		ns

Note: 1. f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable.
f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG}.
2. f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5906

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC9572-7		XC9572-10		XC9572-15		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
t_{IN}	Input buffer delay		2.5		3.5		4.5	ns
t_{GCK}	GCK buffer delay		1.5		2.5		3.0	ns
t_{GSR}	GSR buffer delay		4.5		6.0		7.5	ns
t_{GTS}	GTS buffer delay		5.5		6.0		11.0	ns
t_{OUT}	Output buffer delay		2.5		3.0		4.5	ns
t_{EN}	Output buffer enable/disable delay		0.0		0.0		0.0	ns
Product Term Control Delays								
t_{PTCK}	Product term clock delay		3.0		3.0		2.5	ns
t_{PTSR}	Product term set/reset delay		2.0		2.5		3.0	ns
t_{PTTS}	Product term 3-state delay		4.5		3.5		5.0	ns
Internal Register and Combinatorial delays								
t_{PDI}	Combinatorial logic propagation delay		0.5		1.0		3.0	ns
t_{SUI}	Register setup time	1.5		2.5		3.5		ns
t_{HI}	Register hold time	3.0		3.5		4.5		ns
t_{COI}	Register clock to output valid time		0.5		0.5		0.5	ns
t_{AOI}	Register async. S/R to output delay		6.5		7.0		8.0	ns
t_{RAI}	Register async. S/R recovery before clock	7.5		10.0		10.0		ns
t_{LOGI}	Internal logic delay		2.0		2.5		3.0	ns
t_{LOGILP}	Internal low power logic delay		10.0		11.0		11.5	ns
Feedback Delays								
t_{F}	FastCONNECT matrix feedback delay		8.0		9.5		11.0	ns
t_{LF}	Function Block local feeback delay		4.0		3.5		3.5	ns
Time Adders								
t_{PTA}[3]	Incremental Product Term Allocator delay		1.0		1.0		1.0	ns
t_{SLEW}	Slew-rate limited delay		4.0		4.5		5.0	ns

Note: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

XC9572 I/O Pins

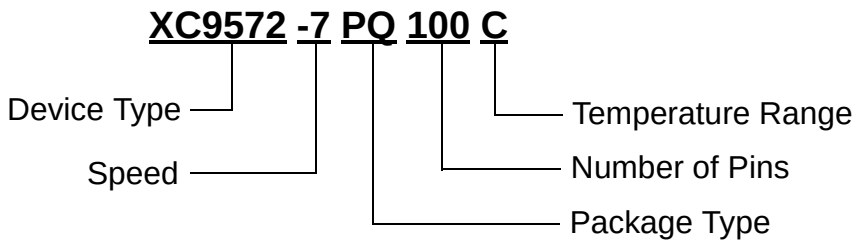
Function Block	Macrocell	PC 44	PC 84	PQ 100	TQ 100	BScan Order	Notes
1	1	–	4	18	16	213	
1	2	1	1	15	13	210	
1	3	–	6	20	18	207	
1	4	–	7	22	20	204	
1	5	2	2	16	14	201	
1	6	3	3	17	15	198	
1	7	–	11	27	25	195	
1	8	4	5	19	17	192	
1	9	5	9	24	22	189	[1]
1	10	–	13	30	28	186	
1	11	6	10	25	23	183	[1]
1	12	–	18	35	33	180	
1	13	–	20	38	36	177	
1	14	7	12	29	27	174	[1]
1	15	8	14	31	29	171	
1	16	–	23	41	39	168	
1	17	9	15	32	30	165	
1	18	–	24	42	40	162	
2	1	–	63	89	87	159	
2	2	35	69	96	94	156	
2	3	–	67	93	91	153	
2	4	–	68	95	93	150	
2	5	36	70	97	95	147	
2	6	37	71	98	96	144	
2	7	–	76	5	3	141	[2]
2	8	38	72	99	97	138	
2	9	39	74	1	99	135	[1]
2	10	–	75	3	1	132	
2	11	40	77	6	4	129	[1]
2	12	–	79	8	6	126	
2	13	–	80	10	8	123	
2	14	42	81	11	9	120	[3]
2	15	43	83	13	11	117	
2	16	–	82	12	10	114	
2	17	44	84	14	12	111	
2	18	–	–	94	92	108	
3	1	–	25	43	41	105	
3	2	11	17	34	32	102	
3	3	–	31	51	49	99	
3	4	–	32	52	50	96	
3	5	12	19	37	35	93	
3	6	–	34	55	53	90	
3	7	–	35	56	54	87	
3	8	13	21	39	37	84	
3	9	14	26	44	42	81	
3	10	–	40	62	60	78	
3	11	18	33	54	52	75	
3	12	–	41	63	61	72	
3	13	–	43	65	63	69	
3	14	19	36	57	55	66	
3	15	20	37	58	56	63	
3	16	–	45	67	65	60	
3	17	22	39	60	58	57	
3	18	–	–	61	59	54	
4	1	–	46	68	66	51	
4	2	24	44	66	64	48	
4	3	–	51	73	71	45	
4	4	–	52	74	72	42	
4	5	25	47	69	67	39	
4	6	–	54	78	76	36	
4	7	–	55	79	77	33	
4	8	26	48	70	68	30	
4	9	27	50	72	70	27	
4	10	–	57	83	81	24	
4	11	28	53	76	74	21	
4	12	–	58	84	82	18	
4	13	–	61	87	85	15	
4	14	29	56	80	78	12	
4	15	33	65	91	89	9	
4	16	–	62	88	86	6	
4	17	34	66	92	90	3	
4	18	–	–	81	79	0	

Notes: [1] Global control pin
[2] Global control pin GTS1 for PC84, PQ100, and TQ100
[3] Global control pin GTS1 for PC44

XC9572 Global, JTAG and Power Pins

Pin Type	PC44	PC84	PQ100	TQ100
I/O/GCK1	5	9	24	22
I/O/GCK2	6	10	25	23
I/O/GCK3	7	12	29	27
I/O/GTS1	42	76	5	3
I/O/GTS2	40	77	6	4
I/O/GSR	39	74	1	99
TCK	17	30	50	48
TDI	15	28	47	45
TDO	30	59	85	83
TMS	16	29	49	47
V_{CCINT} 5 V	21,41	38,73,78	7,59,100	5,57,98
V_{CCIO} 3.3 V/5 V	32	22,64	28,40,53,90	26,38,51,88
GND	10,23,31	8,16,27,42, 49,60	2,23,33,46,64,71, 77,86	100,21,31,44,62,69, 75, 84
No Connects	–	—	4,9,21,26,36,45,48, 75, 82	2,7,19,24,34,43,46, 73, 80

Ordering Information



Speed Options

-15 15 ns pin-to-pin delay
-10 10 ns pin-to-pin delay
-7 7.5 ns pin-to-pin delay

Packaging Options

PC44 44-Pin Plastic Leaded Chip Carrier (PLCC)
PC84 84-Pin Plastic Leaded Chip Carrier (PLCC)
PQ100 100-Pin Plastic Quad Flat Pack (PQFP)
TQ100 100-Pin Very Thin Quad Flat Pack (TQFP)

Temperature Options

C Commercial0°C to +70°C
I Industrial–40°C to +85°C

Component Availability

Pins		44	84	100	
Type		Plastic PLCC	Plastic PLCC	Plastic PQFP	Plastic TQFP
Code		PC44	PC84	PQ100	TQ100
XC9572	–15	C(I)	C(I)	C(I)	C(I)
	–10	C(I)	C(I)	C(I)	C(I)
	–7	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to +85°C

Revision Control

Date	Revision
12/04/98	Update AC Characteristics and Internal Parameters