

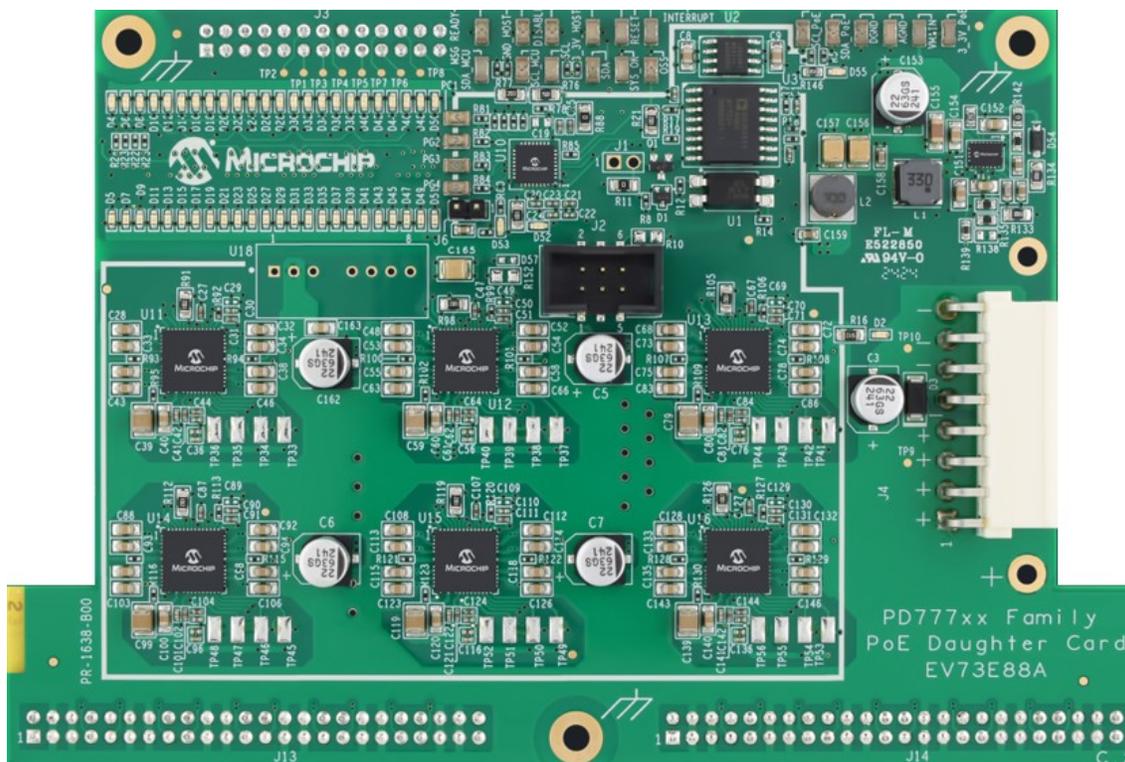
Introduction

The EV73E88A evaluation board is based on Microchip's PD77718 PoE manager and the PD77010 PoE controller. The EV73E88A operates in Controller mode using the PD77010 and demonstrates 24 x 4-pair PoE IEEE® 802.3bt ports using 6 x PD77718T4 devices. The EV73E88A is designed to interface with SparX-5i PCB135 and Laguna TSN switches.

The PD77718 and PD77010 devices are a part of the seventh generation IEEE 802.3bt compliant Power over Ethernet (PoE) Power Sourcing Equipment (PSE) family from Microchip. The PD77718 device is a fully integrated eight port PoE manager, with integrated Field Effect Transistor (FET) switches and current sense resistors. The PD77718 and PD77010 chipset supports IEEE 802.3af/at/bt standards, as well as legacy/pre-standard PD detection. The device is available in a 56-pin, 8 mm × 8 mm Quad flat no-lead (QFN) package.

The following figure shows the top view of the evaluation board.

Figure 1. Evaluation Board - Top View



Features

The evaluation board has the following features.

- Two 24x2 Header Connectors to Connect to the RJ45 and Magnetic on the MB (Motherboard).
- One 13x2 Header Connector to Connect Communication and Control Signals with MB
- 48 2-Pair Ports or 24 4-Pair Ports, Structured by Six PD77718 Devices and Controlled by the PD77010
- I²C Communication between Six PoE PSE ICs to PoE Controller
- Manual Disable Port Jumpers
- Two Bi-Color (Green and Yellow) LEDs Per Port to Provide Visual Status of each Port
- Requires only a Single Power Source
- 0°C to 40°C Operating Temperature
- RoHS Compliant

The following images show the system block diagram and the layout of the evaluation board.

Figure 2. EV73E88A Evaluation Board Block Diagram

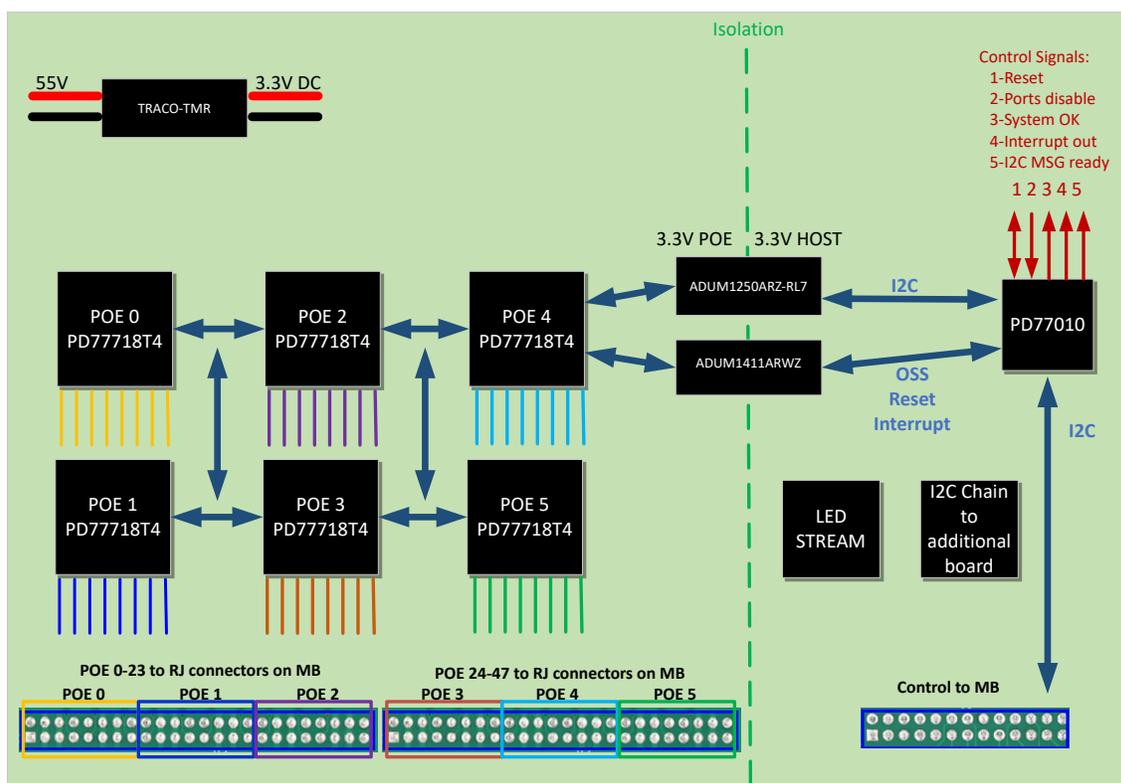


Figure 3. EV73E88A Layout

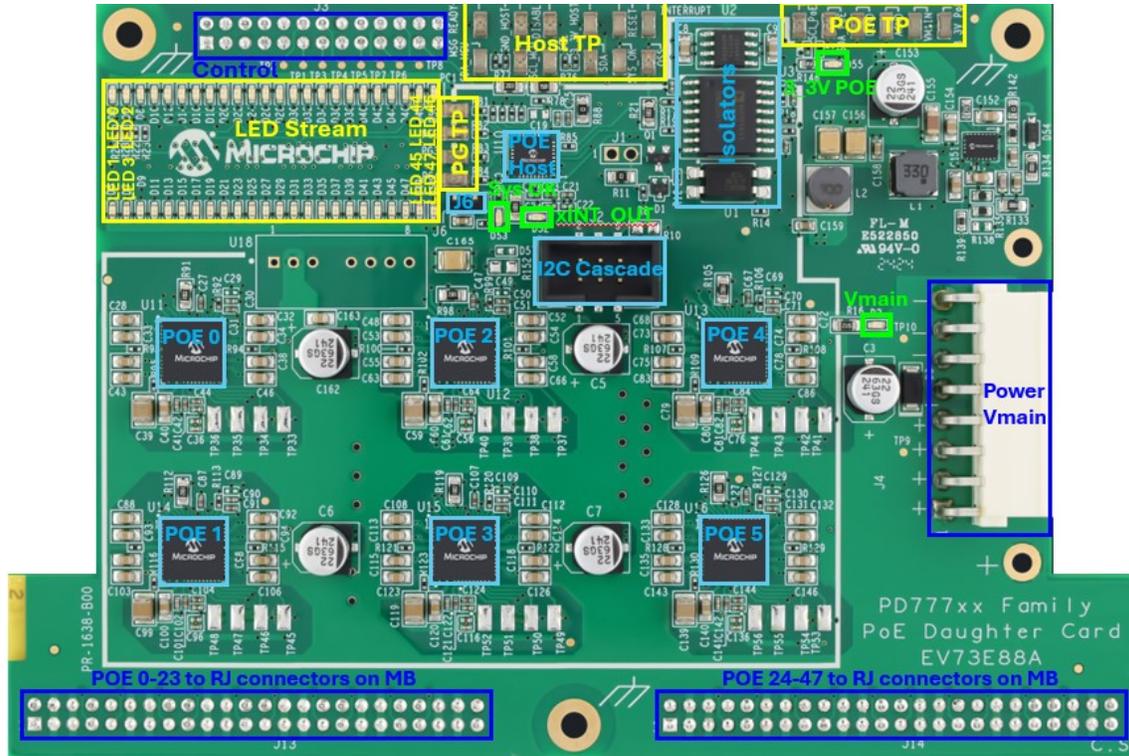


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1. Overview

This section provides the basic overview of the EV73E88A Evaluation board.

1.1. Power

The EVB is powered by a single source through the DC connector J4. The input voltage level can be selected according to the following IEEE® 802.3 PoE standards:

1. IEEE 802.3af: 44 V_{DC} to 57 V_{DC}
2. IEEE 802.3at: 50 V_{DC} to 57 V_{DC}
3. IEEE 802.3bt:
 - a. 50 V_{DC} to 57 V_{DC} for type 3
 - b. 52 V_{DC} to 57 V_{DC} for type 4

The recommended voltage level is 53 V_{DC} to 55 V_{DC}, which covers all the PoE standards. The EVB has three power domains as follows:

1. PoE domain (VMAIN), which is fed directly by the main supply and is the power domain provided to the RJ45
2. 3.3 V_{DC} POE which feeds the PD77718 and serial communication peripherals, same ground as the PoE domain. That 3.3 V_{DC} is generated by DC/DC module.
3. 3.3 V_{DC} Host for the PD77010, LED stream, and for the USB port; this power is coming from the Motherboard (MB).

Note: The EVB is polarity sensitive. The correct polarity is shown in the following figure.

Figure 1-1. DC Connector Power Polarity

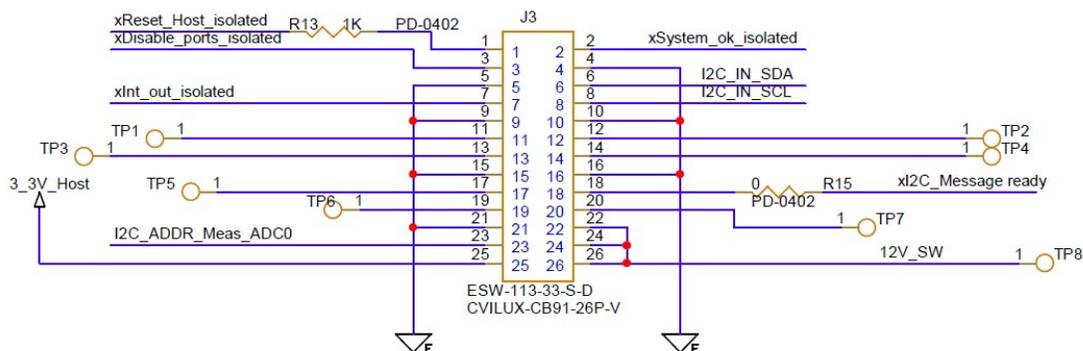


1.2. Interface and Control

This section describes the set-up procedures for serial communication, Over Supply Shutdown (OSS), PoE ports disable, power good input (PGD1–PGD4), and additional test points.

Communication and Control are connected to the EVB and the MB through J3

Figure 1-2. Schematics–Interface and Control

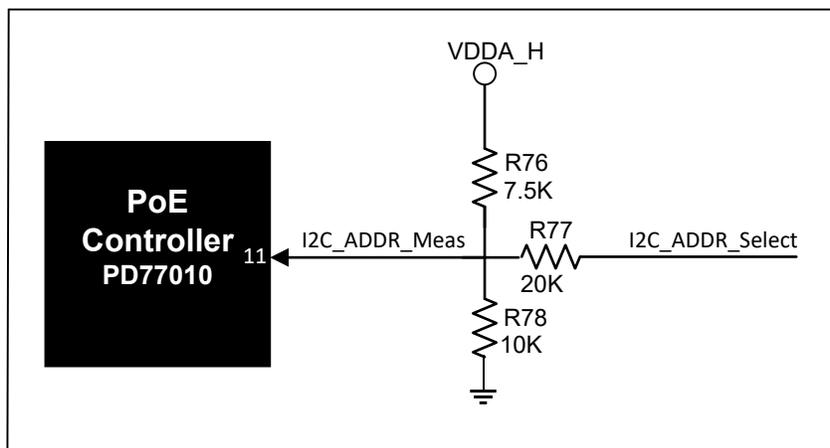


1.2.1. Serial Communication

The EVB supports serial communication with the PD77010 by I²C.

- I²C Address Select
 - 0 = I2C 0x2C (1.55V)
 - 1 = I2C 0x3C (2.13V)

Figure 1-3. I²C Address Setting Diagram



- I²C Cascade from EVB to EVB (J2)
If the system uses two PoE cards, connect a 6 pin flat cable in to J2 of both cards, to cascade both PoE cards.
In such implementation, one of the PD77010 is hold in reset, and the other PD77010 controls 12x PD7718.
Note: The first EVB I²C select should be 0, and the second EVB I²C select should be 1.

Figure 1-4. I²C Cascade



Figure 1-5. Circuit Diagram

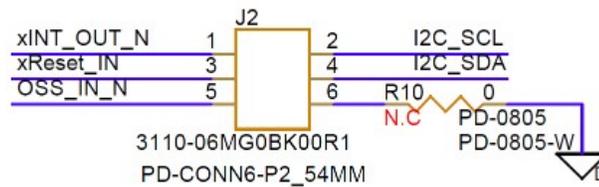


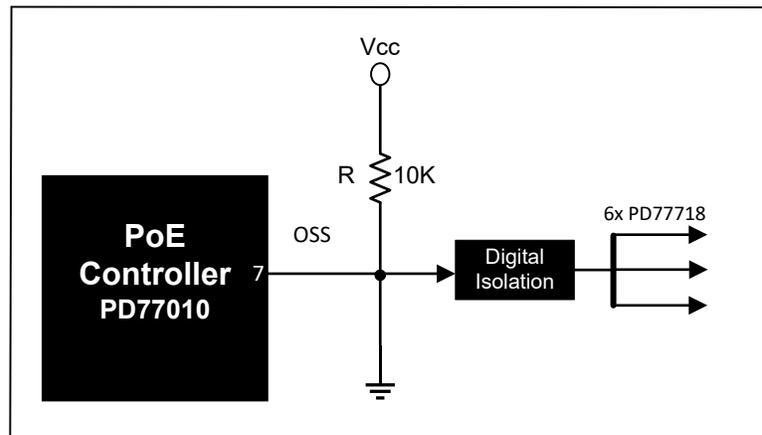
Figure 1-6. Flat Cable



1.2.2. Over Supply Shutdown (OSS)

OSS is used to shut down ports based on the priority settings. The following figure shows the OSS control diagram.

Figure 1-7. OSS Control Diagram



1.2.3. PoE Ports Disable Settings

The jumper J6 is connected to the Disable pin of the PD77010.

- When the jumper J6 is not installed, the ports are controlled by Host POE PD77010 SW.
- When the jumper J6 is installed, all ports are disabled.

In normal operations, the host can disable all ports by setting this pin to '0'.

The following figures show the J6 jumper settings and its location on the evaluation board.

Figure 1-8. J6 Jumper Setting

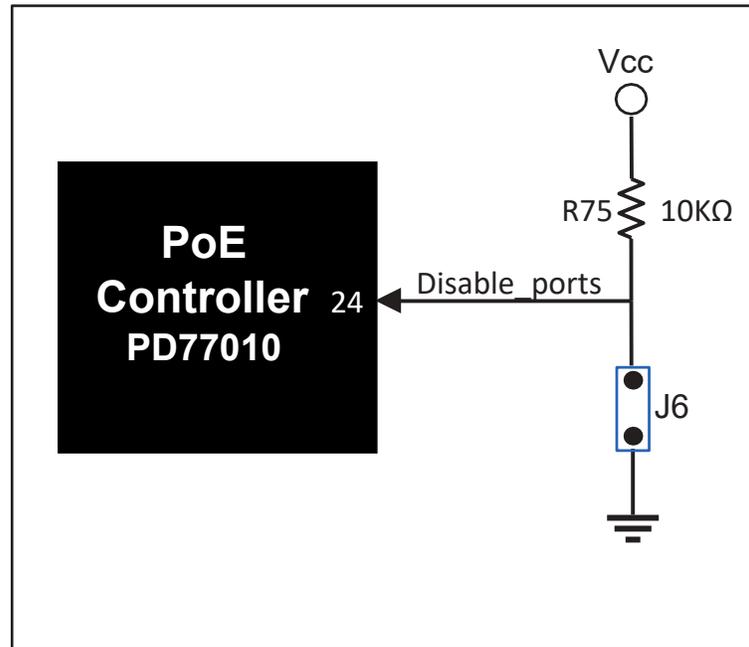
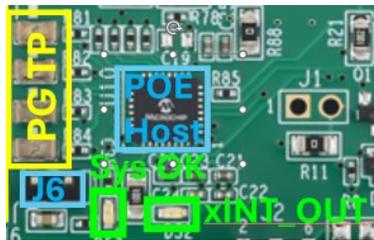


Figure 1-9. J6 Jumper Location



1.2.4. PoE and Host Test Points

The PoE and Host test points are located as follows:

- PoE I²C and power signals are placed on the right side of the isolators.
- Host I²C, Control, and power signals are placed on the left side of the isolators.

The placement of these test points on the evaluation board is as shown in the following figures.

Figure 1-10. Host and PoE Test Points

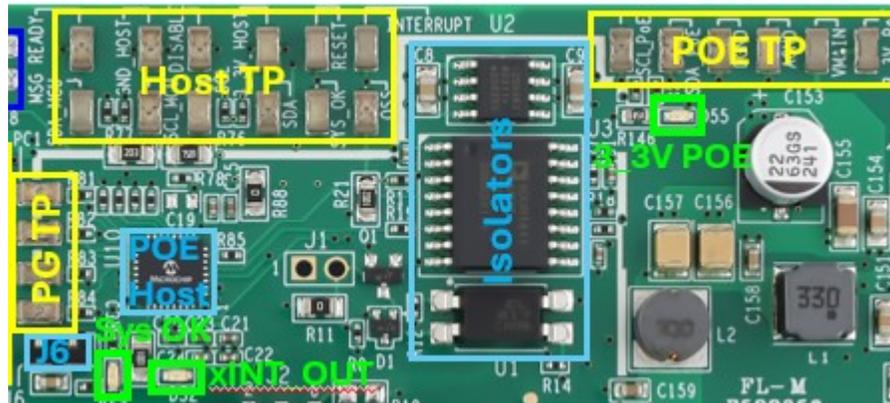
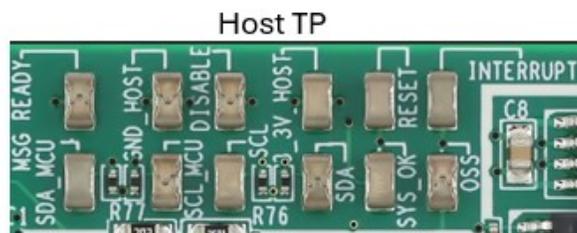


Figure 1-11. PoE Test points



Figure 1-12. Host Test Points



1.2.5. Power Good Input (PGD) Settings and Test Points

The EVB supports feeding from up to four power supplies, which includes 5 power banks (bank 0 to bank 4). Each power supply must generate a digital signal (0-3.3 V_{DC}), which indicates the power supply is active. The generated digital signal must be connected to one of the PG pins of PD77010 (pins 17, 18, 19, and 20).

On the EVB, four PGD pins are pulled down with a 10K resistor to GND_HOST, which sets the default power bank to 0x00. To set a different bank than 0x00, the user can use the PG1-PG4 test points, PD77010 POE host.

The four PG signals are referenced to the PD77010 domain (GND_HOST), see the following figures.

Figure 1-13. PG1-PG4 Test Points Diagram

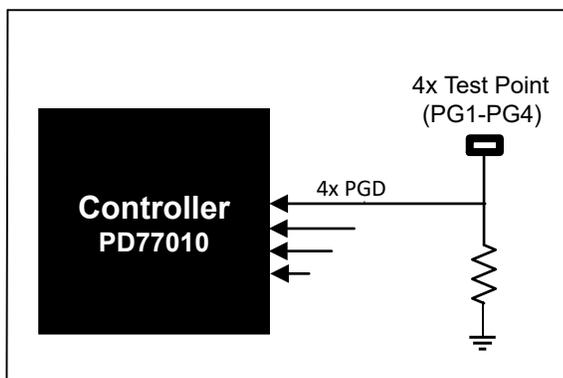
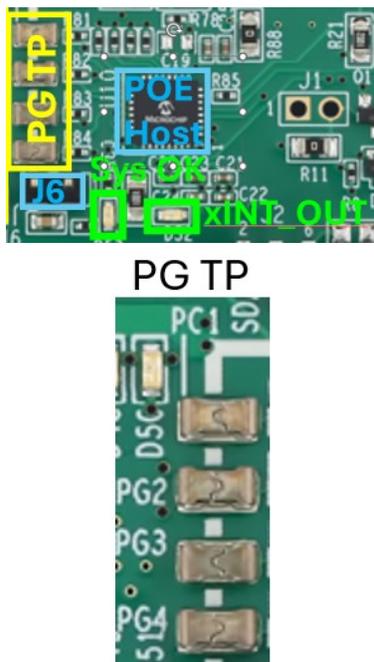


Figure 1-14. PG1-PG4 Test Points Location



1.3. LED Indication

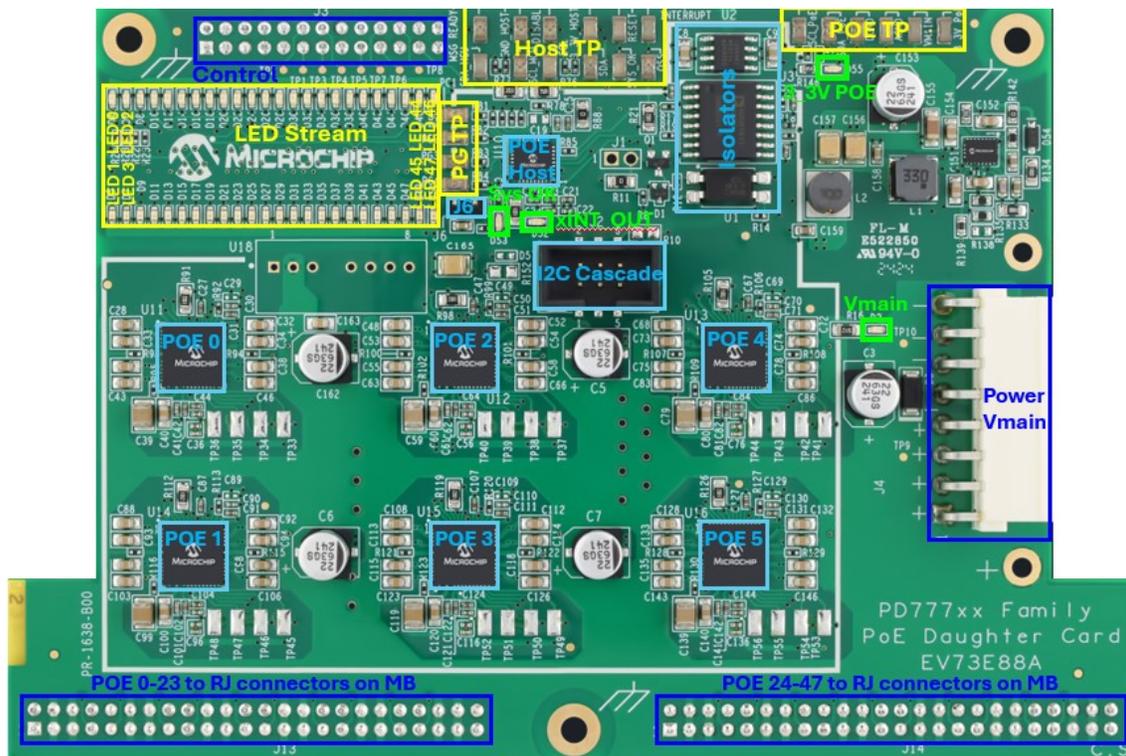
The evaluation board contains status indication LED. These LEDs and their corresponding functions are listed in the following table.

Table 1-1. LED List

Designation	Function
D2	V _{MAIN} ON - Light green on when V _{MAIN} is provided to the EVB through the power connector.
D55	3.3V-POE- Light green on when 3.3V is provided to the POE section
D53	System OK-Light green on when the host is communicating properly with the 6 x POE devices
D52	Interrupt out-Light green on when at least one of the six POE devices send interrupt to the host (SW option)
LED stream array	<ul style="list-style-type: none"> • LED per port • Green LED on when port is on • Green Blinking when underload event • LED OFF when port is OFF • Yellow ON due to error/power management

The following figure shows the location of these status LEDs on the EVB.

Figure 1-15. LED Location



2. Installation and Setting

This section describes the steps required to install and operate the EVB. Take the following precautions before starting the installation:

- Ensure that the 52 V_{DC}- 57V_{DC} power supply of the board is turned off before plugging in the DC connector
- Turn the main power supply on only after the DC connector is plugged in
- Ensure the correct polarity of the power supply cable. The polarity of the power supply cable is as shown in [Figure 1-1](#).

2.1. Port Matrix

Configure the port matrix per the following tables.

Table 2-1. One Board Assembled: 4P BT, SparX-5i PCB135 and Laguna TSN Switches

Logical Port	Physical Port A	Physical Port B
0	0	1
1	2	3
2	4	5
3	6	7
4	24	25
5	26	27
6	28	29
7	30	31
8	8	9
9	10	11
10	32	33
11	34	35
12	12	13
13	14	15
14	36	37
15	38	39
16	16	17
17	18	19
18	20	21
19	22	23
20	40	41
21	42	43
22	44	45
23	46	47

Table 2-2. Two Boards Assembled: 4P BT, SparX-5i PCB135

Logical Port	Physical Port A	Physical Port B
0	0	1
1	2	3
2	4	5
3	6	7
4	24	25

Table 2-2. Two Boards Assembled: 4P BT, SparX-5i PCB135 (continued)

Logical Port	Physical Port A	Physical Port B
5	26	27
6	28	29
7	30	31
8	8	9
9	10	11
10	32	33
11	34	35
12	12	13
13	14	15
14	36	37
15	38	39
16	16	17
17	18	19
18	20	21
19	22	23
20	40	41
21	42	43
22	44	45
23	46	47
24	64	65
25	66	67
26	68	69
27	70	71
28	88	89
29	90	91
30	92	93
31	94	95
32	72	73
33	74	75
34	96	97
35	98	99
36	76	77
37	78	79
38	100	101
39	102	103
40	80	81
41	82	83
42	84	85
43	86	87
44	104	105
45	106	107
46	108	109
47	110	111

2.2. Schematics

Contact Microchip for the full-board schematics.

3. Accessories

The three extenders shown in the following figure are included in the box.

Figure 3-1. Extenders



They should be mounted to J3, J13, J14, in the board bottom. When there is high heat sinks on the mother board components, these extenders avoid physical contact between the mother board and the daughter board.

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
A	September 2025	Initial Revision

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