FAIRCHILD SEMICONDUCTOR®

June 2005

FDS4685
40V P-Channel PowerTrench® MOSFET

Features

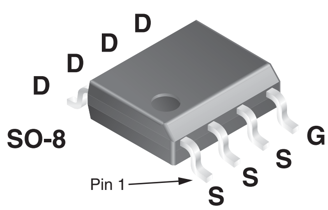
- –8.2 A, –40 V $R_{DS(ON)}$ = 0.027 Ω @ V_{GS} = –10 V
$R_{DS(ON)}$ = 0.035 Ω @ V_{GS} = –4.5 V
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

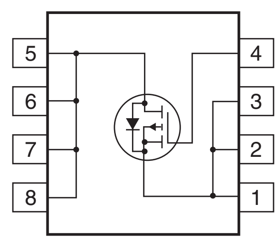
Applications

- Power management
- Load switch
- Battery protection

General Description

This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gate drive voltage ratings (4.5V – 20V).





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–40	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	–8.2	A
	- Pulsed		–50	
P_D	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.4	
		(Note 1c)	1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C
Thermal Characteristics				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	

Package Marking and Ordering Information

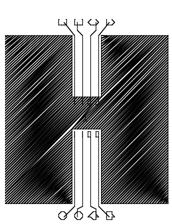
Device Marking	Device	Reel Size	Tape width	Quantity
FDS4685	FDS4685	13"	12mm	2500 units

Electrical Characteristics $T_A = 25°C$ unless otherwise noted

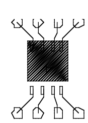
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ µA	–40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		–32		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -32$ V, $V_{GS} = 0$ V			–1	µA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20$ V, $V_{DS} = 0$ V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ µA	–1	–1.6	–3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250$ µA, Referenced to 25°C		4.7		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10$ V, $I_D = -8.2$ A $V_{GS} = -4.5$ V, $I_D = -7$ A $V_{GS} = -10$ V, $I_D = -8.2$ A, $T_J = 125°C$		22 29 31	27 35 42	mΩ
g_{FS}	Forward Transconductance	$V_{DS} = -5$ V, $I_D = -8.2$ A		22		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -20$ V, $V_{GS} = 0$ V, f = 1.0 MHz		1872		pF
C_{oss}	Output Capacitance			256		pF
C_{rss}	Reverse Transfer Capacitance			134		pF
R_G	Gate Resistance	$V_{GS} = 15$ mV, f = 1MHz		4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -20$ V, $I_D = -1$ A, $V_{GS} = -10$ V, $R_{GEN} = 6$ Ω		14	25	ns
t_r	Turn–On Rise Time			11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			50	80	ns
t_f	Turn–Off Fall Time			18	32	ns
Q_g	Total Gate Charge	$V_{DS} = -20$ V, $I_D = -8.2$ A, $V_{GS} = -5$ V		19	27	nC
Q_{gs}	Gate–Source Charge			5.6		nC
Q_{gd}	Gate–Drain Charge			6.1		nC
Drain–Source Diode Characteristics						
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -2.1$ A (Note 2)		–0.7	–1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -8.2$ A, $d_{iF}/d_t = 100$ A/µs		26		nS
Q_{rr}	Diode Reverse Recovery Charge			15		nC

Notes:

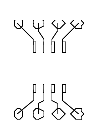
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design..



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 105°/W when mounted on a .04 in^2 pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics:

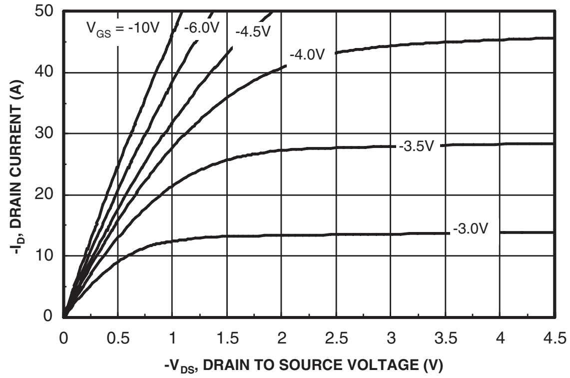


Figure 1. On-Region Characteristics.

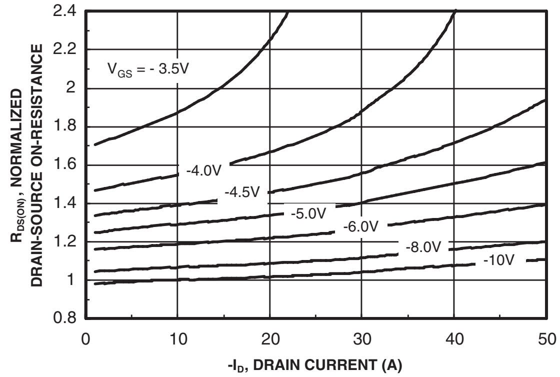


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

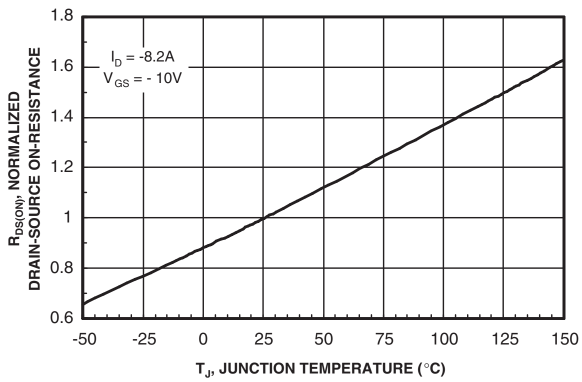


Figure 3. On-Resistance Variation with Temperature.

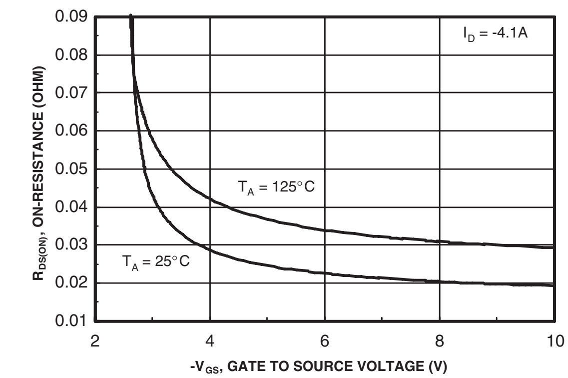


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

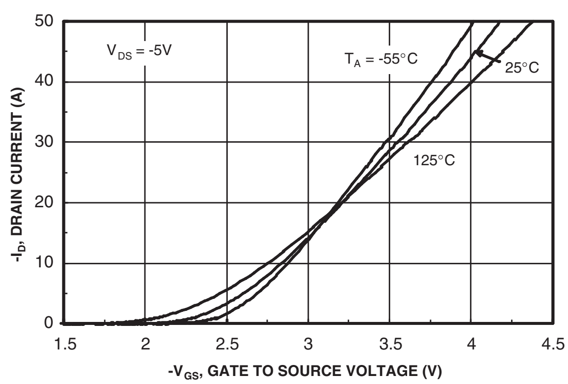


Figure 5. Transfer Characteristics.

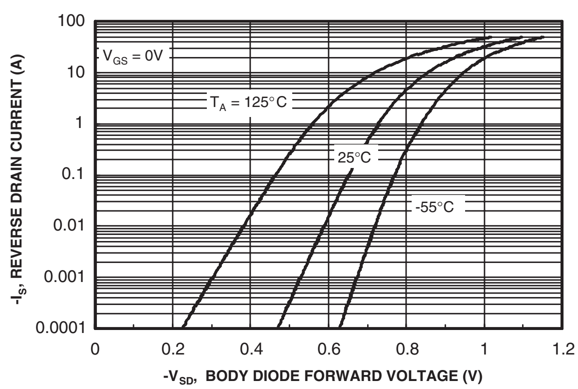


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics:

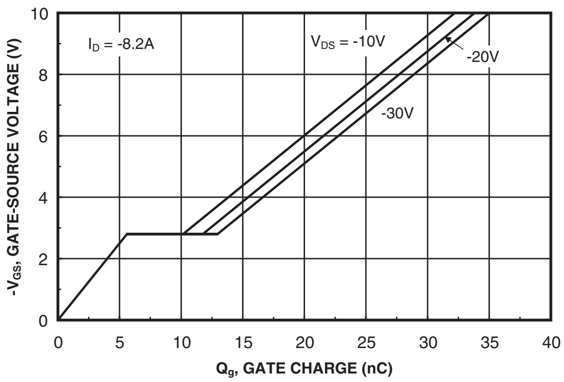


Figure 7. Gate Charge Characteristics.

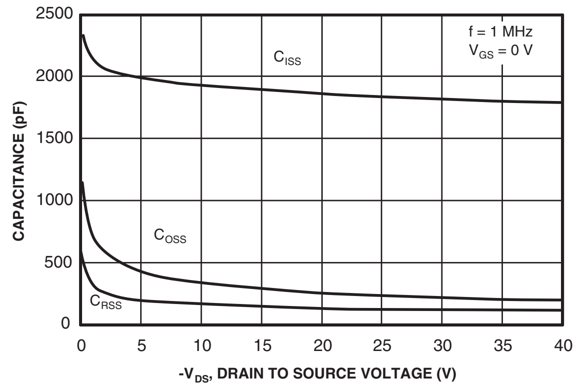


Figure 8. Capacitance Characteristics.

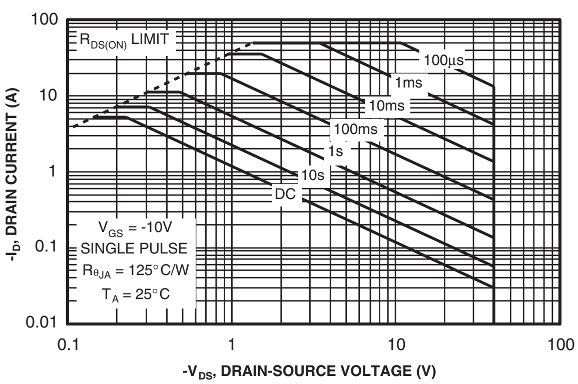


Figure 9. Maximum Safe Operating Area.

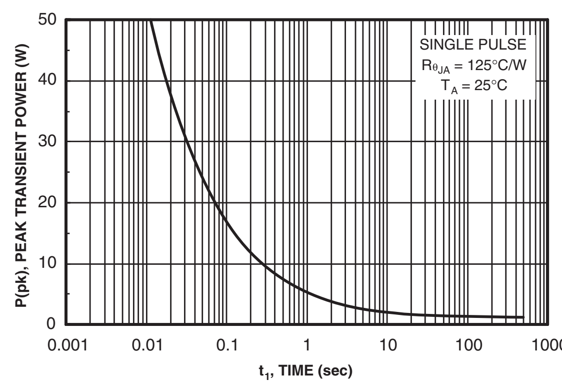


Figure 10. Single Pulse Maximum Power Dissipation.

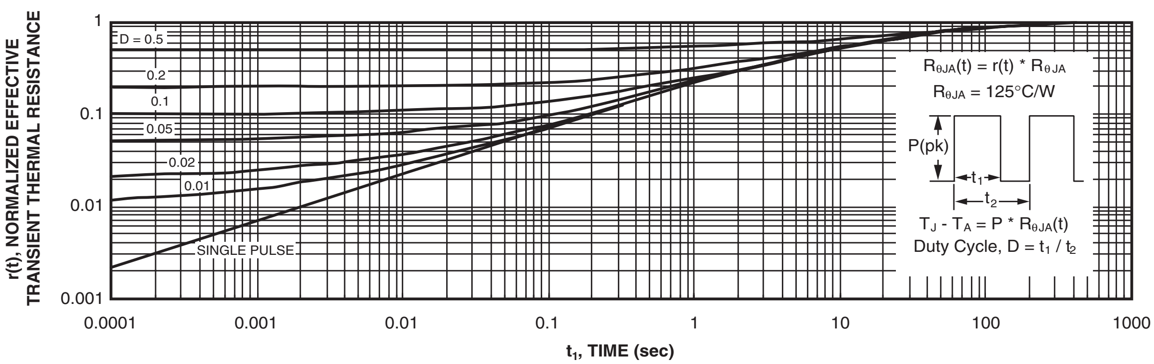


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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