SP Industrial
Reliable Embedded Partner

Datasheet

Industrial microSD Card 6.1

SDT5R0 Series

Specifications Overview

- **Capacity**
  - 4GB, 8GB, 16GB, 32GB, 64GB, 128GB
- **Form Factor**
  - microSD
- **Interface**
  - SD6.1 UHS-I
- **Performance**
  - Sequential Read: up to 97 MB/s
  - Sequential Write: up to 83 MB/s
- **Temperature Range**
  - Operation temperature:
    Normal temperature: -25°C to +85°C
    Wide temperature: -40°C to +85°C
- **Power Consumption**
  - Supply Voltage: DC +3.3V
  - Read (Max.): 0.74 mA
  - Write (Max.): 0.76mA
  - Idle (Avg.): 0.18m A
- **Reliability**
  - TBW:
    4GB: 105 TB
    8GB: 211 TB
    16GB: 421 TB
    32GB: 843 TB
    64GB: 1,685 TB
    128GB: 3,371 TB
  - MTBF: > 3,000,000 hrs
- **ECC Performance**
  - LDPC
- **Environment Specification**
  - Shock
  - Vibration
- **Compliant Specifications**
  - RoHS
- **Feature Support**
  - Bad Block Management
  - Over Provisioning

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Revision History

Revision	Date	Major Changes
1.0	2020/11/30	First release
1.1	2021/02/08	Update 2.5.1 TBW data, sequential and enterprise
1.2	2021/03/15	Revise 2.5.1 TBW data, sequential and enterprise
1.3	2021/06/07	Modify TBW workload capacity
1.4	2021/10/01	Add new description 16GB SA3309 + BiCS4 256Gb*2 pSLC
1.5	2022/02/22	Modify format issue
2.0	2022/08/11	Add description BOM code for firmware B0721 Add SA3309AC solution
2.1	2022/09/13	Add wild temperature ordering information Modify Maximum Sequential Access
2.2	2023/04/10	Add SA3309AC+BiCS5 series solution Add 4GB ordering information
2.3	2023/12/11	Modify MTBF
2.4	2023/12/20	Add 8GB ordering information.
2.5	2024/05/20	Adjust Format
2.6	2024/10/24	Adjust Temperature info
2.7	2025/01/08	Fixed format error
2.8	2025/01/14	Add new solution 256GB pSLC
2.9	2025/03/04	Correct TBW
3.0	2025/04/01	Add YMTC X1 solution Correct Physical Dimension Update order information
3.1	2025/08/26	Add new solution 128GB pSLC
3.2	2026/02/06	New Logo Format Update Power Consumption Update Ordering Information
3.3	2026/04/30	Update Ordering Information

1 Product Description

1.1 Overview

Silicon Power's Industrial microSD Card SDT5R0 series is a series of memory cards that adopt 3D TLC flash memory technology and content protection mechanism that is fully compliant to the specification released by SD Card Association.

This SDT5R0 series comes with 8-pin interface, designed to operate at a maximum operating frequency of 208MHz. It can alternate communication protocol between the SD mode and SPI mode. The SDT5R0 series optimizes algorithm for wear-leveling to increase the lifespan of microSD card and applies LDPC of ECC circuitry to reach 30K PE cycles endurance.

1.2 Features

- pSLC Flash Technology with 30K PE cycles endurance
- Global Wear Leveling, Static & Dynamic Wear Leveling and Early weak block retirement to ensure an even level of wearing out
- LDPC ECC engine with hardware decode, read retry & software decode capable of correcting error to 125 bits/KB to guarantee 3K PE cycles for 3D NAND
- Offline training with AI for firmware to monitor the status of 3D NAND dynamically to determine the optimized parameters for LDPC ECC software decode
- Sudden Power-Off Recovery (SPOR) resilient firmware with capability to avoid firmware crash when sudden power loss or unstable voltage occurs during operation mode and device initialization stage
- Auto Read-Refresh, Read retry, Garbage collection to ensure reliability and optimized performance
- SP microSD / SD supports S.M.A.R.T. information
- SP SMART IoT providing cloud service with alarm and notifications which monitors and analyzes the health and status of SP Flash products inside the connected devices
- Supports SD specification 6.1 Low Voltage Signaling (LVS)

1.3 System Requirements

- Voltage: DC +3.3V
- Operating System: Linux, Windows 10, 11 or Windows Embedded Systems.

2 Specification

2.1 Physical Dimension

2.1.1 Dimension

The Dimensions of microSD Card are illustrated in Figure 1 and described in Table 1.

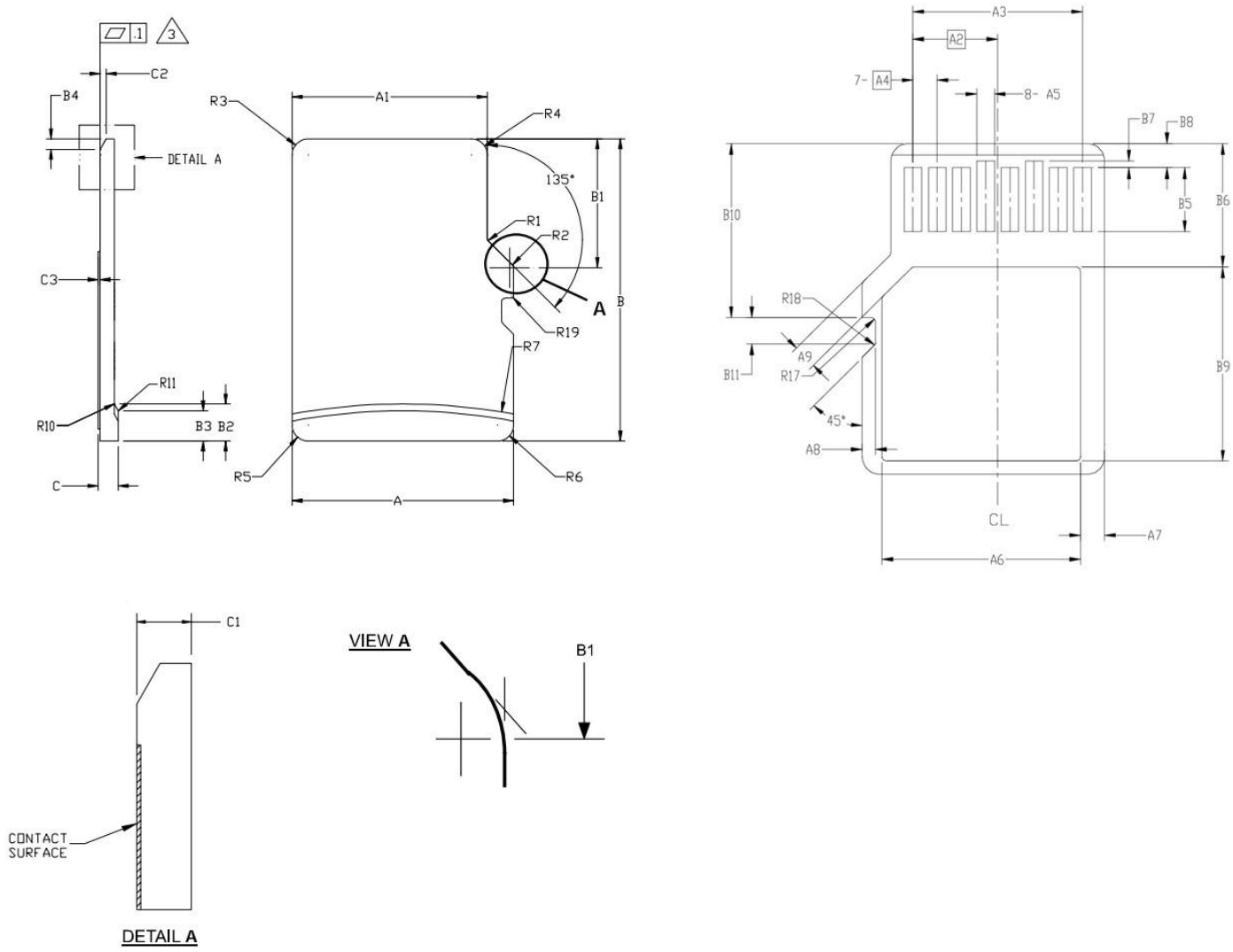

Figure 1 : MicroSD Card Dimensions

Table 1 : MicroSD Card Physical Dimension

COMMON DIMENSIONS **Unit: mm**									
SYMBOL	**MIN.**	**NORM.**	**MAX.**	**NOTE**	**SYMBOL**	**MIN.**	**NORM.**	**MAX.**	**NOTE**
A	10.90	11.00	11.10		C	0.90	1.00	1.10	
A1	9.60	9.70	9.80		C1	0.60	0.70	0.80	
A2	-	3.85	-	BASIC	C2	0.20	0.30	0.40	
A3	7.60	7.70	7.80		C3	0.00	-	0.15	
A4	-	1.10	-	BASIC	D1	1.00	-	-	

COMMON DIMENSIONS Unit: mm									
SYMBOL	**MIN.**	**NORM.**	**MAX.**	**NOTE**	**SYMBOL**	**MIN.**	**NORM.**	**MAX.**	**NOTE**
A5	0.75	0.80	0.85		D2	1.00	-	-	
A6	-	-	8.50		D3	1.00	-	-	
A7	0.90	-	-		R1	0.20	0.40	0.60	
A8	0.60	0.70	0.80		R2	0.20	0.40	0.60	
A9	0.80	-	-		R3	0.70	0.80	0.90	
B	14.90	15.00	15.10		R4	0.70	0.80	0.90	
B1	6.30	6.40	6.50		R5	0.70	0.80	0.90	
B2	1.64	1.84	2.04		R6	0.70	0.80	0.90	
B3	1.30	1.50	1.70		R7	29.50	30.00	30.50	
B4	0.42	0.52	0.62		R10	-	0.20	-	
B5	2.80	2.90	3.00		R11	-	0.20	-	
B6	5.50	-	-		R17	0.10	0.20	0.30	
B7	0.20	0.30	0.40		R18	0.20	0.40	0.60	
B8	1.00	1.10	1.20		R19	0.05	-	0.20	
B9	-	-	9.00						
B10	7.80	7.90	8.00						
B11	1.10	1.20	1.30						

2.1.2 Weight

- 0.25g ± 5%

2.2 Electrical Specifications

2.2.1 Operating Condition

- Supply Voltage: DC 2.7V to 3.6V

Table 2 : Power Consumption

Mode	Power Consumption						Unit
	4GB	8GB	16GB	32GB	64GB	128GB	
Read (Max.)	65	65	73	72	74	70	mA
Write (Max.)	73	73	75	74	76	75	mA
Stand-by/Sleep	0.07	0.07	0.1	0.07	0.1	0.18	mA

Notice: The value is various bases on the capacity and the test platform.
Notice: Power consumption is measured during the sequential read and write operations performed by CrystalDiskMark.
Notice: Power consumption of Idle is measured when the platform gets into a steady-state mode after IOMeter runs "Idle" script for 10mins.

※ Testing Platform:
Mother-Board: ASUS Z690-A, CPU: Intel(R) Core i5-12500K CPU 3.0GHz, Chipset: Intel Z690-A, Main Memory: DDR4-2133 8GB X 1pcs, Operating System: Win 10, 64bit
Test Temperature: 25°C

2.3 Performance

2.3.1 Interface SD Specification

SD 6.1 UHS-1, and backward compatible to SD 3.0 specification

2.3.2 Speed Class

Class 10, U3

2.3.3 Transfer Modes

SD mode (1~ 4 bits) or SPI mode

- DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
- HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
- SDR12: 1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
- SDR25: 1.8V signaling, frequency up to 50MHz, up to 25MB/sec
- SDR50: 1.8V signaling, frequency up to 100MHz, up to 50MB/sec
- SDR104: 1.8V signaling, frequency up to 208MHz, up to 104MB/sec
- DDR50: 1.8V signaling, frequency up to 50MHz, sampled on both clock edges, up to 50MB/s

2.3.4 TeraByte Write

Table 3 : TBW Data

Mode	TBW Data						Unit
	4GB	8GB	16GB	32GB	64GB	128GB	
Client	105	211	421	843	1685	3,371	TB
Enterprise	15	30	61	122	244	488	TB

Notice: TBW is estimated by formula **TBW = (Capacity x PE Cycles) x (1 + OP) x (WLE) / (WAF)**

- **OP = (Physical Capacity / Logical Capacity) - 1**
- **WLE =** It could be different depended on the workload or usage containing data size and access rate.
- **Client workload:** Sequential write workload.
- **Enterprise workload:** Follow JESD219A enterprise workload which is generated by VDBENCH script and tested by VDBENCH.

2.3.5 Wear-Leveling

- Enhanced endurance by global Wear-Leveling.

2.4 Environmental Conditions

Table 4 : Environmental Conditions

Feature	Operating	Storage
Temperature (Normal Grade)	-25°C to +85°C	-55°C to +95°C
Temperature (Wide-Temperature Grade)	-40°C to +85°C	-55°C to +95°C
Humidity	10% to 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

2.5 Reliability

Table 5 : Reliability

Feature	Specification
ECC Capability	Hardware LDPC ECC engine
MTBF	3,000,000 hrs.
Program / Erase Endurance	3,0000 P/E cycles
Optimal sustained performance	Dynamic SLC Cache Architecture
Data Endurance & Data integrity	Early weak block retirement, Global Wear leveling
Data Retention	10% of program / Erase Endurance cycles: 10 Years
	100% of program / Erase Endurance cycles: 1 Years

Notice:

- Data retention: The value is based on normal program/erase endurance at room temperature. High environmental temperature may shorten the retention period.

2.6 Compliance Specifications

- RoHS
- Reach

2.7 Technique

2.7.1 Wide Temperature

Products for industrial applications often have to withstand extreme temperature conditions. SP Industrial offers solutions that are able to operate in all systems and environments, including harsh operating environments and industries such as defense and telecommunications. Select SD controllers from SP Industrial are equipped with wide temperature technology to operate reliably from a wide temperature range of -40°C to +85°C.

2.7.2 pSLC

To fill the gap between SLC and MLC/3D TLC solutions, SP Industrial offers pseudo-SLC (pSLC) Flash. It is an advanced variant of MLC/3D TLC that outperforms the latter in speed, program erase cycles, and overall reliability. Pseudo-SLC operates similar to SLC, but with fewer program erase cycles, which makes it a cost-effective alternative to SLC SP Industrial's latest Industrial SSD with pSLC solution.

2.7.3 SLC Cache

The SLC cache technology divides a cache space in the TLC device to be simulated as an SLC, and the speed in the SLC cache can be improved. But when the cache space is run out, the speed will return to the original TLC speed.

2.7.4 Bad Block Management

Bad Block Management is a mechanism for bad blocks implemented by the controller to detect and mark the bad blocks in the flash memory, and it uses reserved spare blocks to replace the bad blocks to prevent the data from being written into the bad block again. Bad Block Management improves the reliability and endurance of data access.

2.7.5 Garbage Collection

Micro-SD uses the storage technology of flash memory (NAND flash). The principle of Micro-SD is that the controller stores the data to be written in the Flash memory. When writing data, the Micro-SD must first erase the data in the old block before writing new data. That is, the new data cannot directly cover the old invalid data. For Micro-SD, Garbage Collection refers to the process of re-transferring existing data to other NAND flash locations and erasing useless data.

2.7.6 Over Provisioning

OP is a firmware technology, mainly reserved by a part of the hard disk storage capacity in the physical partition of the Micro-SD for the controller to use as cache. Over-provisioning improves performance and increases the endurance of a Micro-SD, helping to extend the life of a hard drive.

2.7.7 Wear Leveling

For today's NAND flash devices, the main limitation is Program/Erase lifespan (number of P/E cycles). The key solution for this constraint is to manage the attrition rate in the entire NAND flash device so that each block will be evenly distributed. Therefore, efficient management of wear in whole blocks is required in order to maximize the lifespan of a NAND flash device. To accomplish this, one method is to manage the P/E cycle of each block individually, which will help to regularly distribute them and avoid overlaying on some blocks. This method is called wear leveling.

3 Functional Description

3.1 Architecture

SILICON POWER'S Industrial micro SD Card is designed to operate and work as data or code storage device by NAND flash memory and its controller through SDA standard interface to host systems. Figure showed below is the device architecture of Industrial micro SD Card.

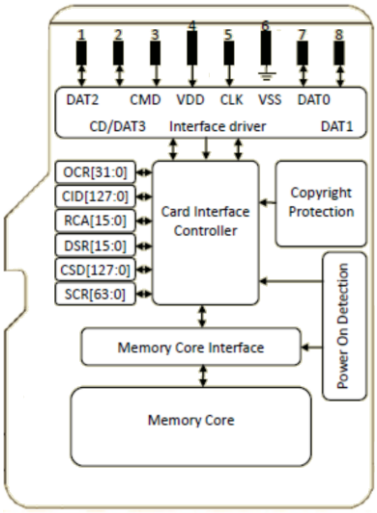

Figure 2 : Industrial microSD card block diagram

3.2 Signal Assignment

The Industrial micro SD Card has 8 pins that support two types of mode: SD Bus Mode and SPI Bus Mode. The functions of each pin in two different modes are listed in the following table. The location of the pins is showed in Figure 3.

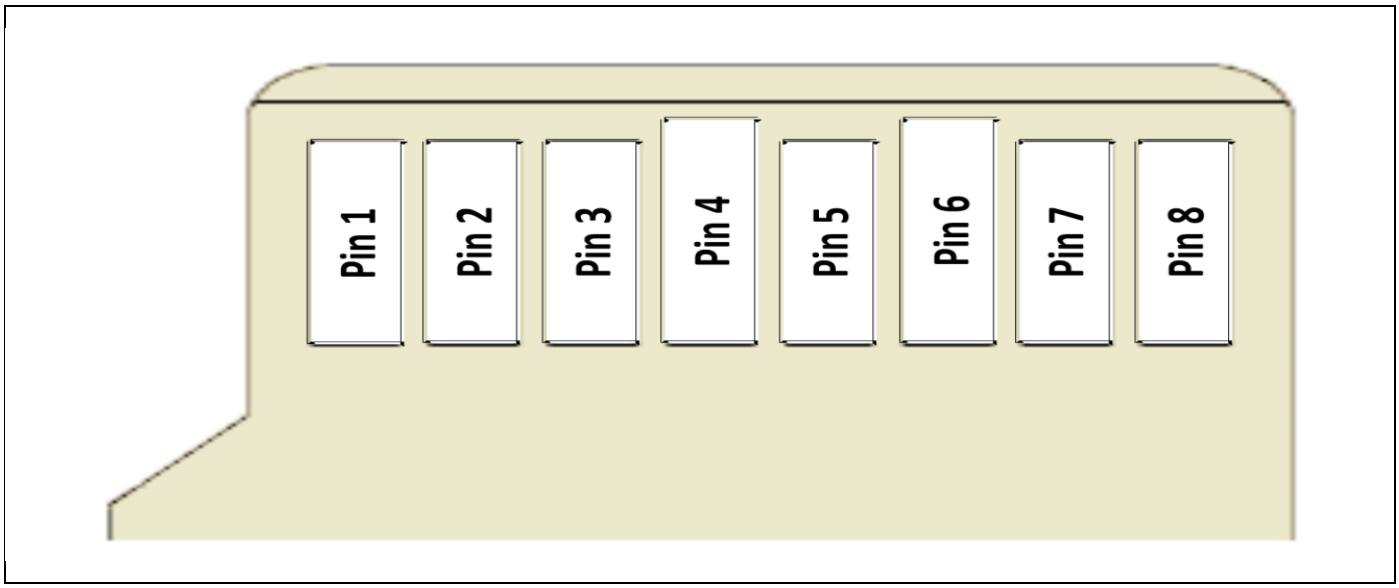

Figure 3 : Micro SD Memory Card Pin Assignment

Table 6 : Micro SD Memory Card Pin Assignment

Mode	SD Wide (4 bit) Mode			SPI Mode		
Pin NO	Name	Type[1]	Description	Name	Type[1]	Description
1	DAT2[2]	I/O/PP	Data Line (Bit 2)	RSV	-	Reserved
2	CD/DAT3[2]	I/O/PP[3]	Card Detect/Data Line (Bit 3)	CS	I	Chip Select (negative true)
3	CMD	PP	Command/Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0[2]	I/O/PP	Data Line (Bit 0)	DO	O/PP	Data Out
8	DAT1[2]	I/O/PP	Data Line (Bit 1)	RSV	-	Reserved

Notice:

1. S: power supply, I: input, O: output using push-pull drivers, PP: I/O using push-pull drivers.

2. The extended DAT lines (DAT1-DAT3) are input on power on. They start to operate as DAT lines after SET_BUS-WIDTH command. The Host shall keep its own DAT1 -DAT3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to MultiMediaCards.

3. After power on this line is input with 50Kohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

3.3 Bus Operation Conditions for 3.3V Signaling List

Table 7 : Threshold Level for High Voltage

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75* V_{DD}		V	I_{OH}=2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.125* V_{DD}	V	I_{OL}=2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625* V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.25* V_{DD}	V	
Power Up Time			250	ms	From 0V to $V_{DD\ min}$

Table 8 : Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Peak voltage on all lines		-0.3	V_{DD}+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

Table 9 : Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	KΩ	To prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card C_{HOST}+C_{BUS} shall not exceed 30pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal inductance			16	nH	
Pull-up resistance inside card	R_{DAT3}	10	90	KΩ	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

Table 10 : Threshold Level for High Voltage

Parameter	Symbol	Min	Max	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4		V	I_{OH}=2mA $V_{DD\ min}$
Output Low Voltage	V_{OL}		0.45	V	I_{OL}=2mA $V_{DD\ min}$
Input High Voltage	V_{IH}	1.27	2.0	V	
Input Low Voltage	V_{IL}	V_{ss}-0.3	0.58	V	

Table 11 : Peak Voltage and Leakage Current

Parameter	Symbol	Min	Max	Unit	Remark
Input Leakage Current		-2	2	uA	DAT3 pull-up is

3.4 System Bus Topology

The SD Bus Mode has a star topology with a single master and multiple slaves. It defines two alternative communication protocols: SD and SPI. Applications can choose either one of modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. Therefore, applications that use only one communication mode do not have to be aware of the other.

SD Memory Card System Bus Topology

The SD bus includes the following signals:

- **CLK:** Host to card clock signal
- **CMD:** Bi-directional Command/Response signal
- **DAT0 - DAT3:** 4 Bi-directional data signals.
- **VDD, VSS1, VSS2:** Power and ground signals.

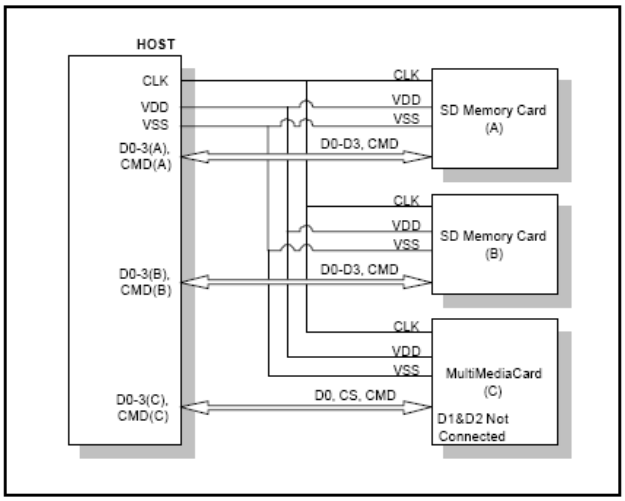

Figure 4 : Micro SD Memory Card System SPI Mode Bus Topology

Another SPI common characteristic is byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a Chip Select (CS) signal. There are no broadcast commands. For each command, a card (slave) is selected by asserting (active low) the CS signal.

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can desert the CS signal without affecting the programming process.

The SPI interface uses the 7 out of the SD 9 signals (DAT1 and DAT 2 are not used, DAT3 is the CS signal) of the SD bus.

3.5 SD Bus Protocol

3.5.1 SD Bus Protocol

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- **Command**: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.

- **Response**: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.

- **Data**: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

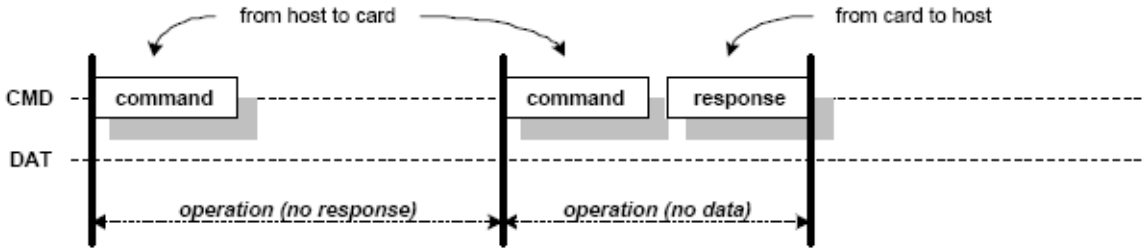

Figure 5 : SD Bus “no response ” and “no data” Operations

Card addressing is implemented using a session address, assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction. This type of bus transactions transfers their information directly within the command or response structure. In addition, some operations have a data token.

Data transfers to/from the SD Memory Card are done in blocks. Data blocks are always succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines (as long as the card supports this feature).

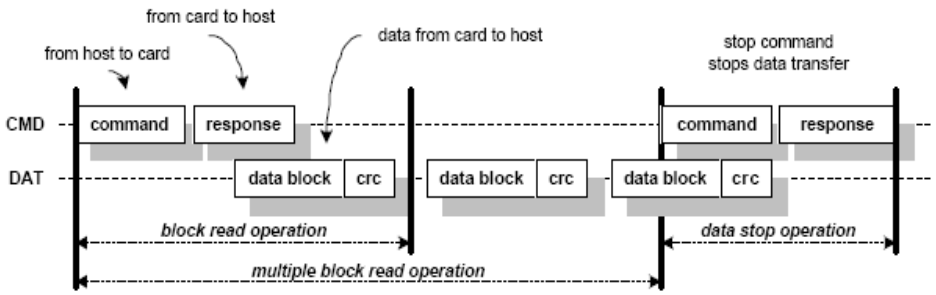

Figure 6 : SD Bus (Multiple) Block read Operation

The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line regardless of the number of data lines used for transferring the data.

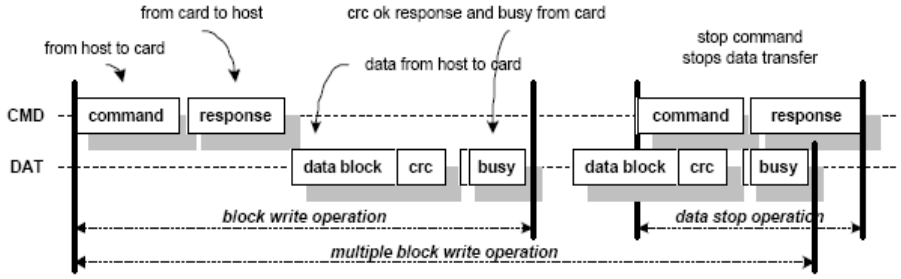

Figure 7 : SD Bus (Multiple) Block Write Operation

Command tokens have the following coding scheme:

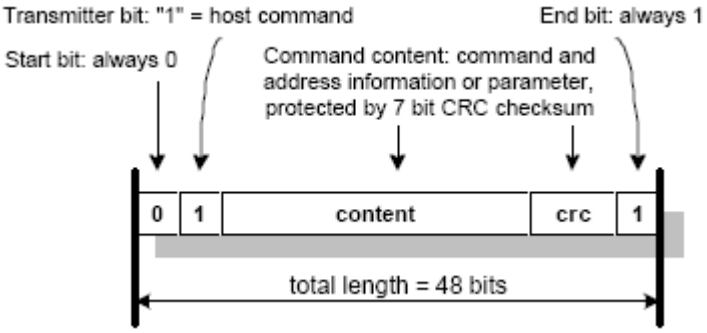

Figure 8 : SD Bus Command Token Format

Each command token is preceded by a start bit (0') and succeeded by an end bit (1'). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected, and the operation may be repeated.

Response tokens have four coding schemes depending on their content. The token length is either 48 or 136 bits. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

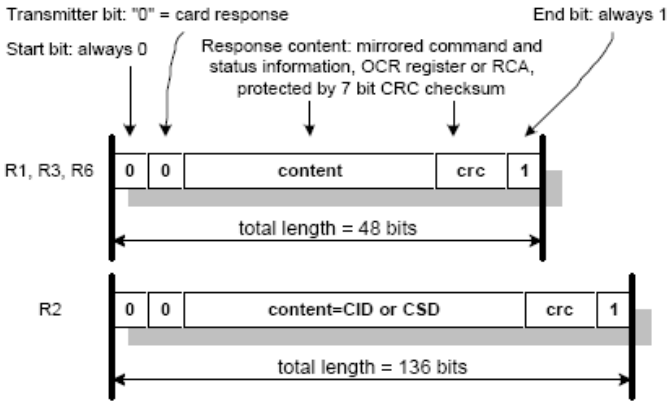

Figure 9 : SD Bus Response Token Format

In the CMD line, the MSB bit is transmitted first and the LSB bit is the last. When the wide bus option is used, the data is transferred 4 bits at a time. Start and end bits, as well as the CRC bits, are transmitted for each one of the DAT lines. CRC bits are calculated and checked for each DAT line individually.

The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 are don't care during that period).

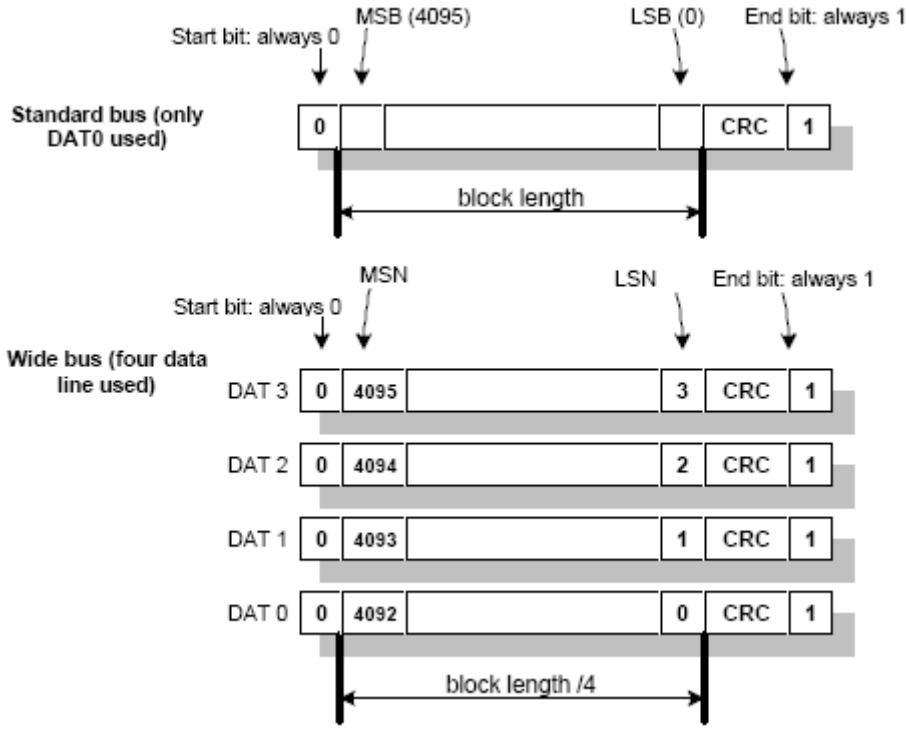

Figure 10 : SD Bus Data Packet Format

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3.5.2 SPI Bus Protocol

While the SD channel is based on command and data bit streams, which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Each command or data block is composed of 8-bit bytes and is byte aligned to the CS signal (i.e. the length is a multiple of 8 clock cycles).

Similar to the SD protocol, the SPI messages consist of command, response and data-block tokens. All communication between host and cards are controlled by the host (master). The host starts each bus transaction by asserting the CS signal low.

The response behavior in the SPI mode differs from the SD mode in the following three aspects:

- The selected card always responds to the command.
- Two new (8 & 16 bit) response structures are used
- When the card encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than a time-out as in the SD mode.

In addition to the command response, each data block sent to the card during write operations will be responded with a special data response token.

- Data Read

Single and multiple blocks read commands are supported in SPI mode. However, in order to comply with the SPI industry standard, only two (unidirectional) signals are used. Upon reception of a valid read command, the card will respond with a response token followed by a data token of the length defined in a previous SET_BLOCKLEN (CMD16) command. A multiple block read operation is terminated, similar to the SD protocol, with the STOP_TRANSMISSION command.

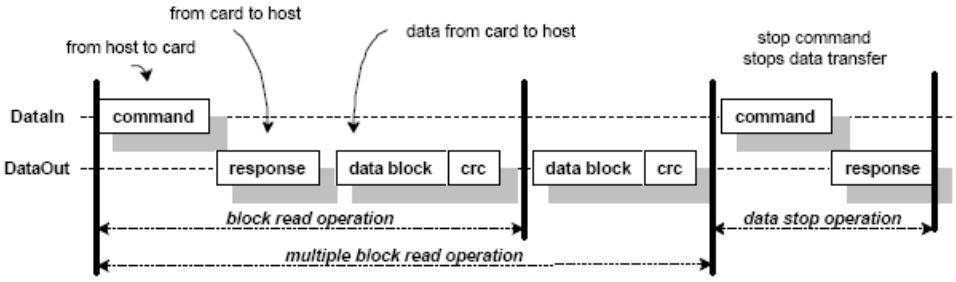

Figure 11 : SPI mode Data read

A valid data block is suffixed with a 16 bit CRC generated by the standard CCITT polynomial x16+x12+x5+1. In case of a data retrieval error, the card will not transmit any data. Instead, a special data error token will be sent to the host. Figure shows a data read operation, which terminated with an error token rather than a data block.

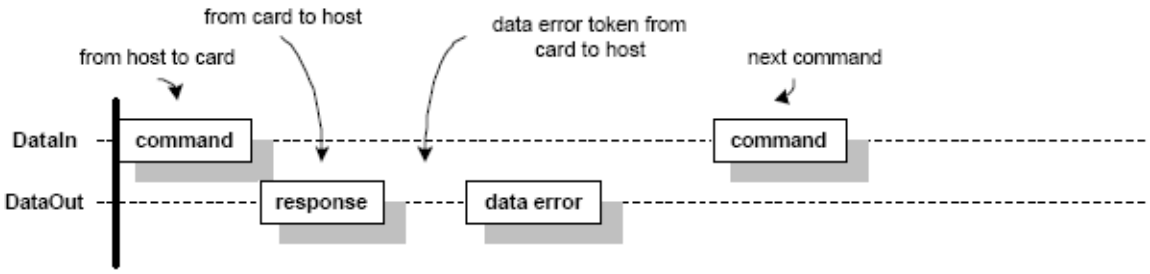

Figure 12 : SPI mode Read Operation - Data Error

- Data Write

Single and multiple blocks write operations are supported in SPI mode. Upon reception of a valid write command, the card will respond with a response token and will wait for a data block to be sent from the host. CRC suffix, block length and start address restrictions are identical to the read operation.

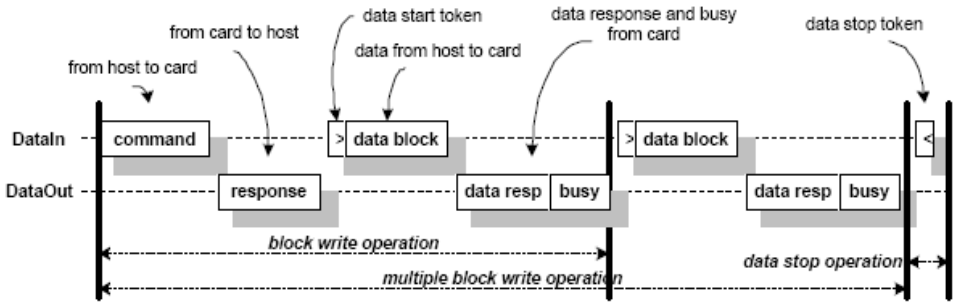

Figure 13 : SPI mode Write Operation

After a data block has been received, the card will respond with a data-response token. If the data block has been received without errors, it will be programmed. As long as the card is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

3.6 Command Set

The following shows the supported SD command set

Table 12 : SD Bus Mode Commands

CMD Index	Abbreviation	Functional Condition	Note
SD Bus Mode Command			
CMD0	GO_IDLE_STATE	+	
CMD2	ALL_SEND_CID	+	
CMD3	SEND_RELATIVE_ADDR	+	
CMD4	SET_DSR	-	1
CMD7	SELECT/DESELECT_CARD	+	
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD15	GO_INACTIVE_STATE	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	2
CMD29	CLR_WRITE_PROT	-	2
CMD30	SEND_WRITE_PROT	-	2
CMD32	ERASE_WR_BLK_START	+	
CMD33	ERASE_WR_BLK_END	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	3
CMD55	APP_CMD	+	
CMD56	GEN_CMD	+	4
Application-specific Commands			
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	5
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	5
ACMD26	SECURE_WRITE_MKB	+	5
ACMD38	SECURE_ERASE	+	5
ACMD41	SD_SEND_OP_COND	+	
ACMD42	SET_CLR_CARD_DELECT	+	
ACMD43	GET_MKB	+	5
ACMD44	GET_MID	+	5
ACMD45	SET_CER_RN1	+	5
ACMD46	GET_CER_RN2	+	5
ACMD47	SET_CER_RES2	+	5
ACMD48	GET_CER_RES1	+	5
ACMD49	CHANGE_SECURE_AREA	+	5
ACMD51	SEND_SCR	+	6

CMD Index	Abbreviation	Functional Condition	Note
NOTE: + used, - not used 1. CMD4 is a DSR register, which is optional. 2. CMD28, CMD29 and CMD30 are not mandatory to support all SD Memory Cards. The High Capacity SD Card does not support these commands. 3. This command (CMD42) is optional in Version 1.0 and 1.1, but it is mandatory in Version 2.0. 4. This command (CMD56) is used to transfer/ get a data block to/ from the card. In a Standard Capacity SD Memory Card, the size of data block is set by the SET_BLOCKLEN command. In a High Capacity SD Memory Card, the size of data block is fixed to 512bytes. RD/WR=1 is for reading data from the card. RD/WR=0 is for writing data to the card. 5. These commands are defined in SD Security Specification. 6. This command (ACMD51) is used to read the SD Configuration Register (SCR). This register is supposed to be set by the SD Memory Card manufacturer.			

3.6.1 SPI Bus Mode Command Set

The following shows the supported SPI mode command set

Table 13 : SPI Bus Mode Commands

CMD Index	Abbreviation	Functional Condition	Note
SPI Bus Mode Commands			
CMD0	GO_IDLE_STATE	+	
CMD1	SEND_OP_COND	+	1
CMD6	SWITCH_FUNC	+	2
CMD9	SEND_CSD	+	
CMD10	SEND_CID	+	
CMD12	STOP_TRANSMISSION	+	
CMD13	SEND_STATUS	+	
CMD16	SET_BLOCKLEN	+	
CMD17	READ_SINGLE_BLOCK	+	
CMD18	READ_MULTIPLE_BLOCK	+	
CMD24	WRITE_BLOCK	+	
CMD25	WRITE_MULTIPLE_BLOCK	+	
CMD27	PROGRAM_CSD	+	
CMD28	SET_WRITE_PROT	-	3
CMD29	CLR_WRITE_PROT	-	3
CMD30	SEND_WRITE_PROT	-	3
CMD32	ERASE_WR_BLK_START_ADDR	+	
CMD33	ERASE_WR_BLK_END_ADDR	+	
CMD38	ERASE	+	
CMD42	LOCK_UNLOCK	+	4
CMD55	APP_CMD	+	
CMD56	GEN_CMD	+	5
CMD58	READ_OCR	+	
CMD59	CRC_ON_OFF	+	
Application-specific Commands			
ACMD6	SET_BUS_WIDTH	+	
ACMD13	SD_STATUS	+	
ACMD18	SECURE_READ_MULTI_BLOCK	+	6
ACMD22	SEND_NUM_WR_BLOCKS	+	
ACMD23	SET_WR_BLK_ERASE_COUNT	+	
ACMD25	SECURE_WRITE_MULTI_BLOCK	+	6
ACMD26	SECURE_WRITE_MKB	+	6
ACMD38	SECURE_ERASE	+	6
ACMD41	SEND_OP_COND	+	
ACMD42	SET_CLR_CARD_DETECT	+	

CMD Index	Abbreviation	Functional Condition	Note
ACMD43	GET_MKB	+	6
ACMD44	GET_MID		6
ACMD45	SET_CER_RN1	+	6
ACMD46	GET_CER_RN2	+	6
ACMD47	SET_CER_RES2	+	6
ACMD48	GET_CER_RES1	+	6
ACMD49	CHANGE_SECURE_AERA	+	6
ACMD51	SEND_SCR	+	6

NOTE: +used, -not used

1. CMD1 is only valid for the thin (1.4mm) Standard SD Memory Card.
2. CMD6 is added in SD Specification Version 2.0.
3. CMD28, CMD29 and CMD30 are not mandatory to support all SD Memory Card. The High Capacity SD Card does not support these commands.
4. This command (CMD42) is optional in version 1.0 and 1.1, but it is mandatory in Version 2.0.
5. This command (CMD56) is used to transfer/get a data block to/from the card. In a Standard Capacity SD Memory Card, the size of data block is set by the SET_BLOCKLEN command. In a High Capacity SD Memory Card, the size of data block is fixed to 512 bytes. RD/WR=1 is for reading data from the card. RD/WR=0 is for writing data to the card.
6. These commands are defined in SD Security Specification.
7. This command (ACMD51) is used to read the SD Configuration Register (SCR). This register is supposed to be set by the SD Memory Card manufacturer.

3.6.2 S.M.A.R.T

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an special function that allows a memory device to automatically monitor its health. Silicon-Power provides a program named SP toolbox Tool to observe Silicon-Power's SD and microSD cards. Note that this tool can only support Silicon-Power's industrial SD and microSD cards. This tool will display the controller version, firmware version, endurance life ratio, spare block, and so forth.

Notice:

For more information about S.M.A.R.T., please contact Silicon Power.

4 Ordering Information

4.1 Part Number Definition

Table 14 : Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	1	2	8	G	I	S	D	T	5	R	5	N	W	0

Code 1-2: Brand	SP: Silicon Power
Code 3-6: Capacity	04G: 4GB; 08G:8GB; 16G: 16GB; 32G: 32GB; 64G: 64GB; 128G: 128GB
Code 7: Product	I: Industrial Grade Product
Code 8-10: Type & Form Factor	SDT: microSD
Code 11-13: Model Series	5R5/5R8: pSLC (SanDisk/YMTC)
Code 14: Series	N: Normal
Code 15: Operation Temperature	E: Normal temperature -25°C to +85°C W: Wide temperature -40°C to +85°C
Code 16: Reserved	0: Standard
Code 17-18	For Customization

4.2 Standard SDT5R0 Series Information

Capacity	Part Number	BOM Code	Description	R/W Performance Maximum (MB/s)
Normal Temperature (-25°C ~ 85°C)				
8GB	SP008GISDT5R5NE0	008GISDT5R5NE0-020	BiCS4 256Gb*1 Firmware: A0115	97/83(MB/s)
		008GISDT5R5NE0-030	BiCS4 256Gb*1 Firmware: B0721	97/83(MB/s)
		008GISDT5R5NE0-040	BiCS5 512Gb*1 Firmware: B0721	97/83(MB/s)
16GB	SP016GISDT5R5NE0	016GISDT5R5NE0-020	BiCS4 512Gb*1 Firmware: A0115	97/83(MB/s)
		016GISDT5R5NE0-030	BiCS4 256Gb*2 Firmware: A0115	97/83(MB/s)

Capacity	Part Number	BOM Code	Description	R/W Performance Maximum (MB/s)
		016GISDT5R5NE0-040	BiCS4 512Gb*1 Firmware: B0721	97/83(MB/s)
		016GISDT5R5NE0-050	BiCS4 256Gb*2 Firmware: B0721	97/83(MB/s)
		016GISDT5R5NE0-060	BiCS5 512Gb*1 Firmware: B0721	97/83(MB/s)
32GB	SP032GISDT5R5NE0	032GISDT5R5NE0-020	BiCS4 512Gb*2 Firmware: A0115	97/83(MB/s)
		032GISDT5R5NE0-030	BiCS4 512Gb*2 Firmware: B0721	97/83(MB/s)
		032GISDT5R5NE0-040	BiCS5 512Gb*2 Firmware: B0721	97/83(MB/s)
64GB	SP064GISDT5R5NE0	064GISDT5R5NE0-020	BiCS4 512Gb*4 Firmware: A0115	97/83(MB/s)
		064GISDT5R5NE0-030	BiCS4 512Gb*4 Firmware: B0721	97/83(MB/s)
		064GISDT5R5NE0-040	BiCS5 512Gb*4 Firmware: B0721	97/83(MB/s)
Wide Temperature (-40°C ~ 85°C)				
4GB	SP004GISDT5R5NW0	004GISDT5R5NW0-010	BiCS4 256Gb*1 Firmware: B0721	97/83(MB/s)
8GB	SP008GISDT5R5NW0	008GISDT5R5NW0-010	BiCS4 256Gb*1 Firmware: B0721	97/83(MB/s)
		008GISDT5R5NW0-020	BiCS5 512Gb*1 Firmware: B0721	93/77(MB/s)
8GB	SP008GISDT5R8NW0	008GISDT5R8NW0-010	YMTC X1 256Gb*1 Firmware: B0721	97/83(MB/s)
16GB	SP016GISDT5R5NW0	016GISDT5R5NW0-010	BiCS4 512Gb*1 Firmware: B0721	97/83(MB/s)
		016GISDT5R5NW0-020	BiCS4 256Gb*2 Firmware: B0721	97/83(MB/s)
		016GISDT5R5NW0-030	BiCS5 512Gb*1 Firmware: B0721	97/83(MB/s)
32GB	SP032GISDT5R5NW0	032GISDT5R5NW0-010	BiCS4 512Gb*2 Firmware: B0721	97/83(MB/s)
		032GISDT5R5NW0-020	BiCS5 512Gb*2 Firmware: B0721	97/83(MB/s)

Capacity	Part Number	BOM Code	Description	R/W Performance Maximum (MB/s)
		032GISDT5R5NW0-030	BiCS5 512Gb*2 Firmware: E1224	97/83(MB/s)
64GB	SP064GISDT5R5NW0	064GISDT5R5NW0-010	BiCS4 512Gb*4 Firmware: B0721	97/83(MB/s)
		064GISDT5R5NW0-020	BiCS5 512Gb*4 Firmware: B0721	97/83(MB/s)
128GB	SP128GISDT5R5NW0	128GISDT5R5NW0-010	BiCS5 512Gb*8 Firmware: E0821	92/83(MB/s)

4.3 Appendix

Table 15 : Abbreviation

Item	Abbreviation	Description
1	TBW	Tera Byte Write
2	MTBF	Mean Time Between Failures
3	LDPC	Low Density Parity Check
4	ECC	Error Correction Code
5	SMART	Self-Monitoring Analysis and Reporting Technology
6	SLC	Single-Level Cell
7	SSD	Solid State Disk
8	OP	Over Provisioning
9	PS	Power Shield
10	DC	Direct Current
11	LED	Light Emitting Diode
12	PE	Program/Erase
13	WAF	Write Amplification Factor
14	WLE	Wear Leveling Efficiency
15	LBA	Logical Block Address

Contact Information

Silicon Power Computer & Communications Incorporation, a solid state memory or storage business company, provides total solutions in the design and marketing of SSD, Flash Module, and Industry Card products. For further supporting or detail information related to the products, please inform us through the following contact email address: isupport@silicon-power.com. We will response the requests soon.