

TLD7002-16ES

User manual

LITIX™ Pixel Rear
Multi-channel LED driver
Z8F80149299

About this document

Scope and purpose

In the following chapters, the OTP registers and the volatile registers are described. The relations between the static OTP configuration and the run time configuration are reported. Both register types are accessible via the high speed lighting interface (HSLI).

Intended audience

Software engineers, hardware engineers

Table of contents

	About this document	1
	Table of contents	2
1	Register functional description	5
1.1	Output channels duty cycle	6
1.2	Output channels current and slew rate set	6
1.3	ADC conversion registers	7
1.4	Diagnosis feedback registers	7
1.5	Diagnosis configuration registers	8
1.6	HSLI interface configuration	9
1.7	OTP register key for emulation and write	10
1.8	OTP emulation and write procedure status	10
1.9	Outputs duty cycle values stored in the OTP memory	10
1.10	Output PWM frequency and phase shift	11
1.11	Voltage regulator feedback feature	11
1.12	Power shift feature	12
1.13	GPINn configuration	13
1.14	CRC protection	13
2	Register Overview - HSLI (ascending Address)	14
3	Volatile registers	17
3.1	LD_PWM_DC_CFG	18
3.2	LD_PWM_DAC_CFG	19
3.3	DIAG_SLS_CFG	20
3.4	TH_OVLD_CFG	21
3.5	LD_ADC_VFWD	22
3.6	VLED	23
3.7	VS	24
3.8	VOUT_MIN	25
3.9	VGPIN0	26
3.10	VGPIN1	27
3.11	OVLD Status	28
3.12	DTS Status	29
3.13	Reconfirmation status	30
3.14	PMU Diagnostic	31
3.15	HSLI Timing	32
3.16	OTP_EMULATION	33
3.17	OTP_WRITE	34
3.18	OTP_STATUS	35
4	OTP registers	37

Table of contents

4.1	OTP_PWM_DC_GPIN1_0	37
4.2	OTP_PWM_DC_GPIN1_1	38
4.3	OTP_PWM_DC_GPIN1_2	39
4.4	OTP_PWM_DC_GPIN1_3	40
4.5	OTP_PWM_DC_GPIN1_4	41
4.6	OTP_PWM_DC_GPIN1_5	42
4.7	OTP_PWM_DC_GPIN1_6	43
4.8	OTP_PWM_DC_GPIN1_7	44
4.9	OTP_PWM_DC_GPIN0_0	45
4.10	OTP_PWM_DC_GPIN0_1	46
4.11	OTP_PWM_DC_GPIN0_2	47
4.12	OTP_PWM_DC_GPIN0_3	48
4.13	OTP_PWM_DC_GPIN0_4	49
4.14	OTP_PWM_DC_GPIN0_5	50
4.15	OTP_PWM_DC_GPIN0_6	51
4.16	OTP_PWM_DC_GPIN0_7	52
4.17	OTP_CH_SAFE_STATE	53
4.18	OTP_CH_ISET_0	54
4.19	OTP_CH_ISET_1	55
4.20	OTP_CH_ISET_2	56
4.21	OTP_CH_ISET_3	57
4.22	OTP_CH_ISET_4	58
4.23	OTP_CH_ISET_5	59
4.24	OTP_CH_ISET_6	60
4.25	OTP_CH_ISET_7_DEV_CFG	61
4.26	OTP_PWM_PHASE_EN	62
4.27	OTP_CUST_CFG0	63
4.28	OTP_CUST_CFG1	65
4.29	OTP_CUST_CFG2	66
4.30	OTP_CUST_CFG3	67
4.31	OTP_CUST_CFG4	68
4.32	OTP_CUST_CFG5	69
4.33	OTP_CUST_CFG6	70
4.34	OTP_CUST_CFG7	71
4.35	OTP_SLAVE_ID	73
4.36	OTP_CUST_SGN	74
4.37	OTP_CUST_CFG8	75
4.38	OTP_CUST_CFG9	77
4.39	OTP_CUST_CFG10	78
4.40	OTP_CUST_CFG11	79
4.41	OTP_LOG_WORD0	80
4.42	OTP_LOG_WORD1	81

Table of contents

4.43	OTP_LOG_WORD2	82
4.44	OTP_LOG_WORD3	83
5	List of abbreviations	84
	References	85
	Revision history	86
	Disclaimer	87

1 Register functional description

1 Register functional description

The TLD7002-16 has 63 volatile registers used for real time monitor/control and 40 OTP permanent configuration registers. In addition there are 4 OTP log words used by the device to log the OTP programming result. The OTP memory is loaded into the device configuration at the state/mode transition IDLE to INIT and the integrity of the safety-relevant contents is checked with a 16-bit CRC protection word.

The OTP memory can be written only once but because of the emulation procedure, it is possible to test the desired configuration before permanently writing into the device. The emulated configuration is reset with a power cycle. For details on Emulation and OTP write please refer to OTP programming procedure application note. [\[3\]](#)

Several volatile registers are filled with OTP register content during IDLE to INIT transition as shown in the table below.

Table 1 Volatile register to OTP register relation

Volatile register	Bitfields copied from OTP to volatile registers during IDLE to INIT transition
LD_PWM_DAC_CFG0	OTP_CH_ISET_0.ISET_OUT0[5:0] --> LD_PWM_DAC_CFG0.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG0.CH_RAMP_EN[8]
LD_PWM_DAC_CFG1	OTP_CH_ISET_0.ISET_OUT1[11:6] --> LD_PWM_DAC_CFG1.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG1.CH_RAMP_EN[8]
LD_PWM_DAC_CFG2	OTP_CH_ISET_1.ISET_OUT2[5:0] --> LD_PWM_DAC_CFG2.DAC_CONFIG1[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG2.CH_RAMP_EN[8]
LD_PWM_DAC_CFG3	OTP_CH_ISET_1.ISET_OUT3[11:6] --> LD_PWM_DAC_CFG3.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG3.CH_RAMP_EN[8]
LD_PWM_DAC_CFG4	OTP_CH_ISET_2.ISET_OUT4[5:0] --> LD_PWM_DAC_CFG4.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG4.CH_RAMP_EN[8]
LD_PWM_DAC_CFG5	OTP_CH_ISET_2.ISET_OUT5[11:6] --> LD_PWM_DAC_CFG5.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG5.CH_RAMP_EN[8]
LD_PWM_DAC_CFG6	OTP_CH_ISET_3.ISET_OUT6[5:0] --> LD_PWM_DAC_CFG6.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG6.CH_RAMP_EN[8]
LD_PWM_DAC_CFG7	OTP_CH_ISET_3.ISET_OUT7[11:6] --> LD_PWM_DAC_CFG7.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG7.CH_RAMP_EN[8]
LD_PWM_DAC_CFG8	OTP_CH_ISET_4.ISET_OUT8[5:0] --> LD_PWM_DAC_CFG8.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG8.CH_RAMP_EN[8]
LD_PWM_DAC_CFG9	OTP_CH_ISET_4.ISET_OUT9[11:6] --> LD_PWM_DAC_CFG9.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG9.CH_RAMP_EN[8]
LD_PWM_DAC_CFG10	OTP_CH_ISET_5.ISET_OUT10[5:0] --> LD_PWM_DAC_CFG10.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG10.CH_RAMP_EN[8]
LD_PWM_DAC_CFG11	OTP_CH_ISET_5.ISET_OUT11[11:6] --> LD_PWM_DAC_CFG11.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG11.CH_RAMP_EN[8]
LD_PWM_DAC_CFG12	OTP_CH_ISET_6.ISET_OUT12[5:0] --> LD_PWM_DAC_CFG12.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG12.CH_RAMP_EN[8]
LD_PWM_DAC_CFG13	OTP_CH_ISET_6.ISET_OUT13[11:6] --> LD_PWM_DAC_CFG13.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG13.CH_RAMP_EN[8]

(table continues...)

1 Register functional description

Table 1 (continued) Volatile register to OTP register relation

LD_PWM_DAC_CFG14	OTP_CH_ISET_7.ISET_OUT14[5:0] --> LD_PWM_DAC_CFG14.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG14.CH_RAMP_EN[8]
LD_PWM_DAC_CFG15	OTP_CH_ISET_7.ISET_OUT15[11:6] --> LD_PWM_DAC_CFG15.DAC_CONFIG[5:0] OTP_CUST_CFG9.RAMP_EN[7] --> LD_PWM_DAC_CFG15.CH_RAMP_EN[8]
DIAG_SLS_CFG	OTP_CUST_CFG3.SLS_TH0[7:0] --> DIAG_SLS_CFG.SLS_TH0[7:0] OTP_CUST_CFG3.SLS_TH1[15:8] --> DIAG_SLS_CFG.SLS_TH1[15:8]
HSLI_TIMING	OTP_CUST_CFG9.HSLI_T_BIT_SMPL[1:0] --> HSLI_TIMING_CFG.BIT_SMPL_ADJ[1:0] OTP_CUST_CFG9.HSLI_T_SYNC_BREAK[3:2] --> HSLI_TIMING_CFG.SYNC_BRK_ADJ[3:2] OTP_CUST_CFG9.HSLI_T_FRAME_DLY[6:4] --> HSLI_TIMING_CFG.FRM_DLY_ADJ[6:4]

1.1 Output channels duty cycle

The register LD_PWM_DC_CFGi contains the duty cycle values ready to be applied to the outputs using the "DC_SYNC" HSLI frame.

If the outputs duty cycle are updated writing these registers via a "WRITE_REG" HSLI frame, the device reports a duty cycle warning if the values are 20% lower with respect to the values set via the "DC_UPDATE" HSLI frame.

The suggested way to update the duty cycle values is to use the "DC_UPDATE" HSLI frame.

Related reference

[LD_PWM_DC_CFG](#) on page 18

1.2 Output channels current and slew rate set

The output channels current and slew rate are defined in the OTP memory and loaded automatically at the transition IDLE to INIT in the LED driver configuration (registers OTP_CH_ISET and property RAMP_EN in the register OTP_CUST_CFG9).

Once loaded, the values can be updated dynamically via the HSLI interface (registers LD_PWM_DAC_CFGi) but the following considerations must be taken into account:

LD_PWM_DAC_CFGi: Writing these HSLI registers, it is possible to change the output currents updating the value loaded from the OTP memory. If the written DAC_CONFIGi value is lower than 15 mA with respect to the OTP value ISET_OUTi, the device will report a current warning on these channels if they are in ON state.

OTP_CH_ISET: The OTP current values ISET_OUTi are automatically loaded at the transition IDLE to INIT in the LED driver configuration (LD_PWM_DAC_CFGi) and used at the output channels activation. These values are moreover used for the current warning mechanism. If the measured output current on channel "i" is lower than 15 mA (max) with respect to the OTP value, the device reports a current warning on these channels if they are in ON state. In order to ensure a CUR_WRN report at 15 mA (max) below the OTP target current, the actual detection threshold is set from 5.5 mA (typ) to 9 mA (typ) below the OTP target current. For example: When the current set in the OTP current value is 76.5 mA (IOUT step=63) the threshold used is 67.5 mA (IOUT step=55). Even if the output currents are updated via the volatile registers (LD_PWM_DAC_CFGi), the current warning mechanism uses the OTP target values (OTP_CH_ISETi) as reference.

Therefore in applications where the DAC_CONFIGi varies runtime via HSLI, it is recommended to set OTP_CH_ISET to the lower end of the DAC_CONFIGi range.

The integrator shall configure the DAC_CONFIGi register according to:

$$I_{OUT} = 5.625mA + DAC_CONFIGi \times 1.125mA \quad (1)$$

1 Register functional description

$$DAC_CONFIGi = (I_{OUT} - 5.625mA) / 1.125mA \quad (2)$$

Related reference

[LD_PWM_DAC_CFG](#) on page 19

[OTP_CH_ISET_0](#) on page 54

[OTP_CH_ISET_1](#) on page 55

[OTP_CH_ISET_2](#) on page 56

[OTP_CH_ISET_3](#) on page 57

[OTP_CH_ISET_4](#) on page 58

[OTP_CH_ISET_5](#) on page 59

[OTP_CH_ISET_6](#) on page 60

[OTP_CUST_CFG9](#) on page 77

1.3 ADC conversion registers

The device provides the ADC reading of the parameters in the HSLI registers listed in the related reference below.

The DTS sensor is used internally by the TLD7002-16ES for the thermal derating feature. The sensor is providing an average device temperature value. The accuracy of the DTS depends on the power distribution of the specific application. As a rule of thumb, the DTS sensor accuracy is similar to TJSTOP accuracy (PRQ452).

Related reference

[LD_ADC_VFWD](#) on page 22

[VLED](#) on page 23

[VS](#) on page 24

[VOUT_MIN](#) on page 25

[VGPI0](#) on page 26

[VGPI1](#) on page 27

[DTS Status](#) on page 29

1.4 Diagnosis feedback registers

Most of the diagnosis feedbacks are present on the output status byte and on the channel status, which are not addressable physical registers. They can be requested as a reply to a READ_OST frame (channel status byte) or as a slave reply at the end of the HSLI frame (output status byte).

Some feedbacks are instead present on addressable volatile register, which can be read with a READ_REG frame. The following diagnosis information can be collected from the volatile registers:

- Overload status of the output channels via the register TH_OVLD_STATUS
- Device internal diagnosis information via the register PMU_DIAG
- Device temperature status via the DTS_STAT register
- Device in reconfirmation status via the RECON_STAT register

If DIAG_mngt_SET=1 then RECON_STAT.RECON_FLAG is set to 1 in case of fault. This indicates that a fault is present on the output channels and the device is performing a load reconfirmation cycle.

Related reference

[OVLD Status](#) on page 28

1 Register functional description

[TH_OVLD_CFG](#) on page 21

[PMU Diagnostic](#) on page 31

[Reconfirmation status](#) on page 30

[OTP_CUST_CFG7](#) on page 71

1.5 Diagnosis configuration registers

Using the following parameters, available on OTP registers or volatile registers, it is possible to configure all the diagnosis related information of the device (e.g. reaction in case of a fault, voltage thresholds for the diagnosis activation, ...)

DIAG_DEBOUNCE (register OTP_CH_ISET_7_DEV_CFG): The value sets the debounce time (in PWM periods), for error detection. If, after the DIAG_DEBOUNCE PWM periods, a fault is still present, the device will report a fault.

LP_INIT (register OTP_CH_ISET_7_DEV_CFG): Activating LP_INIT (LP_INIT=0b1) the device enters into low power mode during the INIT state.

The LP_INIT mode is useful in case the device operates in standalone mode and diagnosis information is reported to the LCU via current consumption since, if a fault is detected, the device moves into INIT mode entering into low power mode automatically.

If the device is operating in INIT mode with LP_INIT active, the maximum HSLI baudrate is 500 kb/s and the watchdog timeout is multiplied by a factor 3.

DIAG_VDEN_VS and DIAG_VDEN_VLED (register OTP_CUST_CFG1): The two parameters set the diagnosis activation voltage threshold for the channels mapped to VS and the channels mapped to VLED respectively.

DIAG_TDELAY (register OTP_CUST_CFG1): The parameters set the delay time, from the channel activation, after which the device starts with all the measurements to perform the diagnosis on the channel. It could be useful to set a high delay time in case of oscillation in the output channel or in case of a not very stable front-end voltage regulator.

DIAG_OUT15_ERRn_EN (register OTP_CUST_CFG1): Parameter used to set OUT15 as standard output channel or as ERRN feedback report.

TH_OVLD_CFG the overload reaction and the overload status flag TH_OVLD_STATUS, can be configured using the volatile register TH_OVLD_CFG, and can be set in latched mode or auto retry mode.

SHORT_WRN_EN (register OTP_CUST_CFG2): The register is used to set in which channels the “short between adjacent pin” OUT_SHORT_WRN must be activated. If two or more channels work in parallel or if an output is not used, the warning shall be disabled in these channels.

There is a direct mapping between the bit position in the register and the outputs, so if SHORT_WRN_EN bit N is set, the short warning is enabled between output_n and output_n-1.

The short between adjacent pins is a diagnosis check used in safety applications to detect the short between the pins associated to two different functions.

If two or more channels work in parallel or in the same function or if an output is not used, the warning shall be disabled in these channels. Short warning on OUT0 shall be disabled.

The SHORT_WRN_EN is disabled by default, all constraints for this feature are present in the safety manual.

SLS_TH0 and SLS_TH1 (register OTP_CUST_CFG3): The two parameters set respectively the single LED short voltage threshold for the channels mapped to VS and for the channels mapped to VLED. The two voltage thresholds (OTP_CUST_CFG3SLS_TH0 and SLS_TH1) will automatically be loaded in the LED driver volatile register (DIAG_SLS_CFG SLS_TH0 DIAG_SLS_CFG. SLS_TH1) at the transition IDLE to INIT. At the next power cycle the device will reload the default values from the OTP memory. DIAG_SLS_LOCK (register OTP_CUST_CFG7) is used to define the source of the SLS thresholds: either from volatile register (DIAG_SLS_CFG) or locked to the OTP register (OTP_CUST_CFG3).

DIAG_OUT_GROUP (register OTP_CUST_CFG4): The register is used to set the diagnostic group of each output (VS or VLED related diagnosis).

1 Register functional description

VFWD_VLED_TH and VFWD_VS_TH (register OTP_CUST_CFG7): The two parameters set the forward voltage warning (VFWD_WRN) thresholds for VS and VLED diagnostic group respectively. This diagnosis can be used to detect a short to supply.

If the forward voltage of the LED is below the VFWD_VS_THR for more than n_{debounce} PWM periods, then the VFWD_WRN flag is set.

The forward voltage is measured as a difference from the OUTn pin and the respective supply pin (either VS and VLED, selected in the DIAG_OUT_GROUP register).

DIAG_mngt_SET (register OTP_CUST_CFG7): Parameter to set the behavior of the device in case of an external fault. If “DIAG_mngt_SET” is set to 0b1, reading the HSLI register RECON_STAT it is possible to know if the device is in the reconfirmation cycle due to a load fault. If the DIAG_mngt_SET is set to 1, and a load fault (OL, SLS, OVLD) or ERRn is recognized, the device will move to INIT switching off all the outputs and it is ready to perform a reconfirmation cycle. Load warnings (CUR_WRN, DC_WRN, VFWD_WRN, OUT_SHORT_WRN) do not trigger an INIT transition unless the DIAG_OUT15_ERRn_EN is enabled in OTP. In this last case, the INIT transition happens due to the ERRn reaction. This configuration is useful if the device operates in standalone mode without the HSLI interface (light function activated only via GPINn control). If DIAG_mngt_SET is set to 0, the outputs are not turned off in case of OL, SLS and ERRn, and the device does not moves to INIT. The LCU can take care of disabling the failing output based on the application diagnostic strategy. User shall set DIAG_OUT_SWOFF_DC100 to 0 when DIAG_mngt_SET is set to 1.

DIAG_OUT_SWOFF_DC100 (register OTP_CUST_CFG7): If the “short between adjacent channels” diagnosis is enabled in a channel with duty cycle 100%, the check cannot be performed because the device needs a cycle OFF-ON of the output to check the short.

To overcome the limitation, the parameter DIAG_OUT_SWOFF_DC100 has been implemented: if it is set to 0b1, the channels with 100% of duty cycle and short to adjacent pin diagnosis enabled will be switched off every 4 PWM periods, for a very short time to perform the diagnosis check. In order to use the automatic switch off feature on channel n, the phase shift of ch<n> (with DC=100%) and ch<n-1> shall be enabled. The automatically introduced off time, on the channel with 100% duty cycle will last up to phase shift time approximately 20 μ s. This introduced off time, being periodic and leaving high remaining duty cycle, will be very likely not perceived, but the effect has to be checked in the final application.

Note that DIAG_OUT_SWOFF_DC100 will introduce an OFF time on the channel only if the duty cycle is 100%. If the duty cycle is different from 100% (e.g. 99.9%), the automatic switch off feature is not forcing the proper duty cycle for the short to adjacent channel detection. The integrator shall, in this last case, set a duty cycle with an OFF time bigger than $t_{\text{diag_dly}} + 2 \cdot t_{\text{diag_on}}$. Detailed operational conditions are presented in the safety manual

CURR_WRN_REP_DIS (register OTP_CUST_CFG7): Parameter used to disable the report of the current warning on the ERRN output.

Related reference

[OTP_CH_ISET_7_DEV_CFG](#) on page 61

[OTP_CUST_CFG1](#) on page 65

[OTP_CUST_CFG2](#) on page 66

[OTP_CUST_CFG3](#) on page 67

[OTP_CUST_CFG4](#) on page 68

1.6 HSLI interface configuration

The HSLI configuration is stored in the OTP memory (register OTP_CUST_CFG9) and can be updated via the HSLI interface (register HSLI_TIMING_CFG).

At every start-up, the devices will load in the volatile registers the values from the OTP memory.

1 Register functional description

HSLI_T_BITSMPL or BIT_SMPL_ADJ: Contain the UART bit sampling time in the OTP register, **OTP_CUST_CFG9** and the volatile register **HSLI_TIMING_CFG**. In case of ringing or noise in the HSLI bus, it could be useful to change the sampling time of the UART interface to prevent the interference of noise in communication.

FRM_DLY_ADJ and HSLI_T_FRAME_DLY: Contain the minimum interframe delay in the volatile **HSLI_TIMING_CFG** register and **OTP_CUST_CFG9** registers. The interframe delay is the minimum timing between the end of an HSLI frame and the beginning of the next frame, which the master node shall respect. If the interframe delay is not respected, the device will discard all the frames received after the first one.

Related reference

[HSLI Timing](#) on page 32

[OTP_CUST_CFG9](#) on page 77

1.7 OTP register key for emulation and write

The volatile registers **OTP_EMULATION** and **OTP_WRITE** shall be written with the specific key to enter into emulation or write mode of the OTP memory.

The register **OTP_EMULATION** shall be written with 0x3BD2 to enter into emulation mode.

The register **OTP_WRITE** shall be written with 0xA47B to enter into write mode.

Related reference

[OTP_EMULATION](#) on page 33

[OTP_WRITE](#) on page 34

1.8 OTP emulation and write procedure status

The volatile register **OTP_STATUS**, cleared after read, can be read after each HSLI **WRITE_REG** frame during the emulation/writing OTP memory procedure, to check if the requested frame is successful.

Related reference

[OTP_STATUS](#) on page 35

1.9 Outputs duty cycle values stored in the OTP memory

In the OTP memory, it is possible to store two different duty cycle values for each output with the following purpose:

DC1_OUTi (in the registers **OTP_PWM_DC_GPIN1_0to7**)

If the **GPIN1** is configured as digital input and the device receives an outputs activation request via **GPIN1**, the duty cycle values of all and only the outputs mapped to **GPIN1** will be updated with the content of these registers.

The duty cycle value is defined by a linear 8 bit duty cycle law.

DC0_OUTi (in the registers **OTP_PWM_DC_GPIN0_0to7**)

The duty cycle values stored in these registers will be used on two different conditions:

- If the **GPIN0** is configured as digital input and the device receives an outputs activation request via **GPIN0**, the duty cycle values of all and only the outputs mapped to **GPIN0** will be updated with the content of these registers
- If the device reaches the fail-safe state, the duty cycle values of all and only the outputs mapped active in fail-safe state will be updated with the content of these registers

1 Register functional description

The duty cycle value is defined by a linear 8-bit duty cycle law.

Related reference

[OTP_PWM_DC_GPIN1_0](#) on page 37
[OTP_PWM_DC_GPIN1_1](#) on page 38
[OTP_PWM_DC_GPIN1_2](#) on page 39
[OTP_PWM_DC_GPIN1_3](#) on page 40
[OTP_PWM_DC_GPIN1_4](#) on page 41
[OTP_PWM_DC_GPIN1_5](#) on page 42
[OTP_PWM_DC_GPIN1_6](#) on page 43
[OTP_PWM_DC_GPIN1_7](#) on page 44
[OTP_PWM_DC_GPIN0_0](#) on page 45
[OTP_PWM_DC_GPIN0_1](#) on page 46
[OTP_PWM_DC_GPIN0_2](#) on page 47
[OTP_PWM_DC_GPIN0_3](#) on page 48
[OTP_PWM_DC_GPIN0_4](#) on page 49
[OTP_PWM_DC_GPIN0_5](#) on page 50
[OTP_PWM_DC_GPIN0_6](#) on page 51
[OTP_PWM_DC_GPIN0_7](#) on page 52

1.10 Output PWM frequency and phase shift

The parameter PWM_FREQ (register OTP_CUST_CFG0) is used to set the frequency of the outputs PWM (common for all the outputs).

Once the PWM frequency is defined, it is possible to define the PWM_PHASE_SHIFT parameter. This represents the phase shift time applied to activate two consecutive outputs (OUTn and OUTn+1) and it is expressed as a percentage of the PWM period.

The register OTP_PWM_PHASE_EN can be used to define the outputs that must be activated with the phase shift defined in the parameter PWM_PHASE_SHIFT.

The integrator shall configure at phase shift t_{PH} according to:

$$t_{PH} > t_{diag_dly} + 2 \cdot t_{DIAG_ON} \quad (3)$$

Related reference

[OTP_PWM_PHASE_EN](#) on page 62
[OTP_CUST_CFG0](#) on page 63

1.11 Voltage regulator feedback feature

The voltage regulator feedback feature, allows the OUT0 to set an offset on the output of an external voltage regulator. This is used to implement a voltage head room control, and optimize power dissipation. The LCU shall take care of adjusting the OUT0 current (by writing the volatile register LD_PWM_DAC_CFG0) in order to set the proper voltage head room. OUT0 shall be connected to the external voltage regulator feedback network as shown in the figure below. The OUT0 current produces an offset in addition to the external voltage regulator target. For example an IOUT0 of 9 mA with 100 Ω resistance in the voltage regulator feedback loop creates an offset of 900 mV.

1 Register functional description

CH_DCDC_OUT0_EN (register OTP_CUST_CFG0): the bit enables the headroom control feature by masking OUT0 for the min(VOUTn) measurements, in addition following diagnostic mechanism are masked out on OUT0:

- Open load detection
- Forward voltage warning (VFWD_WRN)
- Current warning (CUR_WRN)

When CH_DCDC_OUT0_EN is set, LD_ADC_VFWD0 shows the output voltage VOUT instead of the forward voltage VFWD to directly provide the feedback voltage.

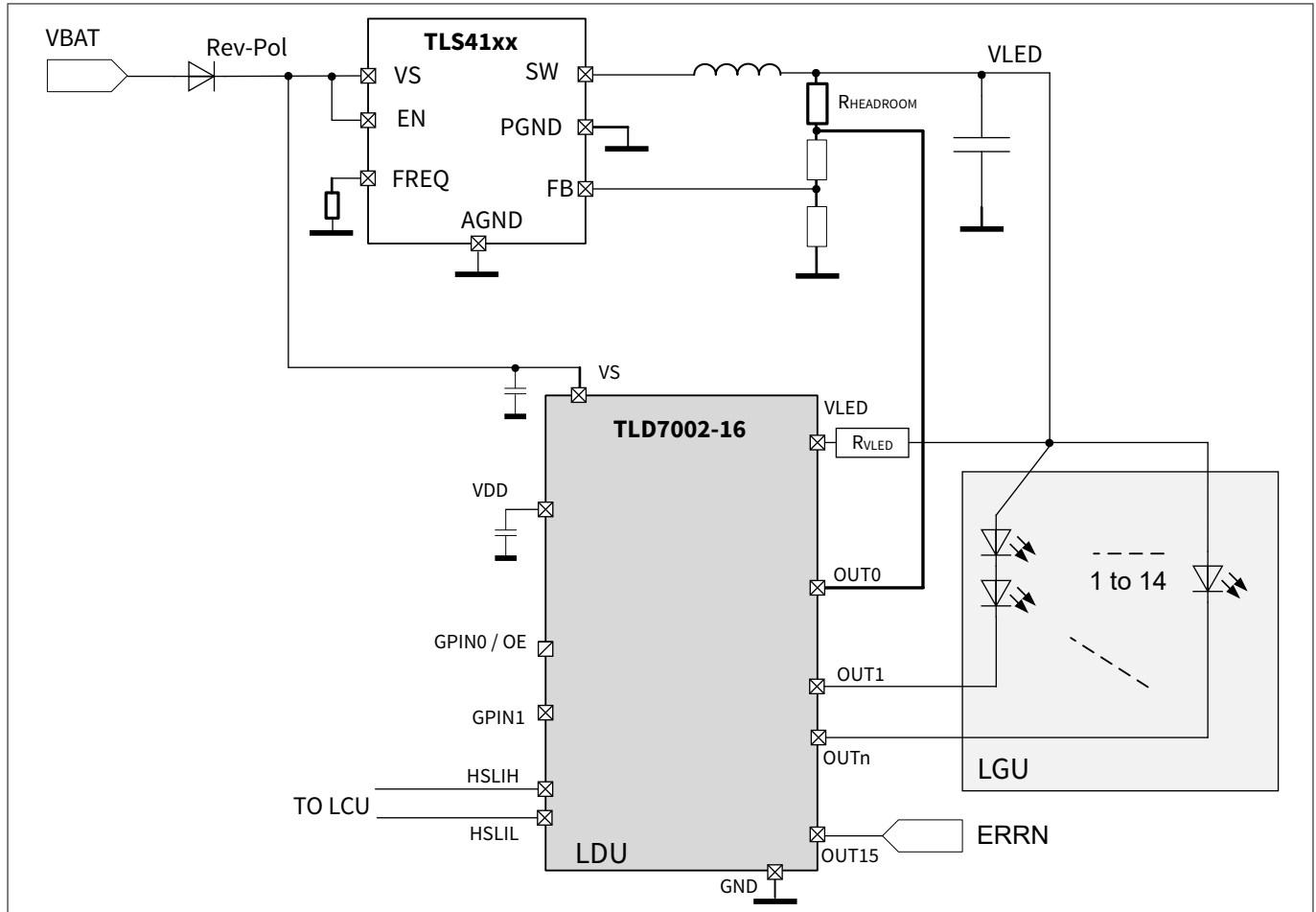


Figure 1 TLD7002-16ES system with voltage head room control (simplified schematic)

Related reference

[OTP_CUST_CFG0](#) on page 63

1.12 Power shift feature

The power shift feature (power off load) can be activated and configured using the following OTP parameters:

PWR_OFF_LOAD_EN (register OTP_CUST_CFG7): It is the global enable of the power shift

PWR_OFF_LOAD_CH_SET (register OTP_CUST_CFG8): It is the enable of the channels couples that work in parallel to implement the power shift feature

PWR_OFF_LOAD_TH_CHij_SET (register OTP_CUST_CFG8, ij = 01,23,89,1011): The parameter sets, for each channels couple, the higher voltage channel threshold within which all the current is shifted from the primary channel(0, 2, 8 and 10) to the secondary channel (1,3,9 and 11).

1 Register functional description

Related reference

[OTP_CUST_CFG7](#) on page 71

[OTP_CUST_CFG8](#) on page 75

1.13 GPINn configuration

GPIN0 and GPIN1 functionalities can be configured in the OTP memory using some properties in the register OTP_CUST_CFG0.

The mapping between outputs and GPIN0/GPIN1 for the direct control can be configured using the register OTP_CUST_CFG5 and the register OTP_CUST_CFG6 respectively.

If in the GPIN0 is set as analog input in the OTP_CUST_CFG0 register, the device cannot enter emulation mode anymore.

Related reference

[OTP_CUST_CFG0](#) on page 63

[OTP_CUST_CFG5](#) on page 69

[OTP_CUST_CFG6](#) on page 70

1.14 CRC protection

The register OTP_CUST_SGN stores the CRC protection word used by the device to check the integrity of the OTP registers from address 0x83 (register OTP_PWM_DC_GPIN1_0) to address 0xA5 (register OTP_SLAVE_ID).

The cyclic redundancy check (CRC) is calculated from the register 0x83 to register 0xA5.

The initial value (seed) is 0xFFFF and the polynomial is 0x1021.

Further details about the OTP programming procedure and the CRC calculation can be found in the OTP Programming application note [\[3\]](#) available on the website of the product.

Related reference

[OTP_CUST_SGN](#) on page 74

2 Register Overview - HSLI (ascending Address)

2 Register Overview - HSLI (ascending Address)

Table 2 Register Overview - HSLI (ascending Address)

Short Name	Long Name	Address	Page Number
LD_PWM_DC_CFGi	LD_PWM_DC_CFG	000 _{H+i}	18
LD_PWM_DAC_CFGi	LD_PWM_DAC_CFG	010 _{H+i}	19
DIAG_SLS_CFG	DIAG_SLS_CFG	020 _H	20
TH_OVLD_CFG	TH_OVLD_CFG	021 _H	21
LD_ADC_VFWDi	LD_ADC_VFWD	022 _{H+i}	22
LD_ADC_VLED	VLED	032 _H	23
LD_ADC_VS	VS	033 _H	24
LD_ADC_VOUT_MIN	VOUT_MIN	034 _H	25
LD_ADC_VGPIN0	VGPIN0	035 _H	26
LD_ADC_VGPIN1	VGPIN1	036 _H	27
TH_OVLD_STATUS	OVLD Status	037 _H	28
DTS_STAT	DTS Status	038 _H	29
RECON_STAT	Reconfirmation status	039 _H	30
PMU_DIAG	PMU Diagnostic	03A _H	31
HSLI_TIMING_CFG	HSLI Timing	03B _H	32
OTP_EMULATION	OTP_EMULATION	080 _H	33
OTP_WRITE	OTP_WRITE	081 _H	34
OTP_STATUS	OTP_STATUS	082 _H	35
OTP_PWM_DC_GPIN1_0	OTP_PWM_DC_GPIN1_0	083 _H	37
OTP_PWM_DC_GPIN1_1	OTP_PWM_DC_GPIN1_1	084 _H	38
OTP_PWM_DC_GPIN1_2	OTP_PWM_DC_GPIN1_2	085 _H	39
OTP_PWM_DC_GPIN1_3	OTP_PWM_DC_GPIN1_3	086 _H	40
OTP_PWM_DC_GPIN1_4	OTP_PWM_DC_GPIN1_4	087 _H	41
OTP_PWM_DC_GPIN1_5	OTP_PWM_DC_GPIN1_5	088 _H	42
OTP_PWM_DC_GPIN1_6	OTP_PWM_DC_GPIN1_6	089 _H	43
OTP_PWM_DC_GPIN1_7	OTP_PWM_DC_GPIN1_7	08A _H	44
OTP_PWM_DC_GPIN0_0	OTP_PWM_DC_GPIN0_0	08B _H	45

(table continues...)

2 Register Overview - HSLI (ascending Address)

Table 2 (continued) Register Overview - HSLI (ascending Address)

Short Name	Long Name	Address	Page Number
OTP_PWM_DC_GPIN0_1	OTP_PWM_DC_GPIN0_1	08C _H	46
OTP_PWM_DC_GPIN0_2	OTP_PWM_DC_GPIN0_2	08D _H	47
OTP_PWM_DC_GPIN0_3	OTP_PWM_DC_GPIN0_3	08E _H	48
OTP_PWM_DC_GPIN0_4	OTP_PWM_DC_GPIN0_4	08F _H	49
OTP_PWM_DC_GPIN0_5	OTP_PWM_DC_GPIN0_5	090 _H	50
OTP_PWM_DC_GPIN0_6	OTP_PWM_DC_GPIN0_6	091 _H	51
OTP_PWM_DC_GPIN0_7	OTP_PWM_DC_GPIN0_7	092 _H	52
OTP_CH_SAFE_STATE	OTP_CH_SAFE_STATE	093 _H	53
OTP_CH_ISET_0	OTP_CH_ISET_0	094 _H	54
OTP_CH_ISET_1	OTP_CH_ISET_1	095 _H	55
OTP_CH_ISET_2	OTP_CH_ISET_2	096 _H	56
OTP_CH_ISET_3	OTP_CH_ISET_3	097 _H	57
OTP_CH_ISET_4	OTP_CH_ISET_4	098 _H	58
OTP_CH_ISET_5	OTP_CH_ISET_5	099 _H	59
OTP_CH_ISET_6	OTP_CH_ISET_6	09A _H	60
OTP_CH_ISET_7_DEV_CFG	OTP_CH_ISET_7_DEV_CFG	09B _H	61
OTP_PWM_PHASE_EN	OTP_PWM_PHASE_EN	09C _H	62
OTP_CUST_CFG0	OTP_CUST_CFG0	09D _H	63
OTP_CUST_CFG1	OTP_CUST_CFG1	09E _H	65
OTP_CUST_CFG2	OTP_CUST_CFG2	09F _H	66
OTP_CUST_CFG3	OTP_CUST_CFG3	0A0 _H	67
OTP_CUST_CFG4	OTP_CUST_CFG4	0A1 _H	68
OTP_CUST_CFG5	OTP_CUST_CFG5	0A2 _H	69
OTP_CUST_CFG6	OTP_CUST_CFG6	0A3 _H	70
OTP_CUST_CFG7	OTP_CUST_CFG7	0A4 _H	71
OTP_SLAVE_ID	OTP_SLAVE_ID	0A5 _H	73
OTP_CUST_SGN	OTP_CUST_SGN	0A6 _H	74
OTP_CUST_CFG8	OTP_CUST_CFG8	0A7 _H	75

(table continues...)

2 Register Overview - HSLI (ascending Address)**Table 2** (continued) Register Overview - HSLI (ascending Address)

Short Name	Long Name	Address	Page Number
OTP_CUST_CFG9	OTP_CUST_CFG9	0A8 _H	77
OTP_CUST_CFG10	OTP_CUST_CFG10	0A9 _H	78
OTP_CUST_CFG11	OTP_CUST_CFG11	0AA _H	79
OTP_LOG_WORD0	OTP_LOG_WORD0	0AB _H	80
OTP_LOG_WORD1	OTP_LOG_WORD1	0AC _H	81
OTP_LOG_WORD2	OTP_LOG_WORD2	0AD _H	82
OTP_LOG_WORD3	OTP_LOG_WORD3	0AE _H	83

3 Volatile registers

3 Volatile registers

3.1 LD_PWM_DC_CFG

LD_PWM_DC_CFGi (i=0-15)

Address: 000_H + i

LD_PWM_DC_CFG

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		PWM_DCi													
r		rw													

Field	Bits	Type	Description
PWM_DCi	13:0	rw	PWM duty cycle Output duty cycle configuration 0 _D (0 _H), 0% duty cycle 16383 _D (3FFF _H), 100% duty cycle
RES	15:14	r	reserved

Related information

[Output channels duty cycle](#) on page 6

3 Volatile registers

3.2 LD_PWM_DAC_CFG

LD_PWM_DAC_CFGi (i=0-15)

Address: 010_H+i

LD_PWM_DAC_CFG

Reset value(unwritten device): 0120_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES							CH_ RAMP_ P_EN i	RES		DAC_CONFIGi					
r							rw	r		rw					

Field	Bits	Type	Description
DAC_CONFIGi	5:0	rw	Current configuration Output current configuration 0 _D (0 _H), 5 mA 63 _D (3F _H), 76.5 mA Reset value from OTP: OTP_CH_ISET_x (0-7)
RES	7:6, 15:9	r	reserved
CH_RAMP_ENi	8	rw	Output slew rate Output slew rate configuration 0 _B , fast slew rate 1 _B , normal slew rate (default) Reset value from OTP: OTP_CUST_CFG9.RAMP_EN[7]

Related information

[Output channels current and slew rate set](#) on page 6

3 Volatile registers

3.3 DIAG_SLS_CFG

DIAG_SLS_CFG

Address: 020_H

DIAG_SLS_CFG

Reset value(unwritten device): 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLS_TH1								SLS_TH0							
rw								rw							

Field	Bits	Type	Description
SLS_TH0	7:0	rw	SLS threshold VS related VFWD SLS threshold for VS related VFWD measurement from 0V to 20.034V in 256 steps. 0 _D (00 _H), 0.000 V 1 _D (01 _H), 0.078 V ... 8 _D (08 _H), 0.63 V (default) ... 255 _D (FF _H), 19.95 V Reset value from OTP: OTP_CUST_CFG3.SLS_TH0[7:0]
SLS_TH1	15:8	rw	SLS threshold VLED related VFWD SLS threshold for VLED related VFWD measurement from 0V to 20.034V in 256 steps. 0 _D (00 _H), 0.000 V 1 _D (01 _H), 0.078 V ... 8 _D (08 _H), 0.63 V (default) ... 255 _D (FF _H), 19.95 V Reset value from OTP: OTP_CUST_CFG3.SLS_TH1[15:8]

3 Volatile registers

3.4 TH_OVLD_CFG

TH_OVLD_CFG

Address: 021_H

TH_OVLD_CFG

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TH_OVLD_CFG1	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF	TH_OVL D_CF
5	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TH_OVLD_CFG n (n=0-15)	n	rw	Thermal overload configuration register 0 _B , the TH_OVLD fault is latched, clear operation is needed to reset the fault and channel restart. (default) 1 _B , the TH_OVLD fault is sampled continuously, automatic reset and restart behavior is selected.

Related information

[Diagnosis feedback registers](#) on page 7

3 Volatile registers

3.5 LD_ADC_VFWD

LD_ADC_VFWDi (i=0-15)

Address: 022_H+i

LD_ADC_VFWD

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			VAL_Fi	RES		VFWDi									
r			rh	r		r									

Field	Bits	Type	Description
VFWDi	9:0	r	VFWD conversion result Contains the conversion result of VFWD. 0 _D (0 _H), 0 V 1023 _D (3FF _H), 20.034 V
RES	11:10, 15:13	r	reserved
VAL_Fi	12	rh	VFWD valid flag Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfield VFWD has been updated with new results value

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.6 VLED

LD_ADC_VLED

Address: 032_H

VLED

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			VAL_F	RES		VLED									
r			rh	r		r									

Field	Bits	Type	Description
VLED	9:0	r	VLED conversion result Contains the conversion result of VLED. 0 _D (0 _H), 0 V 1023 _D (3FF _H), 20.034 V
RES	11:10, 15:13	r	reserved
VAL_F	12	rh	VLED valid flag Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfield VLED has been updated with new results value

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.7 VS

LD_ADC_VS

Address: 033_H

VS

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			VAL_F	RES		VS									
r			rh	r		r									

Field	Bits	Type	Description
VS	9:0	r	VS conversion result Contains the conversion result of VS. 0 _D (0 _H), 0 V 1023 _D (3FF _H), 20.034 V
RES	11:10, 15:13	r	reserved
VAL_F	12	rh	VS valid flag Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfield VS has been updated with new results value

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.8 VOUT_MIN

LD_ADC_VOUT_MIN

Address: 034_H

VOUT_MIN

Reset value: 03FF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOUT_MIN_CHN				RES	VAL_F	VOUT_MIN									
r				r	r	r									

Field	Bits	Type	Description
VOUT_MIN	9:0	r	VOUT minimum calculation result VOUT_MIN contains the min(VOUT _n) result. 0 _D (0 _H), 0 V 1023 _D (3FF _H), 20.034 V
VAL_F	10	rh	VOUT min data valid flag Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfields VOUT_MIN and VOUT_MIN_CHN has been updated with new results value
RES	11, 16	r	reserved
VOUT_MIN_CHN	15:12	r	min(VOUT_n) output channel index VOUT_MIN_CHN contains the channel number of the min(VOUT _n) calculation process.

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.9 VGPIN0

LD_ADC_VGPIN0

Address: 035_H

VGPIN0

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			VAL_F	RES		VGPIN0_OUT									
r			rh	r		r									

Field	Bits	Type	Description
VGPIN0_OUT	9:0	r	VGPIN0 conversion result Contains the conversion result of VGPIN0 0 _D (0 _H), 0 V 1023 _D (3FF _H), 5.496 V
RES	11:10, 15:13	r	reserved
VAL_F	12	rh	VGPIN0 data valid flag Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfield VGPIN0 has been updated with new results value

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.10 VGPIN1

LD_ADC_VGPIN1

Address: 036_H

VGPIN1

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES			VAL_F	RES		VGPIN1_OUT									
r			rh	r		r									

Field	Bits	Type	Description
VGPIN1_OUT	9:0	r	VGPIN1 conversion result Contains the conversion result of VGPIN1. 0 _D (0 _H), 0 V 1023 _D (3FF _H), 5.496 V
RES	11:10, 15:13	r	reserved
VAL_F	12	rh	VGPIN1 data valid flag Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfield VGPIN1 has been updated with new results value.

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.11 OVLD Status

TH_OVLD_STATUS
Address: 037_H

OVLD Status

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OVLD 15	OVL D14	OVL D13	OVL D12	OVL D11	OVL D10	OVL D9	OVL D8	OVL D7	OVL D6	OVL D5	OVL D4	OVL D3	OVL D2	OVL D1	OVL D0
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
OVLDk (k=0-15)	k	r	Thermal overload status flag 0 _B , no thermal overload event occurred since last clear. 1 _B , thermal overload event occurred since last clear.

Related information

[Diagnosis feedback registers](#) on page 7

3 Volatile registers

3.12 DTS Status

DTS_STATAddress: 038_H

DTS Status

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		DTS_TEMP										RES	DTS_OVE RTE MP	DTS_ TEM P_RE ADY	
r		r										r	rh	rh	

Field	Bits	Type	Description
DTS_TEMP_READY	0	rh	Temperature conversion ready Indicates a new result 0 _B , no new result available since last readout. 1 _B , bitfield DTS_TEMP has been updated with new results value
DTS_OVERTEMP	1	rh	DTS Overtemperature Thermal derating active status. This is valid only if DTS_STAT.DTS_TEMP_READY = 1. 0 _B , thermal derating is not active 1 _B , T _J exceeded the T _{J_start} threshold. Thermal derating is active.
RES	3:2	r	reserved
DTS_TEMP	13:4	r	Device temperature Contains the conversion result of the last valid temperature reading. $T_{DTS}(^{\circ}\text{C}) = (\text{DTS_TEMP}[13:4] / 1.1396) - 273.15$

Related information

[ADC conversion registers](#) on page 7

3 Volatile registers

3.13 Reconfirmation status

RECON_STAT

Reconfirmation status

Address: 039_HReset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES															REC ON_ FLAG
r															rh

Field	Bits	Type	Description
RECON_FLAG	0	rh	Reconfirmation flag Reports the reconfirmation status 0 _B , reconfirmation cycle task not in progress. 1 _B , reconfirmation cycle task in progress.
RES	15:1	r	reserved

Related information

[Diagnosis feedback registers](#) on page 7

3 Volatile registers

3.14 PMU Diagnostic

PMU_DIAG

PMU Diagnostic

Address: 03A_H

Reset value: --

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES							VREG_CAN_C URR_LIM	VREG_CAN_O T	VS_OTP_UV	VPRG_OTP_UV	VPRG_OTP_OV	VREG_CAN_O V	VREG_CAN_U V	VREG_5V_UV	VREG_2V5_UV
r							r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
VREG_2V5_UV	0	r	2v5 regulator undervoltage 0 _B , no under voltage event occurred since last readout. 1 _B , under voltage event occurred since last readout.
VREG_5V_UV	1	r	5v regulator undervoltage
VREG_CAN_UV	2	r	CAN regulator undervoltage
VREG_CAN_OV	3	r	CAN regulator overvoltage
VPRG_OTP_OV	4	r	OTP regulator overvoltage
VPRG_OTP_UV	5	r	OTP regulator undervoltage
VS_OTP_UV	6	r	VS OTP undervoltage
VREG_CAN_OT	7	r	CAN regulator overtemperature
VREG_CAN_CU RR_LIM	8	r	5v CAN current limitation
RES	15:9	r	Reserved Returns 0 if read; should be written with 0.

Related information

[Diagnosis feedback registers](#) on page 7

3 Volatile registers

3.15 HSLI Timing

HSLI_TIMING_CFG

HSLI Timing

Address: 03B_HReset value: 004C_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES									FRM_DLY_ADJ			SYNC_BRK_ADJ		BIT_SMPL_ADJ	
r									rw			rw		rw	

Field	Bits	Type	Description
BIT_SMPL_ADJ	1:0	rw	HSLI Bit sampling adjust field 0 _D : 7,8,9 (default) 1 _D : 8,9,10 2 _D : 9,10,11 3 _D : 10,11,12 Reset value from OTP: OTP_CUST_CFG9.HSLI_T_BIT_SMPL[1:0]
SYNC_BRK_ADJ	3:2	rw	HSLI synch break time adjust field 0 _D , 100 us 1 _D , 250 us 2 _D , 750 us 3 _D , 1 ms (default) Reset value from OTP: OTP_CUST_CFG9.HSLI_T_SYNC_BREAK[3:2]
FRM_DLY_ADJ	6:4	rw	HSLI frame delay time adjust field 0 _D , 50 us 1 _D , 100 us 2 _D , 250 us 3 _D , 500 us 4 _D , 1 ms (default) 5 _D , 2.5 ms Reset value from OTP: OTP_CUST_CFG9.HSLI_T_FRAME_DLY[6:4]
RES	15:7	r	Reserved Returns 0 if read; should be written with 0.

Related information

[HSLI interface configuration](#) on page 9

3 Volatile registers

3.16 OTP_EMULATION

OTP_EMULATION

Address: 080_H

OTP_EMULATION

Reset value: --

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECRET															
rw															

Field	Bits	Type	Description
SECRET	15:0	rw	

Related information

[OTP register key for emulation and write](#) on page 10

3 Volatile registers

3.17 OTP_WRITE

OTP_WRITE

Address: 081_H

OTP_WRITE

Reset value: --

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SECRET															
rw															

Field	Bits	Type	Description
SECRET	15:0	rw	

Related information

[OTP register key for emulation and write](#) on page 10

3 Volatile registers

3.18 OTP_STATUS

OTP_STATUS

Address: 082_H

OTP_STATUS

Reset value: 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES						VIRG IN	PRG _FAI LED	DATA _INV ALID	VDD_ 2V5	VDD_ 5V	VDD_ PRO G	VS	OTP_ STAT US2	OTP_STATU S0	
r						r	r	r	r	r	r	r	r	r	

Field	Bits	Type	Description
OTP_STATUS0	1:0	r	OTP power mode status Reports the power mode status during OTP programming. 00 _B , reserved 01 _B , OTP emulation mode 10 _B , reserved 11 _B , OTP programming mode
OTP_STATUS2	2	r	OTP mode status 0 _B , device is not in OTP mode. 1 _B , device is in OTP mode.
VS	3	r	Reports the supply condition on VS during OTP mode. 0 _B , VS is in range 1 _B , VS is above overvoltage or below undervoltage threshold
VDD_PROG	4	r	Reports the supply condition on VDD_PROG during OTP mode. 0 _B , VDD_PROG is in range 1 _B , VDD_PROG is above overvoltage or below undervoltage threshold
VDD_5V	5	r	Reports the supply condition on 2V5 regulator input during OTP mode. 0 _B , VDD5V is in range 1 _B , VDD5V is above overvoltage or below undervoltage threshold
VDD_2V5	6	r	Reports the supply condition on VDD_2V5 during OTP mode. 0 _B , VDD_2V5 is in range 1 _B , VDD_2V5 is above overvoltage or below undervoltage threshold
DATA_INVALID	7	r	Reports validation errors. 0 _B , data valid 1 _B , data invalid
PRG_FAILED	8	r	Reports programming status. 0 _B , OK if DATA_INVALID = 0 _B 0 _B , reserved if DATA_INVALID = 1 _B 1 _B , programming error occurred before start if DATA_INVALID = 0 _B 1 _B , programming error occurred during process if DATA_INVALID = 1 _B

(table continues...)

3 Volatile registers

(continued)

Field	Bits	Type	Description
VIRGIN	9	r	Reports OTP state 0 _B , no destination address was already programmed 1 _B , at least one destination address was already programmed; DATA_INVALID = 0 _B and PRG_FAILED = 1 _B
RES	15:10	r	

Related information

[OTP emulation and write procedure status](#) on page 10

4 OTP registers

4 OTP registers

4.1 OTP_PWM_DC_GPIN1_0

OTP_PWM_DC_GPIN1_0

Address: 083_H

OTP_PWM_DC_GPIN1_0

Default register value
(unwritten device): 8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT1								DC1_OUT0							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT0	7:0	rwp	PWM DC for OUT0 and mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT1	15:8	rwp	PWM DC for OUT1 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.2 OTP_PWM_DC_GPIN1_1

OTP_PWM_DC_GPIN1_1

Address: 084_H

OTP_PWM_DC_GPIN1_1

Default register value
(unwritten device): 8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT3								DC1_OUT2							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT2	7:0	rwp	PWM DC for OUT2 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT3	15:8	rwp	PWM DC for OUT3 and mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.3 OTP_PWM_DC_GPIN1_2

OTP_PWM_DC_GPIN1_2

Address:

085_H

OTP_PWM_DC_GPIN1_2

Default register value
(unwritten device):8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT5								DC1_OUT4							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT4	7:0	rwp	PWM DC for OUT4 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT5	15:8	rwp	PWM DC for OUT5 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.4 OTP_PWM_DC_GPIN1_3

OTP_PWM_DC_GPIN1_3

Address: 086_H

OTP_PWM_DC_GPIN1_3

Default register value
(unwritten device): 8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT7								DC1_OUT6							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT6	7:0	rwp	PWM DC for OUT6 and mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT7	15:8	rwp	PWM DC for OUT7 and mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.5 OTP_PWM_DC_GPIN1_4

OTP_PWM_DC_GPIN1_4

Address:

087_H

OTP_PWM_DC_GPIN1_4

Default register value
(unwritten device):8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT9								DC1_OUT8							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT8	7:0	rwp	PWM DC for OUT8 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT9	15:8	rwp	PWM DC for OUT9 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.6 OTP_PWM_DC_GPIN1_5

OTP_PWM_DC_GPIN1_5

Address: 088_H

OTP_PWM_DC_GPIN1_5

Default register value
(unwritten device): 8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT11								DC1_OUT10							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT10	7:0	rwp	PWM DC for OUT10 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT11	15:8	rwp	PWM DC for OUT11 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.7 OTP_PWM_DC_GPIN1_6

OTP_PWM_DC_GPIN1_6

Address: 089_H

OTP_PWM_DC_GPIN1_6

Default register value
(unwritten device): 8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT13								DC1_OUT12							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT12	7:0	rwp	PWM DC for OUT12 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT13	15:8	rwp	PWM DC for OUT13 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.8 OTP_PWM_DC_GPIN1_7

OTP_PWM_DC_GPIN1_7

Address:

08A_H

OTP_PWM_DC_GPIN1_7

Default register value
(unwritten device):8080_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC1_OUT15								DC1_OUT14							
rwp								rwp							

Field	Bits	Type	Description
DC1_OUT14	7:0	rwp	PWM DC for OUT14 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC1_OUT15	15:8	rwp	PWM DC for OUT15 mapped to GPIN1 Contains the direct control duty cycle via GPIN1 configuration. 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.9 OTP_PWM_DC_GPIN0_0

OTP_PWM_DC_GPIN0_0

Address:

08B_H

OTP_PWM_DC_GPIN0_0

Default register value
(unwritten device):0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT1								DC0_OUT0							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT0	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT0 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT1	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT1 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.10 OTP_PWM_DC_GPIN0_1

OTP_PWM_DC_GPIN0_1

Address: 08C_H

OTP_PWM_DC_GPIN0_1

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT3								DC0_OUT2							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT2	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT2 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT3	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT3 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.11 OTP_PWM_DC_GPIN0_2

OTP_PWM_DC_GPIN0_2

Address:

08D_H

OTP_PWM_DC_GPIN0_2

Default register value
(unwritten device):0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT5								DC0_OUT4							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT4	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT4 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT5	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT5 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.12 OTP_PWM_DC_GPIN0_3

OTP_PWM_DC_GPIN0_3

Address:

08E_H

OTP_PWM_DC_GPIN0_3

Default register value
(unwritten device):0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT7								DC0_OUT6							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT6	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT6 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT7	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT7 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.13 OTP_PWM_DC_GPIN0_4

OTP_PWM_DC_GPIN0_4

Address:

08F_H

OTP_PWM_DC_GPIN0_4

Default register value
(unwritten device):0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT9								DC0_OUT8							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT8	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT8 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT9	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT9 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.14 OTP_PWM_DC_GPIN0_5

OTP_PWM_DC_GPIN0_5

Address: 090_H

OTP_PWM_DC_GPIN0_5

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT11								DC0_OUT10							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT10	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT10 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT11	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT11 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.15 OTP_PWM_DC_GPIN0_6

OTP_PWM_DC_GPIN0_6

Address: 091_H

OTP_PWM_DC_GPIN0_6

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT13								DC0_OUT12							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT12	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT12 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT13	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT13 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.16 OTP_PWM_DC_GPIN0_7

OTP_PWM_DC_GPIN0_7

Address: 092_H

OTP_PWM_DC_GPIN0_7

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DC0_OUT15								DC0_OUT14							
rwp								rwp							

Field	Bits	Type	Description
DC0_OUT14	7:0	rwp	Fail-safe PWM DC and GPIN0 DC for OUT14 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle
DC0_OUT15	15:8	rwp	Fail-safe PWM DC and GPIN0 DC for OUT15 Contains the fail-safe duty cycle and direct control duty cycle via GPIN0 configuration 0 _D (0 _H), 0% duty cycle 255 _D (FF _H), 100% duty cycle

Related information

[Outputs duty cycle values stored in the OTP memory](#) on page 10

4 OTP registers

4.17 OTP_CH_SAFE_STATE

OTP_CH_SAFE_STATE

Address: 093_H

OTP_CH_SAFE_STATE

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SS_EN15	SS_EN14	SS_EN13	SS_EN12	SS_EN11	SS_EN10	SS_EN9	SS_EN8	SS_EN7	SS_EN6	SS_EN5	SS_EN4	SS_EN3	SS_EN2	SS_EN1	SS_EN0
rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp

Field	Bits	Type	Description
SS_ENn (n=0-15)	n	rwp	Output state in FAIL SAFE MODE 0 _B , OUTn is OFF in FAIL SAFE MODE 1 _B , OUTn is ON in FAIL SAFE MODE with DC defined in DC0.OUTn<7:0> and current defined in ISET_OUTn<5:0>

4 OTP registers

4.18 OTP_CH_ISET_0

OTP_CH_ISET_0

Address: 094_H

OTP_CH_ISET_0

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT1						ISET_OUT0					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT0	5:0	rwp	Current set for OUT0 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT1	11:6	rwp	Current set for OUT1 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.19 OTP_CH_ISET_1

OTP_CH_ISET_1

Address: 095_H

OTP_CH_ISET_1

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT3						ISET_OUT2					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT2	5:0	rwp	Current set for OUT2 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT3	11:6	rwp	Current set for OUT3 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.20 OTP_CH_ISET_2

OTP_CH_ISET_2

Address: 096_H

OTP_CH_ISET_2

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT5						ISET_OUT4					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT4	5:0	rwp	Current set for OUT4 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT5	11:6	rwp	Current set for OUT5 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.21 OTP_CH_ISET_3

OTP_CH_ISET_3

Address: 097_H

OTP_CH_ISET_3

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT7						ISET_OUT6					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT6	5:0	rwp	Current set for OUT6 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT7	11:6	rwp	Current set for OUT7 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.22 OTP_CH_ISET_4

OTP_CH_ISET_4

Address: 098_H

OTP_CH_ISET_4

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT9						ISET_OUT8					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT8	5:0	rwp	Current set for OUT8 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT9	11:6	rwp	Current set for OUT9 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.23 OTP_CH_ISET_5

OTP_CH_ISET_5

Address: 099_H

OTP_CH_ISET_5

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT11						ISET_OUT10					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT10	5:0	rwp	Current set for OUT10 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT11	11:6	rwp	Current set for OUT11 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.24 OTP_CH_ISET_6

OTP_CH_ISET_6

Address: 09A_H

OTP_CH_ISET_6

Default register value
(unwritten device): 0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES				ISET_OUT13						ISET_OUT12					
r				rwp						rwp					

Field	Bits	Type	Description
ISET_OUT12	5:0	rwp	Current set for OUT12 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT13	11:6	rwp	Current set for OUT13 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
RES	15:12	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

4 OTP registers

4.25 OTP_CH_ISET_7_DEV_CFG

OTP_CH_ISET_7_DEV_CFG

Address: 09B_H

OTP_CH_ISET_7_DEV_CFG

Default register value
(unwritten device): 1820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	LP_I NIT	DIAG_DEBO UNCE	ISET_OUT15							ISET_OUT14					
rwp	rw	rwp	rwp							rwp					

Field	Bits	Type	Description
ISET_OUT14	5:0	rwp	Current set for OUT14 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
ISET_OUT15	11:6	rwp	Current set for OUT15 Default and fail-safe output current configuration 0 _D (0 _H), 5.625 mA 63 _D (3F _H), 76.5 mA
DIAG_DEBOUN CE	13:12	rwp	DIAG_DEBOUNCE Diagnostic debouncing configuration 0 _D , reserved 1 _D , $n_{debounce}$ is set to 2 2 _D , $n_{debounce}$ is set to 4 3 _D , $n_{debounce}$ is set to 6
LP_INIT	14	rw	LP_INIT LP_INIT configuration 0 _B , Low power during init option is disabled, LP_INIT = '0' 1 _B , Low power during init mode feature is enabled, LP_INIT = '1'
RES	15	rwp	Reserved Returns 0 if read; shall be written with 0.

Related information

[Diagnosis configuration registers](#) on page 8

4 OTP registers

4.26 OTP_PWM_PHASE_EN

OTP_PWM_PHASE_EN

Address:

09C_H

OTP_PWM_PHASE_EN

Default register value
(unwritten device):FFFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHIF T_EN 15	SHIF T_EN 14	SHIF T_EN 13	SHIF T_EN 12	SHIF T_EN 11	SHIF T_EN 10	SHIF T_EN 9	SHIF T_EN 8	SHIF T_EN 7	SHIF T_EN 6	SHIF T_EN 5	SHIF T_EN 4	SHIF T_EN 3	SHIF T_EN 2	SHIF T_EN 1	SHIF T_EN 0
rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp

Field	Bits	Type	Description
SHIFT_ENn (n=0-15)	n	rwp	Phase shift ENable 0 _B , OUTn has no phase shift compared to OUTn-1 1 _B , OUTn has a phase shift compared to OUTn-1 (default) Note: PWM_PHASE_SHIFT_EN.OUT0 is always 0, means no phase shift.

Related information

[Output PWM frequency and phase shift](#) on page 11

4 OTP registers

4.27 OTP_CUST_CFG0

OTP_CUST_CFG0

Address: 09D_H

OTP_CUST_CFG0

Default register value
(unwritten device): 86F3_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIN 1_HiZ _EN	GPIN 0_HiZ _EN	GPIN 0_Fu nc_O E	GPIN 1_IN V_EN	CH_ DCD C_O UTO_ EN	GPIN 1_DC _DEC _EN	GPIN 0_DC _DEC _EN	PWM_PHASE_SHIFT					PWM_FREQ			
rwp	rwp	rwp	rwp	rwp	rwp	rwp	rwp					rwp			

Field	Bits	Type	Description
PWM_FREQ	3:0	rwp	PWM base frequency 0 _D , 100 Hz 1 _D , 200 Hz 2 _D , 240 Hz 3 _D , 300 Hz (default) 4 _D , 360 Hz 5 _D , 400 Hz 6 _D , 540 Hz 7 _D , 600 Hz 8 _D , 660 Hz 9 _D , 720 Hz 10 _D , 780 Hz 11 _D , 900 Hz 12 _D , 1200 Hz 13 _D , 1500 Hz 14 _D , 1800 Hz 15 _D , 2000 Hz Note: values above are rounded. For exact numbers please refer to the datasheet.
PWM_PHASE_SHIFT	8:4	rwp	Set the delay between channel n and channel n-1 0 _D , 0 _D as 14-bit duty cycle reference or 0% 1 _D , equivalent to 32 _D as 14-bit duty cycle reference or 0.195% ... 15 _D , equivalent to 480 _D as 14-bit duty cycle reference or 2.9% (default) 16 _D , equivalent to 512 _D as 14-bit duty cycle reference or 3.125% ... 31 _D , equivalent to 992 _D as 14-bit duty cycle reference or 6.0547%
GPIN0_DC_DEC_EN	9	rwp	Duty cycle decoder enable for GPIN0 0 _B , GPIN0 will be decoded according to the static level at pin 1 _B , GPIN0 will be decoded according duty cycle level (default)

(table continues...)

4 OTP registers

(continued)

Field	Bits	Type	Description
GPIN1_DC_DE C_EN	10	rwp	Duty cycle decoder enable for GPIN1 0 _B , GPIN1 will be decoded according to the static level at pin 1 _B , GPIN1 will be decoded according duty cycle level (default)
CH_DCDC_OUT0_EN	11	rwp	OUT0 voltage regulator feedback (Head room control) enable 0 _B , OUT0 set as standard output (default) 1 _B , OUT0 set as voltage regulator feedback
GPIN1_INV_EN	12	rwp	GPIN1 inverter enable 0 _B , the GPIN1 is not inverted. (default) 1 _B , the GPIN1 is inverted signal.
GPIN0_Func_OE	13	rwp	Out enable function GPIN0 is used to enable the output stage 1 _B , GPIN0 is the outputs enable GPIN0='0' outputs are disabled GPIN0='1' outputs are enabled 0 _B , GPIN0 is not used as output enable function (default)
GPIN0_HiZ_EN	14	rwp	GPIN configuration for Analog or Digital input 0 _B , GPIN0 is set as Digital Input and pull down is enabled and ADC will convert the GPIN0 value. (default) 1 _B , GPIN0 is set as Analog Input and pull down is disable and ADC will convert the GPIN0 voltage value.
GPIN1_HiZ_EN	15	rwp	GPIN configuration for Analog or Digital input 0 _B , GPIN1 is set as Digital Input and pull down is enabled and ADC will convert the GPIN1 value. 1 _B , GPIN1 is set as Analog Input and pull down is disable and ADC will convert the GPIN1 voltage value. (default)

Related information

[Output PWM frequency and phase shift](#) on page 11

[Voltage regulator feedback feature](#) on page 11

[GPINn configuration](#) on page 13

4 OTP registers

4.28 OTP_CUST_CFG1

OTP_CUST_CFG1

Address: 09E_H

OTP_CUST_CFG1

Default register value
(unwritten device): 09D0_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIAG_OUT15_ERRn_EN				DIAG_TDELAY				DIAG_VDEN_VLED				DIAG_VDEN_VS			
rwp				rwp				rwp				rwp			

Field	Bits	Type	Description
DIAG_VDEN_VS	4:0	rwp	VDEN Threshold for VS VDEN_threshold from 0V up to 19.408V in 0.626V steps. 0 _D , 0 V 1 _D , 0.626V ... 16 _D , 10.017 V (default) ... 31 _D , 19.408V
DIAG_VDEN_VLED	9:5	rwp	VDEN Threshold for VLED VDEN_threshold from 0V up to 19.408V in 0.626V steps. 0 _D , 0 V 1 _D , 0.626 V ... 14 _D , 8.765 V (default) ... 31 _D , 19.408 V
DIAG_TDELAY	12:10	rwp	Delay time for the start of the ADC conversion Diagnostic sample delay from 8 us up to 600 us. 0 _D , 8 us 1 _D , 16 us 2 _D , 24 us (default) 3 _D , 48 us 4 _D , 96 us 5 _D , 192 us 6 _D , 300 us 7 _D , 600 us
DIAG_OUT15_ERRn_EN	15:13	rwp	ERRN enable on OUT15 ERRN active on OUT15 000 _B , ERRN function disabled on OUT15 (default) 111 _B , ERRN function enabled on OUT15

Related information

[Diagnosis configuration registers](#) on page 8

4 OTP registers

4.29 OTP_CUST_CFG2

OTP_CUST_CFG2

Address:

09F_H

OTP_CUST_CFG2

Default register value
(unwritten device):FFFF_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHORT_WRN_EN															
rwp															

Field	Bits	Type	Description
SHORT_WRN_EN	15:0	rwp	Short monitor channel enable 0 _B , OUTn short between adjacent channel is disabled (for channel working in parallel) 1 _B , OUTn short between adjacent channel is enabled (default)

Related information

[Diagnosis configuration registers](#) on page 8

4 OTP registers

4.30 OTP_CUST_CFG3

OTP_CUST_CFG3

Address: 0A0_H

OTP_CUST_CFG3

Default register value
(unwritten device): 2020_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLS_TH1								SLS_TH0							
rwp								rwp							

Field	Bits	Type	Description
SLS_TH0	7:0	rwp	SLS threshold VS related VFWD SLS threshold for VS related VFWD measurement from 0V to 20.034V in 256 steps. 0 _D , 0.000 V 1 _D , 0.078 V ... 32 _D , 2.50 V (default) ... 255 _D , 19.95 V
SLS_TH1	15:8	rwp	SLS threshold VLED related VFWD SLS threshold for VLED related VFWD measurement from 0V to 20.034V in 256 steps. 0 _D , 0.000 V 1 _D , 0.078 V ... 32 _D , 2.50 V (default) ... 255 _D , 19.95 V

Related information

[Diagnosis configuration registers](#) on page 8

4 OTP registers

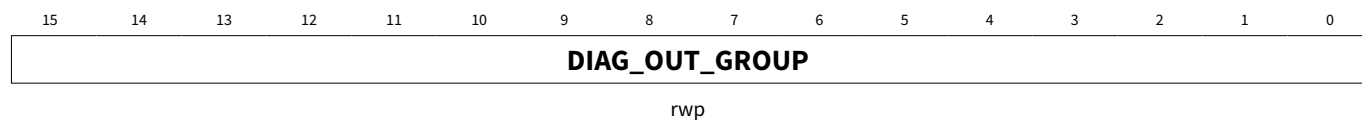
4.31 OTP_CUST_CFG4

OTP_CUST_CFG4

Address:

0A1_H

OTP_CUST_CFG4

Default register value
(unwritten device):FFFF_H

Field	Bits	Type	Description
DIAG_OUT_GRP OUP	15:0	rwp	Diagnostic Group for the anode voltage for LED 0 _B , VFWDn = VS - VOUTn 1 _B , VFWDn = VLED - VOUTn (default)

Related information

[Diagnosis configuration registers](#) on page 8

4 OTP registers

4.32 OTP_CUST_CFG5

OTP_CUST_CFG5

Address:

0A2_H

OTP_CUST_CFG5

Default register value
(unwritten device):0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIN0_MAP															
rwp															

Field	Bits	Type	Description
GPIN0_MAP	15:0	rwp	Map of the 16 channels to the GPIN0 0 _B , OUTn is not mapped to the GPIN0 (default) 1 _B , OUTn is mapped to GPIN0 with DC defined in DC0.OUTn<7:0>

Related information

[GPINn configuration](#) on page 13

4 OTP registers

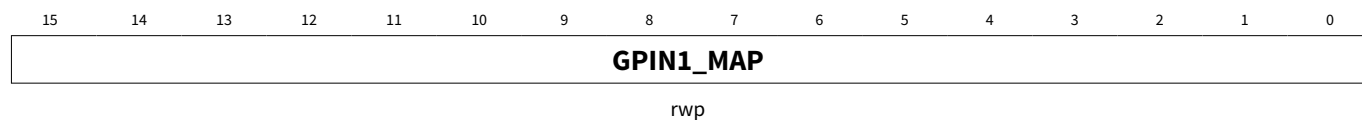
4.33 OTP_CUST_CFG6

OTP_CUST_CFG6

Address:

0A3_H

OTP_CUST_CFG6

Default register value
(unwritten device):0000_H

Field	Bits	Type	Description
GPIN1_MAP	15:0	rwp	Map of the 16 channels to the GPIN1 0 _B , OUTn is not mapped to the GPIN1 (default) 1 _B , OUTn is mapped to GPIN1 with DC defined in DC1.OUTn<7:0>

Related information

[GPINn configuration](#) on page 13

4 OTP registers

4.34 OTP_CUST_CFG7

OTP_CUST_CFG7

Address: 0A4_H

OTP_CUST_CFG7

Default register value
(unwritten device): 0007_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURR_WRN_REP_DIS	DIAG_SLS_LOC_K	PWR_OFF_LOA_D_EN	DIAG_OUT_S_WOF_F_DC100	DIAG_mgmt_SET	VFWD_VS_TH				VFWD_VLED_TH				DIAG_WDT_SET		
rwp	rwp	rwp	rwp	rwp	rwp				rwp				rwp		

Field	Bits	Type	Description
DIAG_WDT_SET	2:0	rwp	Watchdog timeout 0 _D , disabled 1 _D , 20 ms (60 ms) 2 _D , 50 ms (150 ms) 3 _D , 100 ms (300 ms) 4 _D , 200 ms (600 ms) 5 _D , 500 ms (1500 ms) 6 _D , 1000 ms (3000 ms) 7 _D , 2000 ms (6000 ms) (default) Numbers in brackets refer to LP_INIT = '1' AND device in init mode
VFWD_VLED_TH	6:3	rwp	Thresholds for the short to VLED - LSB=1.25 V 0 _D , 0V 1 _D , 1.25V 2 _D , 2.51V 3 _D , 3.76V 4 _D , 5.02V 5 _D , 6.27V 6 _D , 7.52V 7 _D , 8.78V 8 _D , 10.03V 9 _D , 11.29V 10 _D , 12.54V 11 _D , 13.80V 12 _D , 15.05 13 _D , 16.30V 14 _D , 17.56V 15 _D , 18.81V

(table continues...)

4 OTP registers

(continued)

Field	Bits	Type	Description
VFWD_VS_TH	10:7	rwp	Thresholds for the short to VS - LSB=1.25 V 0 _D , 0V 1 _D , 1.25V 2 _D , 2.51V 3 _D , 3.76V 4 _D , 5.02V 5 _D , 6.27V 6 _D , 7.52V 7 _D , 8.78V 8 _D , 10.03V 9 _D , 11.29V 10 _D , 12.54V 11 _D , 13.80V 12 _D , 15.05 13 _D , 16.30V 14 _D , 17.56V 15 _D , 18.81V
DIAG_mgnt_SE	11	rwp	Fault management configuration Fault management configuration 0 _B , no state change (default) 1 _B , change to init mode (power stages are turned off) if VS ≥ VDEN_threshold for VS related diagnostic AND VLED ≥ VDEN_threshold for VLED related diagnostic
DIAG_OUT_SW OFF_DC100	12	rwp	Diagnostic switch OFF for outputs with 100% duty cycle 0 _B , the output with DC=100% will not have the diagnostic switch OFF (default) 1 _B , the output with DC=100% will be switched OFF every 4 periods to allow the short detection with its adjacent output.
PWR_OFF_LOAD_EN	13	rwp	Power shift enable function Power off load enable 0 _B , Power shift disabled (default) 1 _B , Power shift enabled
DIAG_SLS_LOCK	14	rwp	Lock of the SLS thresholds 0 _B , SLS thresholds used by LED driver is in DIAG_SLS_CFG (default) 1 _B , SLS thresholds used by LED driver is in OTP_CUST_CFG3
CURR_WRN_REP_DIS	15	rwp	Current Warning ERRN report Disable 0 _B , Current warning reporting on ERRN enabled (default) 1 _B , Current warning reporting on ERRN disabled

Related information

[Diagnosis feedback registers](#) on page 7

[Power shift feature](#) on page 12

4 OTP registers

4.35 OTP_SLAVE_ID

OTP_SLAVE_ID

Address: 0A5_H

OTP_SLAVE_ID

Default register value
(unwritten device): 0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES											HSLI_ADDR				
r											rwp				

Field	Bits	Type	Description
HSLI_ADDR	4:0	rwp	HSLI slave node address Defines the BUS-ID ranging from 1 to 31.
RES	15:5	r	Reserved Returns 0 if read; shall be written with 0.

4 OTP registers

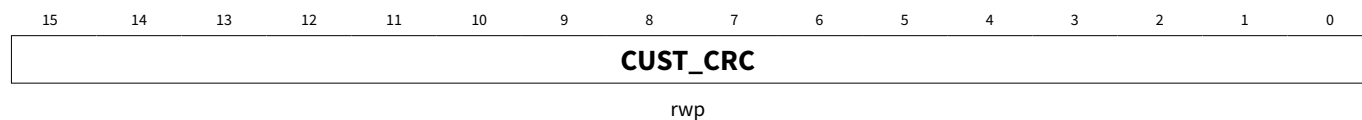
4.36 OTP_CUST_SGN

OTP_CUST_SGN

Address:

0A6_H

OTP_CUST_SGN

Default register value
(unwritten device):FFFF_H

Field	Bits	Type	Description
CUST_CRC	15:0	rwp	CRC to secure the OTP CUST DATA

Related information

[CRC protection](#) on page 13

4 OTP registers

4.37 OTP_CUST_CFG8

OTP_CUST_CFG8

Address:

0A7_H

OTP_CUST_CFG8

Default register value
(unwritten device):0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWR_OFF_LOAD_TH_CH 1011_SET		PWR_OFF_LOAD_TH_CH H89_SET		PWR_OFF_LOAD_TH_CH H23_SET		PWR_OFF_LOAD_TH_CH H01_SET		PWR_OFF_LOAD_CH_SE T			CH_TH_DER_TH			CH_TH_DER_EN	
rwp		rwp		rwp		rwp		rwp			rwp			rwp	

Field	Bits	Type	Description
CH_TH_DER_EN	0	rwp	Thermal derating Enable 0 _B , thermal derating is disabled (default) 1 _B , thermal derating is enabled
CH_TH_DER_TH	3:1	rwp	Thermal derating TJDER configuration 0 _D , 20 °C - TJstart = TJstop - 20 °C (default) 1 _D , 30 °C - TJstart = TJstop - 30 °C 2 _D , 40 °C - TJstart = TJstop - 40 °C 3 _D , 50 °C - TJstart = TJstop - 50 °C 4 _D , 60 °C - TJstart = TJstop - 60 °C
PWR_OFF_LOAD_CH_SET	7:4	rwp	Power shift channel enable set 0 _B , output pair for power off load is not coupled (default) 1 _B , output pair for power off load is coupled PWR_OFF_LOAD_CH_SET[0] refers to OUT0 and OUT1 PWR_OFF_LOAD_CH_SET[1] refers to OUT2 and OUT3 PWR_OFF_LOAD_CH_SET[2] refers to OUT8 and OUT9 PWR_OFF_LOAD_CH_SET[3] refers to OUT10 and OUT11
PWR_OFF_LOAD_TH_CH01_SET	9:8	rwp	0 _D , V _{OUTPS_HI} = 2 V 1 _D , V _{OUTPS_HI} = 3 V 2 _D , V _{OUTPS_HI} = 6 V 3 _D , V _{OUTPS_HI} = 10 V
PWR_OFF_LOAD_TH_CH23_SET	11:10	rwp	0 _D , V _{OUTPS_HI} = 2 V 1 _D , V _{OUTPS_HI} = 3 V 2 _D , V _{OUTPS_HI} = 6 V 3 _D , V _{OUTPS_HI} = 10 V
PWR_OFF_LOAD_TH_CH89_SET	13:12	rwp	0 _D , V _{OUTPS_HI} = 2 V 1 _D , V _{OUTPS_HI} = 3 V 2 _D , V _{OUTPS_HI} = 6 V 3 _D , V _{OUTPS_HI} = 10 V

(table continues...)

4 OTP registers**(continued)**

Field	Bits	Type	Description
PWR_OFF_LOA D_TH_CH1011 _SET	15:14	rwp	$0_D, V_{OUTPS_HI} = 2\text{ V}$ $1_D, V_{OUTPS_HI} = 3\text{ V}$ $2_D, V_{OUTPS_HI} = 6\text{ V}$ $3_D, V_{OUTPS_HI} = 10\text{ V}$

Related information[Power shift feature](#) on page 12

4 OTP registers

4.38 OTP_CUST_CFG9

OTP_CUST_CFG9

Address: 0A8_H

OTP_CUST_CFG9

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								RAM P_EN	HSLI_T_FRAME_D LY		HSLI_T_SY NC_BREAK		HSLI_T_BIT SMPL		
r								rwp	rwp		rwp		rwp		

Field	Bits	Type	Description
HSLI_T_BITSMPL	1:0	rwp	Setup of the sampling time 0 _D (default): 7,8,9 1 _D : 8,9,10 2 _D : 9,10,11 3 _D : 10,11,12
HSLI_T_SYNC_BREAK	3:2	rwp	Setup of the sync break time 0 _D , 100 us 1 _D , 250 us 2 _D , 750 us 3 _D (default), 1 ms
HSLI_T_FRAME_DLY	6:4	rwp	Setup of the frame delay time 0 _D , 50 us 1 _D , 100 us 2 _D , 250 us 3 _D , 500 us 4 _D (default), 1 ms 5 _D , 2.5 ms
RAMP_EN	7	rwp	Led Driver RAMP enable for each channel 0 _B , (default) fast slew rate is set for all output channels; can be changed via REG_WRITE 1 _B , normal slew rate is set for all output channels; can be changed via REG_WRITE
RES	15:8	r	Reserved Returns 0 if read; shall be written with 0.

Related information

[Output channels current and slew rate set](#) on page 6

[HSLI interface configuration](#) on page 9

4 OTP registers

4.39 OTP_CUST_CFG10

OTP_CUST_CFG10

Address: 0A9_H

OTP_CUST_CFG10

Default register value
(unwritten device): 0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES					CH_TH_DER_G PIN	VGPI0_TJSTOP					VGPI0_TJSTART				
r					rwp	rwp					rwp				

Field	Bits	Type	Description
VGPI0_TJSTART	4:0	rwp	VGPI0 thermal derating start Thermal derating threshold from 0V to 5.333V in 32 steps. 0 _D , 0.000 V (default) 1 _D , 0.172 V ... 31 _D , 5.333 V
VGPI0_TJSTOP	9:5	rwp	VGPI0 thermal derating stop Thermal derating threshold from 0V to 5.333V in 32 steps. 0 _D , 0.000 V (default) 1 _D , 0.172 V ... 31 _D , 5.333 V
CH_TH_DER_G PIN	10	rwp	Thermal derating source selection 0 _B , (default) thermal derating is based on the digital temperature sensor (DTS) 1 _B , thermal derating is based on the VGPI0 conversion result
RES	15:11	r	Reserved Returns 0 if read; shall be written with 0.

4 OTP registers

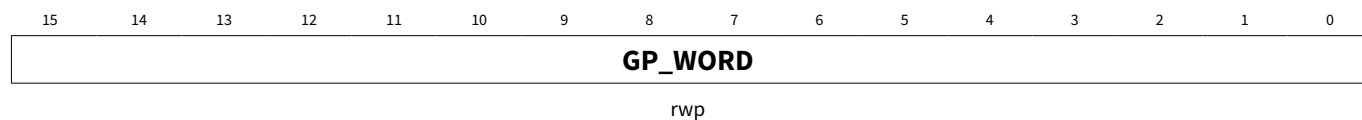
4.40 OTP_CUST_CFG11

OTP_CUST_CFG11

Address:

0AA_H

OTP_CUST_CFG11

Default register value
(unwritten device):0000_H

Field	Bits	Type	Description
GP_WORD	15:0	rwp	General purpose word General purpose word, dedicated to store customer information.

4 OTP registers

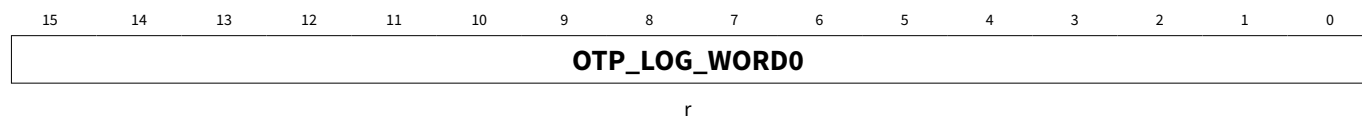
4.41 OTP_LOG_WORD0

OTP_LOG_WORD0

Address:

0AB_H

OTP_LOG_WORD0

Default register value
(unwritten device):FFFF_H

Field	Bits	Type	Description
OTP_LOG_WORD0	15:0	r	OTP_LOG_WORD0 Contains OTP programming feedback.

4 OTP registers

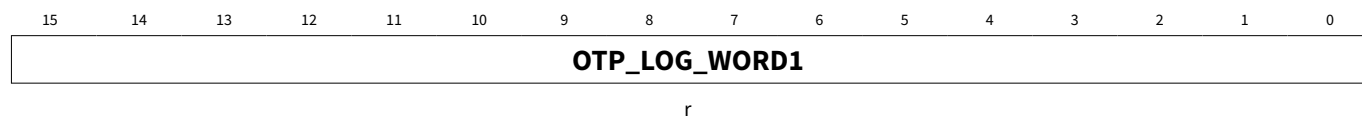
4.42 OTP_LOG_WORD1

OTP_LOG_WORD1

Address:

0AC_H

OTP_LOG_WORD1

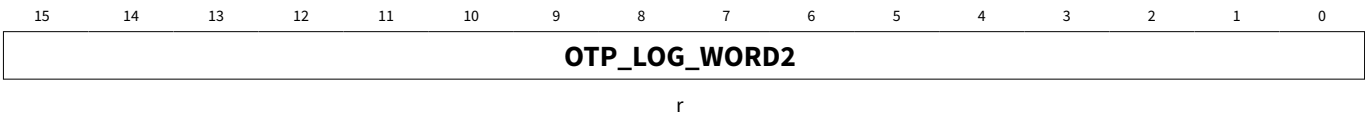
Default register value
(unwritten device):FFFF_H

Field	Bits	Type	Description
OTP_LOG_WORD1	15:0	r	OTP_LOG_WORD1 Contains OTP programming feedback.

4 OTP registers

4.43 OTP_LOG_WORD2

OTP_LOG_WORD2	Address:	0AD _H
OTP_LOG_WORD2	Default register value (unwritten device):	FFFF _H



Field	Bits	Type	Description
OTP_LOG_WORD2	15:0	r	OTP_LOG_WORD2 Contains OTP programming feedback.

4 OTP registers

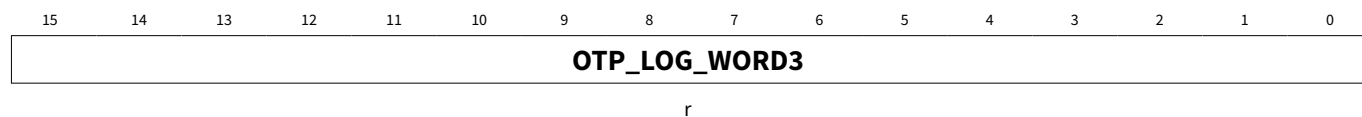
4.44 OTP_LOG_WORD3

OTP_LOG_WORD3

Address:

0AE_H

OTP_LOG_WORD3

Default register value
(unwritten device):FFFF_H

Field	Bits	Type	Description
OTP_LOG_WORD3	15:0	r	OTP_LOG_WORD3 Contains OTP programming feedback.

5 List of abbreviations

Table 3 List of abbreviations

Acronym	Description
LED	Light-emitting diode
CRC	Cyclic redundancy check
OTP	One-time programmable
HSLI	High-speed lighting interface
LCU	Light control unit
ADC	Analog-to-digital converter
r	read only
rw	read - write
rwp	read - write protected, write limited to OTP emulation and OTP write mode only
rh	read only, clear on read

References

- [1] *TLD7002-16ES Datasheet*, Z8F64248201
- [2] *TLD7002-16ES Safety Manual*, Z8F64248202
- [3] *TLD7002-16ES OTP programming procedure Application Note*, Z8F64247081

Revision history

Revision history

Document version	Date of release	Description of changes
Rev. 1.30	2025-03-14	Output channels current and slew rate set: added DAC_CONFIGi formula ADC conversion registers: added DTS sensor details Diagnosis configuration registers: added details on DIAG_mgnt_SET usage Register Overview - HSLI (ascending Address): removed offset word OTP_CH_ISET_0: fixed rounding on OTP_CH_ISET_0 OTP_CH_ISET_0 to OTP_CH_ISET_7_DEV_CFG: fixed rounding on OTP_CH_ISET_i OTP_CUST_CFG1: fixed rounding DIAG_VDEN_VS and _VLED OTP_CUST_CFG7: changed default DIAG_WDT_SET
Rev.1.20	2022-05-03	Product family name is assigned as LITIX™ Pixel Rear
Rev.1.10	2022-04-27	- Editorial changes - Figure 1 added for voltage feedback control - Improved bit field descriptions
Rev.1.00	2021-07-12	Initial User manual release

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