

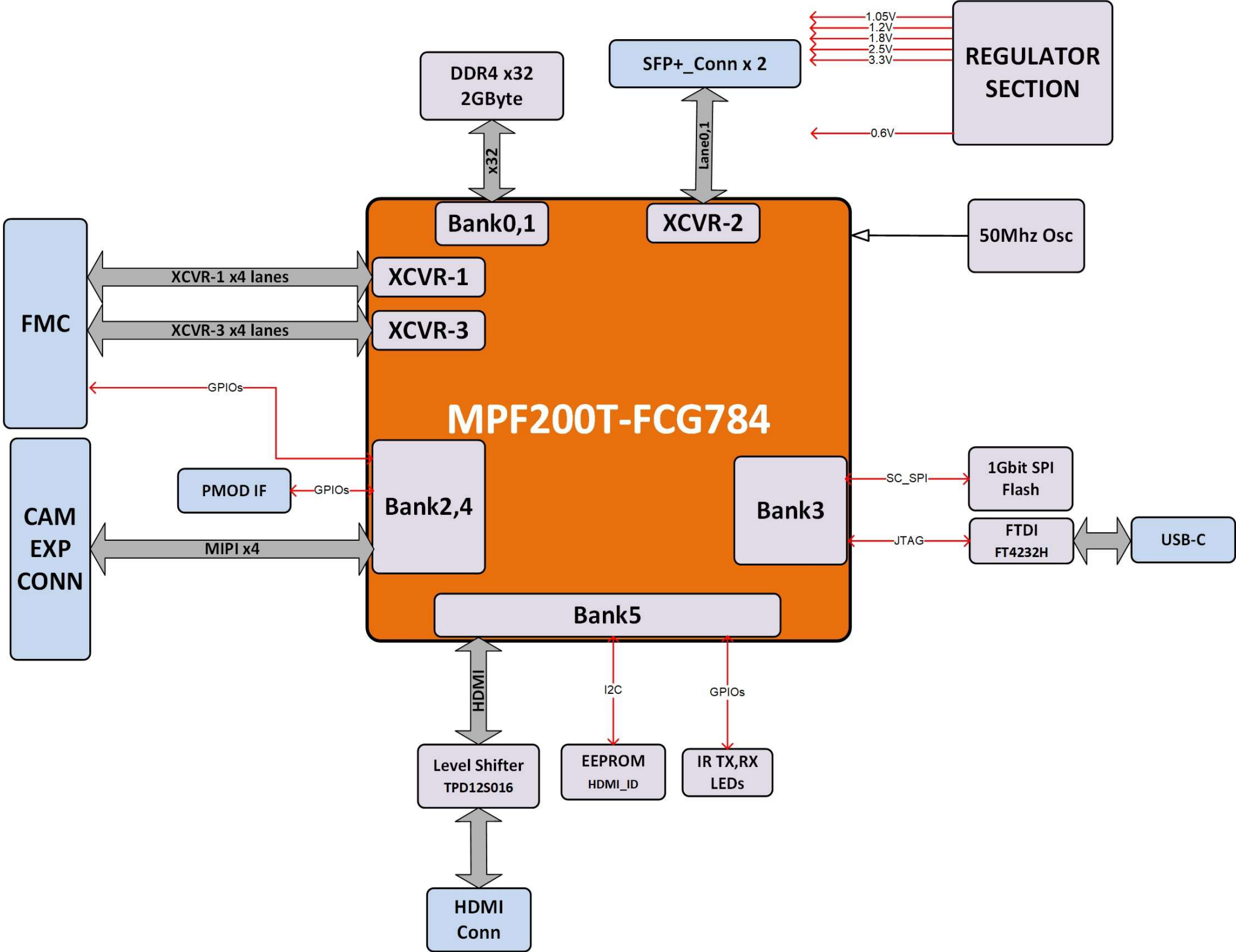
PolarFire_Eth_Sensor_Bridge

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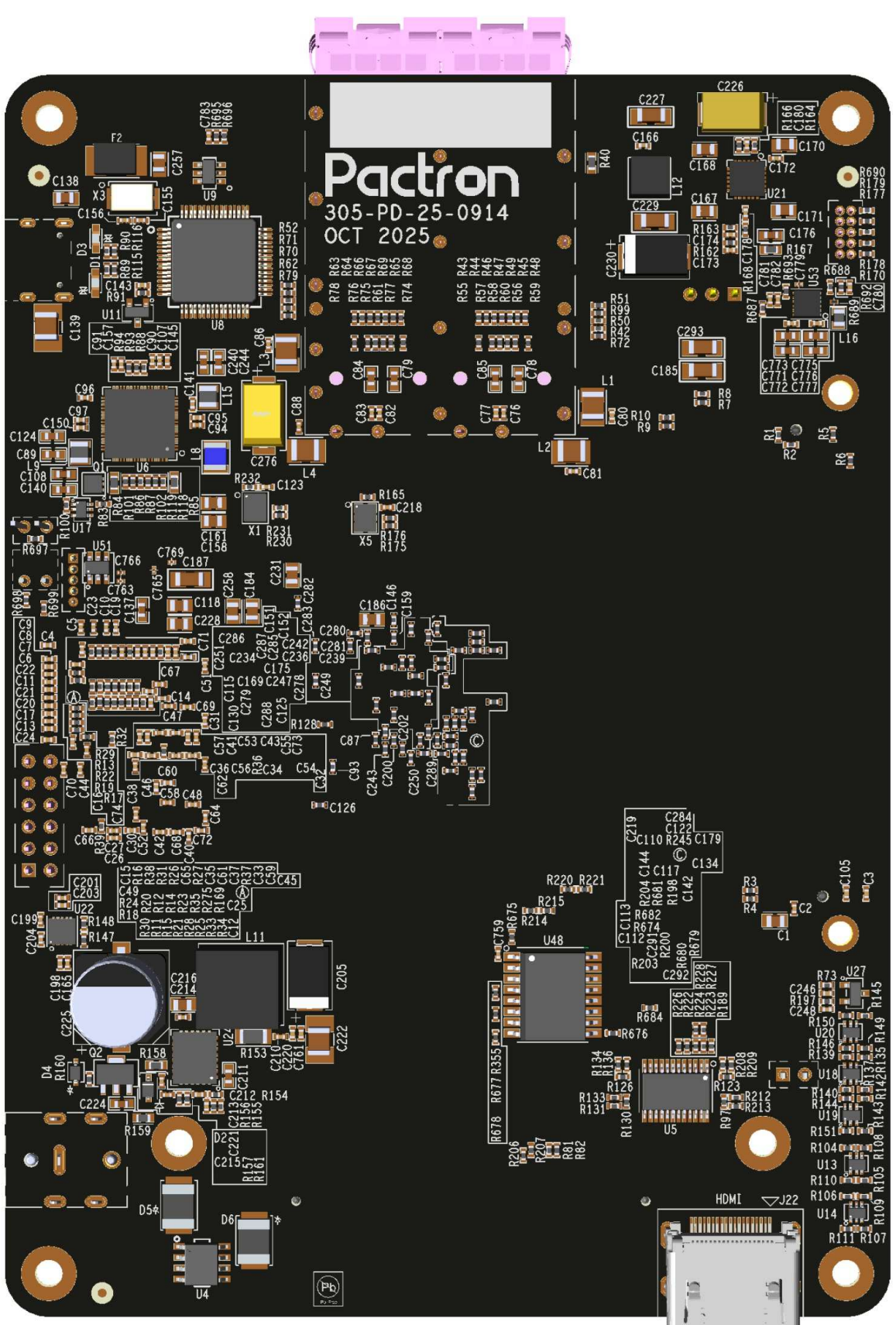
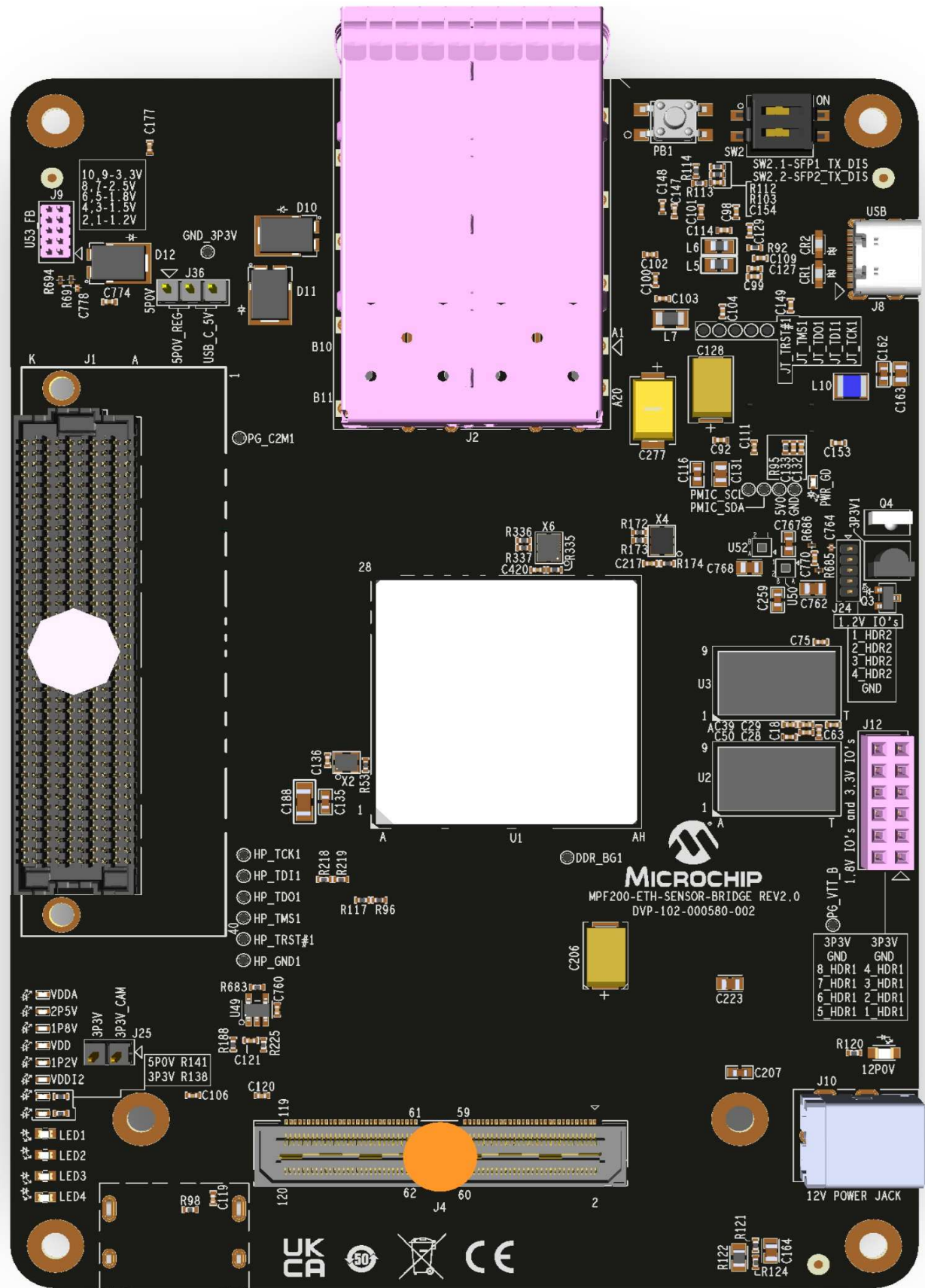


Project Name:		
MPF200-ETH-SENSOR-BRIDGE		
Rev	Part Number:	PACTRON:
2	DVP-100-000580-002	
Originator:		
Size	Date:	Sheet
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MPF200-ETH-SENSOR-BRIDGE



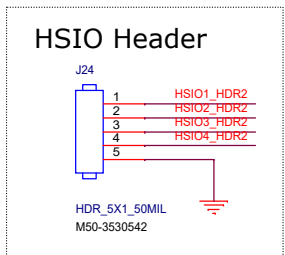
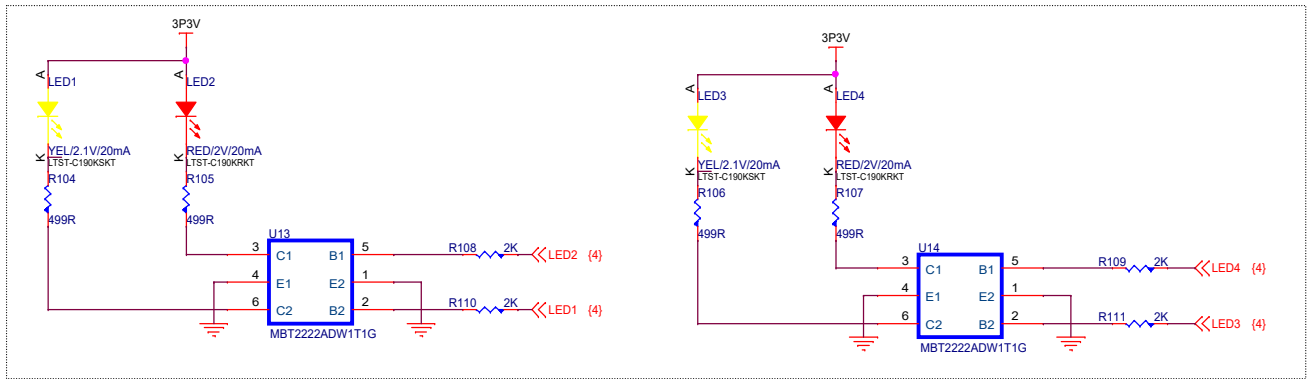
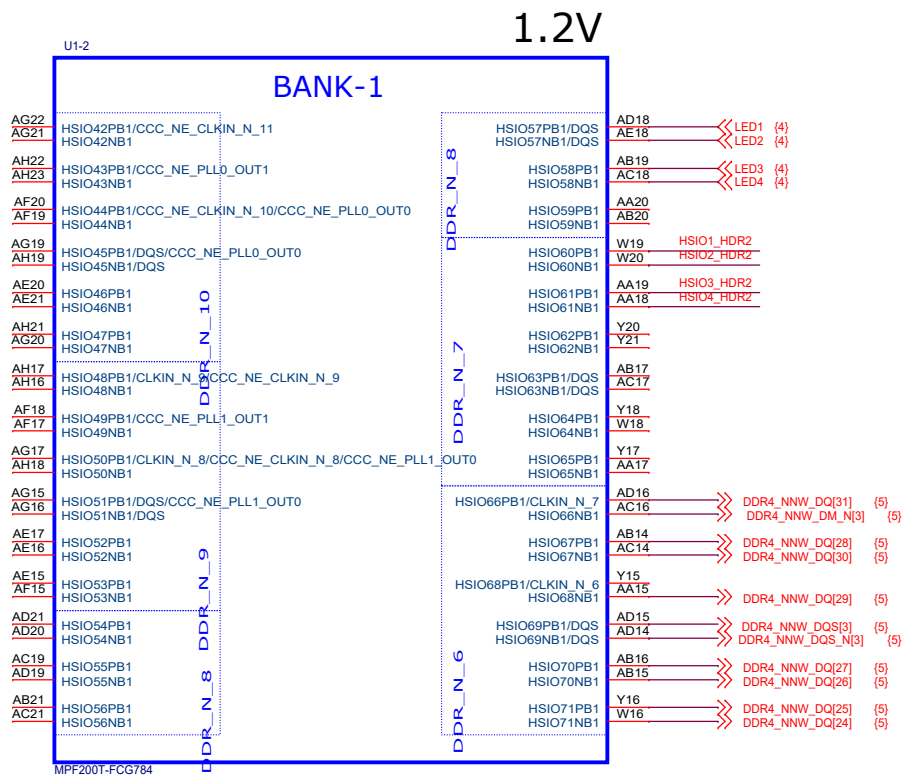
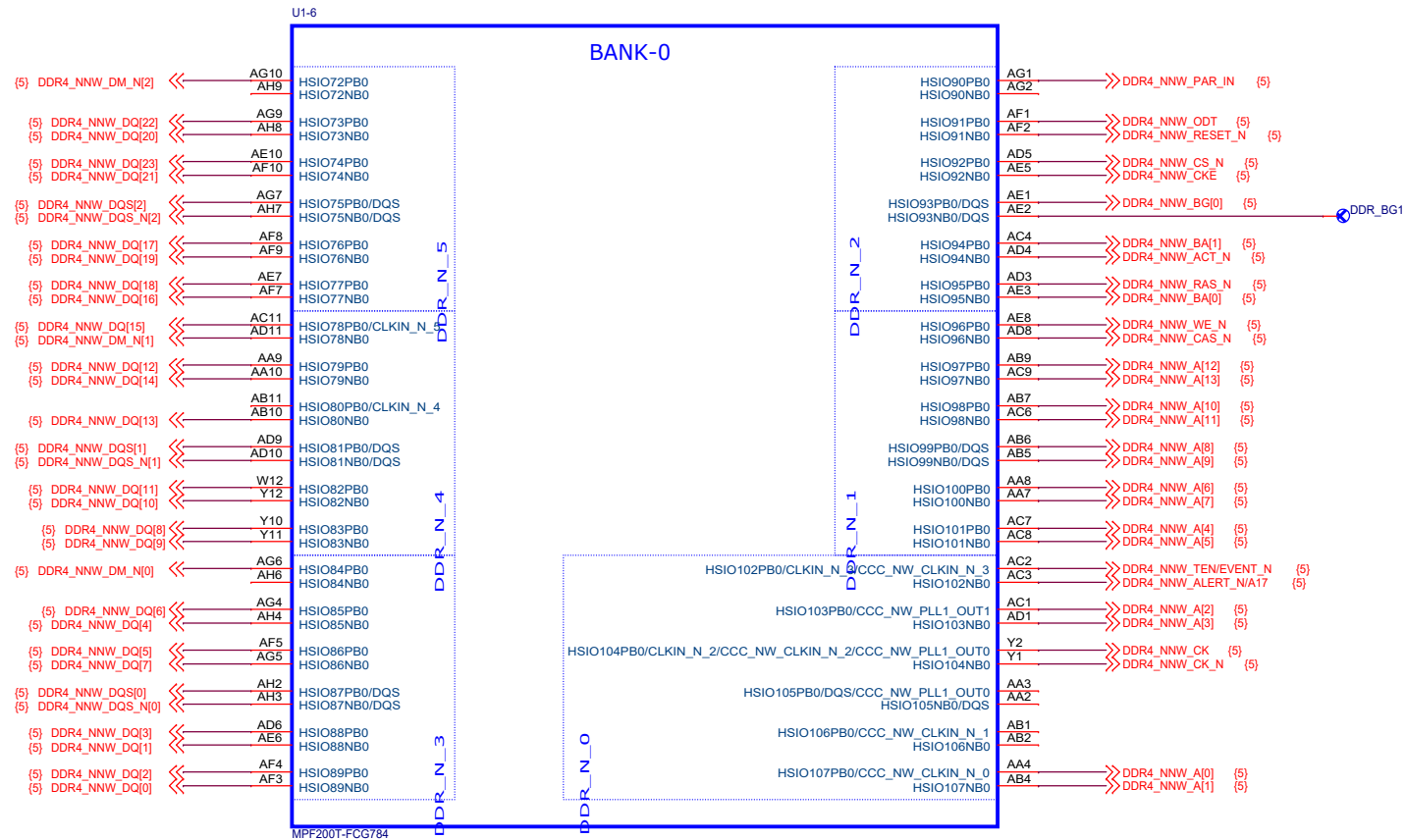
TITLE		
MPF200-ETH-SENSOR-BRIDGE		
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HSIO Bank 0,1 CONNECTION

1.2V



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A diagram of a linear chromosome with four segments labeled A, B, C, and D from left to right. Segment B is highlighted with a thick black arrow pointing to it from the left.

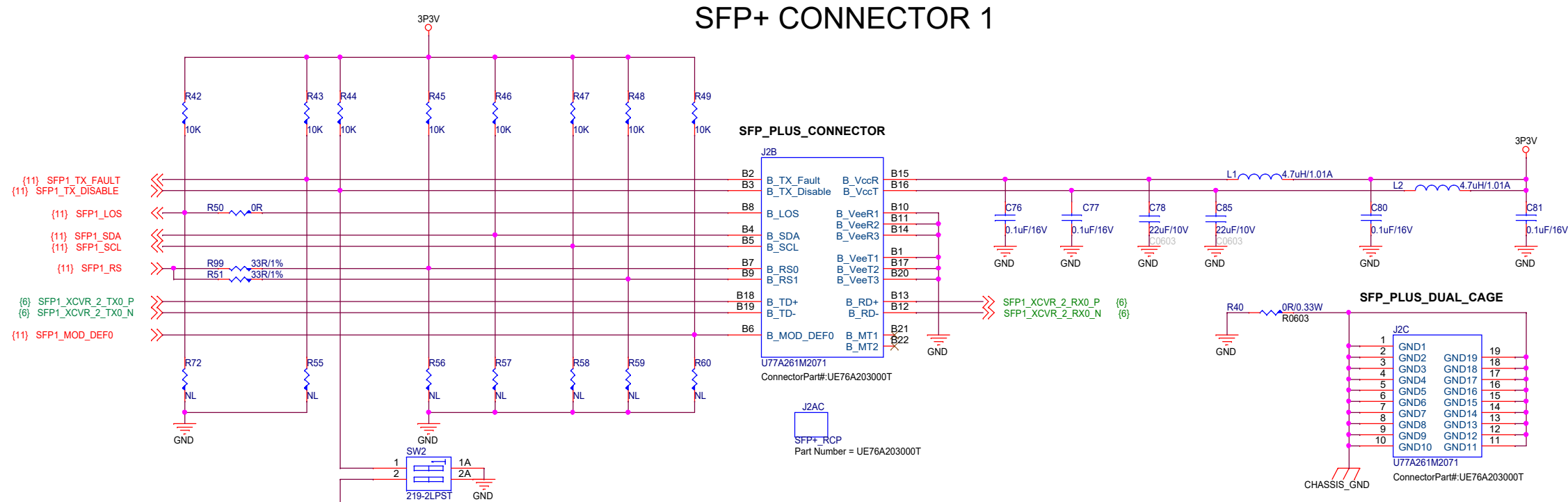


A

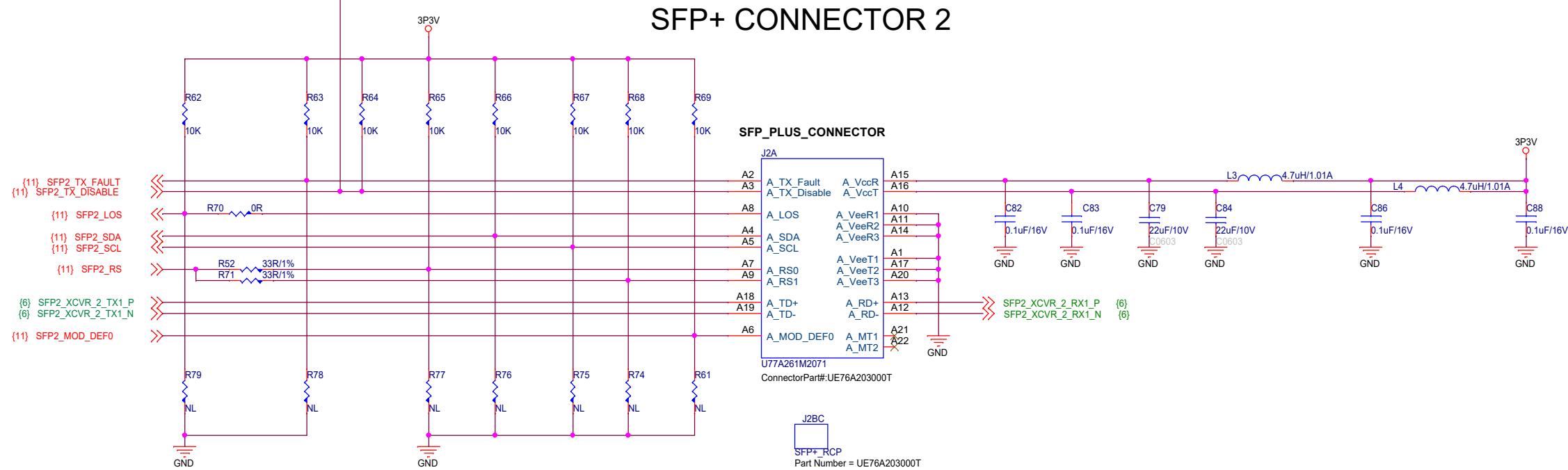


TITLE			
MPF200-ETH-SENSOR-BRIDGE			
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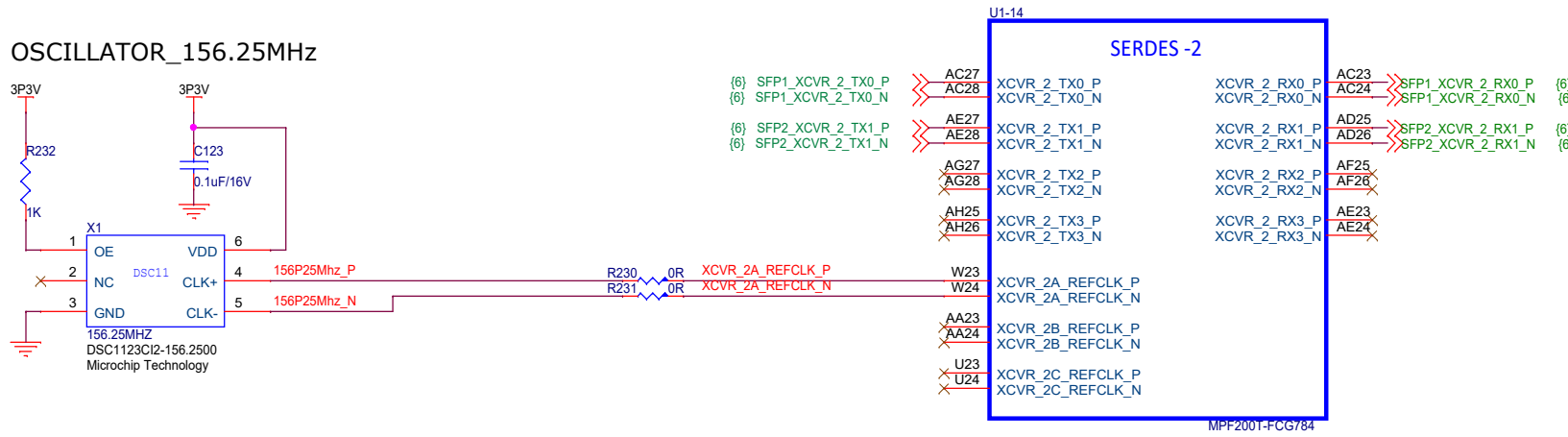
SFP+ CONNECTOR 1



SFP+ CONNECTOR 2

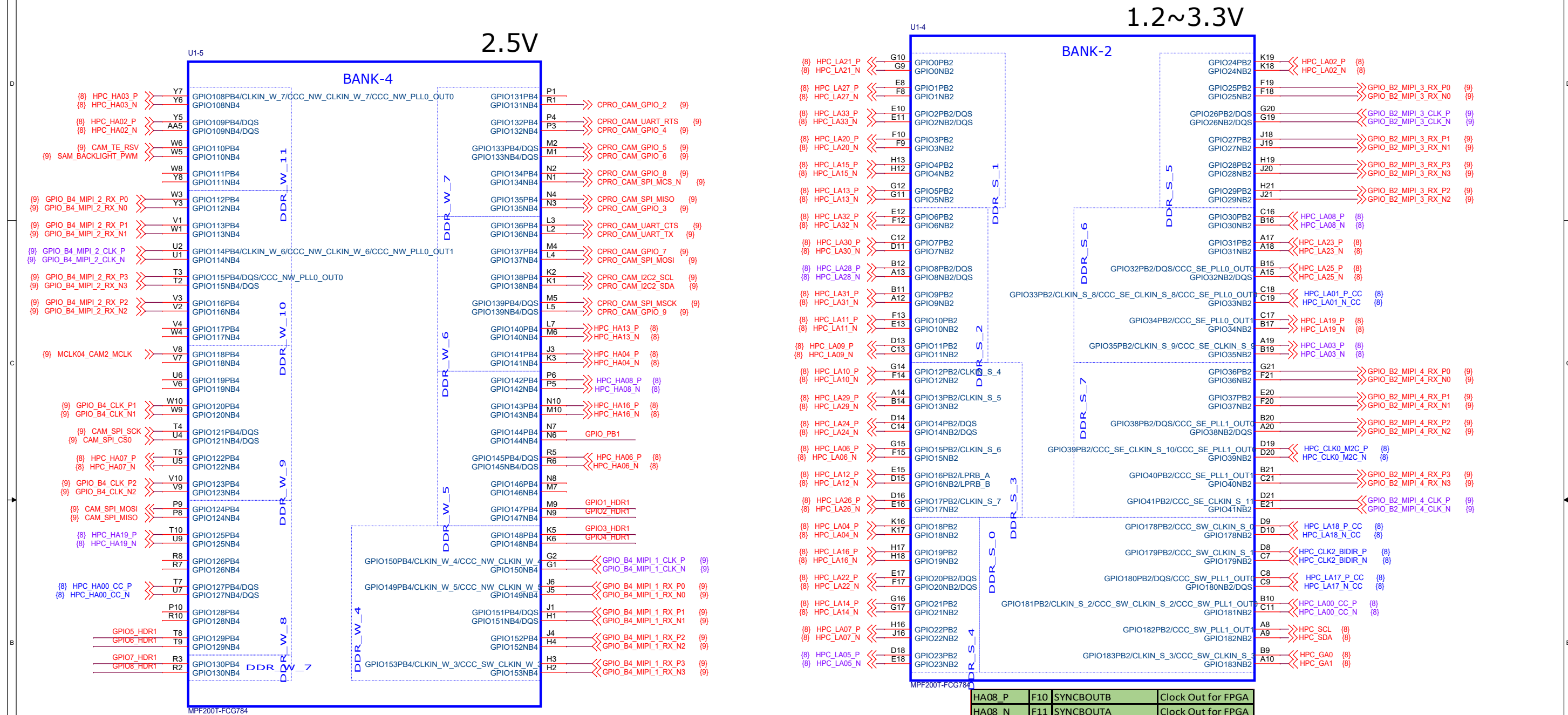


SERDES-2



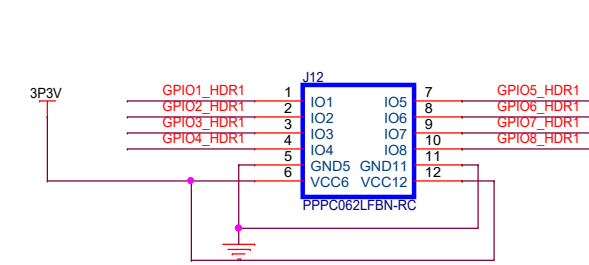
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MPF200-ETH-SENSOR-BRIDGE		
Microchip		
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GPIO Bank 2,4, SERDES3 CONNECTION

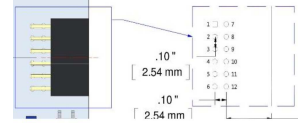


All the MIPI signals must be assigned on same DDR bank and clk should be connected to CCC_CLK_IN pin of FPGA

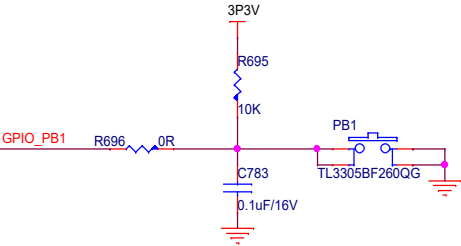
Pmod Interface Type 1A (Expanded GPIO)



The pinout have been fixed based on PMOD Spec



Push Button

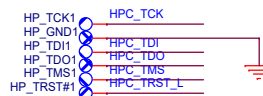
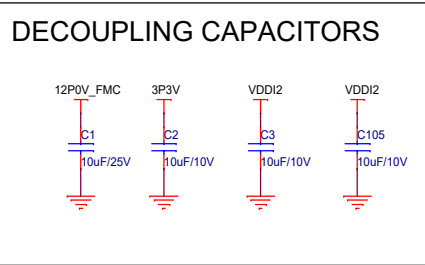
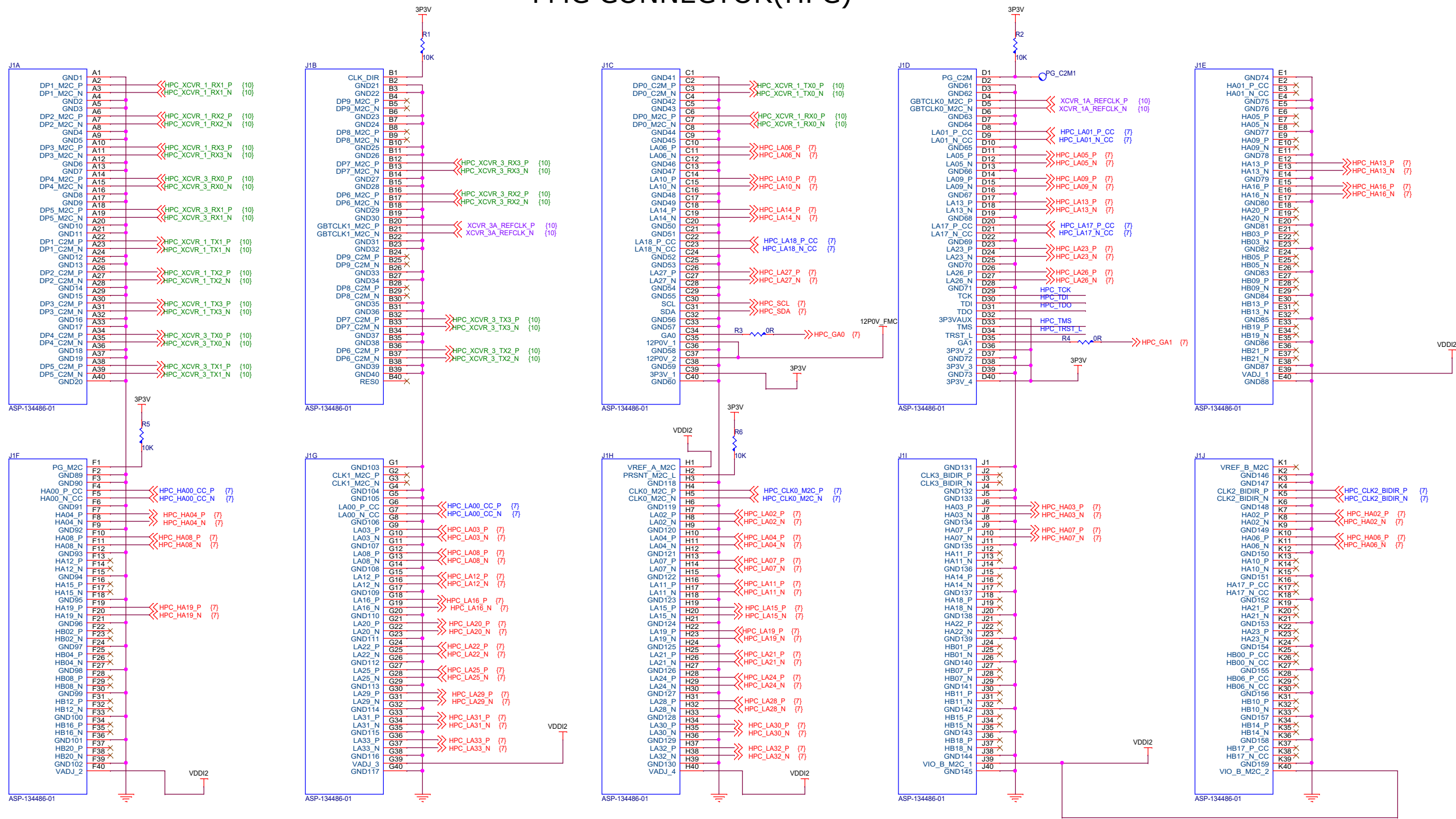


HA08_P	F10	SYNCOUBTB	Clock Out for FPGA
HA08_N	F11	SYNCOUBTA	Clock Out for FPGA
HA19_P	F20	SYNCOUBTD	Clock Out for FPGA
HA19_N	F21	SYNCOUBTC	Clock Out for FPGA
LA08_P	G12	SYNCBINB	Clock Out for FPGA
LA08_N	G13	SYNCBINA	Clock Out for FPGA
LA28_P	H31	SYNCBIND	Clock Out for FPGA
LA28_N	H32	SYNCBINC	Clock Out for FPGA
LA03_P	G9	ADC_SYSREF_P	Clock in for FPGA
LA03_N	G10	ADC_SYSREF_N	Clock in for FPGA
LA05_P	D11	DAC_SYSREF_P	Clock in for FPGA
LA05_N	D12	DAC_SYSREF_N	Clock in for FPGA
LA00_P_CC	G6	FPGA_JESD_CLK_B_P	Clock in for FPGA
LA00_N_CC	G7	FPGA_JESD_CLK_B_N	Clock in for FPGA



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FMC CONNECTOR(HPC)



Daughter Board Support List

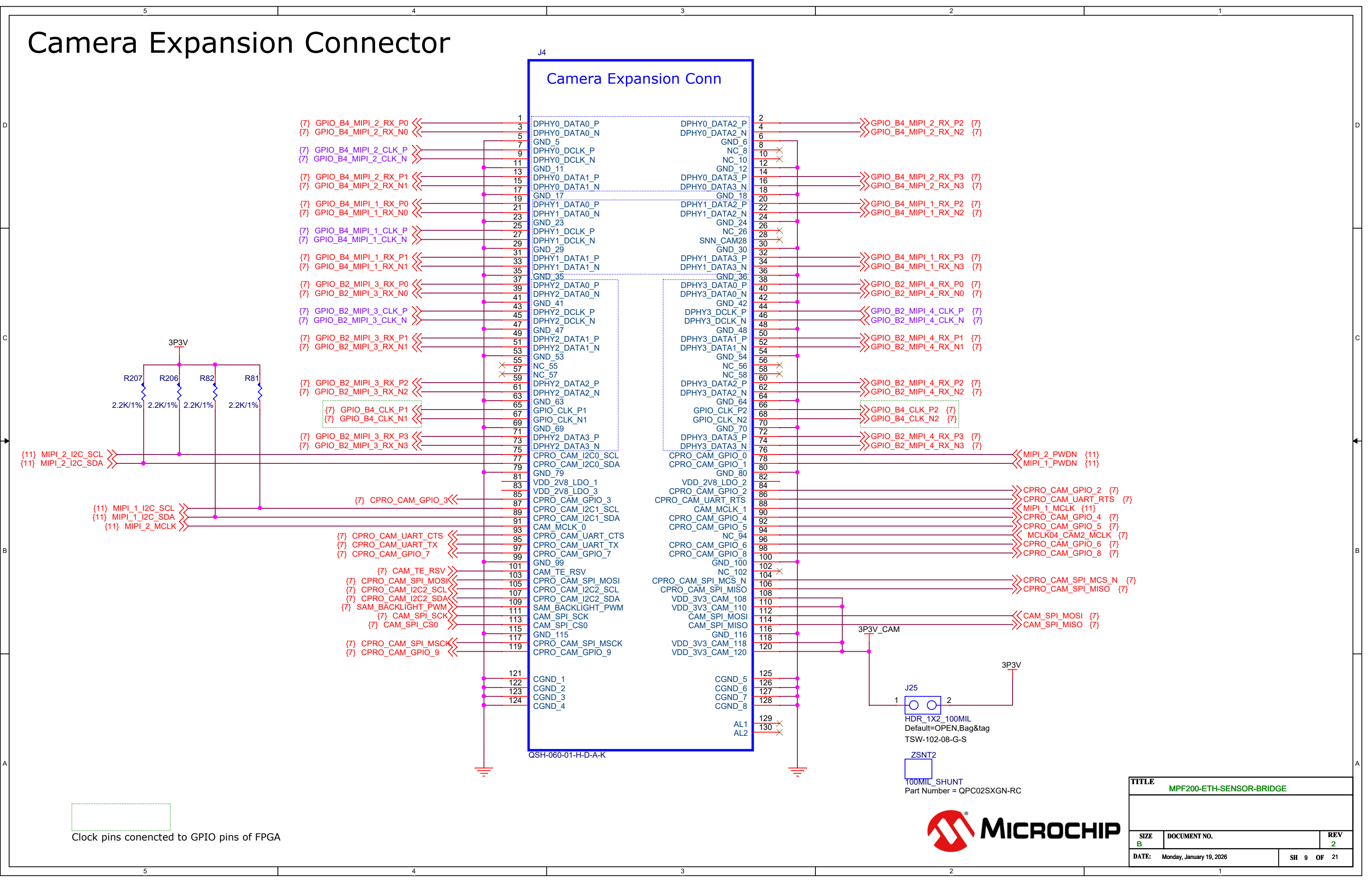
S.No	DB Card
01	DAC38RF8xEVM_RevE
02	LI-IMX530-SLVS-FMC_V1.01
03	DC079C_AFE77xxEVM

NOTE:
 1.FMC HPC LA ,HA and HB bank IO's support maximum of 3.3V.
 2.The Supporting Voltages of FMC HPC(VCCIO_HPC_VADJ) are 1.2V,1.5V,1.8V, 2.5V and 3.3V.



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Camera Expansion Connector



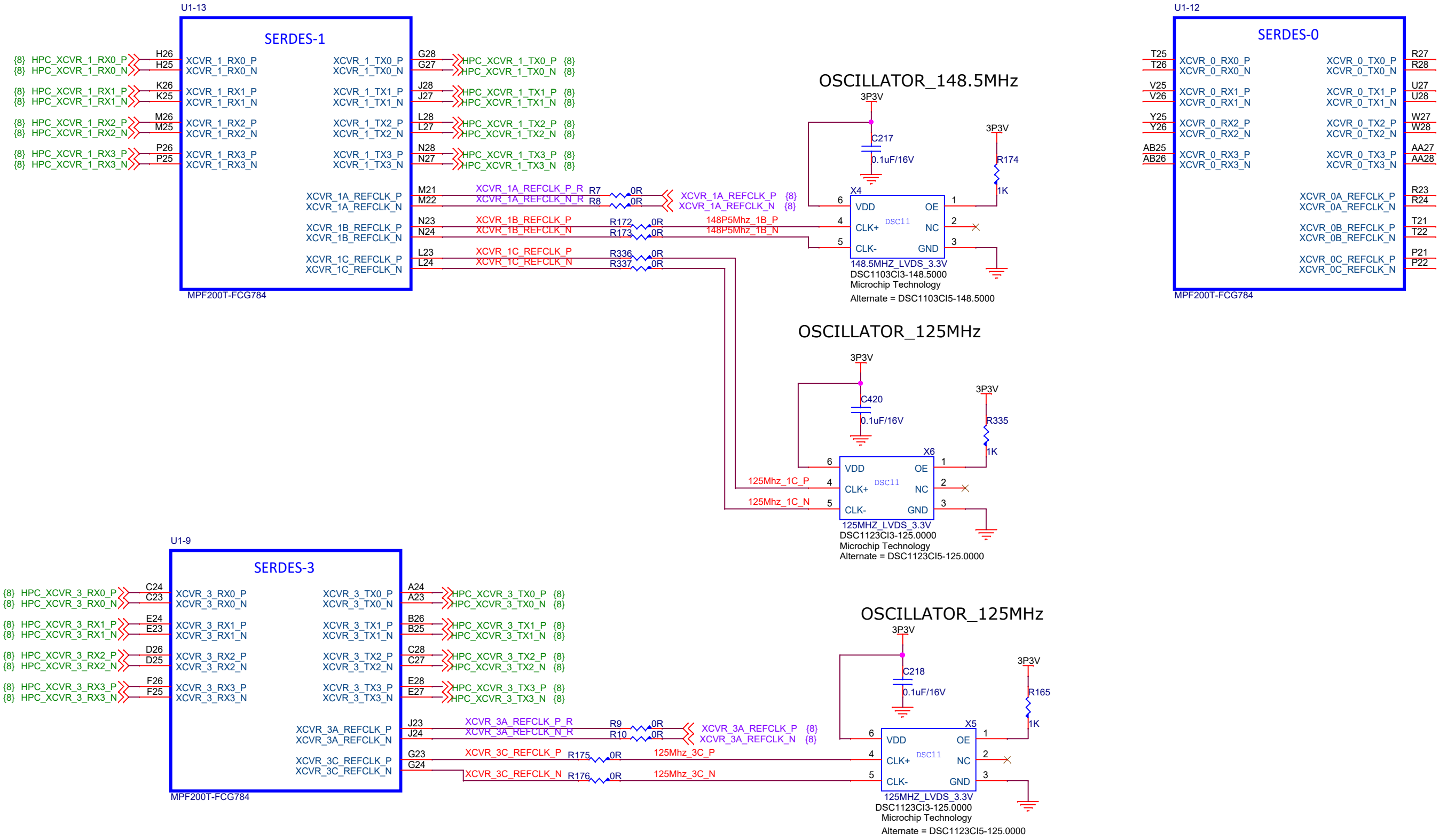
Clock pins conected to GPIO pins of FPGA



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MPF200-ETH-SENSOR-BRIDGE		
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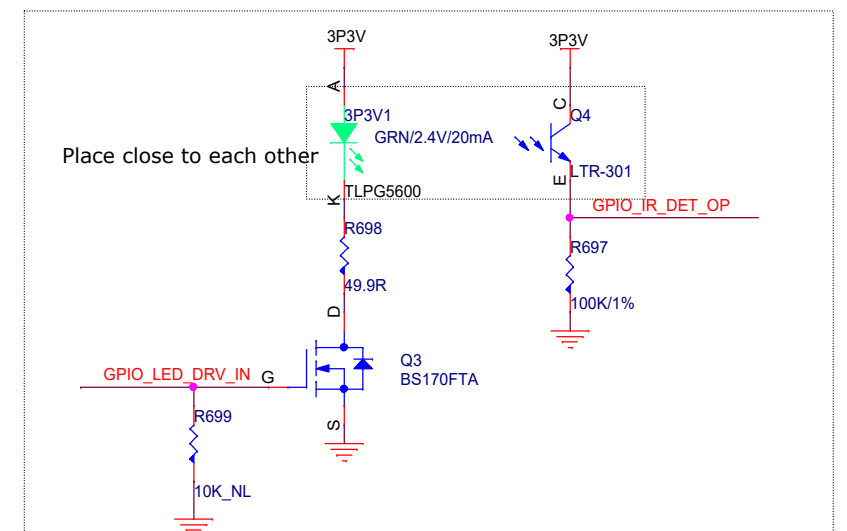
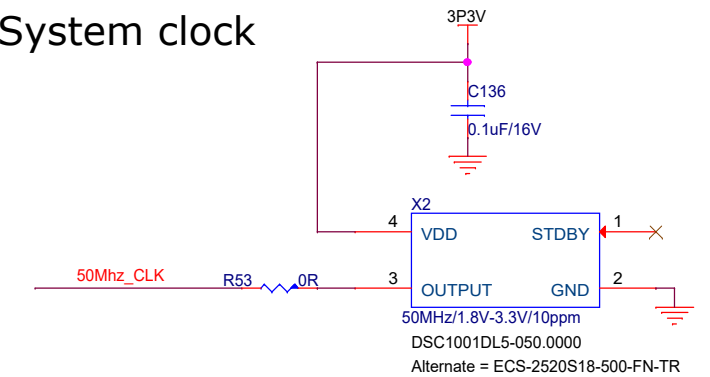
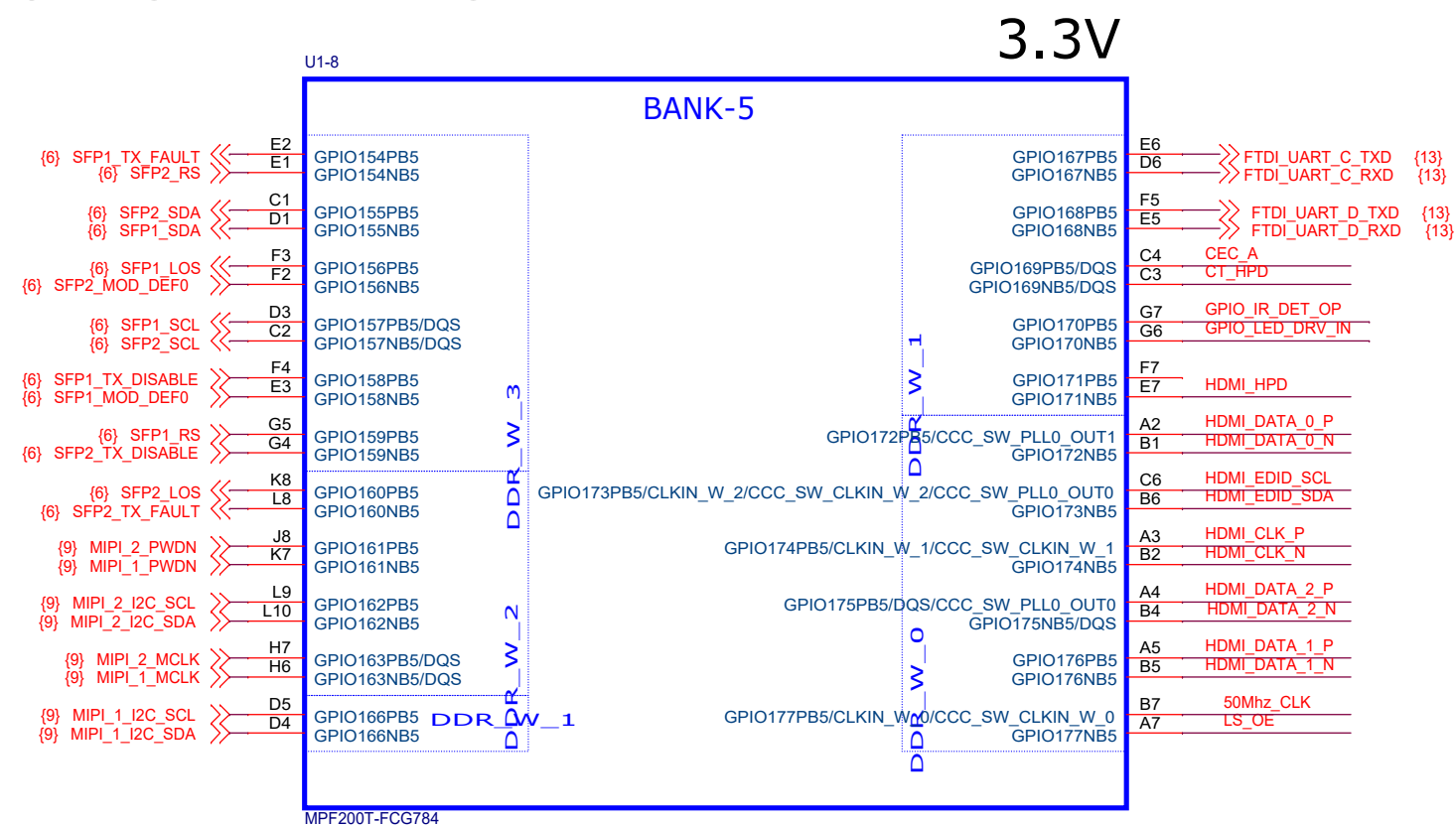
SERDES CONNECTION

NC

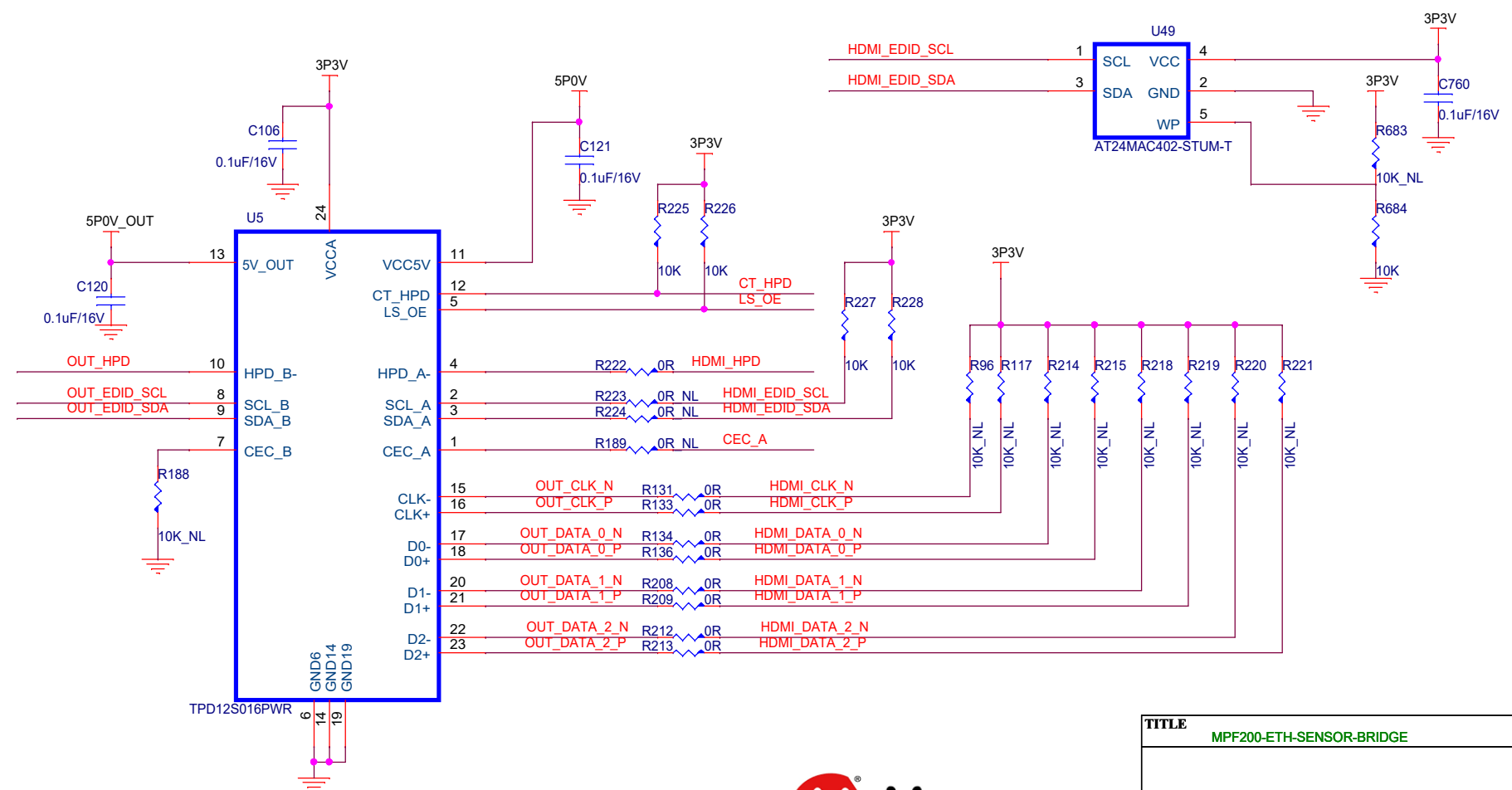
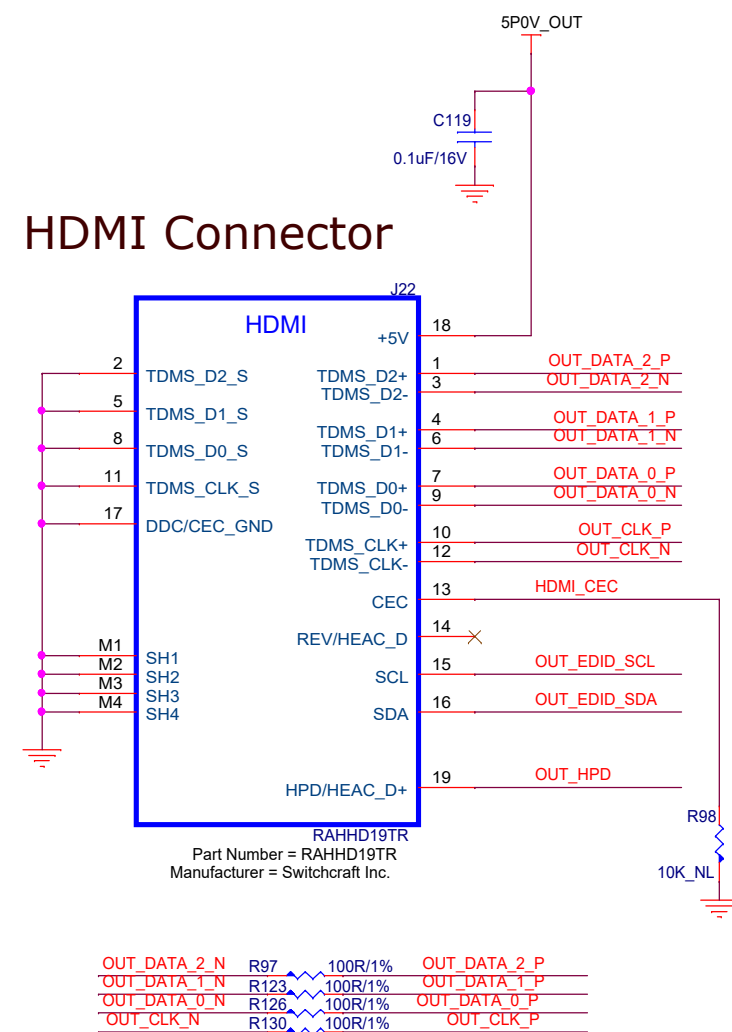


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MPF200-ETH-SENSOR-BRIDGE		
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GPIO Bank 5 CONNECTION

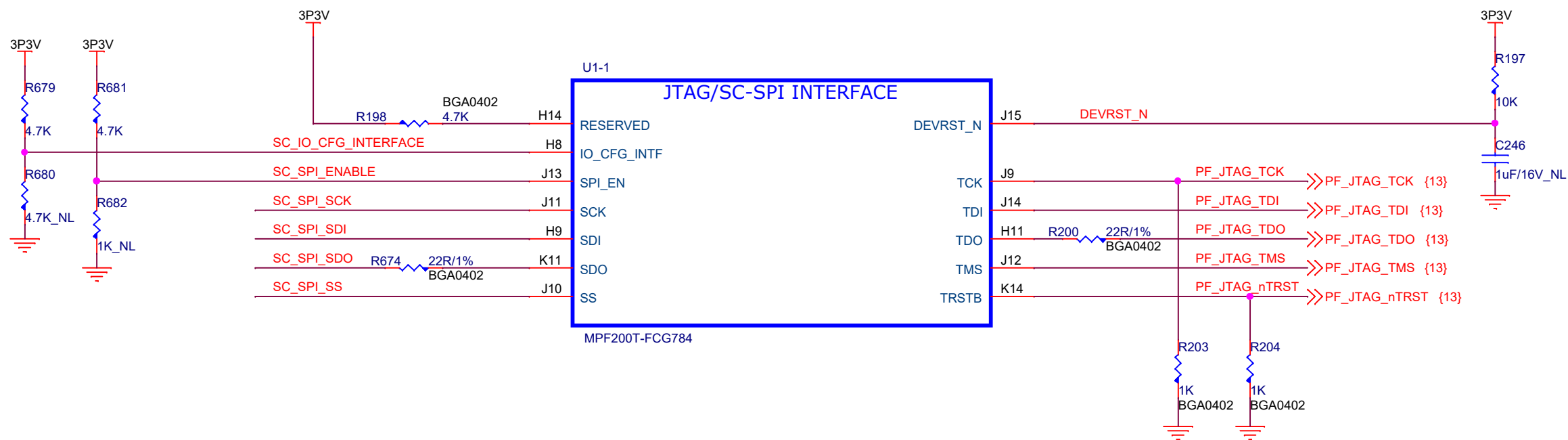


HDMI Connector

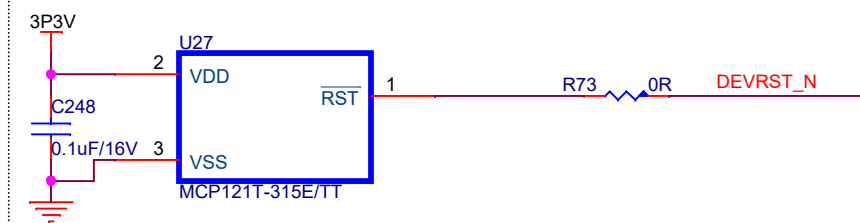


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SIZE Custom	DOCUMENT NO.		REV 2
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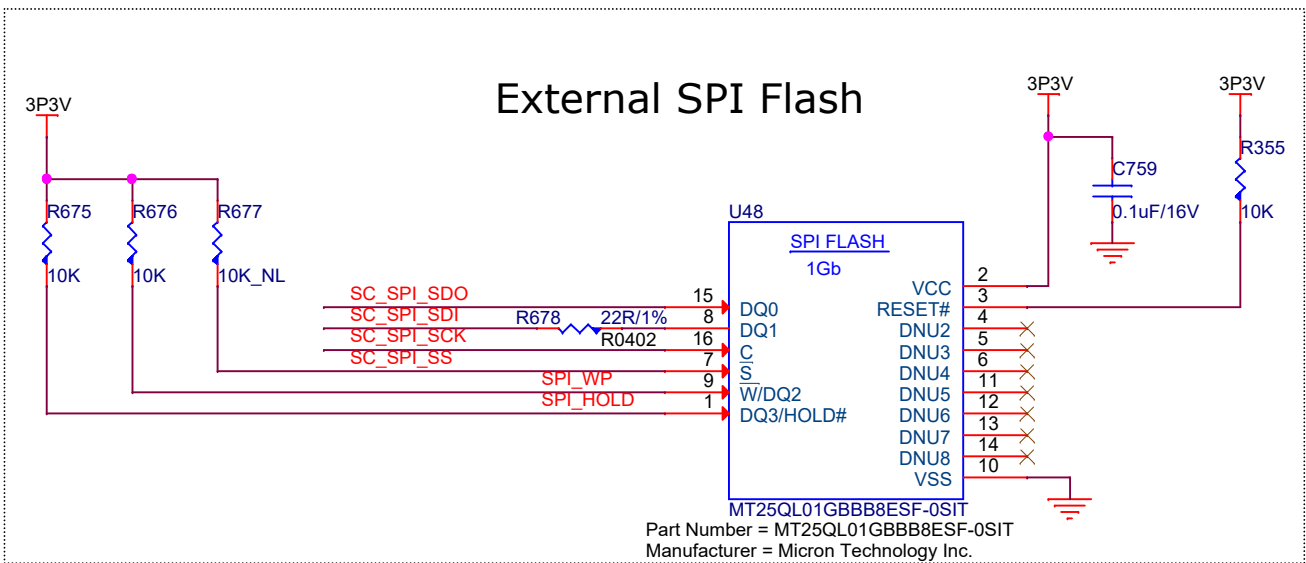
Bank 3 CONNECTION



Device Reset

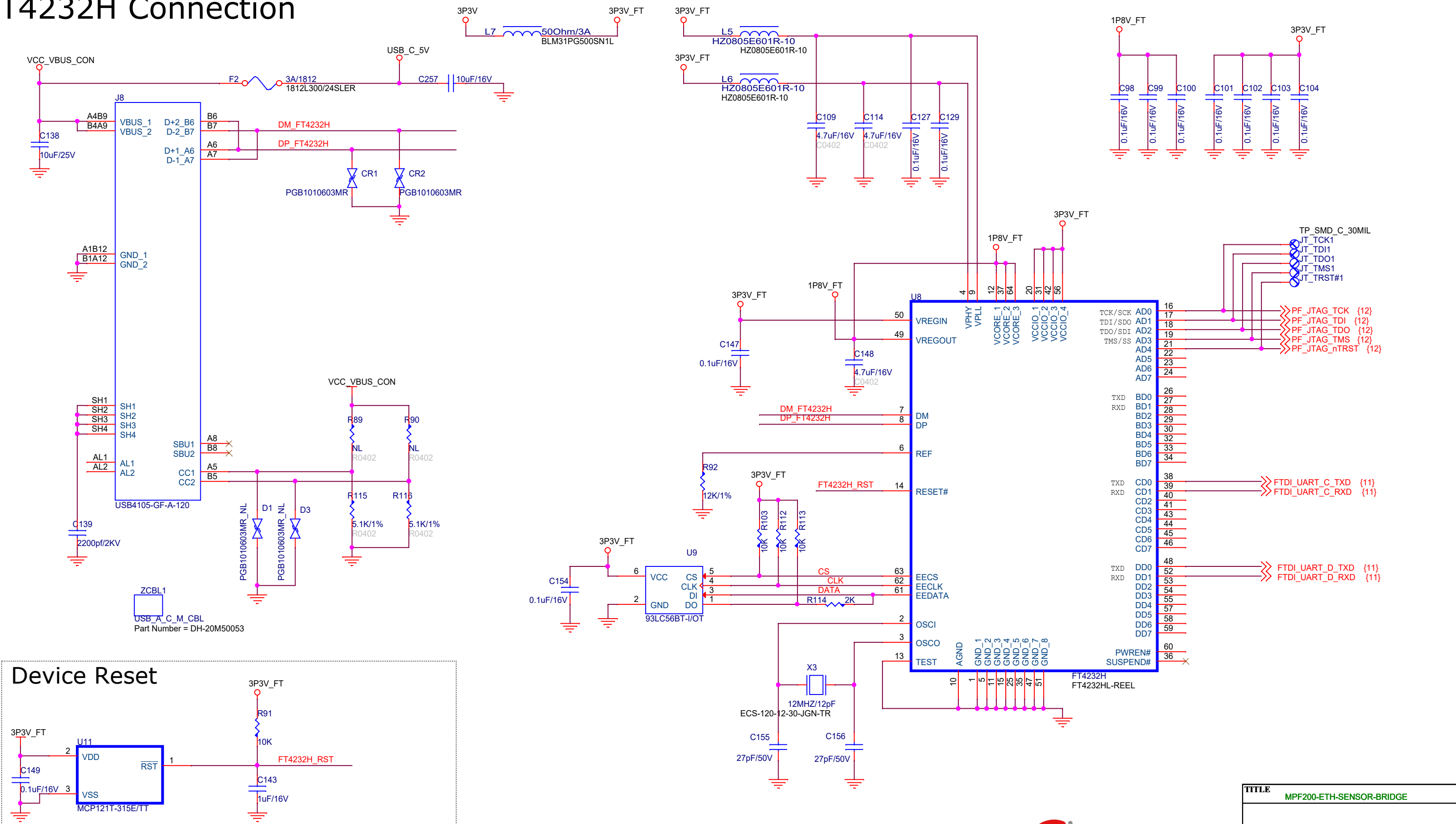


External SPI Flash



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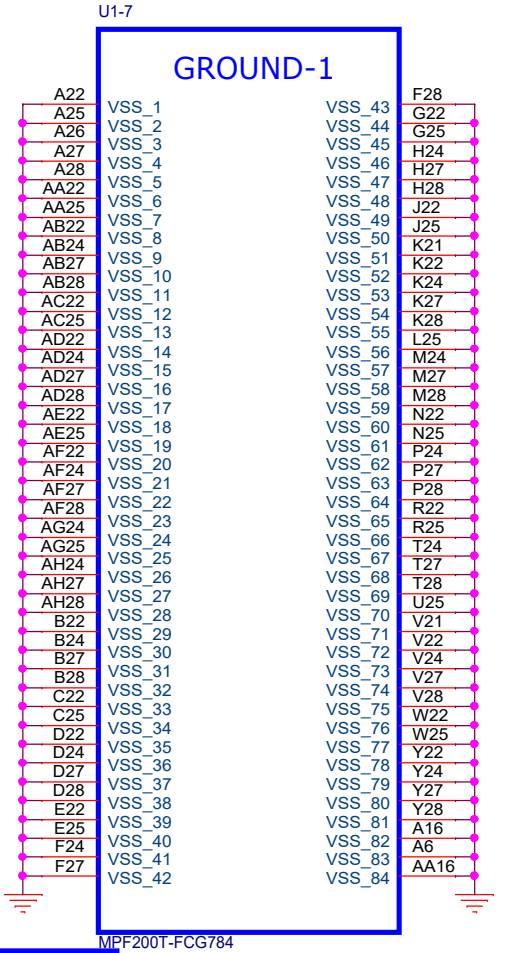
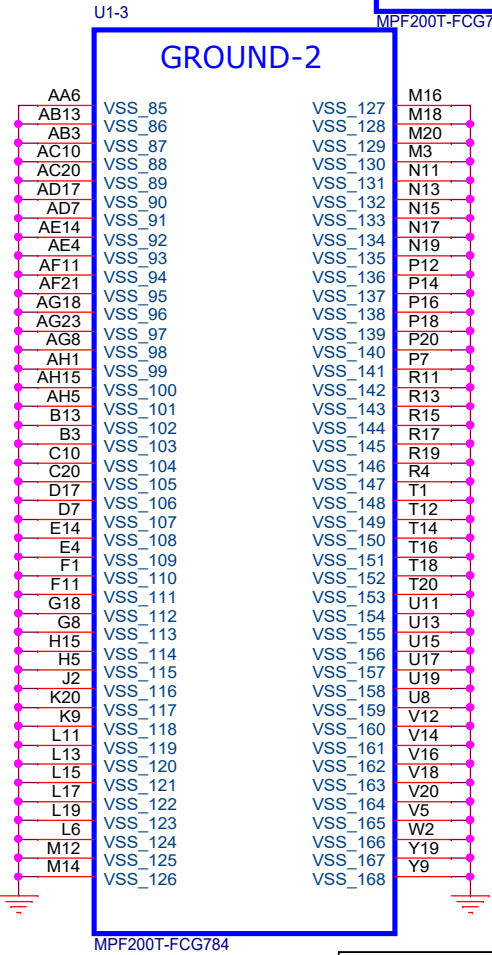
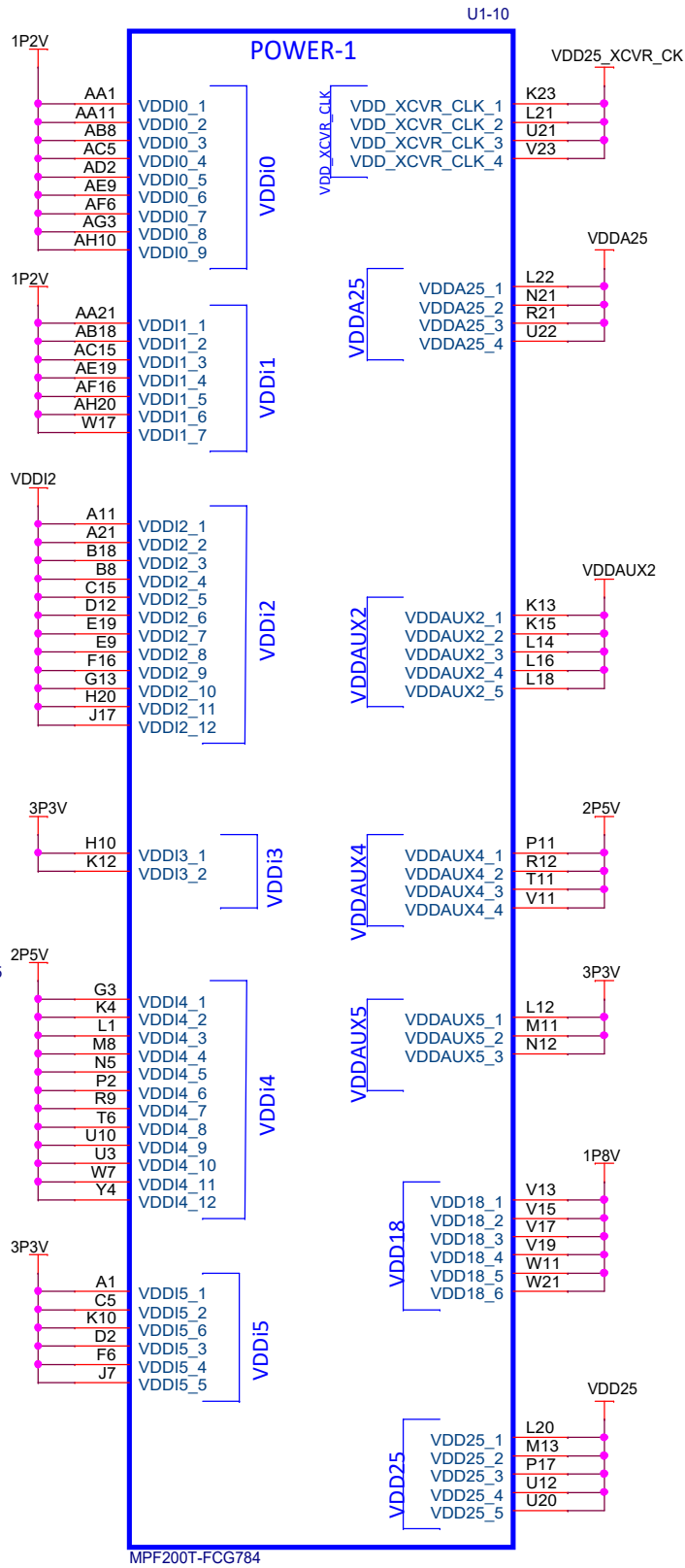
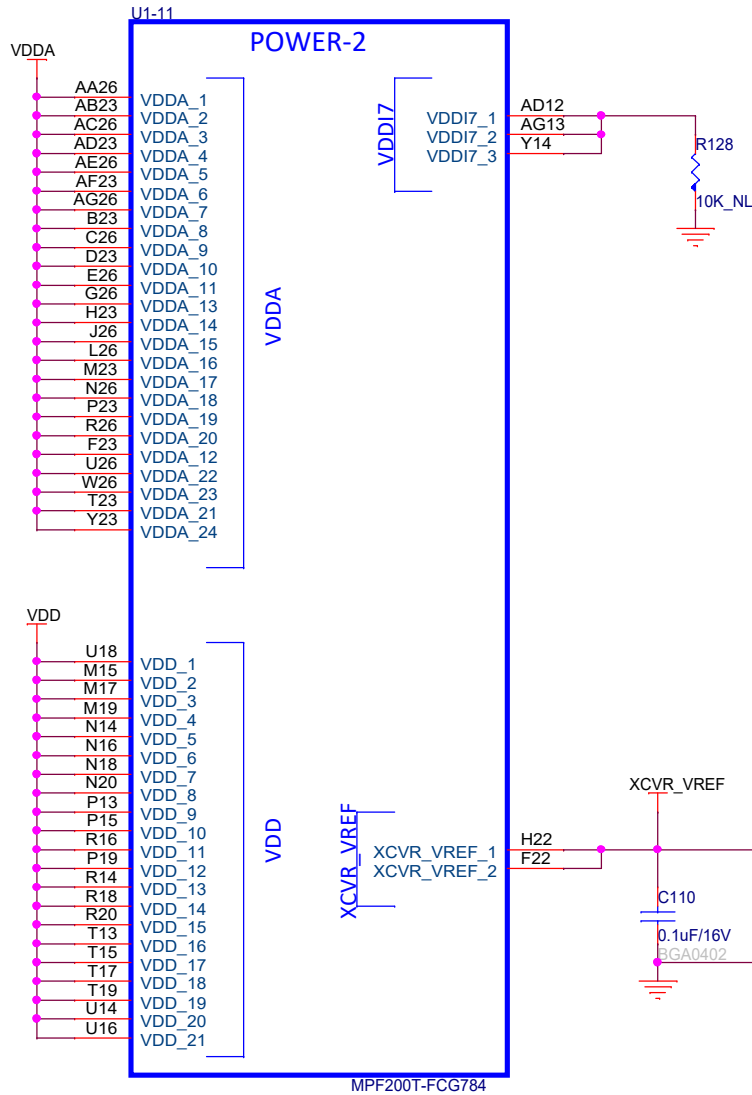
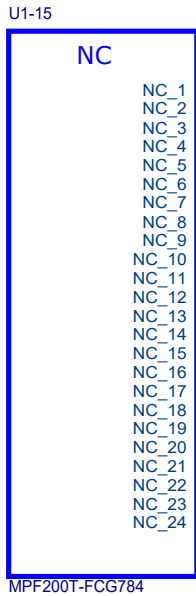
FT4232H Connection



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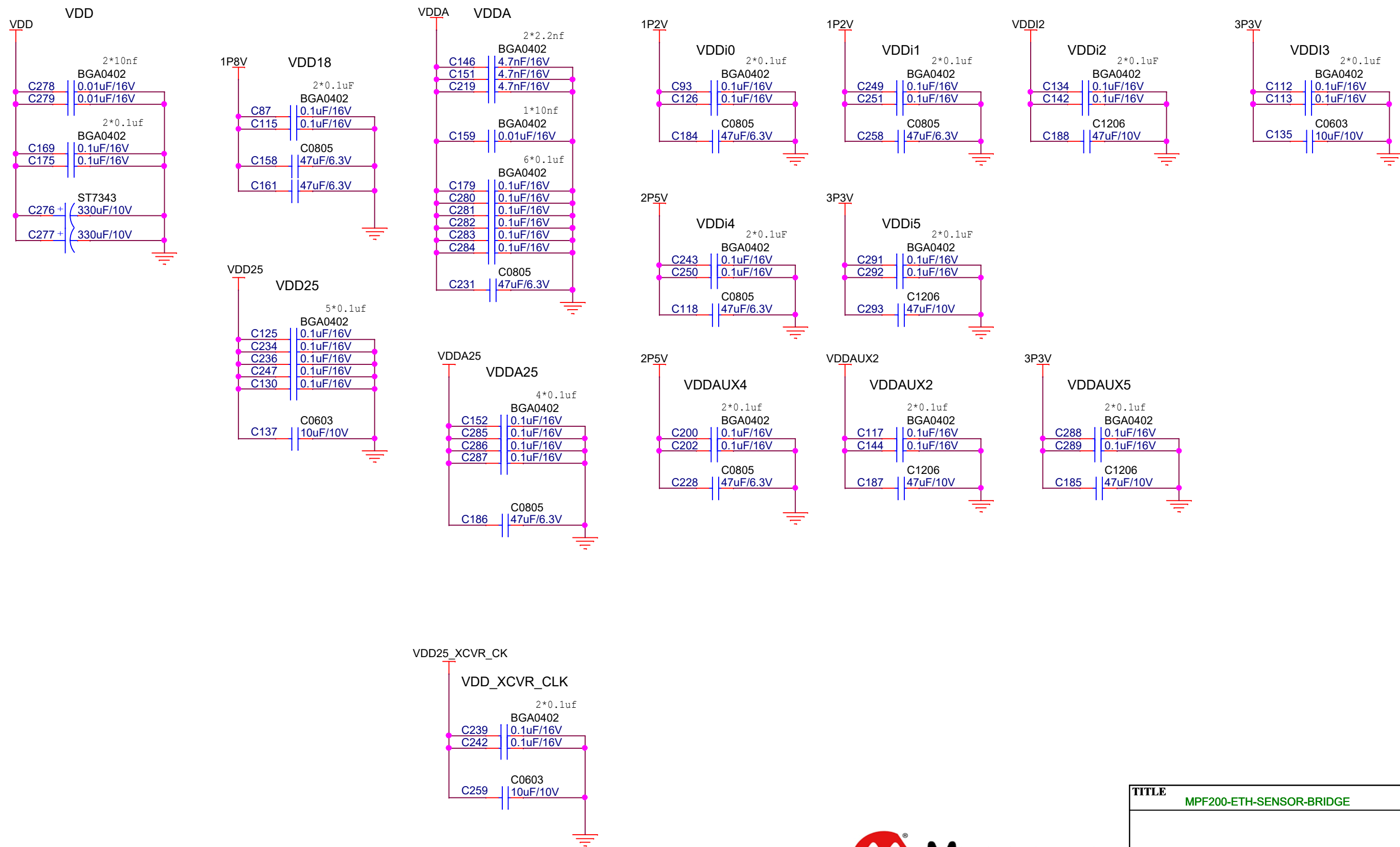
POWER CONNECTION

D
C
B
A



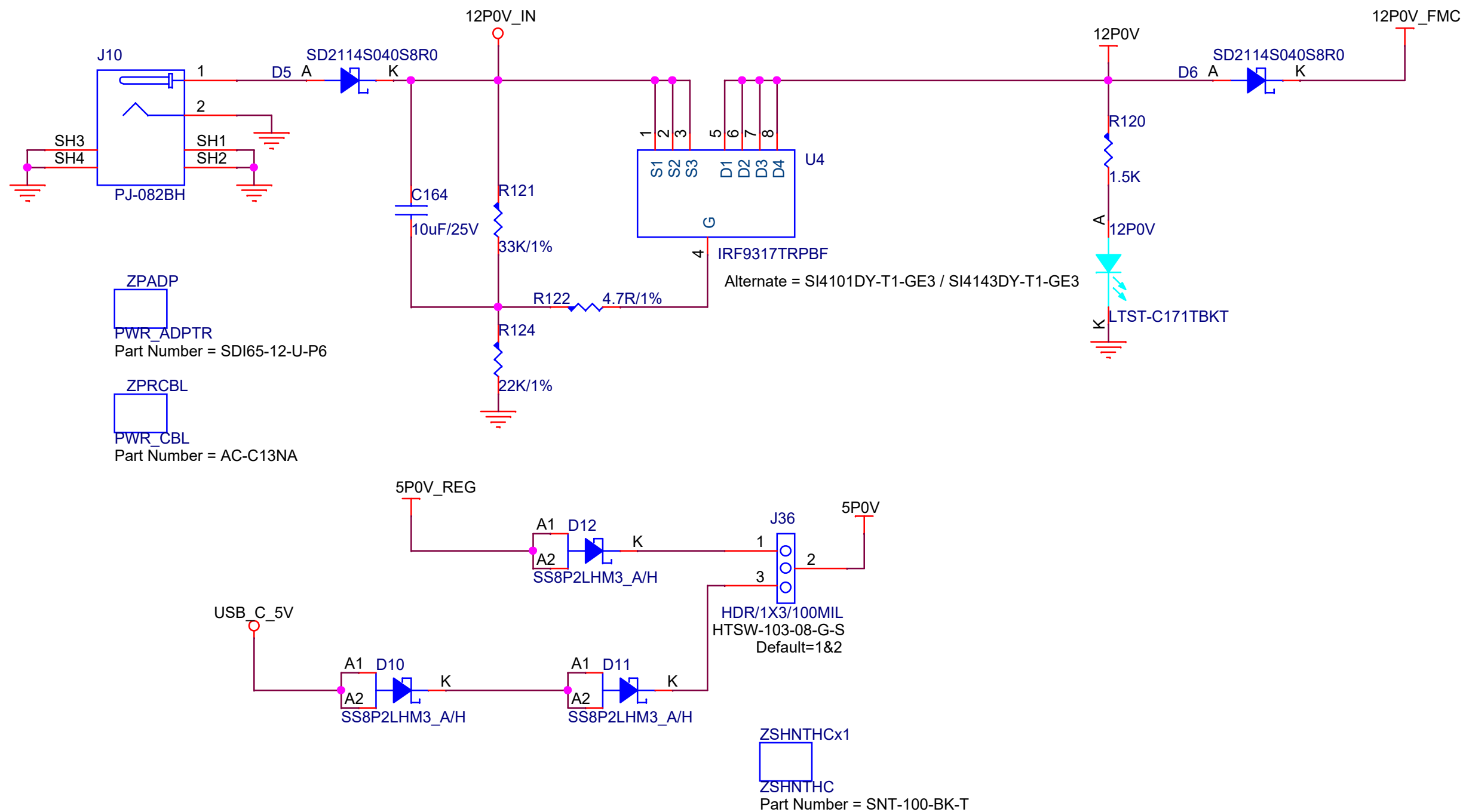
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MPF200-ETH-SENSOR-BRIDGE		
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Decoupling Capacitors



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12V DC Supply

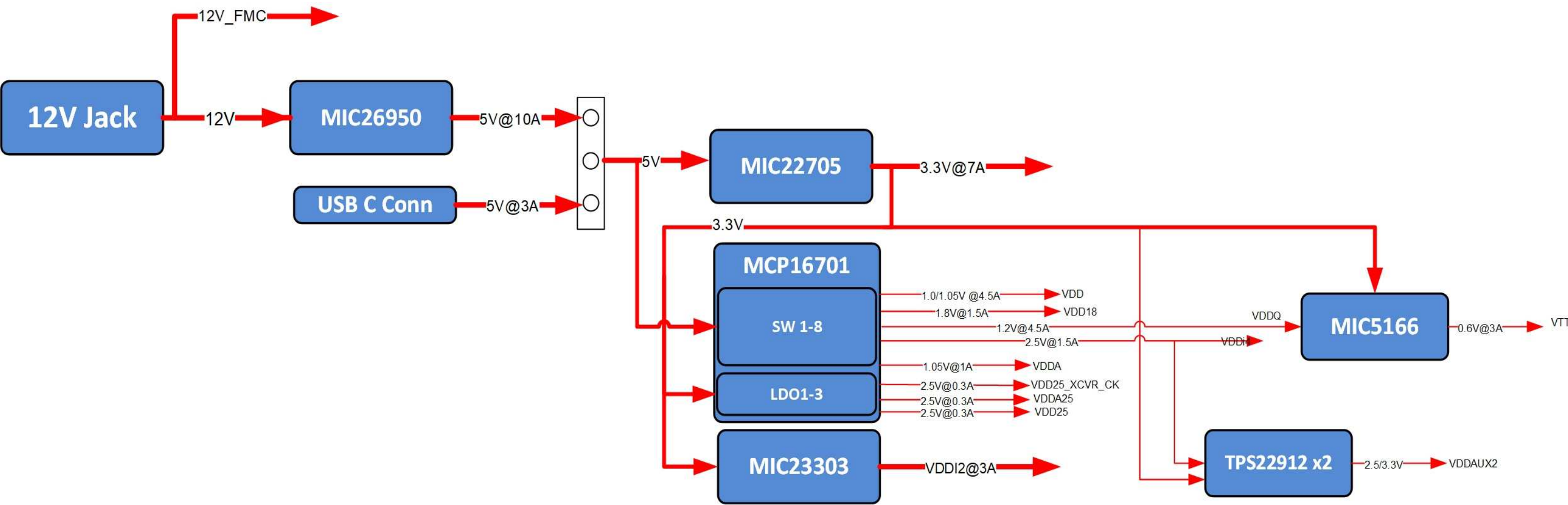


Select the 12V-to-5V regulator if the board power consumption exceeds 15 W or when the FMC connector or HDMI interface is in use.



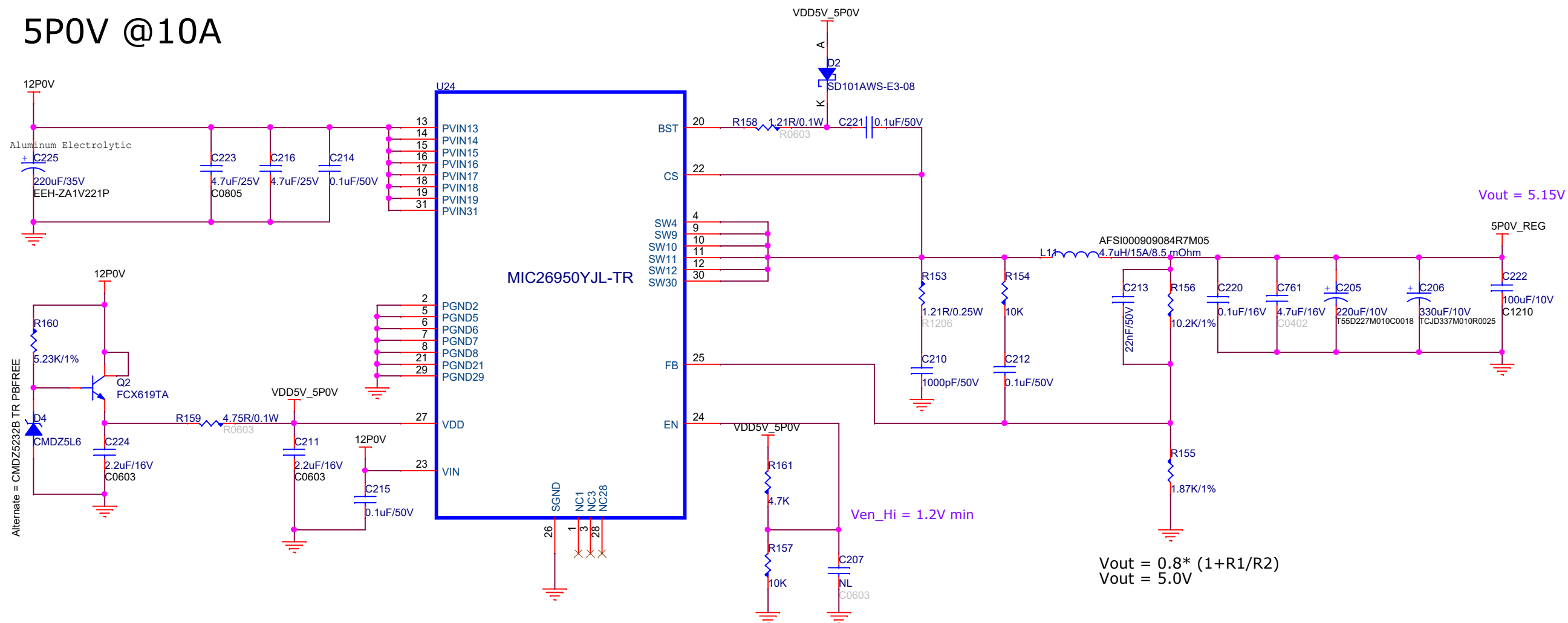
TITLE		
MPF200-ETH-SENSOR-BRIDGE		
Microchip		
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A		2
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Power Flow Diagram

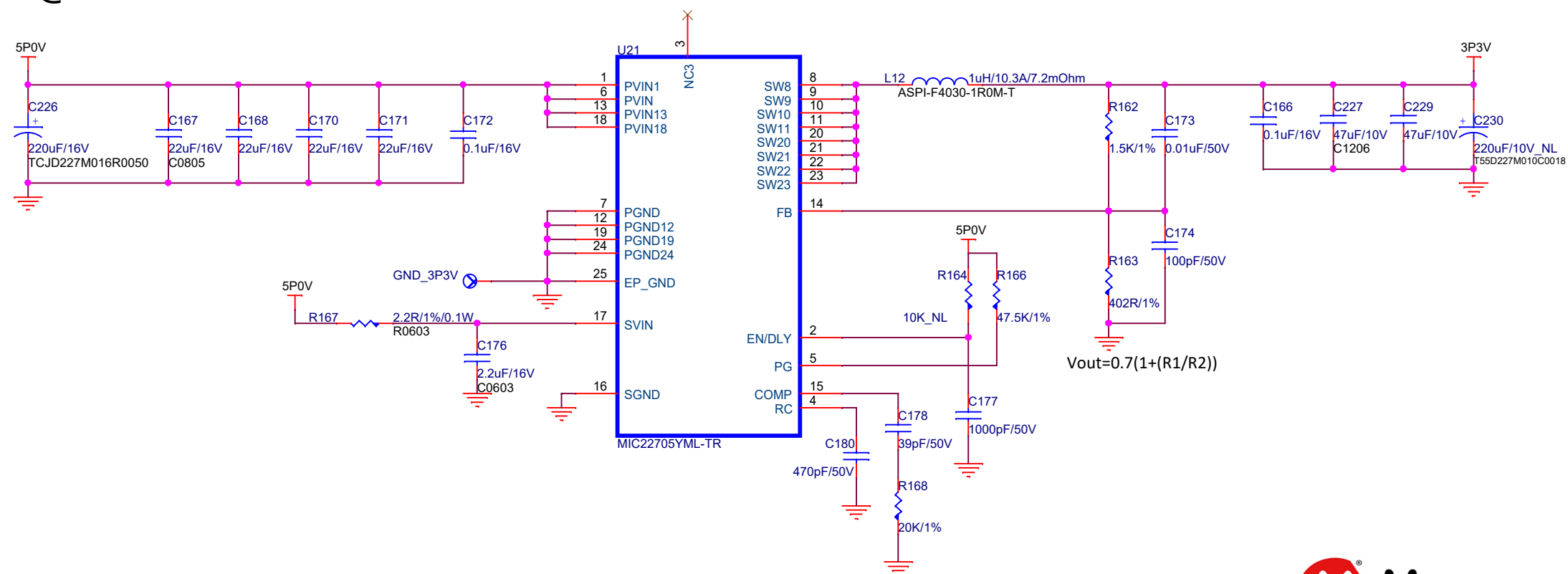


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5P0V @10A



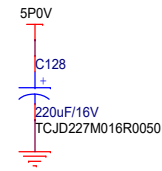
3P3V @7A



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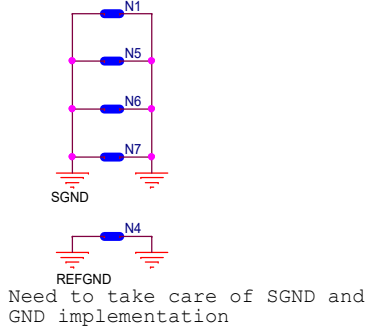
PMIC Connection 1.2V @4.5A

1.0/1.05V @4.5A



2P5V for VDDAUX4, VDDI4, VPP @1.5A

1.8V @1.5A

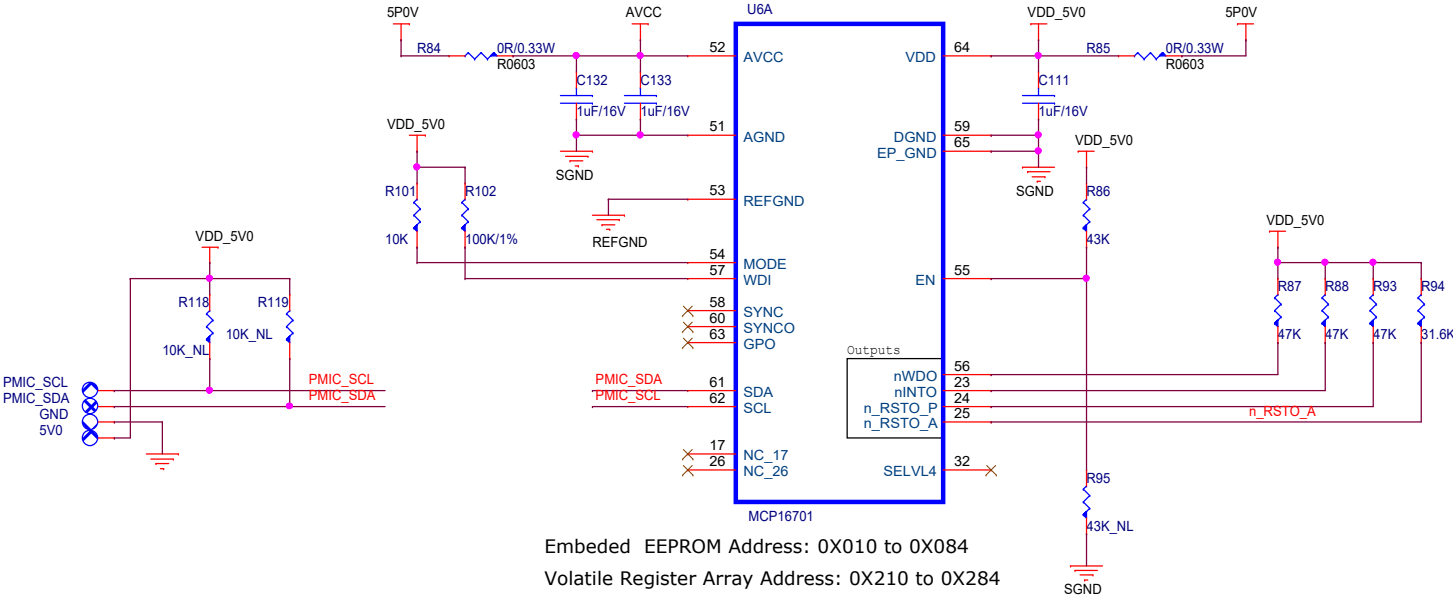


VDD25 @0.3A

VDD_XCVR_CK @0.3A

VDDA25 @0.3A

1.0/1.05V @1A



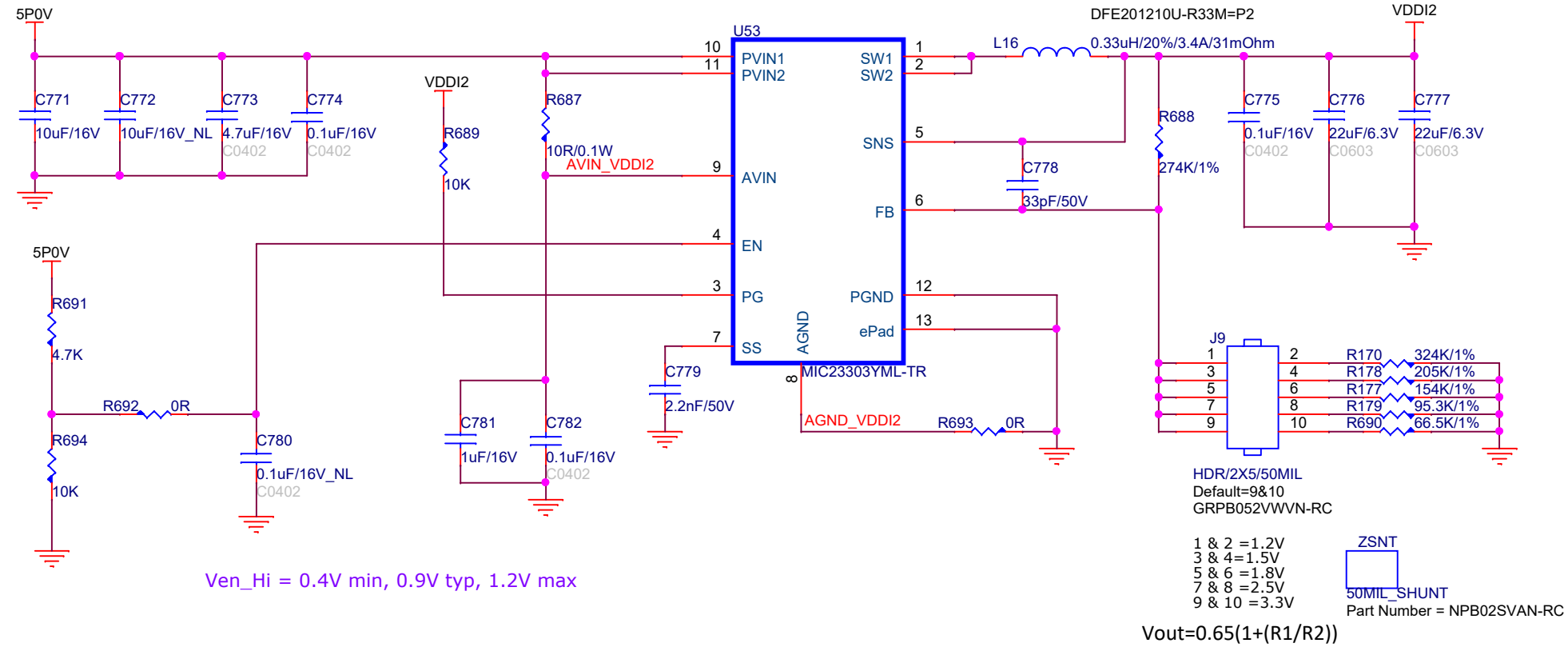
Embedded EEPROM Address: 0X010 to 0X084
Volatile Register Array Address: 0X210 to 0X284

GPO, SYNCO (Output) - Voh = 2.6Vmin, Vol=0.4max
SCL, SDA - Vih = 1.5Vmin, Vil=0.4max
En, WDI, SYNC (Input) - Vih = 1.5Vmin, Vil=0.4max
nWDO, nINTO, nRSTO_P, nRSTO_A (Open Drain Output) - Vol = 0.4max

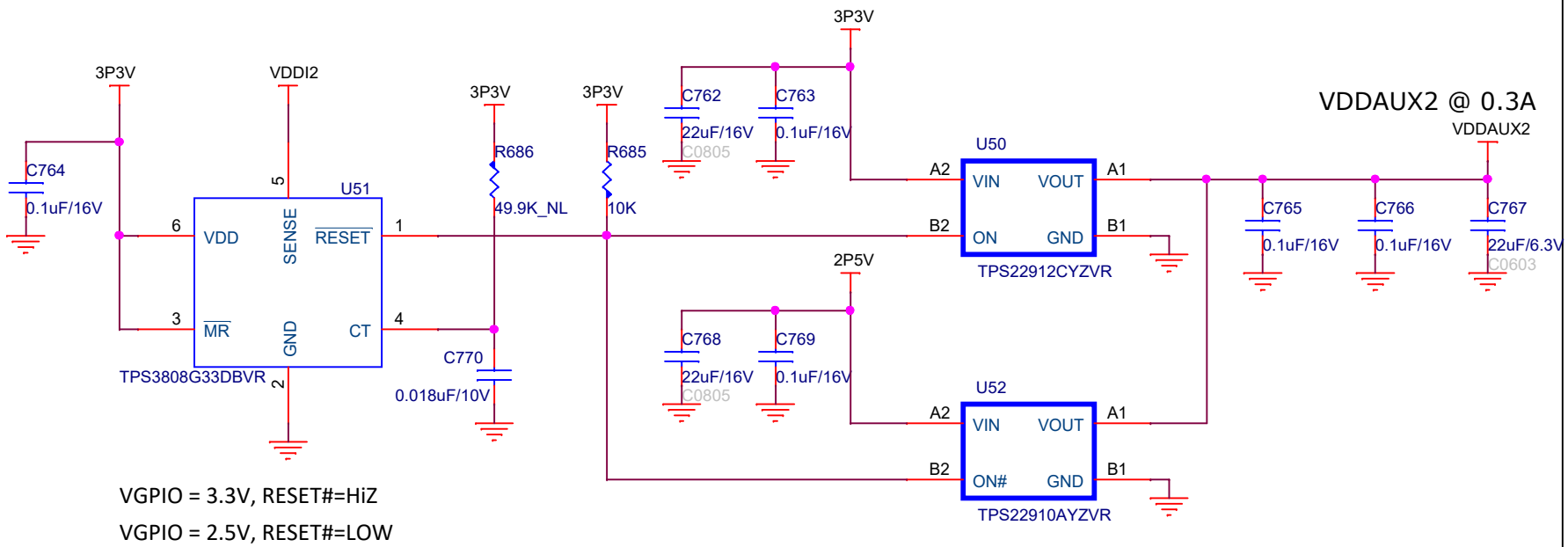


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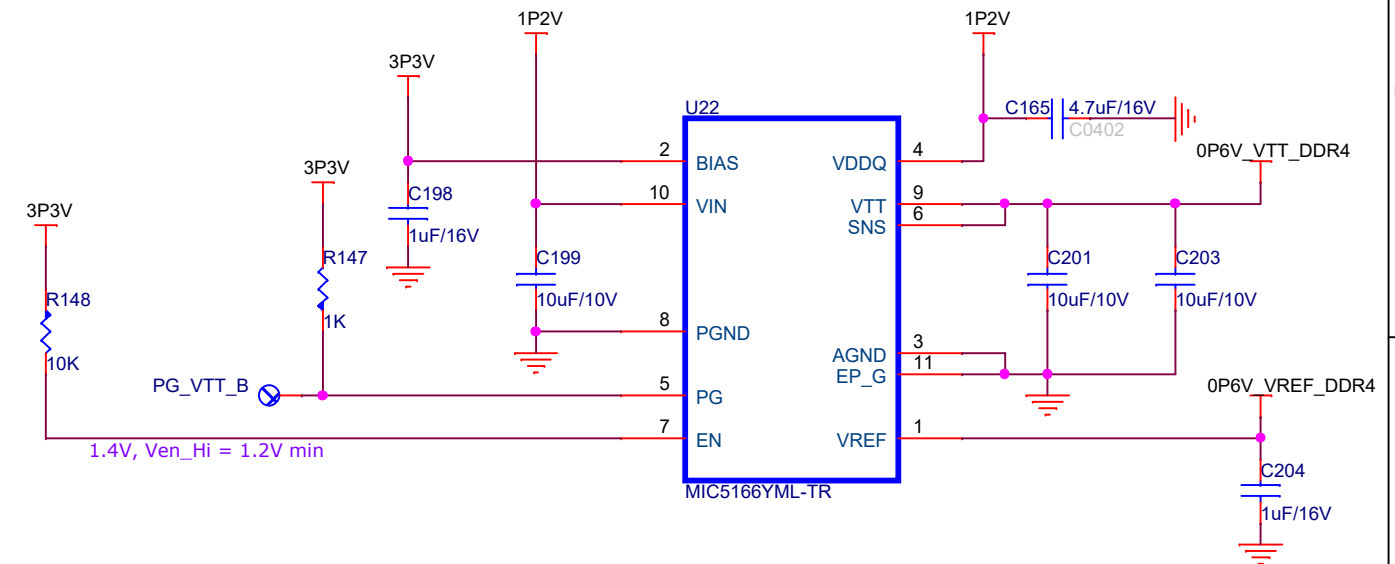
POWER:VDDI2 @3A (1.2/1.5/1.8/2.5/3.3V)



POWER:2.5/3.3V Selection for VDDAUX1

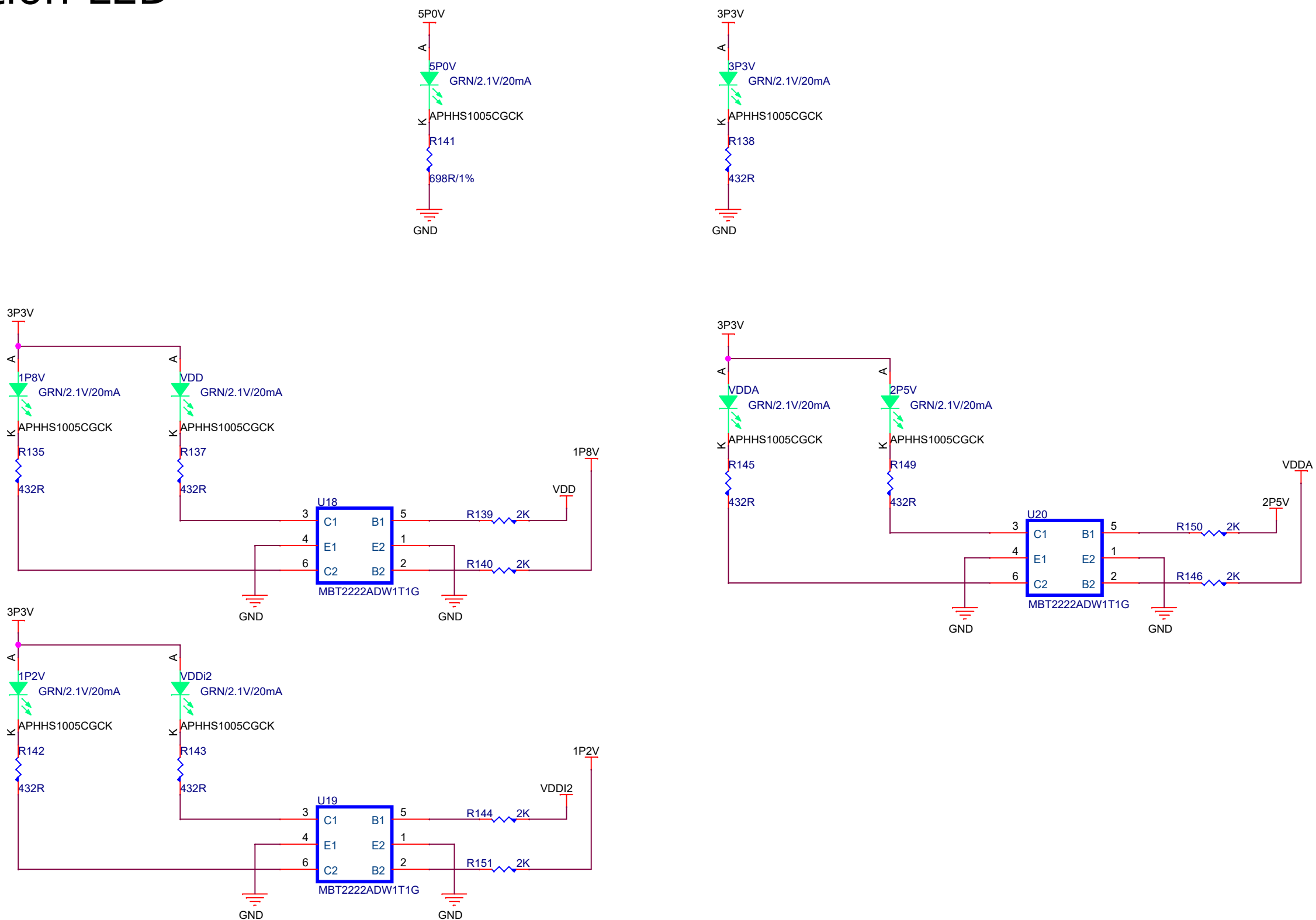


POWER:0.6V for DDR4_VREF



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Power Indication LED



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