X67BC8321.L12

1 General information

1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX67	X67 system user's manual
MAEMV	Installation / EMC guide

1.2 Order data

Order number	Short description	Figure
	Bus controller modules	
X67BC8321.L12	X67 bus controller, 1 POWERLINK interface, X2X Link power supply 15 W, 16 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz, M12 connectors, high-density module	

Table 1: X67BC8321.L12 - Order data

Required accessories
See "Required cables and connectors" on page 9. For a general overview, see section "Accessories - General overview" in the X67 system user's manual.

1.3 Module description

The bus controller makes it possible to connect X2X Link I/O nodes to POWERLINK. It is also possible to operate the X2X Link cycle synchronously 1:1 or synchronous to POWERLINK using a prescaler.

The interface is equipped with 2 connections. Both connections are connected to an integrated switch. This makes it easy to implement daisy chain cabling.

Functions:

- POWERLINK
- Digital inputs
- Event counter / Gate measurement
- Digital outputs
- Monitoring the operating limits

POWERLINK

POWERLINK is a standard protocol for Fast Ethernet equipped with hard real-time characteristics.

Digital inputs

The digital inputs are equipped with an input filter with a configurable input delay. The input states can also be latched if required.

Event counter / Gate measurement

The module has 2 counter channels that can be used either as event counters or for gate measurement.

Monitoring status of the digital outputs

The output signal of the digital outputs is monitored for short circuit or overload.

Monitoring operating limits

The voltage of the I/O power supply is monitored for voltage overshoot or undershoot.

2 Technical description

2.1 Technical data

Order number	X67BC8321.L12
Short description	
Bus controller	POWERLINK (V1/V2) controlled node
General information	
Inputs/Outputs	16 digital channels, configurable as inputs or outputs using software, inputs with additional functions
Insulation voltage between channel and bus	500 V_{eff}
Nominal voltage	24 VDC
B&R ID code	
Bus controller	0xA90E
Internal I/O module	0x1A1D
Sensor/Actuator power supply	0.5 A summation current
Status indicators	I/O function per channel, supply voltage, bus function
Diagnostics	
Outputs	Yes, using LED status indicator and software
I/O power supply	Yes, using LED status indicator and software
Support	
Dynamic node allocation (DNA)	Yes
Connection type	
Fieldbus	M12, D-coded
X2X Link	M12, B-coded
Inputs/Outputs	8x M12, A-coded
I/O power supply	M8, 4-pin
Power output	15 W X2X Link power supply for I/O modules
Power consumption	
Fieldbus	4.2 W
Internal I/O	2.5 W
X2X Link power supply	24.3 W at maximum power output for connected I/O modules
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA IIA T5 Gc IP67, Ta = 0 - Max. 60°C TÜV 05 ATEX 7201X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
EAC	Yes
KC	Yes
Interfaces	
Fieldbus	POWERLINK (V1/V2) controlled node
Type	Type 2 [1]
Variant	2x M12 interface (hub), 2x female connector on module
Line length	Max. 100 m between 2 stations (segment length)
Transfer rate	100 Mbit/s
Transfer	
Physical layer	100BASE-TX
Half-duplex	Yes
Full-duplex	No
Autonegotiation	Yes
Auto-MDI/MDIX	Yes
Hub propagation delay	0.96 to 1 µs
Min. cycle time [2]	
Fieldbus	200 µs
X2X Link	200 µs
Synchronization between bus systems possible	Yes
I/O power supply	
Nominal voltage	24 VDC
Voltage range	18 to 30 VDC
Integrated protection	Reverse polarity protection
Power consumption	
Sensor/Actuator power supply	Max. 12 W [3]
Sensor/Actuator power supply	
Voltage	I/O power supply minus voltage drop for short-circuit protection
Voltage drop for short-circuit protection at 0.5 A	Max. 2 VDC
Summation current	Max. 0.5 A
Short-circuit proof	Yes

Table 2: X67BC8321.L12 - Technical data

Order number	X67BC8321.L12
Digital inputs	
Input characteristics per EN 61131-2	Type 1
Input voltage	18 to 30 VDC
Input current at 24 VDC	Typ. 4 mA
Input circuit	Sink
Input filter	
Hardware	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 16)
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Input resistance	Typ. 6 kΩ
Additional functions	50 kHz event counting, gate measurement
Switching threshold	
Low	<5 VDC
High	>15 VDC
Event counters	
Quantity	2
Signal form	Square wave pulse
Evaluation	Each negative edge, cyclic counter
Input frequency	Max. 50 kHz
Counter 1	Input 1
Counter 2	Input 3
Counter frequency	Max. 50 kHz
Counter size	16-bit
Gate measurement	
Quantity	1
Signal form	Square wave pulse
Evaluation	Positive edge - Negative edge
Counter frequency	
Internal	48 MHz, 3 MHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 2 or input 4
Digital outputs	
Variant	Current-sourcing FET
Switching voltage	I/O power supply minus residual voltage
Nominal output current	0.5 A
Total nominal current	8 A
Output circuit	Source
Output protection	Thermal shutdown in the event of overcurrent or short circuit, integrated protection for switching inductive loads, reverse polarity protection of the output power supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when the output is switched off	5 µA
Switching on after overload shutdown	Approx. 10 ms (depends on the module temperature)
Residual voltage	<0.3 V at 0.5 A nominal current
Peak short-circuit current	<12 A
Switching delay	
0 → 1	<400 µs
1 → 0	<400 µs
Switching frequency	
Resistive load	Max. 100 Hz
Inductive load	See section "Switching inductive loads".
Braking voltage when switching off inductive loads	50 VDC
Electrical properties	
Electrical isolation	Bus isolated from POWERLINK and channel Channel not isolated from channel
Operating conditions	
Mounting orientation	
Any	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP67
Ambient conditions	
Temperature	
Operation	-25 to 60°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Mechanical properties	
Dimensions	
Width	53 mm
Height	155 mm
Depth	42 mm

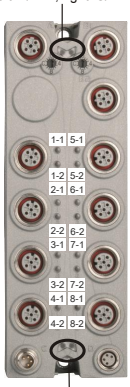
Table 2: X67BC8321.L12 - Technical data

Order number	X67BC8321.L12
Weight	350 g
Torque for connections	
M8	Max. 0.4 Nm
M12	Max. 0.6 Nm

Table 2: X67BC8321.L12 - Technical data

1) For additional information, see section "Communication / POWERLINK / General information / Hardware - CN" in Automation Help.
2) The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring.
3) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

2.2 LED status indicators

Figure	LED	Color	Status	Description
Status indicator 1: Left: L/A IF; right: S/E  Status indicator 2: Left: Green, Right: Red	**Status indicator 1:** Status indicator for POWERLINK bus controller			
	L/A IF	Green	On	The link to the remote station is established.
			Blinking	The link to the remote station is established. The LED blinks if Ethernet activity is taking place on the bus.
	S/E [1]	Green/Red		LED "Status/Error". LED states are described in section "Status/Error LED "S/E"" on page 5.
	I/O LEDs			
	1-1/2 to 8-1/2	Orange	-	Input/Output state of the corresponding channel
	Status indicator 2: Status indicator for module functionality			
	Left	Green	Off	No power to module
			Single flash	Mode RESET
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	Right	Red	Off	Module not supplied with power or everything OK
			On	Error or reset state
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not within the valid range

1) LED "Status/Error" is a green/red dual LED.

2.2.1 Status/Error LED "S/E"

LED "Status/Error" is a green and red dual LED. The color green (status) is superimposed on the color red (error).

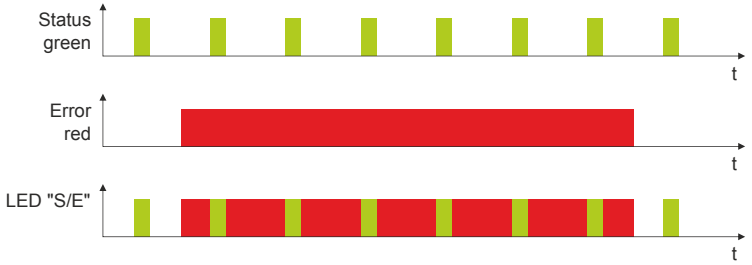
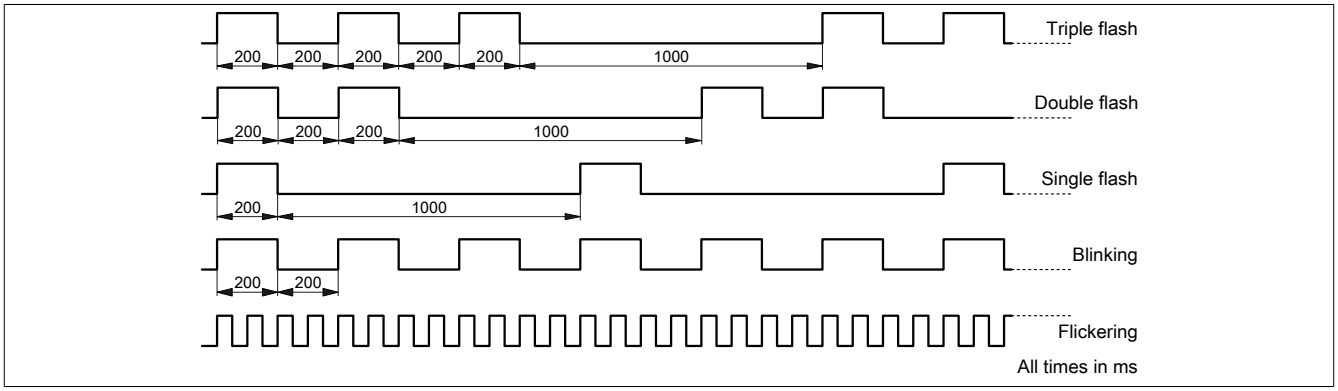
Color red - Error	Description
On	The controlled node (CN) is in an error state (failed Ethernet frames, increased number of collisions on the network, etc.). If an error occurs in the following states, the red LED is superimposed by the green flashing LED: • PRE_OPERATIONAL_1 • PRE_OPERATIONAL_2 • READY_TO_OPERATE  Note: • Several red blinking signals are displayed immediately after the device is switched on. This is not an error, however. • The LED lights up red for CNs with set physical node number 0 that have not yet been assigned a node number via dynamic node allocation (DNA).

Table 3: Status/Error LED lit red: LED indicating error state

Color green - Status	Description
Off	No power supply or mode NOT_ACTIVE. The controlled node (CN) is either not supplied with power or it is in state NOT_ACTIVE. The CN waits in this state for about 5 s after a restart. Communication is not possible with the CN. If no POWERLINK communication is detected during these 5 s, the CN changes to state BASIC_ETHERNET (flickering). If POWERLINK communication is detected before this time expires, however, the CN immediately changes to state PRE_OPERATIONAL_1.
Green flickering (approx. 10 Hz)	Mode BASIC_ETHERNET. The CN has not detected any POWERLINK communication. In this state, it is possible to communicate directly with the CN (e.g. with UDP, IP). If POWERLINK communication is detected in this state, the CN changes to state PRE_OPERATIONAL_1.
Single flash (approx. 1 Hz)	Mode PRE_OPERATIONAL_1. When operating on a POWERLINK V1 manager, the CN immediately changes to state PRE_OPERATIONAL_2. When operating on a POWERLINK V2 manager, the CN waits until an SoC frame is received and then changes to state PRE_OPERATIONAL_2.
Double flash (approx. 1 Hz)	Mode PRE_OPERATIONAL_2. The CN is normally configured by the manager in this state. It is then switched to state READY_TO_OPERATE by command (POWERLINK V2) or by setting flag "Data valid" in the output data (POWERLINK V1).
Triple flash (approx. 1 Hz)	Mode READY_TO_OPERATE. In a POWERLINK V1 network, the CN switches to state OPERATIONAL automatically as soon as input data is present. In a POWERLINK V2 network, the manager switches to state OPERATIONAL by command.
On	Mode OPERATIONAL. PDO mapping is active and cyclic data is evaluated.
Blinking (approx. 2.5 Hz)	Mode STOPPED. Output data is not being output, and no input data is being provided. It is only possible to switch to or leave this state after the manager has given the appropriate command.

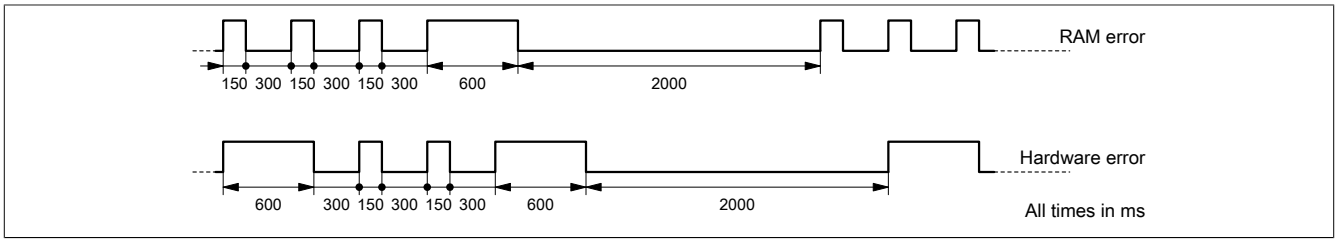
Table 4: Status/Error LED lit green: LED indicating operating state



2.2.2 System stop error codes

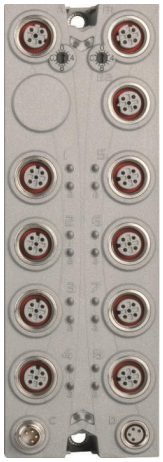
A system stop error can occur due to incorrect configuration or defective hardware.

The error code is indicated by LED "S/E" blinking red. The blinking signal of the error code consists of 4 switch-on phases with short (150 ms) or long (600 ms) duration. The error code is repeated every 2 seconds.



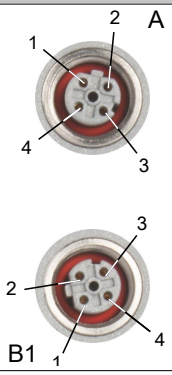
Error	Error description
RAM error	The device is defective and must be replaced.
Hardware error	The device or a system component is defective and must be replaced.

2.3 Operating and connection elements



2.3.1 Fieldbus interfaces

The module is connected to the network using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout		
	Pin	Name	
	1	TXD	Transmit data
	2	RXD	Receive data
	3	TXD\	Transmit data\
	4	RXD\	Receive data\
	Shield connection made via threaded insert in the module A → D-coded (female), input B1 → D-coded (female), output		

Information:

The color of the wires used in field-assembled cables for connecting to the fieldbus interface may deviate from the standard.

It is very important to ensure that the pinout is correct (see section "Accessories - POWERLINK cables" in the X67 user's manual).

2.3.1.1 Wiring guidelines for bus controllers with Ethernet cable

Some X67 system bus controllers are based on Ethernet technology. POWERLINK cables offered by B&R can be used for wiring.

Order number	Connection type
X67CA0E41.xxxx	Attachment cables - RJ45 to M12
X67CA0E61.xxxx	Connection cables - M12 to M12

The following cabling guidelines must be observed:

- Use Cat 5 SFTP cables.
- Observe the bend radius of the cable (see the data sheet of the cable)

Information:

Using POWERLINK cables offered by B&R (X67CA0E61.xxxx and X67CA0E41.xxxx) meets product standard EN 61131-2.

The customer must implement additional measures in the event of further requirements.

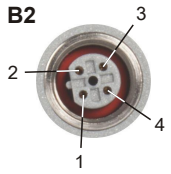
2.3.2 POWERLINK node number

The node number for the POWERLINK node is set using the two number switches.

Switch position	Description
0x00	Only permitted when operating the POWERLINK node in DNA mode.
0x01 - 0xEF	Node number of the POWERLINK node. Operation as a controlled node (CN).
0xF0 - 0xFF	Reserved, switch position not permitted.

2.3.3 X2X Link

Additional modules are connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout	
	Pin	Name
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	Shield connection made via threaded insert in the module	
	B2 → B-coded (female), output	

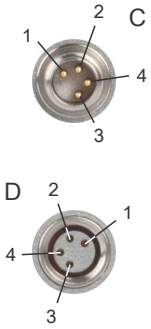
2.3.4 I/O power supply 24 VDC

The I/O power supply is connected via M8 connectors C and D. The power supply is fed via connector C (male). Connector D (female) is used to route the power supply to other modules.

The fieldbus / X2X Link power supply and I/O power supply are supplied separately via pins 1 and 2.

Information:

The maximum permissible current for the I/O power supply is 8 A (4 A per pin)!

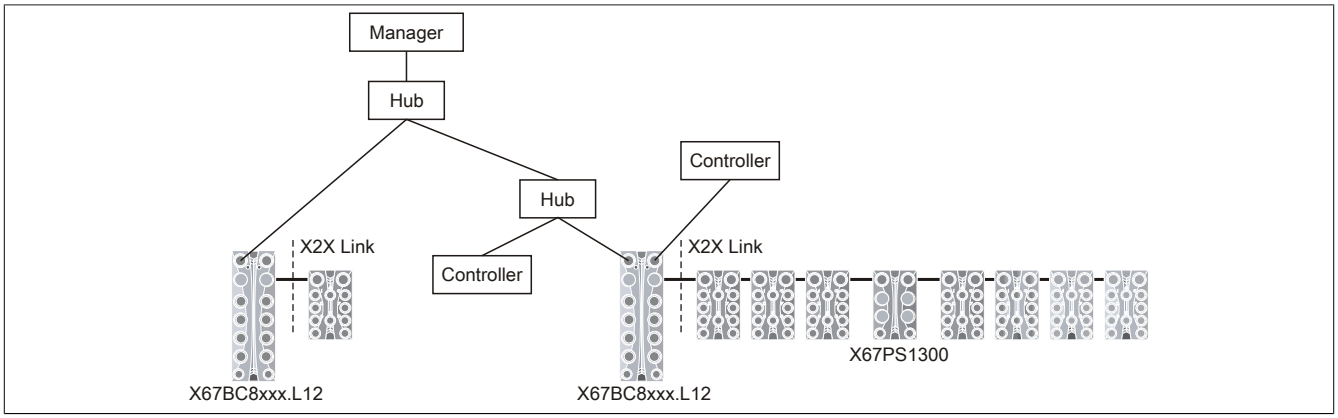
Connection	Pinout		
	Pin	Connector C (male)	Connector D (female)
	1	24 VDC fieldbus / X2X Link	24 VDC I/O
	2	24 VDC I/O	24 VDC I/O
	3	GND	GND
	4	GND	GND
	C → Connector (male) in module, supply for I/O power supply D → Connector (female) in module, routing of I/O power supply		

Information:

If the summation current of the outputs is >4 A, current must also be supplied via connector D, pin 2.

2.4 System configuration

A digital mixed module is already integrated in the bus controller. Maximum 250 I/O modules can be connected to the bus controller.



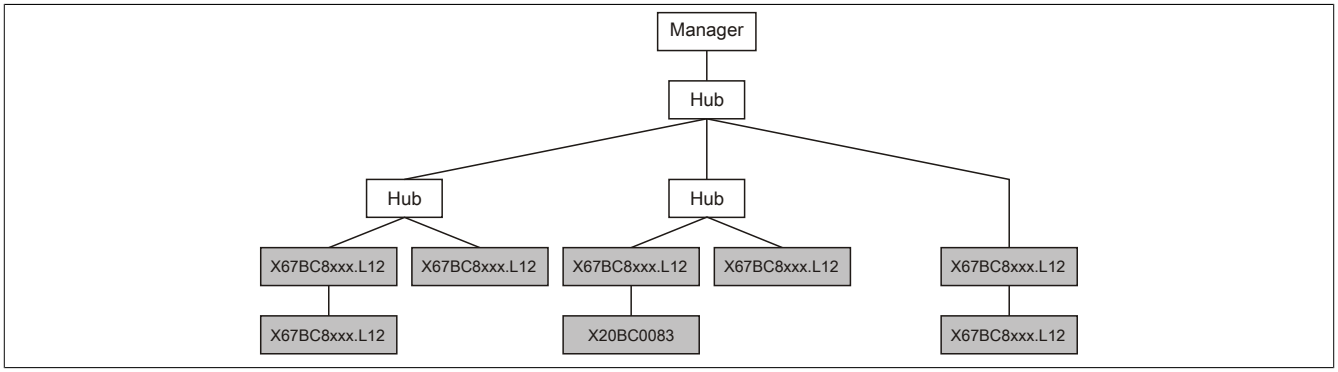
Information:

15 W are made available from the bus controller for additional X67 modules or other modules based on X2X Link.

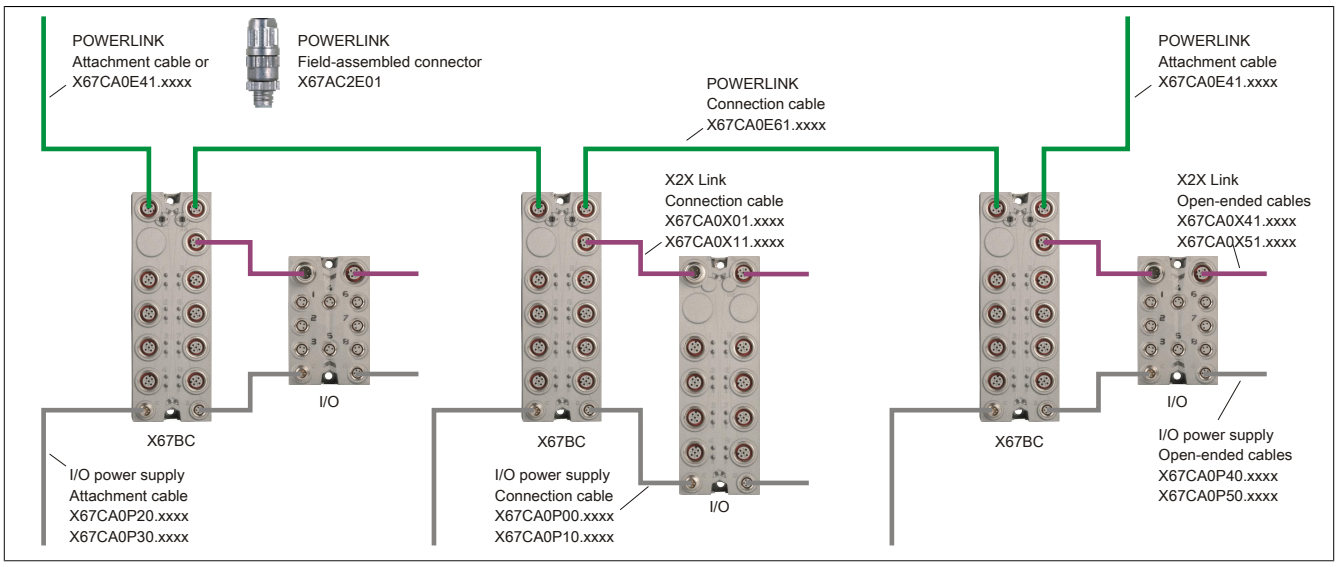
System supply module X67PS1300 is needed for additional power. This system supply module provides 15 W for additional modules. Each should be installed in the middle of the modules to be supplied with power.

2.4.1 Integrating into a POWERLINK network

The bus controller is used in a tree or line structure as follows:



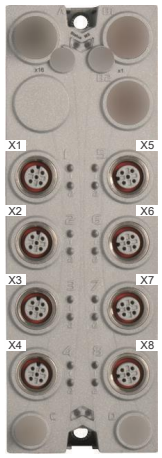
2.5 Required cables and connectors



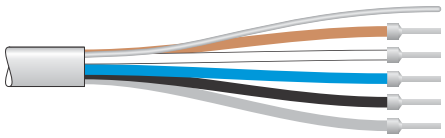
3 Integrated digital mixed module

1 additional mixed module can be saved by the digital mixed module integrated in the bus controller.

3.1 Pinout



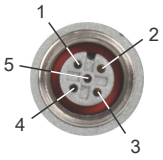
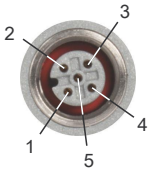
X1 to X8
M12 ①



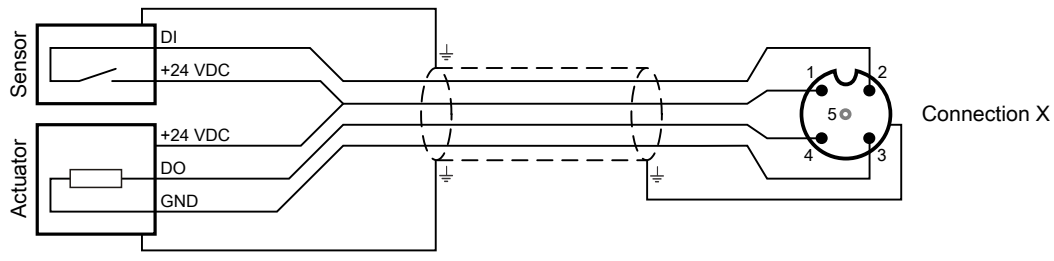
Shield	
1	+24 VDC
2	DI/DO x-1
3	GND
4	DI/DO x-2
5	NC

① X67CA0A41.xxxx: M12 sensor cable, straight
X67CA0A51.xxxx: M12 sensor cable, angled

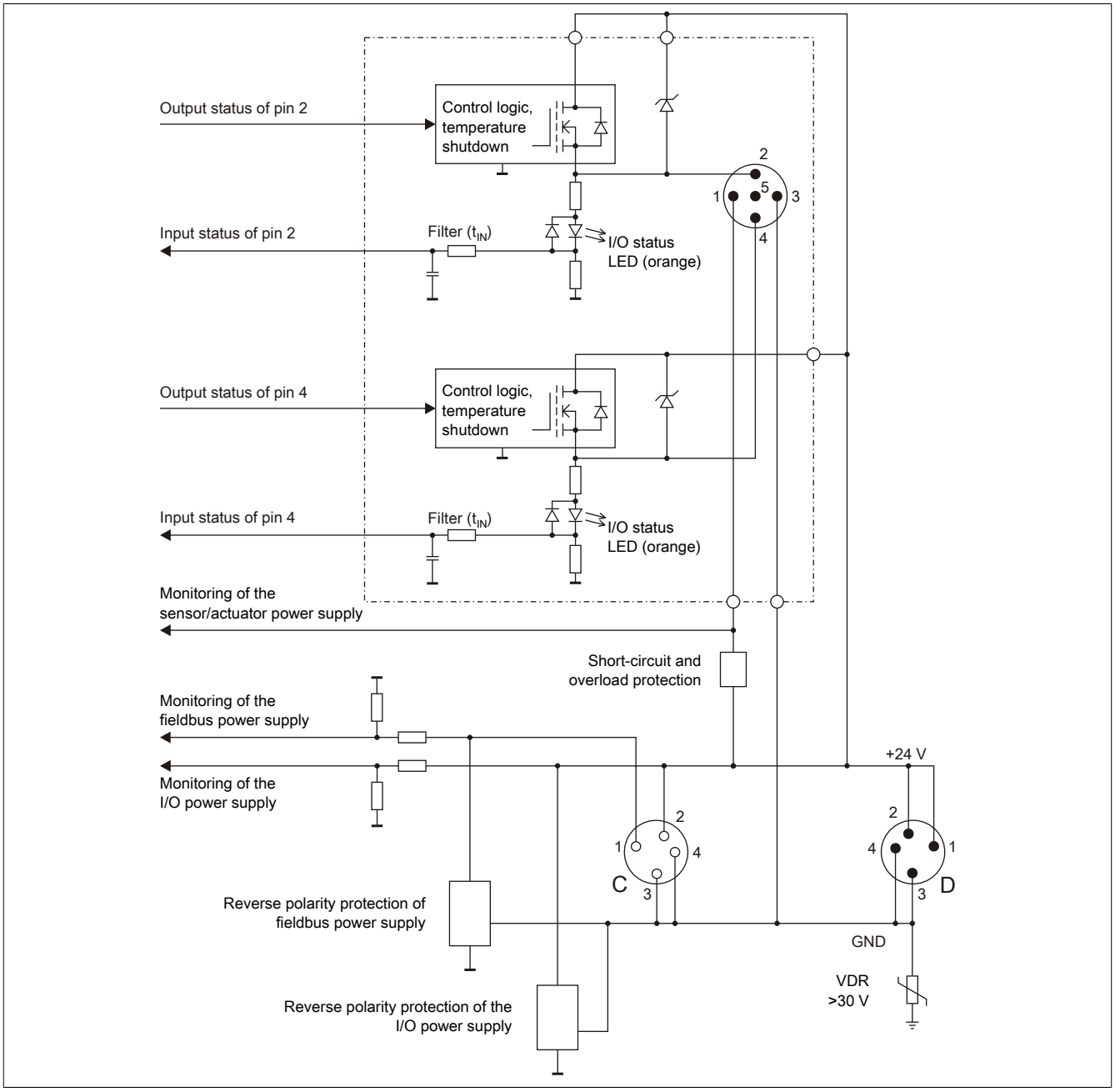
3.2 Connections X1 to X8

M12, 5-pin	Pinout	
Connection 1 to 4	**Pin**	**Name**
	1	24 VDC sensor/actuator power supply[1)]
	2	Input/Output x-1
	3	GND
	4	Input/Output x-2
	5	NC
	Shield connection made via threaded insert in the module. 1) The sensor/actuator power supply is not permitted to be external. X1 to X8 → A-coded (female), input/output	
Connection 5 to 8		

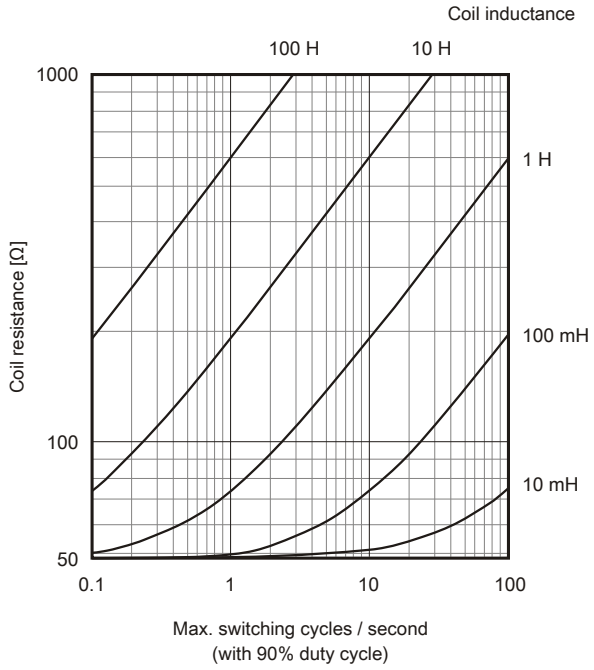
3.3 Connection examples



3.4 Input/Output circuit diagram



3.5 Switching inductive loads



4 Function description

4.1 POWERLINK

POWERLINK is an Ethernet-based, real-time capable fieldbus. POWERLINK extends the IEEE 802.3 Ethernet standard by a deterministic access method and also defines a CANopen-compatible fieldbus interface. POWERLINK distinguishes between process and service data in the same way as CANopen. Process data (PDO) is exchanged cyclically in the cyclic phase, while service data (SDO) is transferred acyclically. Service data objects are transmitted in the acyclic phases of POWERLINK using a connection-oriented protocol. The cyclic transfer of data in PDOs is enabled by "mapping".

For additional information, see POWERLINK bus controller user's manual and www.br-automation.com/en/technologies/powerlink.

4.2 Digital inputs

The module is equipped with 16 digital channels that can be configured as digital inputs.

Information:

The registers are described in "I/O masks 1 to 8" on page 19 and "I/O masks 9 to 16" on page 19.

4.2.1 Recording the input state

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

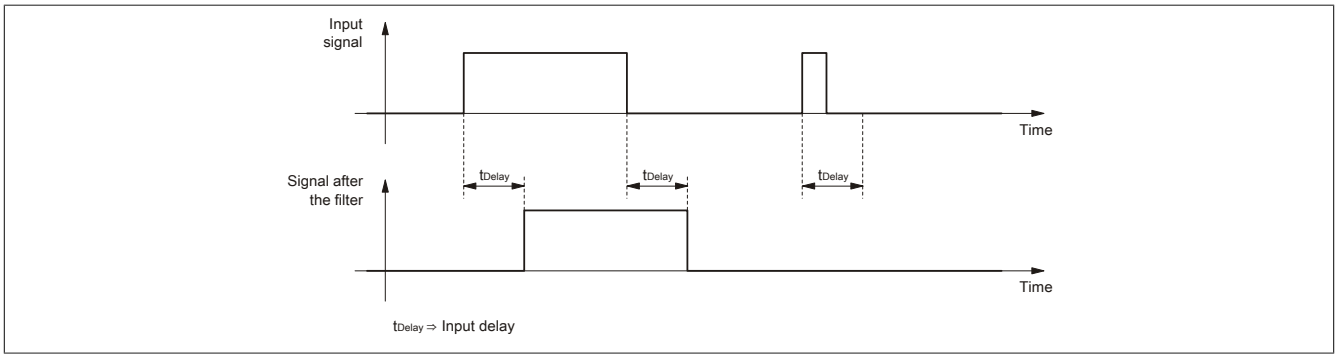
The filtered state is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

Information:

The registers are described in "Input state of digital inputs 1 to 8" on page 20 and "Input state of digital inputs 9 to 16" on page 20.

4.2.2 Input filter

An input filter is available for each input. Disturbance pulses that are shorter than the input delay are suppressed by the input filter.



The input delay can be set in steps of 100 µs. It makes sense, however, to enter values in steps of 2 since the input signals are sampled in an interval of 200 µs.

Values	Filter
0	No software filter
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value.

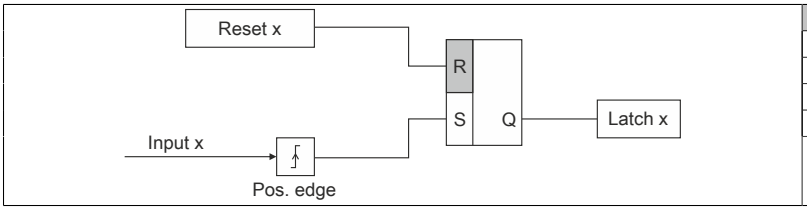
Information:

The register is described in "Digital input filter" on page 19.

4.2.3 Input latch

The positive edges of the input signals can be latched with a resolution of 200 µs.

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	State
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

Information:

The register is described in "Input latch" on page 23.

4.3 Event counter / Gate measurement

The module has 2 counter channels that can be used either as event counters or for gate measurement.

Event counter operation

The falling edges are registered on the counter input.

The counter value is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF).

The recovery time between measurements must be greater than 100 µs.

The measurement result is transferred with the falling edge to the result memory.

Information:

Only one of the counter channels at a time can be used for gate measurement.

Information:

Registers are described in "Configuring counter channels 1 and 2" on page 20 and "Event counter / Gate measurement" on page 24.

4.4 Digital outputs

The module is equipped with 16 digital channels that can be configured as digital outputs.

Information:

The registers are described in "I/O masks 1 to 8" on page 19 and "I/O masks 9 to 16" on page 19.

4.4.1 Monitoring status of the outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read out. A change in the monitoring status is actively transmitted as an error message.

Supervision status	Description
0	Digital output channel: No error
1	Digital output channel: Short circuit or overload

Information:

The register is described in "Monitoring status of the digital outputs" on page 22.

4.5 Monitoring the operating limits

The status of the I/O power supply can be read out.

Bit	Description
0	I/O power supply within the warning limits (18 to 30 V)
1	I/O power supply outside the warning limits (<18 V or >30 V)

Information:

The register is described in "Operating limit status registers" on page 24.

5 Commissioning

5.1 SGx target systems

SG3

This module is not supported on SG3 target systems.

SG4

The module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. With different versions, the Automation Runtime firmware is loaded onto the module.

Current firmware is made available automatically by updating Automation Runtime.

6 Register description

6.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X67 system user's manual.

6.2 Function model 2 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				
0	Input state of digital inputs 1 to 8	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
1	Input state of digital inputs 9 to 16	USINT	•			
	DigitalInput09	Bit 0				
	...	...				
	DigitalInput16	Bit 7				
2	Switching state of digital outputs 1 to 16	UINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput16	Bit 15				
2	Switching state of digital outputs 1 to 8	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput08	Bit 7				
3	Switching state of digital outputs 9 to 16	USINT			•	
	DigitalOutput09	Bit 0				
	...	...				
	DigitalOutput16	Bit 7				
30	Status of digital outputs 1 to 16	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 15				
30	Status of digital outputs 1 to 8	USINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput08	Bit 7				
31	Status of digital outputs 9 to 16	USINT	•			
	StatusDigitalOutput09	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 7				
26	Input latch - Positive edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Positive edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latches 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latches 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

6.3 Function model 1 - Counter

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
17	ConfigIOMask02	USINT				•
20	ConfigOutput01 (counter channel 1)	USINT				•
22	ConfigOutput02 (counter channel 2)	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				
0	Input state of digital inputs 1 to 8	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
1	Input state of digital inputs 9 to 16	USINT	•			
	DigitalInput09	Bit 0				
	...	...				
	DigitalInput16	Bit 7				
2	Switching state of digital outputs 1 to 16	UINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput16	Bit 15				
2	Switching state of digital outputs 1 to 8	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput08	Bit 7				
3	Switching state of digital outputs 9 to 16	USINT			•	
	DigitalOutput09	Bit 0				
	...	...				
	DigitalOutput16	Bit 7				
30	Status of digital outputs 1 to 16	UINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 15				
30	Status of digital outputs 1 to 8	USINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput08	Bit 7				
31	Status of digital outputs 9 to 16	USINT	•			
	StatusDigitalOutput09	Bit 0				
	...	...				
	StatusDigitalOutput16	Bit 7				
26	Input latch - Positive edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
27	Input latch - Positive edges 9 to 16	USINT	•			
	InputLatch09	Bit 0				
	...	...				
	InputLatch16	Bit 7				
28	Acknowledgment - Input latches 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
29	Acknowledgment - Input latches 9 to 16	USINT			•	
	QuitInputLatch09	Bit 0				
	...	...				
	QuitInputLatch16	Bit 7				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Reset counter 1	USINT			•	
	ResetCounter01	Bit 5				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
22	Reset counter 2	USINT			•	
	ResetCounter02	Bit 5				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		
8210	asy_SupplyOutput	USINT		•		

6.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigIOMask01	USINT				•
17	-	ConfigIOMask02	USINT				•
20	-	ConfigOutput01 (counter channel 1)	USINT				•
22	-	ConfigOutput02 (counter channel 2)	USINT				•
18	-	ConfigOutput03 (input filter)	USINT				•
Communication							
0	0	Input state of digital inputs 1 to 16	UINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput16	Bit 15				
2	2	Switching state of digital outputs 1 to 16	UINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput16	Bit 15				
30	-	Status of digital outputs 1 to 16	UINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput16	Bit 15				
26	-	Input latch - Positive edges 1 to 8	USINT	•			
		InputLatch01	Bit 0				
		...	...				
		InputLatch08	Bit 7				
27	-	Input latch - Positive edges 9 to 16	USINT	•			
		InputLatch09	Bit 0				
		...	...				
		InputLatch16	Bit 7				
28	-	Acknowledgment - Input latches 1 to 8	USINT			•	
		QuitInputLatch01	Bit 0				
		...	...				
		QuitInputLatch08	Bit 7				
29	-	Acknowledgment - Input latches 9 to 16	USINT			•	
		QuitInputLatch09	Bit 0				
		...	...				
		QuitInputLatch16	Bit 7				
4	-	Counter01	UINT		•		
6	-	Counter02	UINT		•		
20	-	Reset counter 1	USINT			•	
		ResetCounter01	Bit 5				
22	-	Reset counter 2	USINT			•	
		ResetCounter02	Bit 5				
8192	-	asy_ModulID	UINT		•		
8196	-	asy_SupplyStatus	USINT		•		
8208	-	asy_SupplyInput	USINT		•		
8210	-	asy_SupplyOutput	USINT		•		

1) The offset specifies the position of the register within the CAN object.

6.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X67 user's manual (version 3.30 or later).

6.4.2 CAN I/O bus controller

The module occupies 2 digital logical slots on CAN I/O.

6.5 Configuration

6.5.1 I/O masks 1 to 8

Name:
ConfigIOMask01

Channels can be configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

> **Information:**
>
> **In counter operation, channels 1 to 4 can only be configured as inputs.**

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 8 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

6.5.2 I/O masks 9 to 16

Name:
ConfigIOMask02

Channels can be configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 9 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output
...		...	
7	Channel 16 configured as input/output	0	Configured as input (bus controller default setting)
		1	Configured as output

6.5.3 Digital input filter

Name:
ConfigOutput03

The filter value for all digital inputs can be configured in this register.

The filter value can be configured in steps of 100 µs. It makes sense, however, to enter values in steps of 2 since the input signals are sampled in an interval of 200 µs.

Data type	Values	Filter
USINT	0	No software filter (bus controller default setting)
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value.

6.5.4 Configuring counter channels 1 and 2

Name:
ConfigOutput01 to ConfigOutput02
ResetCounter01 to ResetCounter02

Counter channels 1 and 2 are configured in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Configuration of the counter frequency (only with gate measurement)	000	Counter frequency = 48 MHz (bus controller default setting)
		001	Counter frequency = 3 MHz
		010	Counter frequency = 187.5 kHz
		011 to 111	Reserved
3 - 4	Reserved	0	
5	ResetCounter0x	0	No effect on counter (bus controller default setting)
		1	Clears the counter
6 - 7	Configuration of the operating mode	0	Event counter operation (bus controller default setting)
		1	Gate measurement

6.6 Communication

6.6.1 Digital inputs

6.6.1.1 Input state of digital inputs 1 to 16

Name:
DigitalInput01 to DigitalInput16

This register contains the input state of digital inputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
15	DigitalInput16	0 or 1	Input state - Digital input 16

6.6.1.2 Input state of digital inputs 1 to 8

Name:
DigitalInput01 to DigitalInput08

This register contains the input state of digital inputs 1 to 8.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

6.6.1.3 Input state of digital inputs 9 to 16

Name:
DigitalInput09 to DigitalInput16

This register contains the input state of digital inputs 9 to 16.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput09	0 or 1	Input state - Digital input 9
...		...	
7	DigitalInput16	0 or 1	Input state - Digital input 16

6.6.2 Digital outputs

The output state is transferred to the output channels with a fixed offset in relation to the network cycle (SyncOut).

6.6.2.1 Switching state of digital outputs 1 to 16

Name:
DigitalOutput01 to DigitalOutput16

This register stores the switching state of digital outputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
15	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

6.6.2.2 Switching state of digital outputs 1 to 8

Name:
DigitalOutput01 to DigitalOutput08

This register stores the switching state of digital outputs 1 to 8.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

6.6.2.3 Switching state of digital outputs 9 to 16

Name:
DigitalOutput09 to DigitalOutput16

This register stores the switching state of digital outputs 9 to 16.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput09	0	Digital output 09 reset
		1	Digital output 09 set
...		...	
7	DigitalOutput16	0	Digital output 16 reset
		1	Digital output 16 set

6.6.3 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states.

6.6.3.1 Status of digital outputs 1 to 16

Name:
StatusDigitalOutput01 to StatusDigitalOutput16

This register contains the state of digital outputs 1 to 16.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
15	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

6.6.3.2 Status of digital outputs 1 to 8

Name:
StatusDigitalOutput01 to StatusDigitalOutput08

This register contains the state of digital outputs 1 to 8.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
7	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

6.6.3.3 Status of digital outputs 9 to 16

Name:
StatusDigitalOutput09 to StatusDigitalOutput16

This register contains the state of digital outputs 9 to 16.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput09	0	Channel 09: No error
		1	Channel 09: Short circuit or overload
...		...	
7	StatusDigitalOutput16	0	Channel 16: No error
		1	Channel 16: Short circuit or overload

6.6.4 Input latch

6.6.4.1 Input latch - Positive edges 1 to 8

Name:
InputLatch01 to InputLatch08

The positive edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register "QuitInputLatch0x" on page 23.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch01	0	Do not latch input 1
		1	Latch input 1
...		...	
7	InputLatch08	0	Do not latch input 8
		1	Latch input 8

6.6.4.2 Input latch - Positive edges 9 to 16

Name:
InputLatch09 to InputLatch16

The positive edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is reset again or latching is prevented with register "QuitInputLatch0x" on page 24.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch09	0	Do not latch input 9
		1	Latch input 9
...		...	
7	InputLatch16	0	Do not latch input 16
		1	Latch input 16

6.6.4.3 Acknowledgment - Input latches 1 to 8

Name:
QuitInputLatch01 to QuitInputLatch08

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch01	0	Do not reset input 1
		1	Reset input 1
...		...	
7	QuitInputLatch08	0	Do not reset input 8
		1	Reset input 8

6.6.4.4 Acknowledgment - Input latches 9 to 16

Name:
QuitInputLatch09 to QuitInputLatch16

This register is used to reset the input latch by channel.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch09	0	Do not reset input 9
		1	Reset input 9
...		...	
7	QuitInputLatch16	0	Do not reset input 16
		1	Reset input 16

6.6.5 Event counter / Gate measurement

Name:
Counter01 and Counter02

Depending on the mode, this register contains the counter value or gate time of channel 1 and channel 2.

Data type	Values
UINT	0 to 65535

6.6.6 Reading out the module ID

Name:
asy_ModulID

This register offers the possibility to read the module ID.

Data type	Values
UINT	Module ID

6.6.7 Operating limit status registers

Name:
asy_SupplyStatus

The status of the operating limits can be read out in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Input power supply within/outside the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside the warning limits (<18 V or >30 V)
1	Reserved	0	
2	Output power supply within/outside the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside the warning limits (<18 V or >30 V)
3 - 7	Reserved	0	

6.6.8 I/O supply voltage

Name:
asy_SupplyInput

This register contains the I/O supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

6.6.9 Output supply voltage

Name:
asy_SupplyOutput

This register contains the output supply voltage measured by the module.

Data type	Values	Information
USINT	0 to 255	Resolution 1 V

6.7 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time	
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs

6.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs