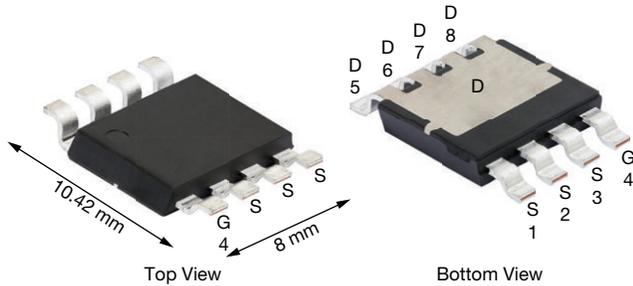
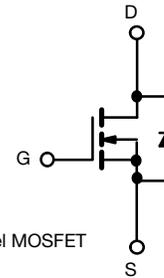


Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® 8 x 8LR

FEATURES

- TrenchFET® Gen IV power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Thin 1.6 mm height
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


N-Channel MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	60
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.00080
I _D (A) ^e	363
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8LR
Lead (Pb)-free and halogen-free	SQJQ160ER (for detailed order number please see www.vishay.com/doc?79776)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage	V _{DS}	60	V		
Gate-source voltage	V _{GS}	± 20			
Continuous drain current ^e	I _D	T _C = 25 °C	363	A	
		T _C = 125 °C	209		
Continuous source current (diode conduction)	I _S	194	mJ		
Pulsed drain current ^{a, e}	I _{DM}	802			
Single pulse avalanche current	I _{AS}	80			
Single pulse avalanche energy	E _{AS}	320	W		
Maximum power dissipation ^e	P _D	T _C = 25 °C			214
		T _C = 125 °C	71		
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C		
Soldering recommendations (peak temperature) ^c		260			

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction-to-ambient	R _{thJA}	44	°C/W	
Junction-to-case (drain) ^d	R _{thJC}	0.7		

Notes

- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257)
- As per JESD51-14
- Values based on R_{thJC} and T_C of 25 °C- Actual values achievable will be dependent on the thermal characteristics of the complete system



SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	2.8	3.5	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 60\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	500	
On-state drain current ^a	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	50	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}$	-	0.00056	0.00080	Ω
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0014	
		$V_{GS} = 10\text{ V}$	$I_D = 20\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0017	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}$		-	220	-	S
Dynamic ^b							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}, f = 1\text{ MHz}$	-	10 944	15 322	μF
Output capacitance	C_{oss}			-	4486	6281	
Reverse transfer capacitance	C_{rss}			-	266	373	
Total gate charge ^c	Q_g	$V_{GS} = 10\text{ V}$	$V_{DS} = 30\text{ V}, I_D = 50\text{ A}$	-	169	254	nC
Gate-source charge ^c	Q_{gs}			-	48	-	
Gate-drain charge ^c	Q_{gd}			-	34	-	
Gate resistance	R_g	f = 1 MHz		0.4	1.6	3.2	Ω
Turn-on delay time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.6\text{ }\Omega,$ $I_D \cong 50\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		-	20	30	ns
Rise time ^c	t_r			-	19	29	
Turn-off delay time ^c	$t_{d(off)}$			-	57	86	
Fall time ^c	t_f			-	18	27	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I_{SM}			-	-	802	A
Forward voltage	V_{SD}	$I_F = 40\text{ A}, V_{GS} = 0\text{ V}$		-	0.7	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 50\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		-	86	172	ns
Body diode reverse recovery charge	Q_{rr}			-	154	308	nC
Reverse recovery fall time	t_a			-	49	-	ns
Reverse recovery rise time	t_b			-	34	-	
Body diode peak reverse recovery current	$I_{RM(REC)}$					-	-3

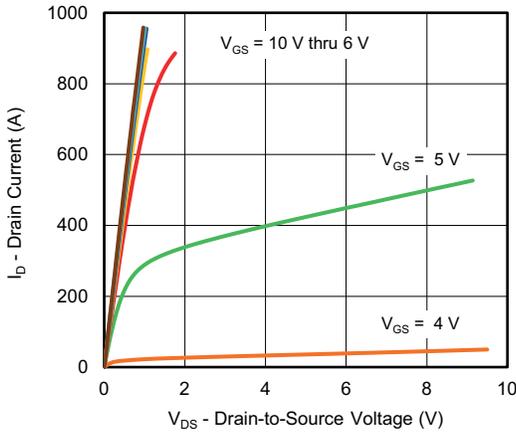
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

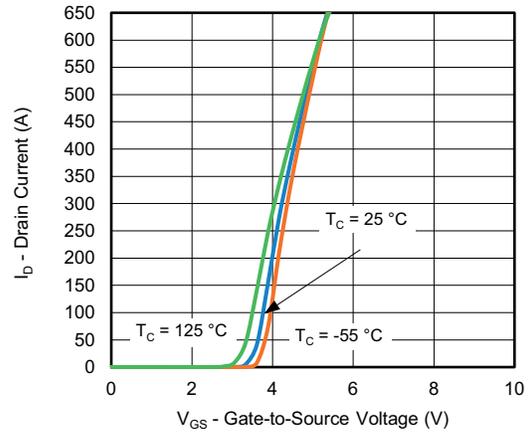
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



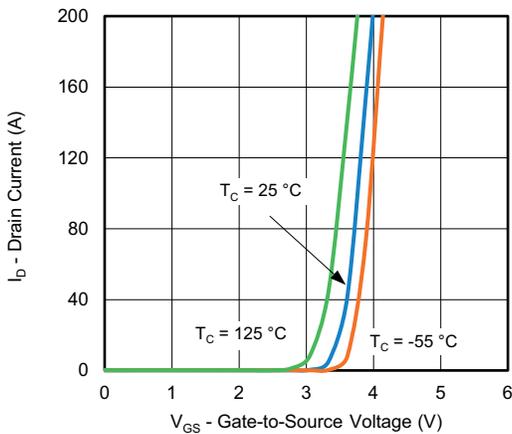
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



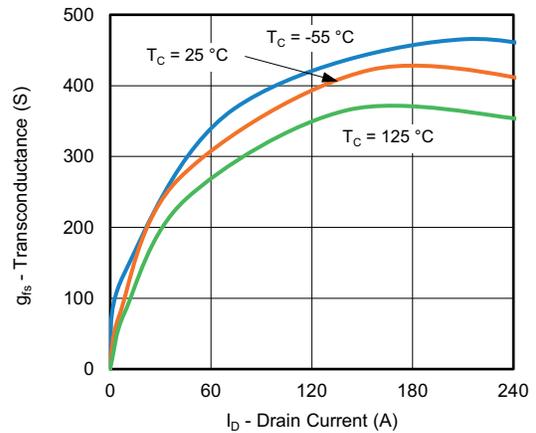
Output Characteristics



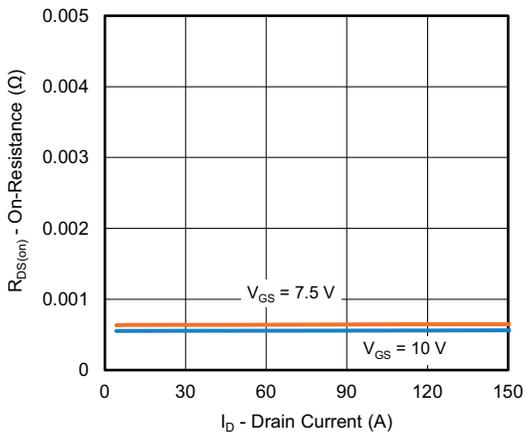
Transfer Characteristics



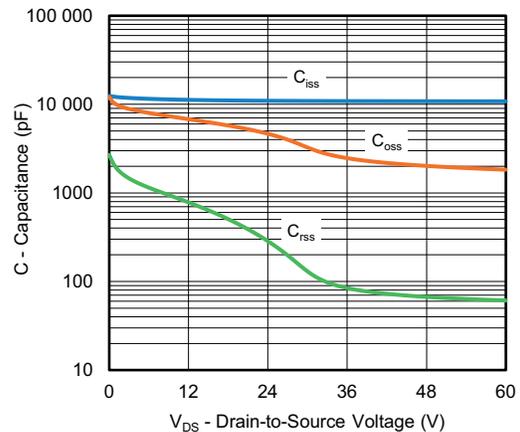
Transfer Characteristics



Transconductance



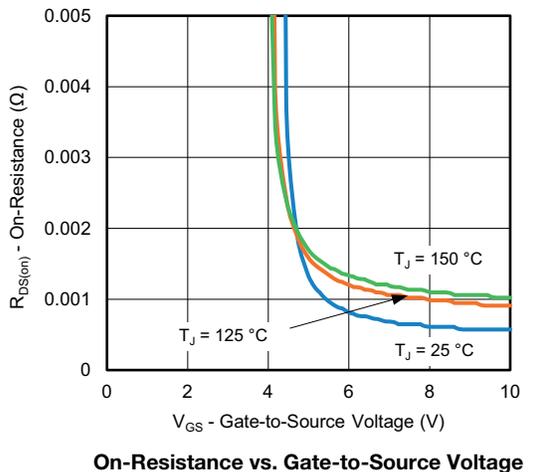
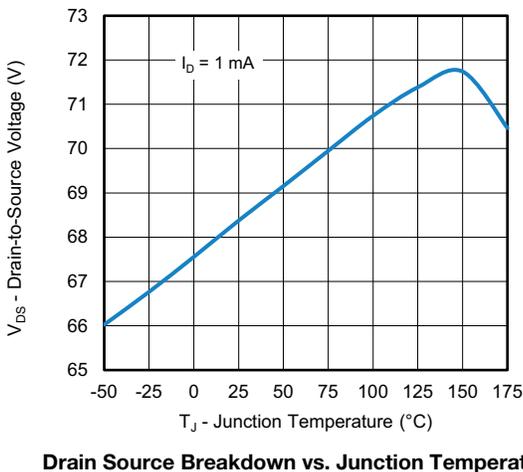
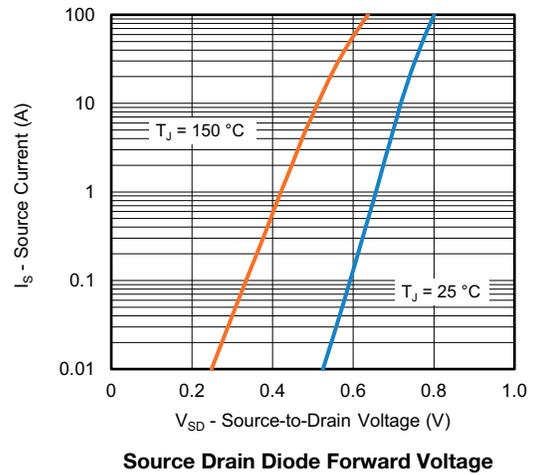
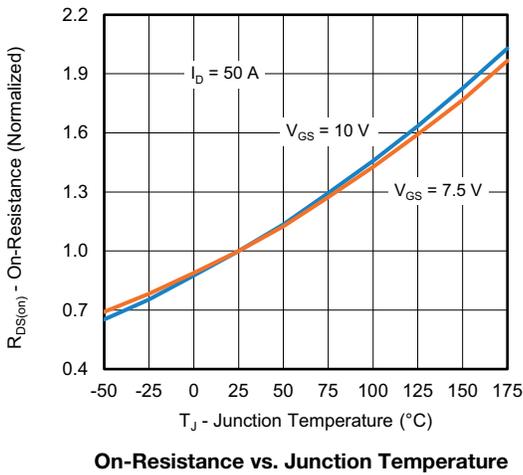
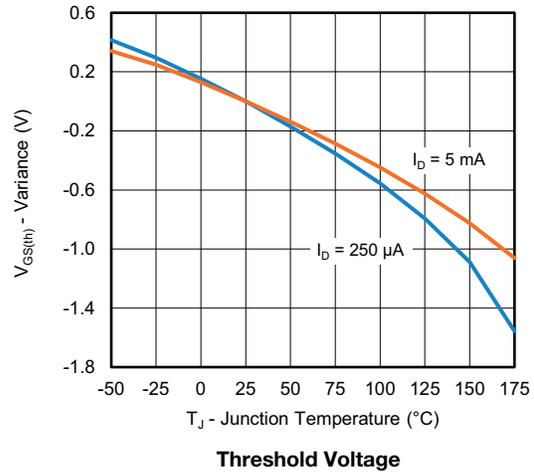
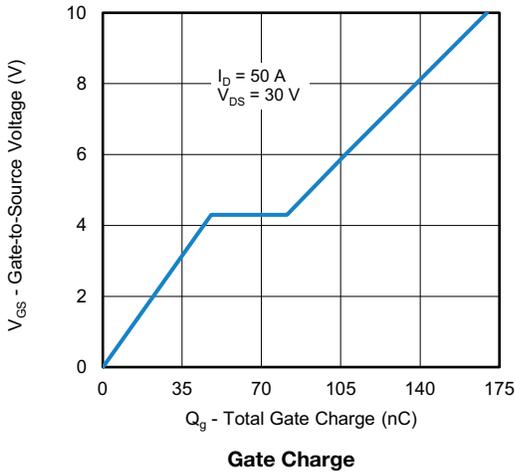
On-Resistance vs. Drain Current



Capacitance

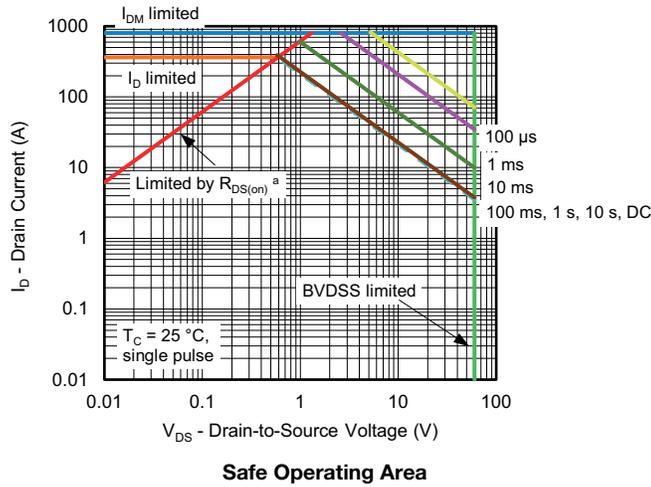


TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



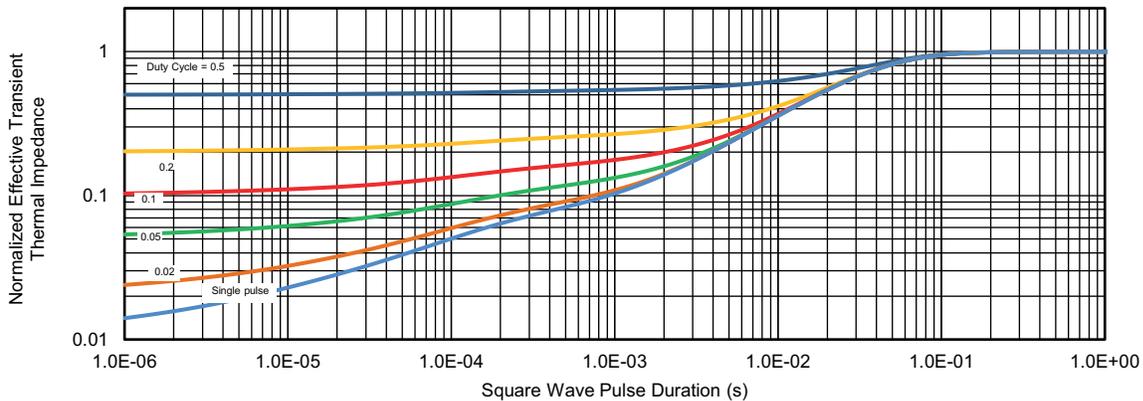


THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

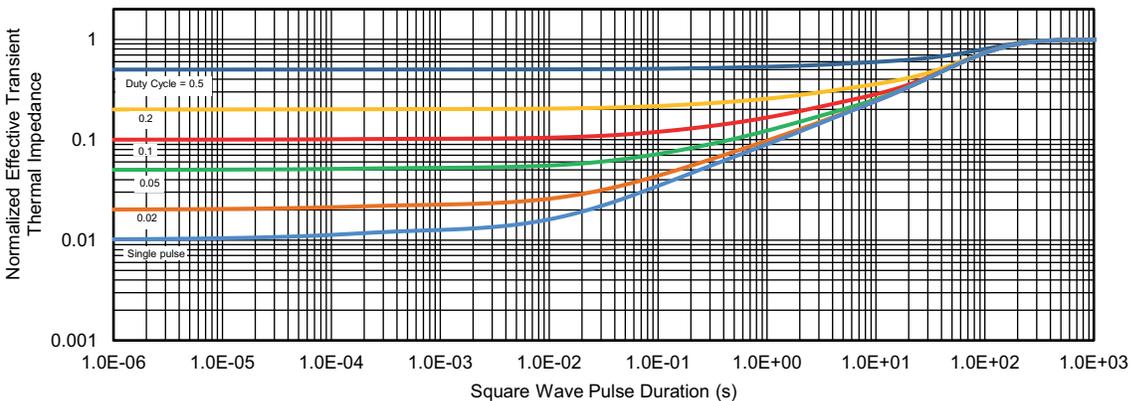


Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

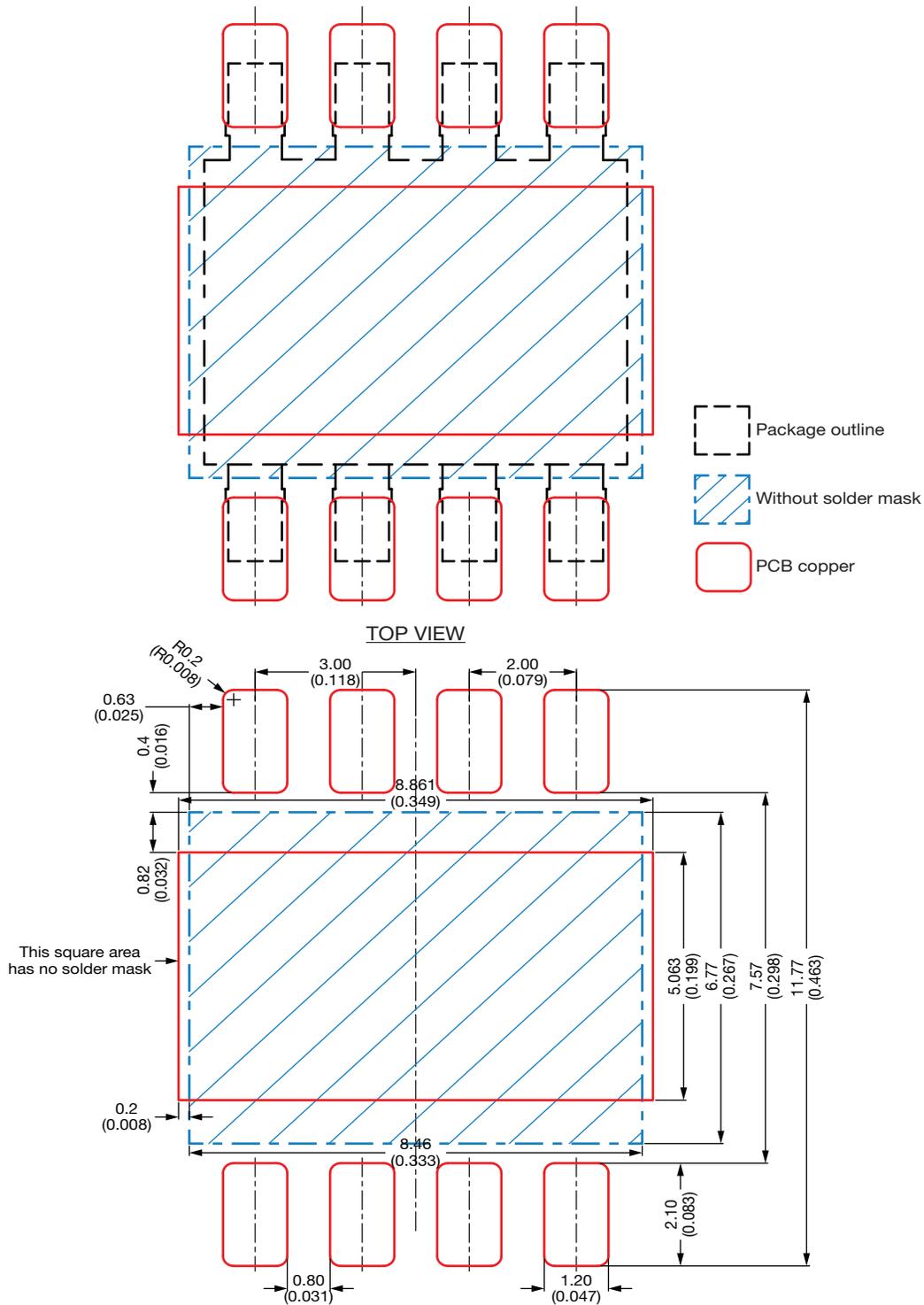


Normalized Thermal Transient Impedance, Junction-to-Ambient



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Recommended Land Pattern PowerPAK® 8 x 8LR



Notes

- This land pattern is for reference
- Proposed stencil thickness 200 µm
- All dimensions are in millimeter (inches)

ECN: C23-0461-Rev. B, 17-Apr-2023
 DWG: 3002



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