uPSD33xx

Turbo Series

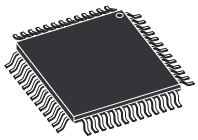
Fast 8032 MCU with Programmable Logic

DATA BRIEFING

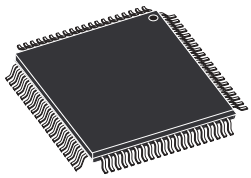
FEATURES SUMMARY

- FAST 8-BIT TURBO 8032 MCU, 40MHz
  - Advanced core, 4-clocks per instruction
  - 10 MIPs peak performance at 40MHz (5V)
  - JTAG Debug and In-System Programming
  - Branch Cache & 6 instruction Prefetch Queue
  - Dual XDATA pointers with auto incr & decr
  - Compatible with 3rd party 8051 tools
- DUAL FLASH MEMORIES WITH MEMORY MANAGEMENT
  - Place either memory into 8032 program address space or data address space
  - READ-while-WRITE operation for In-Application Programming and EEPROM emulation
  - Single voltage program and erase
  - 100K guaranteed erase cycles, 15-year retention
- CLOCK, RESET, AND SUPPLY MANAGEMENT
  - SRAM is Battery Backup capable
  - Flexible 8-level CPU clock divider register
  - Normal, Idle, and Power Down Modes
  - Power-on and Low Voltage reset supervisor
  - Programmable Watchdog Timer
- PROGRAMMABLE LOGIC, GENERAL PURPOSE
  - 16 macrocells
  - Create shifters, state machines, chip-selects, glue-logic to keypads, panels, LCDs, others
- COMMUNICATION INTERFACES
  - I^2C Master/Slave controller, 833KHz
  - SPI Master controller, 10MHz
  - Two UARTs with independent baud rate
  - IrDA protocol support up to 115K baud
  - Up to 46 I/O, 5V tolerant on 3.3V uPSD33xxV

Figure 1. Packages



TQFP52 (T)
52-lead, Thin,
Quad, Flat



TQFP80 (U)
80-lead, Thin,
Quad, Flat

- A/D CONVERTER
  - Eight Channels, 10-bit resolution, 6µs
- TIMERS AND INTERRUPTS
  - Three 8032 standard 16-bit timers
  - Programmable Counter Array (PCA), six 16-bit modules for PWM, CAPCOM, and timers
  - 8/10/16-bit PWM operation
  - 11 Interrupt sources with two external interrupt pins
- OPERATING VOLTAGE SOURCE (±10%)
  - 5V devices use both 5.0V and 3.3V sources
  - 3.3V devices use only 3.3V source

Table 1. Device Summary

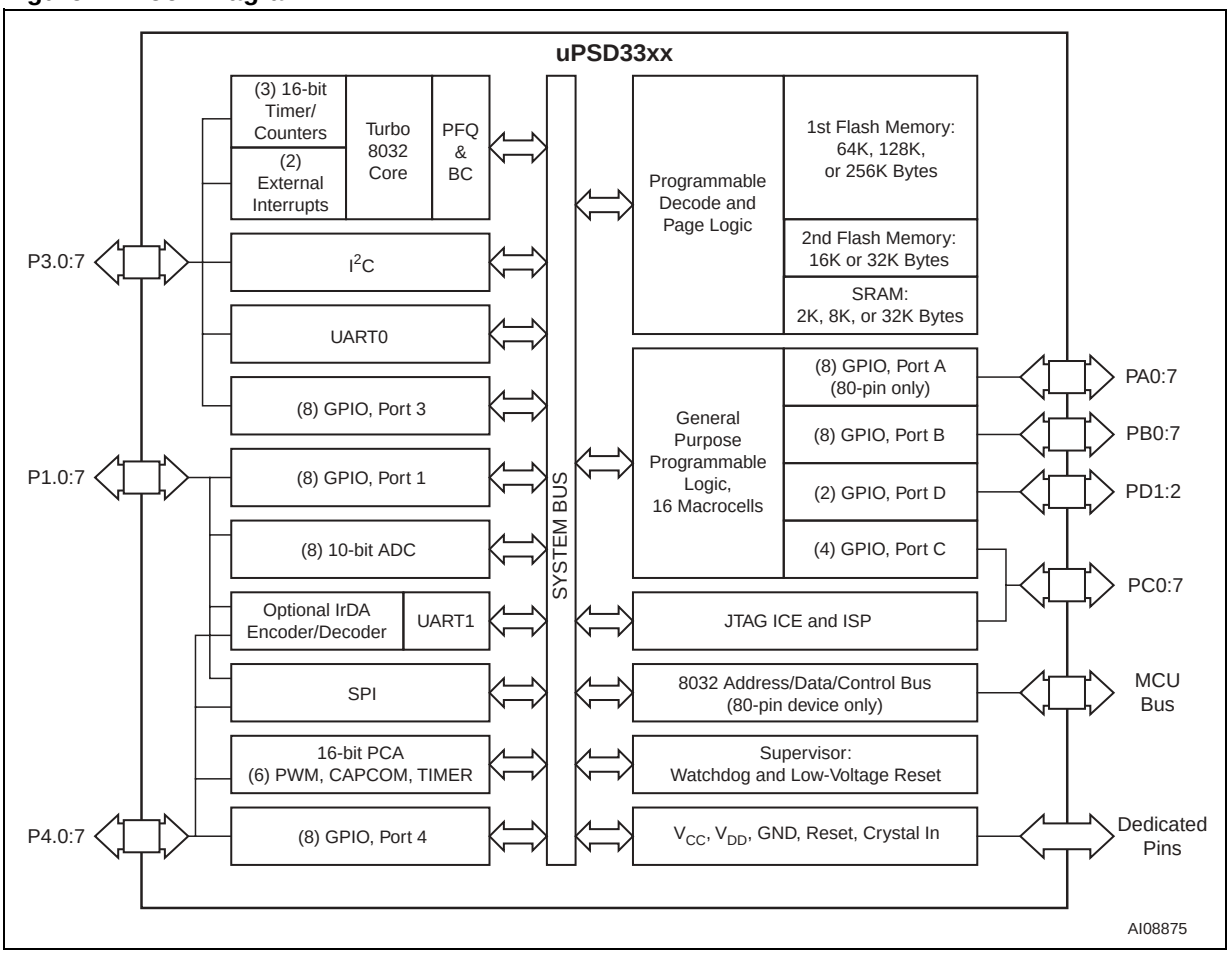
Part Number	1st Flash (bytes)	2nd Flash (bytes)	SRAM (bytes)	GPIO	8032 Bus	V_{CC}	V_{DD}	Pkg.	Temp.
uPSD3312D-40T6	64K	16K	2K	37	No	3.3V	5.0V	TQFP52	–40°C to 85°C
uPSD3312DV-40T6	64K	16K	2K	37	No	3.3V	3.3V	TQFP52	–40°C to 85°C
uPSD3333D-40T6	128K	32K	8K	37	No	3.3V	5.0V	TQFP52	–40°C to 85°C
uPSD3333DV-40T6	128K	32K	8K	37	No	3.3V	3.3V	TQFP52	–40°C to 85°C
uPSD3333D-40U6	128K	32K	8K	46	Yes	3.3V	5.0V	TQFP80	–40°C to 85°C
uPSD3333DV-40U6	128K	32K	8K	46	Yes	3.3V	3.3V	TQFP80	–40°C to 85°C
uPSD3334D-40U6	256K	32K	8K	46	Yes	3.3V	5.0V	TQFP80	–40°C to 85°C
uPSD3334DV-40U6	256K	32K	8K	46	Yes	3.3V	3.3V	TQFP80	–40°C to 85°C
uPSD3354D-40T6	256K	32K	32K	37	No	3.3V	5.0V	TQFP52	–40°C to 85°C
uPSD3354DV-40T6	256K	32K	32K	37	No	3.3V	3.3V	TQFP52	–40°C to 85°C
uPSD3354D-40U6	256K	32K	32K	46	Yes	3.3V	5.0V	TQFP80	–40°C to 85°C
uPSD3354DV-40U6	256K	32K	32K	46	Yes	3.3V	3.3V	TQFP80	–40°C to 85°C

SUMMARY DESCRIPTION

The Turbo uPSD33xx Series combines a powerful 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix to form an ideal embedded controller. At its core is a fast 4-cycle 8032 MCU with a 6-byte instruction prefetch queue (PFQ) and a 4-entry fully associative branching cache (BC) to maximize MCU performance, enabling loops of code in smaller localities to execute extremely fast.

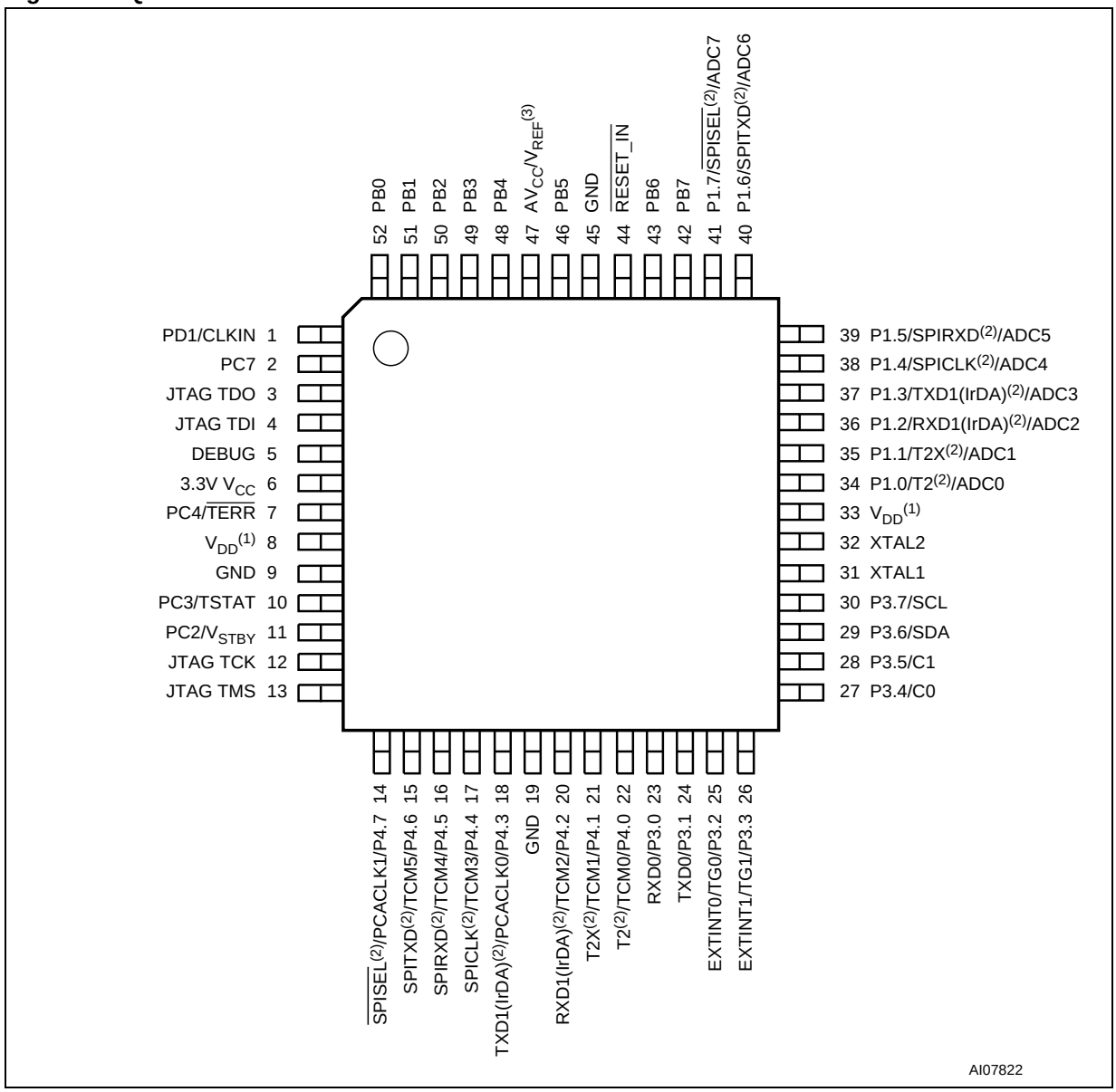
Code development is easily managed without a hardware In-Circuit Emulator by using the serial JTAG debug interface. JTAG is also used for In-System Programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development. The 8032 core is coupled to Programmable System Device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64K bytes using on-chip programmable decode logic. Dual Flash memory banks provide a robust solution for remote product updates in the field through In-Application Programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips. General purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSDsoft Express, available from the web at **www.st.com/psm**, at no charge. The uPSD33xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

Figure 2. Block Diagram



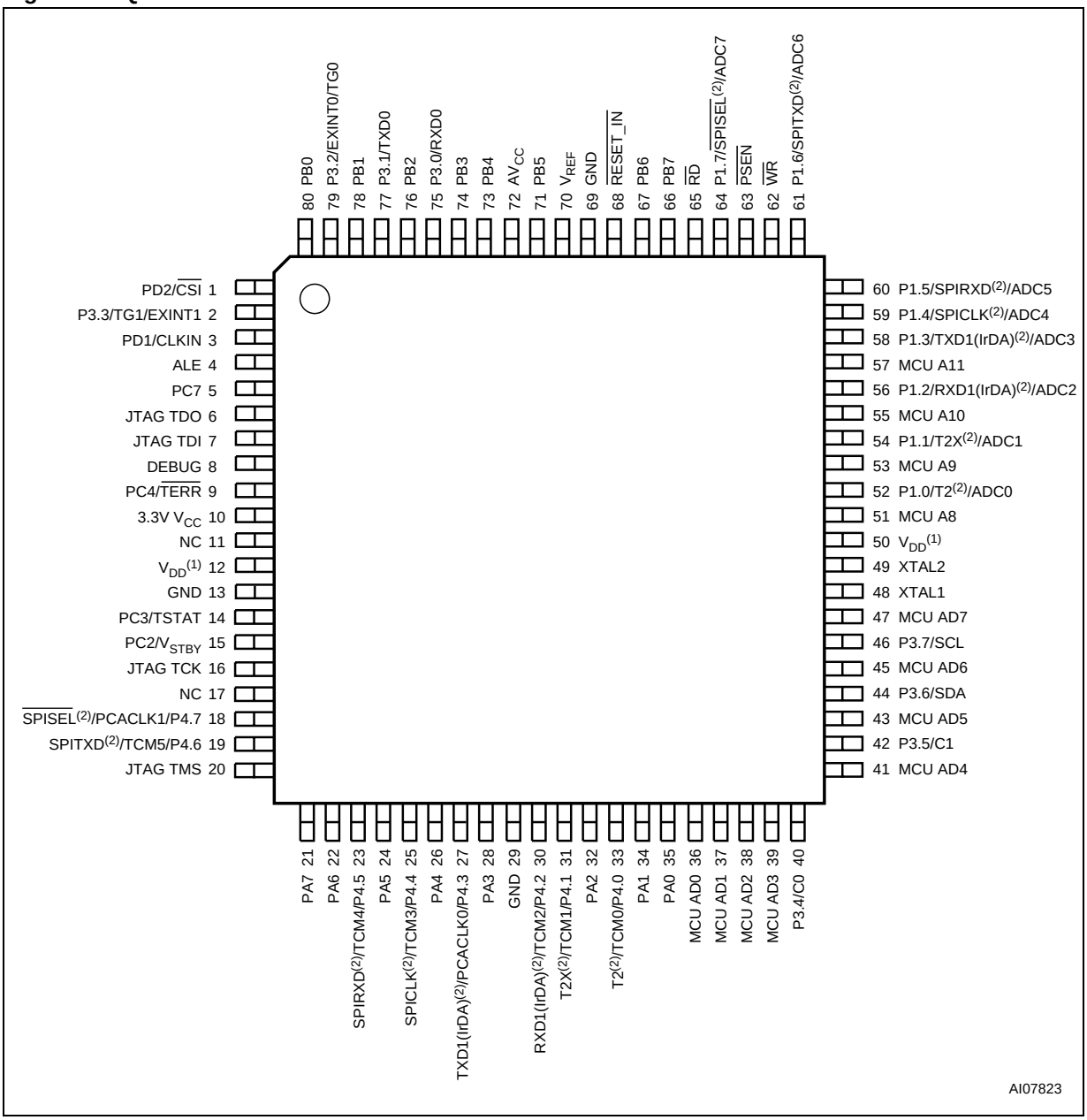
PIN DESCRIPTIONS

Figure 3. TQFP52 Connections



Note: 1. For 5V applications, V_{DD} must be connected to a 5.0V source. For 3.3V applications, V_{DD} must be connected to a 3.3V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.
3. V_{REF} and 3.3V AV_{CC} are shared in the 52-pin package only. ADC channels must use AV_{CC} as V_{REF} for the 52-pin package.

Figure 4. TQFP80 Connections



Note: NC = Not Connected

Note: 1. For 5V applications, V_{DD} must be connected to a 5.0V source. For 3.3V applications, V_{DD} must be connected to a 3.3V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.

Table 2. Major Parameters

Parameter	Test Conditions/Comments	5.0V Value	3.3V Value	Unit
Operating Voltage	–	4.5 to 5.5 (PSD); 3.0 to 3.6 (MCU)	3.0 to 3.6 (PSD and MCU)	V
Operating Temperature	–	–40 to 85	–40 to 85	°C
MCU Frequency	8MHz (min) for I^2C	1 Min, 40 Max	1 Min, 40 Max	MHz
Active Current, Typical (20% of PLD used; 25°C operation)	40MHz Crystal, Turbo	50	40	mA
	40MHz Crystal, Non-Turbo	48	38	mA
	8MHz Crystal, Turbo	21	18	mA
	8MHz Crystal, Non-Turbo	10	8	mA
Idle Current, Typical (20% of PLD used; 25°C operation)	40MHz Crystal divided by 2048 internally. All interfaces are disabled.	16	11	mA
Standby Current, Typical	Power-down Mode needs reset to exit.	140	120	µA
SRAM Backup Current, Typical	If external battery is attached.	0.5	0.5	µA
I/O Sink/Source Current, Ports A, B, C, and D	V_{OL} = 0.45V (max); V_{OH} = 2.4V (min)	I_{OL} = 8 (max); I_{OH} = –2 (min)	I_{OL} = 4 (max); I_{OH} = –1 (min)	mA
I/O Sink/Source Current, Port 4	V_{OL} = 0.6V (max); V_{OH} = 2.4V (min)	I_{OL} = 10 (max); I_{OH} = –10 (min)	I_{OL} = 10 (max); I_{OH} = –10 (min)	mA
PLD Macrocells	For registered or combinatorial logic	16	16	–
PLD Inputs	Inputs from pins, feedback, or MCU addresses	69	69	–
PLD Outputs	Output to pins or internal feedback	18	18	–
PLD Propagation Delay, Typical, Turbo Mode	PLD input to output	15	22	ns

PART NUMBERING

Table 3. Ordering Information Scheme

Example: uPSD 33 3 4 D V – 40 U 6 T

Device Type

uPSD = Microcontroller PSD

Family

33 = Turbo core

SRAM Size

1 = 2Kbyte

3 = 8Kbyte

5 = 32Kbyte

Main Flash Memory Size

2 = 64Kbyte

3 = 128Kbyte

4 = 256Kbyte

IP Mix

D = IP Mix: I^2C, SPI, UART (2), IrDA, ADC, Supervisor, PCA

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V

V = V_{CC} = 3.0 to 3.6V

Speed

–40 = 40MHz

Package

T = 52-pin TQFP

U = 80-pin TQFP

Temperature Range

6 = –40 to 85°C

Shipping Option

Tape & Reel Packing = T

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 4. Document Revision History

Date	Version	Revision Details
July 1, 2003	1.0	First Issue
14-Sep-04	2.0	Reformatted; updated with version 4.0 datasheet
21-Jan-05	3.0	Updated with version 6.0 datasheet