Data Sheet

Micro LCD Character Modules Data Sheet

RS stock number 329-0341, 329-0357, 329-0379 & 329-0385

A range of compact intelligent, alphanumeric, dot matrix modules with integral CMOS microprocessor and LCD display drivers. The modules utilise a 5 x 8 dot matrix font format with cursor, and are capable of displaying 189 different alphanumeric characters and symbols. The modules are available as reflective or transflective in super twisted nematic green mode. The transflective type incorporate an LED backlight.

Applications

- Data terminals
- Medical instruments
- Hand-held instruments
- Hand-held data terminals
- Electronic typewriters
- Point of sale terminals
- Test instruments
- Word processors

Features

- Low power consumption via a single 5V power supply
- Wide viewing angle
- High contrast
- Easy interface to 4 or 8-bit data bus
- ASCII compatible
- Powerful command set
- Chip-on-board technology (COB)
- 189 different characters and symbols
- Up to 8 user definable characters
- Compact and lightweight

Absolute maximum rating

Item	Symbol	Value	Unit
Power supply voltage	Vdd - Vss	-0.3 ~ +7.0	
Driver supply voltage	Vlcd	Vdd -13.5 ~ Vdd +0.3 V	V
Input voltage	Vin	-0.3 ~ Vdd +0.3	
Operating temperature range	Top	0 ~ +50	
Storage temperature range	Tst	-20 ~ +60	°C

Description of terminals

Pin No.	Symbol	Input/Output	Function
1	Vss	I	Ov power supply (Gnd)
2	Vdd	I	+5v power supply
3	Vo	I	LCD contrast adjustment voltage
4	RS	I	Register select RS=1 Data register for read and write RS=0 Instruction register for write Busy flag/Address count for read
5	R/W	I	Read/Write select R/W= 1 Read mode R/W= 0 Write mode
6	E	I	Enable signal initiate read or write of data
7	DBO	I/O	Four low order bidirectional three-state data bus lines. Used to transfer to the LCD module. Note, not used during 4-bit operation
8	DB1	I/O	
9	DB2	I/O	
10	DB3	I/O	
11	DB4	I/O	Four high order bidirectional three-state data bus lines. Used to transfer data to the LCD module. Note, DB7 can be used as a busy flag.
12	DB5	I/O	
13	DB6	I/O	
14	DB7	I/O	
15	A	I	LED backlight Anode. Transflective models only
16	K	I	LED backlight Cathnode. Transflective models only.

Electrical characteristics
(VDD-VSS = 4.5v ~ 5.5v, Ta = 25°C)

Parameter	Sym	Condition	Pin	Min	Typ	Max	Unit
Logic Voltage	V_{DD}	Vss = 0v	V_{DD}	4.5	5.0	5.5	V
Logic Current	I_{DD}	V_{DD} = 5v, f_{OSC} = 270khz	-	-	0.6	1.0	mA
Input voltage	V_{IH}	-	DB0 ~ DB7, RS, R/W, E	2.2	-	V_{DD}	V
	V_{IL}	-		-0.3	-	0.6	V
Output Voltage	V_{OH}	I_{OH} = -0.2 mA	DB0 ~ DB7	V_{DD} -1	-	V_{DD}	V
	V_{OL}	I_{OL} = 1.2 mA		-0.2	-	1.0	V
I/O leakage current	I_{LKG}	V_{IN} = 0 to V_{DD}	-	-1	-	-1	µA
Input Low Current	V_{IL}	V_{IN} = 0v, V_{DD} = 5v	-	-50	-125	-250	µA
Internal Clock	f_{OSC}	R_f = 91kΩ ±2%	-	190	270	350	khz
LCD drive voltage	V_{LCD}	V_{DD} - Vo	Vo	3.0	-	11.0	V

LED Backlight Characteristics

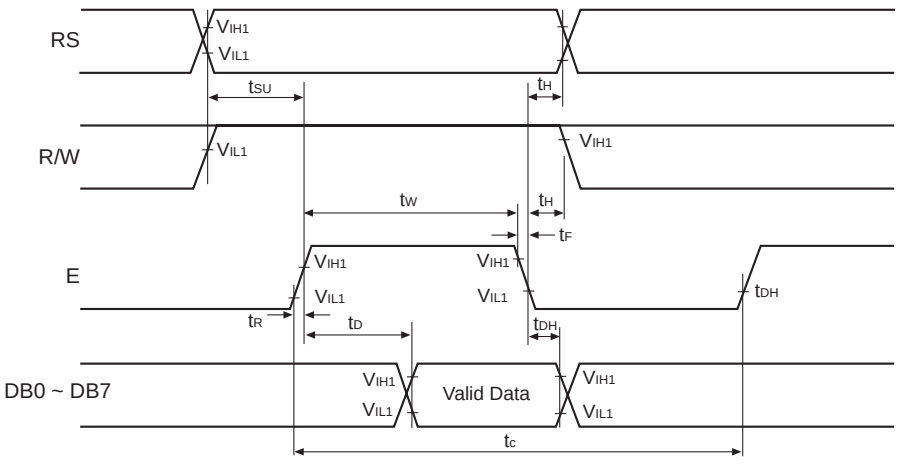
RS Part Number	Condition	Symbol	Typ	Max	Unit
329-0385, 329-0379	Ta = 25°C	I_f	30	40	mA

AC Characteristics
(VDD-VSS = 4.5v ~ 5.5v, Ta = 0 ~ +55°C)

Mode	Characteristic	Sym	Min	Typ	Max	Unit
Write mode (refer to fig -2)	E cycle time	t_c	500	-	-	nS
	E Rise / Fall time	$t_{R,}$ t_F	-	-	20	
	E Pulse width (High, Low)	t_W	230	-	-	
	R/W and RS setup time	t_{SU1}	40	-	-	
	R/W and RS hold time	t_{H1}	10	-	-	
	Data setup time	t_{SU2}	60	-	-	
	Data hold time	t_{H2}	10	-	-	
Read Mode (refer to fig -1)	E cycle time	t_C	500	-	-	nS
	E Rise / Fall time	$t_{R,}$ t_F	-	-	20	
	E Pulse width (High, Low)	t_W	230	-	-	
	R/W and RS setup time	t_{SU}	40	-	-	
	R/W and RS hold time	t_H	10	-	-	
	Data output delay time	t_D	-	-	120	
	Data hold time	t_{DH}	5	-	-	

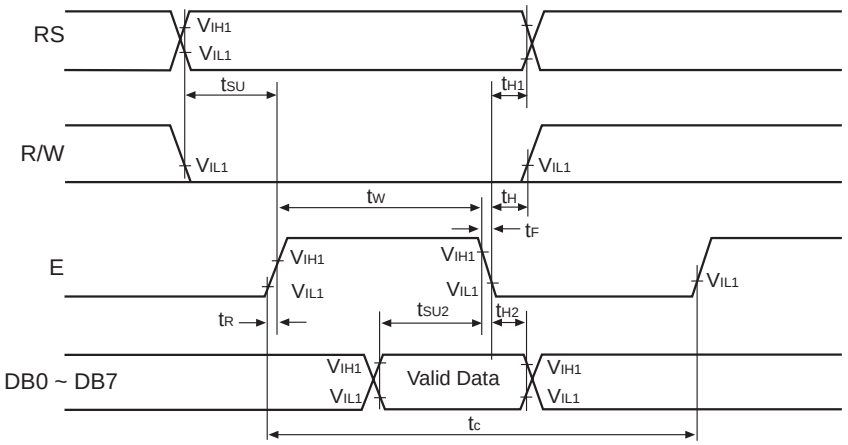
Read mode timing diagram

Figure 1



Write mode timing diagram

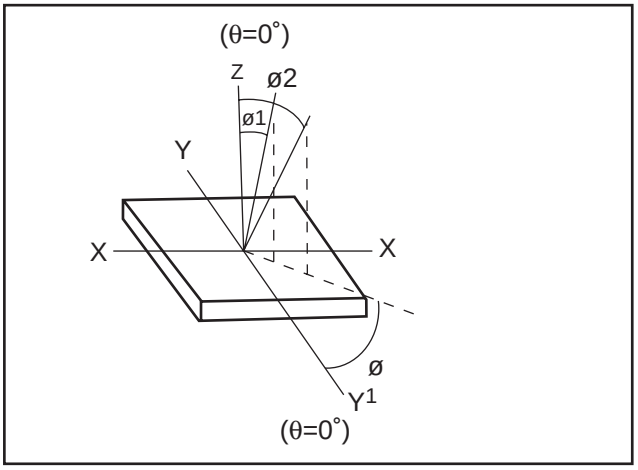
Figure 2



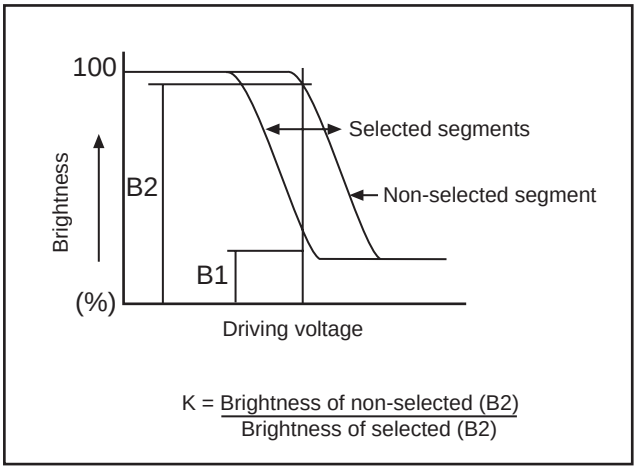
Optical characteristics

Item	Symbol	Condition	Min.	Typ	Max	Unit	Note
Viewing angle	Ø2 - Ø1	K = 1.4	60	-	-	deg.	*1. *2
Contrast ratio	K	Ø = 10°C θ = 0°C	5	-	-	-	*3
Response time (rise)	tr	Ø = 10°C θ = 0°C	-	150	250	ms	*4
Response time (fall)	tf	Ø = 10°C θ = 0°C	-	200	300	ms	*4

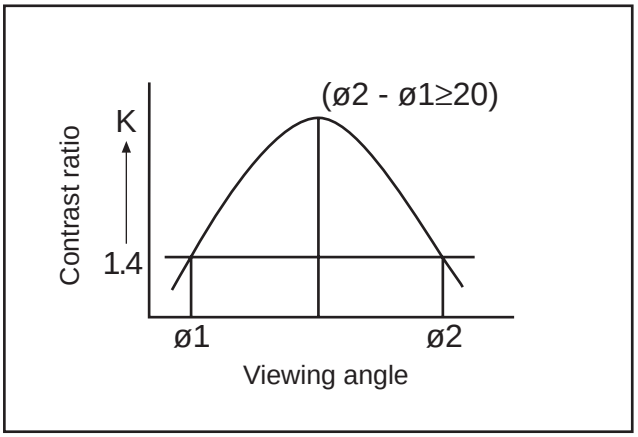
*1. Definition of 0 and θ



*3. Definition of contrast ratio



*2. Contrast vs viewing angle



*4. Definition of optical response

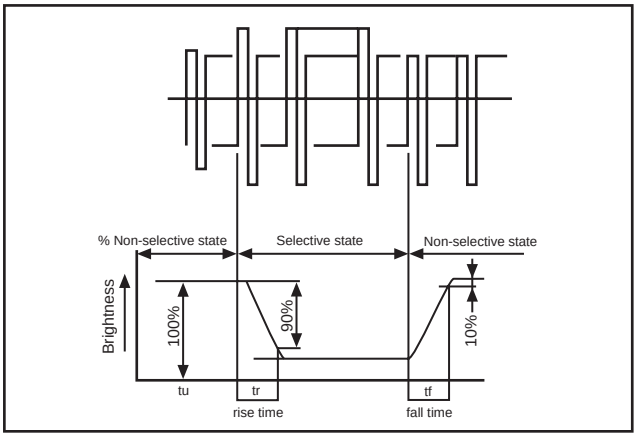


Table 5. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc = 270KHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRAM. and set DDRAM address to “00H” from AC.	1.52 ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to “00H” from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display enable.	37μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C) and blinking of cursor (B) on/off control bit.	37μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing DDRAM data.	37μs
Function Set	0	0	0	0	1	DL	N	F	X	X	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line), display font type (F : 5 x 8 dots/5 x 11 dots)	37μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	37μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	37μs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μs

“X” : don’t care

Instruction description

Outline

To overcome the speed difference between internal clock of KS0066 and MPU clock, KS0066 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (refer to table 5).

Instruction can be divided largely four kinds,

1. KS0066 function set instructions (set display methods, set data length, etc).
2. Address set instructions to internal RAM
3. Data transfer instructions with internal RAM
4. Others

The address of internal RAM is automatically increased or decreased by 1.

* Note: During internal operation, Busy Flag (DB7) is read High. Busy Flag check must precede the next instruction.

Contents

1. Clear display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = “ the 1”).

2. Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return Home is cursor return home instruction. Set DDRAM address to “00H” into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

3. Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of the cursor and display, where:

I/D = 0 (low) Cursor moves to the left and DDRAM is decreased by 1.

I/D = 1 (high) Cursor moves to the right and DDRAM is increased by 1.

SH = 0 (low) When a DDRAM or CGRAM operation is performed the display does not move.

SH = 1 (high) When a DDRAM write operation is performed the entire display is shifted where:

I/D = 0 (low) shift display right.

I/D = 1 (high) shift display left.

4. Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF. (1 bit registers) where:

D = 0 (low) Display turned off, data remains in the DDRAM.

D = 1 (high) Display turned on.

C = 0 (low) Cursor turned off, but its position is maintained in I/D register.

C = 1 (high) Cursor turned on.

B = 0 (low) Cursor blink turned off.

B = 1 (high) Cursor blink turned on.

5. Cursor or display shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Without writing or reading of display data, shift right/left cursor position or display. This instruction is used to correct or search display data (refer to table 4). During 2-line mode display, cursor moves to the 2nd line after 40th digit of 1st line.

Note: That display shift is performed simultaneously in all the line. When displayed data is shifted repeatedly, each line shifts individually. When display shift is performed, the contents of address counter are not changed.

Table 4. Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6. Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL = 0 (low) 4 bit bus mode interface MPU. All data transfers are sent as two 4 bit nibbles.

DL = 1 (high) 8 bit bus mode interface with MPU. All data transfers are sent as one 8 bit byte.

N = 0 (low) 1 line display mode.

N = 1 (high) 2 line display mode.

F = 0 (low) 5 * 8 dots font display mode.

F = 1 (high) 5 * 11 dots font display mode.

7. Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

The instruction makes CGRAM data available to the MPU.

8. Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

The instruction makes DDRAM data available to the MPU, where:

1 line display (N = 0)	DDRAM is from	“00H” to “4FH”
2 line display (N = 1)	DDRAM is from	“00H” to “27H” line 1
		“40H” to “67H” line 2

9. Read busy flag & address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

The instruction shows whether the KS0066 is busy with an internal operation. The instruction also allows the value of the address register to be read.

If BF = 0 Controller not busy

If BF = 1 Controller busy, MPU must wait until BF = 0

10. Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM

The section of RAM from DDRAM, CGRAM, is set by the previous address set instruction : DDRAM address set, CGRAM address set. RAM set instruction can also determine the AC direction to RAM.

After write operation, the address is automatically increased/decreased by 1, according to entry mode.

11. Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM

The section of RAM is set by the previous address set instruction. If address set instruction of RAM is not performed before this instruction, the data read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction : it also transfers RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

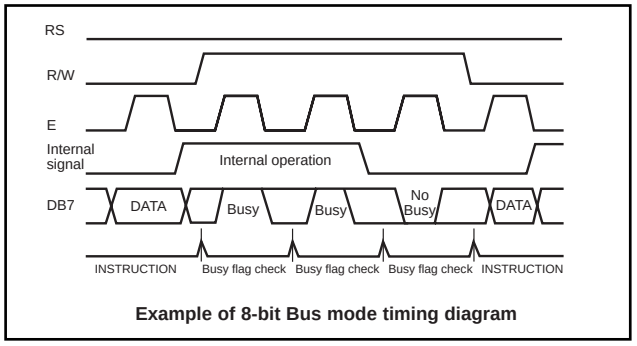
*In case of RAM write operation, after this AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

Interface with MPU

1. Interface with 8-bits MPU

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.

Example of timing sequence is shown below.

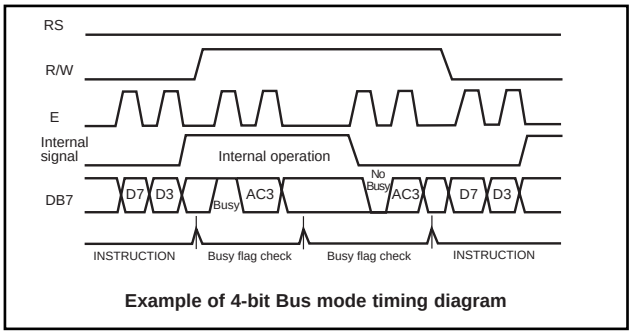


Example of 8-bit Bus mode timing diagram

2. Interface with 4-bits MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus modem the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs “High” after the second transfer are ended.

Example of timing sequence is shown below.



Example of 4-bit Bus mode timing diagram

Power Supply Reset

The internet reset circuit will only operate when the following power supply conditions are satisfied. If it does not operate properly, the unit should be initialised via instructions.

Item	Symbol	Measuring condition	Standard Value min	typ	max	Unit
Power supply rise time	trcc	***	0.1	-	10	mS
Power supply off time	toff	***	1	-	-	mS

Reset Function - initialisation via internal reset circuit

The KS066 automatically initialises (resets) when power is supplied. The following instructions are executed in the initialisation. The busy flag (BF) is kept busy until initialisation ends (BF = 1). The busy state is 10ms after V_{DD} reaches 4.5V with respect to V_{SS}.

1. Display clear
2. Function set:
   - DL = 1,8 bit data interface
   - N = 0,1 line display
   - F = 0,5 * 8 character font
3. Display on/off control:
   - D = 0 Display off
   - C = 0 Cursor off
   - B = 0 Blinking off
4. Entry mode set:
   - I/D = 1 increment by 1
   - S = 0 no shift

Reset Function - initialisation via instructions

The (BF) must not be checked in between sending the first three instructions below (function set).

8-Bit interface

Power On
Wait for > 20ms after Vdd rises to 4.5v

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

Wait for > 4.1ms

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

Wait for > 100µs

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	*	*	*	*

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	N	F	*	*
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	I/D	S

4-Bit interface

Power On
Wait for > 20ms after Vdd rises to 4.5V

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

Wait for > 4.1ms

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

Wait for > 100µs

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	1

RS	R/W	DB7	DB6	DB5	DB4
0	0	0	0	1	0
0	0	0	0	1	0
0	0	N	F	*	*
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	1
0	0	0	0	0	0
0	0	0	1	I/D	S

Standard character font

Handling precautions

a) The display surface is covered with a polariser which is soft and easily damaged. Avoid touching, pressing or rubbing the display with hard objects (e.g. tweezers)

b) The display is made of glass. Avoid dropping or subjecting the module to strong mechanical shocks.

c) Applying pressure to the display surface or its periphery will cause it to change colour. Care must be exercised to keep the area free of unreasonable pressure.

d) Never use organic solvents to clean the display panel as these solvents may adversely affect the polariser. To clean the display panel, dampen a piece of absorbent cotton with Isopropyl alcohol and gently wipe the panel.

e) Avoid touching the PCB terminals/electrodes or LSI leads.

f) Avoid using the display under high temperature and high humidity conditions.

g) Never disassemble the module.

h) Anti-static precautions must be taken as the circuit of the module contains a CMOS LSI.

Operation precautions

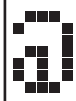
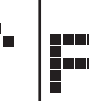
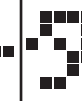
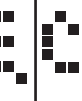
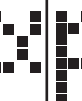
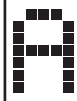
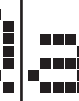
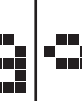
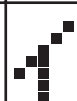
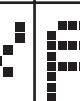
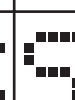
a) Never connect or disconnect the display from the main system while power is being supplied.

b) If the operating temperature drops below the temperature limits the blinking speed of the display will decrease, while if it rises above the prescribed limits, the entire display will turn black. When the temperature returns to within normal limits, the display will operate normally.

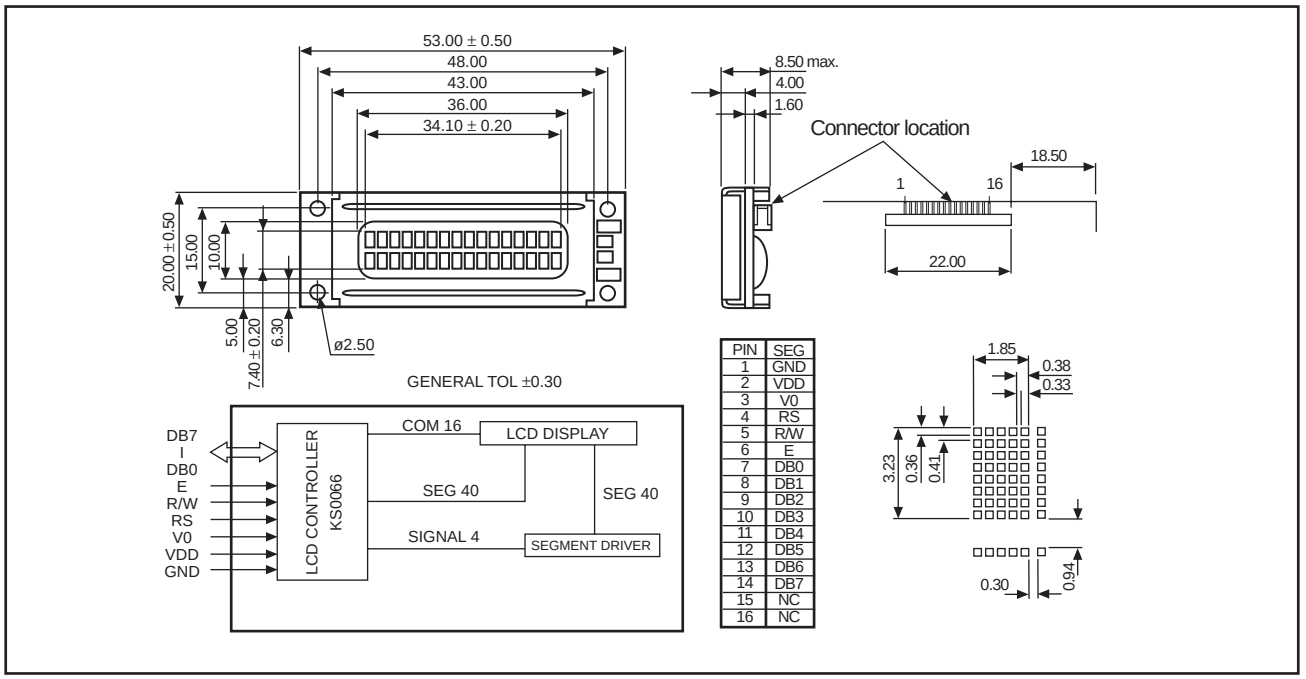
Storage precautions

a) Store away from direct sunlight and fluorescent light, and in a relatively low temperature area (avoid places of high temperature and high humidity or any place where the temperature is expected to drop below 0°C) after placing the LCD module in an electrostatic protection bag. Ideally, the module should be stored in the package provided by the supplier.

Standard character font

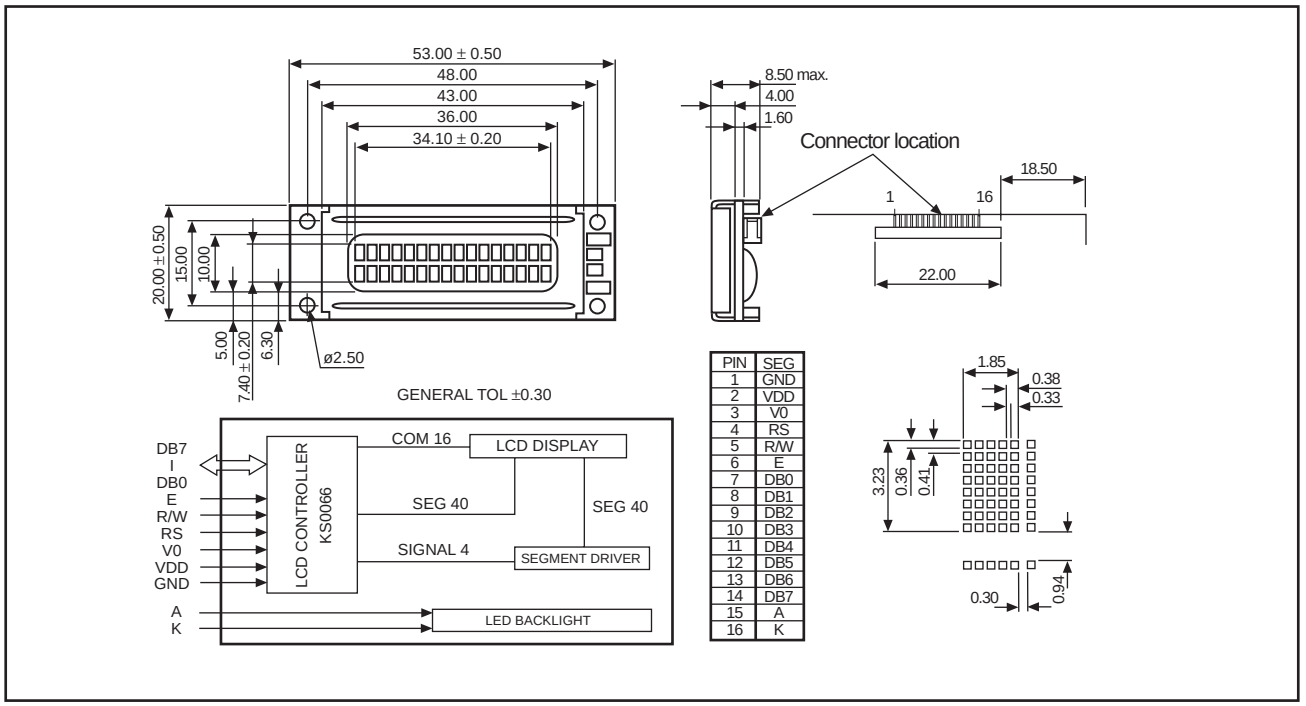
Upper 4-bit / Lower 4-bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

STN 2 x 16 character module **RS** stock no. 329-0341



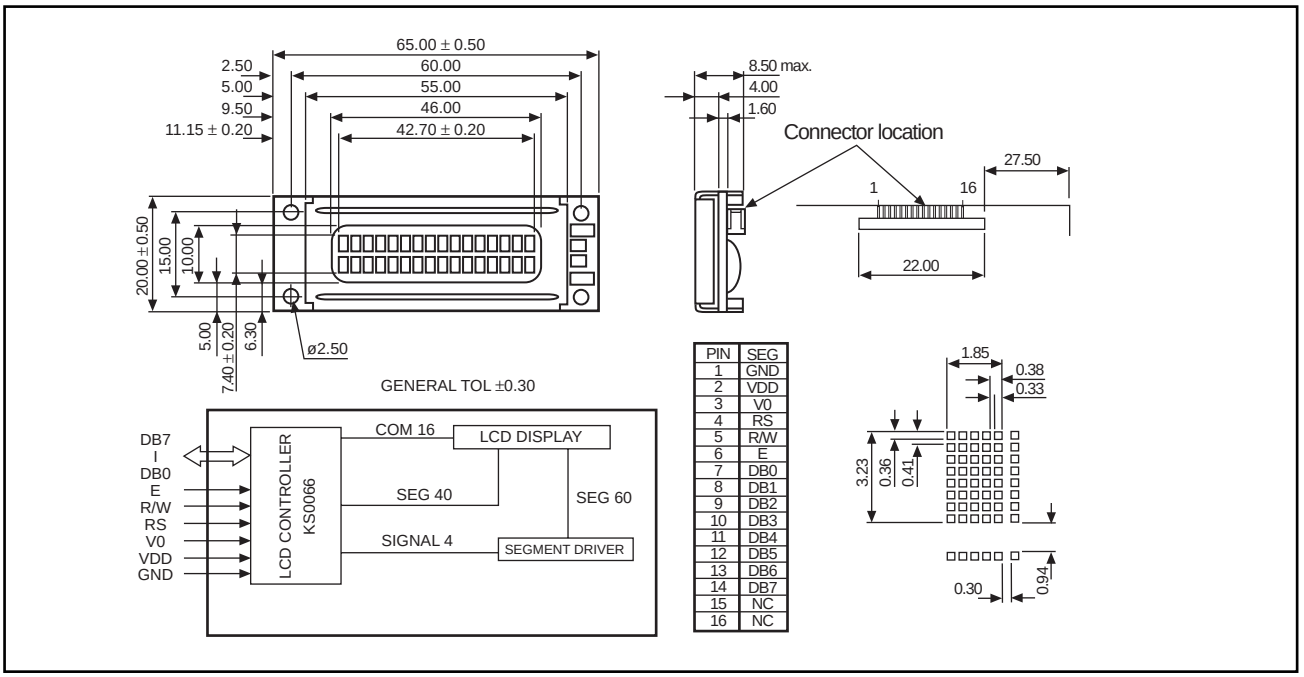
PIN	SEG
1	GND
2	VDD
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	NC
16	NC

STN 2 x 16 character module with LED backlighting **RS** stock no. 329-0379



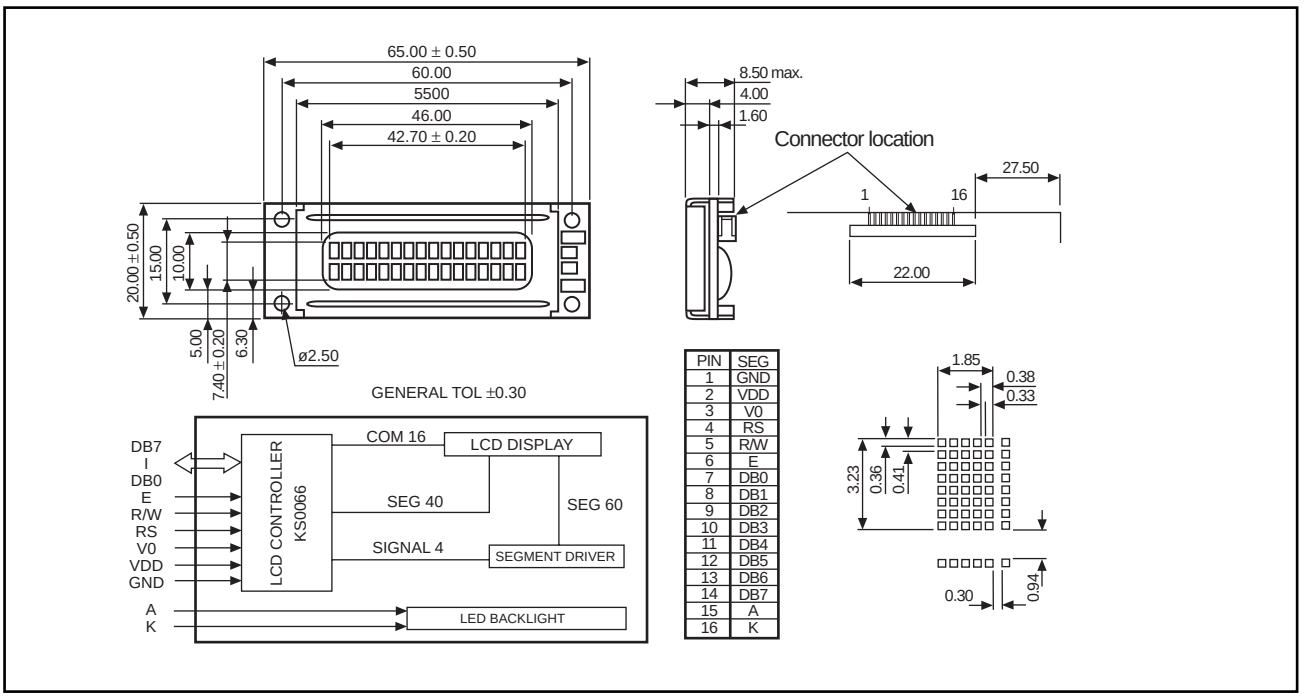
PIN	SEG
1	GND
2	VDD
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A
16	K

STN 2 x 20 character module **RS** stock no. 329-0357



PIN	SEG
1	GND
2	VDD
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	NC
16	NC

STN 2 x 20 character module with LED backlighting **RS** stock no. 329-0385



PIN	SEG
1	GND
2	VDD
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	A
16	K