LMT050DNCFWU-NYN-1

LCD Module User Manual

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Rev.	Descriptions	Release Date
0.1	Preliminary	2022-08-16
0.2	Updata Outline Drawing	2023-04-13

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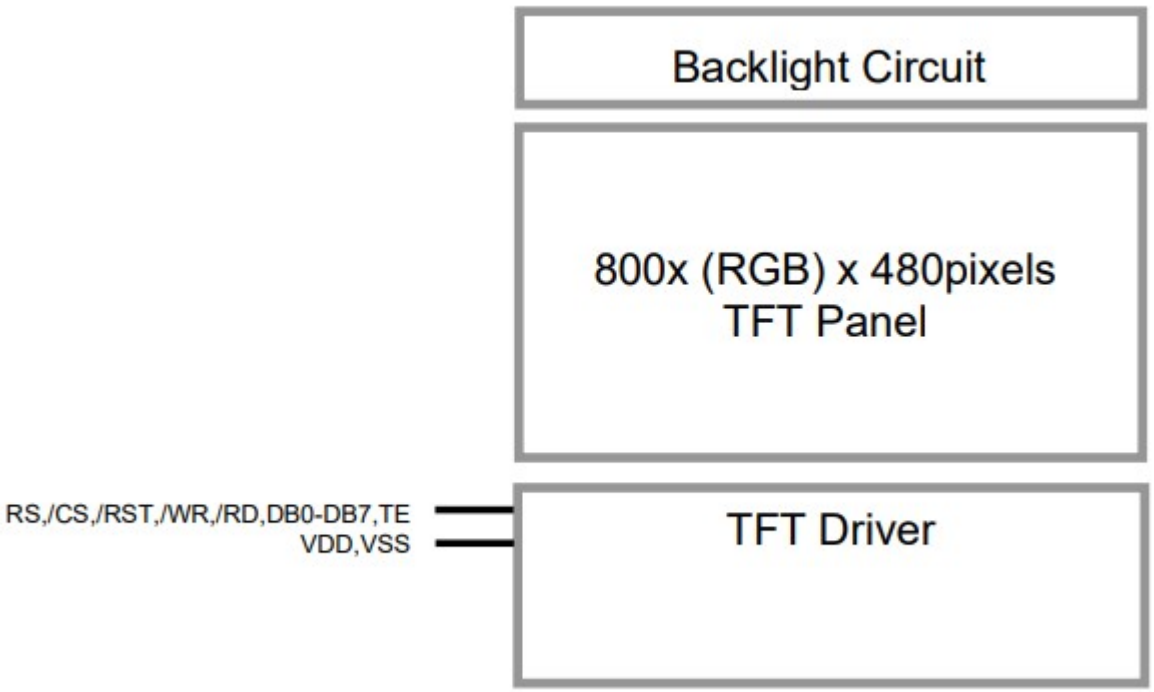
1. General Specification

Screen Size(Diagonal) :	5.0”
Active Area :	108 x 64.8 (mm)
Number of dots :	800 (RGB) x 480
Pixel Pitch：	0.135x0.135(mm)
Color Depth:	256 color
Display Technology :	a-Si TFT active matrix
Display Mode :	Normal White, Transmissive
Display Interface :	MCU_8 bits
Viewing Direction :	6 o’clock(Gray scale Inversion) (*1) 12 o’clock (*2)
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

Note:
*1 Color tune may slightly changed by temperature and driving voltage.
*2. For saturated color display content (eg. pure-red, pure-green, pure-blue, or pure-colors-combinations)
*3. For "color scales" display content

2. Block Diagram



3. Terminal Functions

3.1 Interface

K3 Pin No.	Pin Name	I/O	Descriptions	Note
1~2	VSS	P	Power Ground	
3~4	VDD	P	Positive Power Supply	
5	RS	I	Register Select RS = H, status read/command write cycle is selected. RS = L, data Read/Write cycle is selected.	
6	/CS	I	Chip Select /CS=L, enable access to the LCD interface /CS=H, disable access to the LCD interface	
7	/RST	I	Reset signal /RST = L, Initialization is executed /RST = H, Normal running.	
8~15	DB0~DB7	I	Data Input	
16	TE	O	TE Signal	
17	NC	--	No Connection	
18	/WR	I	/WR=L→H, RD=H; Data or Instruction latch into the LCD module	
19	VSS	P	Power Ground	
20	/RD	I	/WR=H, /RD=L; Data or Status read form the LCD module	
21~26	NC	--	No Connection	

4. Absolute Maximum Ratings

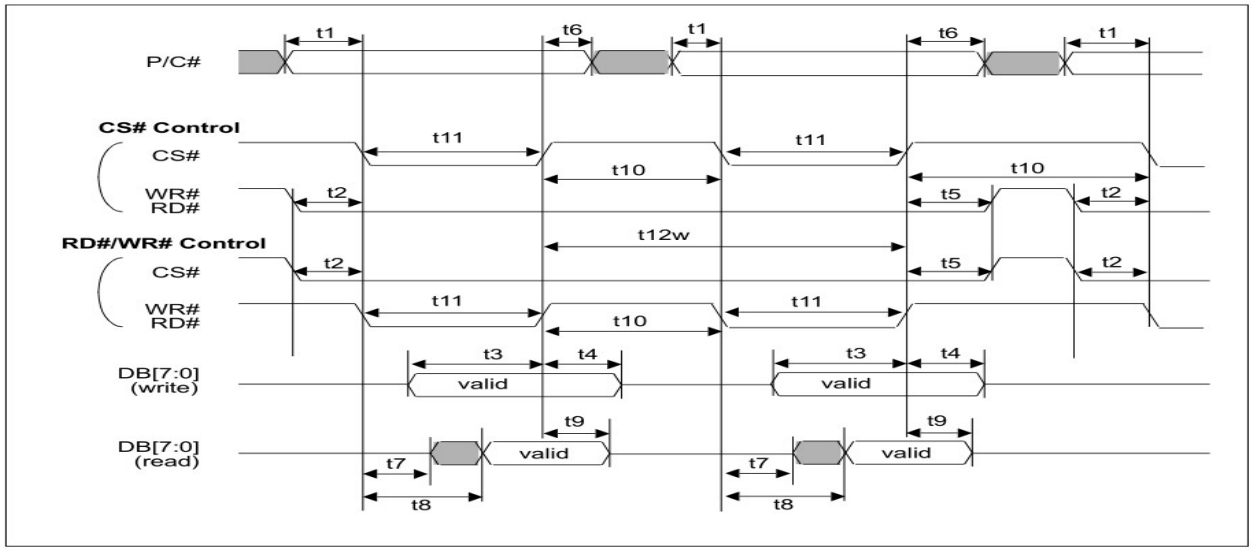
Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	+3.6	V	Vss = 0V
Operating Temperature	T_{OP}	-20	+70	°C	No Condensation
Storage Temperature	T_{ST}	-30	+80	°C	No Condensation

Cautions:
Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Output Signal Low Voltage	VOL	--	--	VSS+0.4	V	
Operating Current	I_{DD}	-	TBD	-	mA	All black, Backlight ON
		-	TBD	-	mA	All black, Backlight OFF

6. 8080 Characteristics

6.1 Indirect 8-bit Timing

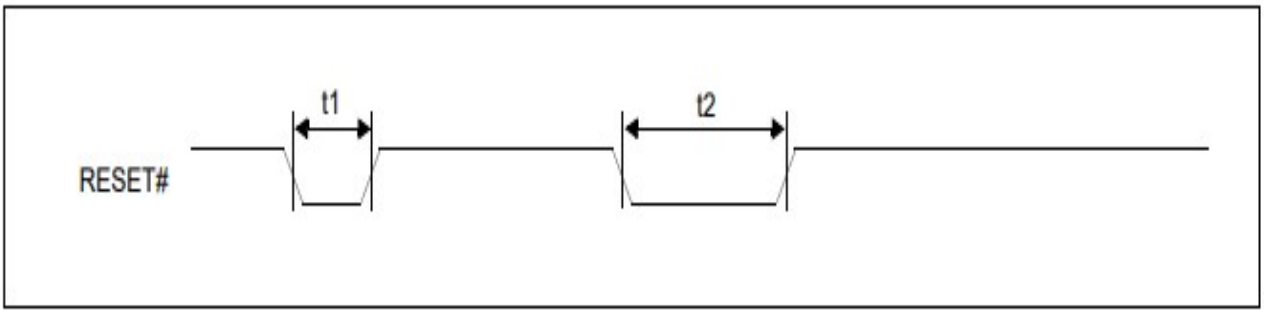


Symbol	Parameter	3.3 Volt		1.8 Volt		Units
		Min	Max	Min	Max	
t1	P/C# setup time to CS# (WR#, RD#)	1	-	1	-	ns
t2	WR#, RD# (CS#) setup time to CS# (WR#, RD#)	1	-	1	-	ns
t3	DB[7:0] setup time to CS# (WR#) rising edge: write cycle	1	-	1	-	ns
t4	DB[7:0] hold time from CS# (WR#) rising edge: write cycle	7	-	8	-	ns
t5w	WR# (CS#) hold time from CS# (WR#) rising edge: write cycle	3	-	3	-	ns
t5r	RD# (CS#) hold time from CS# (RD#) rising edge: read cycle	0	-	0	-	ns
t6	P/C# hold time from CS# (WR#, RD#) rising edge	4	-	4	-	ns
t7	CS# (RD#) falling edge to DB[7:0] driven: read cycle	-	15	-	21	ns
t8	CS# (RD#) falling edge to valid Data: read cycle	-	$4xT_{mclk}+17$	-	$4xT_{mclk}+23$	ns
t9	DB[7:0] hold time from CS# (RD#) rising edge: read cycle	2	12	2	14	ns
t10w	End of write to next read/write	5	-	5	-	ns
t10r	End of read to next read/write	$T_{mclk}+9$	-	$T_{mclk}+10$	-	ns
t11w	CS# (WR#) pulse width for write cycle	3	-	5	-	ns
t12w	CS# (WR#) rise to next CS# (WR#) rise: write cycle	$3xT_{mclk}+6$	-	$3xT_{mclk}+6$	-	ns

P/C#	WR#	RD#	Comments
0	0	1	Command Write (register address)
1	0	1	Data (Parameter) Write
0	1	0	inhibit
1	1	0	Data (Parameter) Read

Note:Refer to the S1D13L01 datasheet for more details

6.2 TFT Controller Reset Timing



VSS=0V, VDD=3.3V, T_{OP}=25°C

Symbol	Parameter	MIN.	MAX.	Unit
t1	Reset Pulse Width is ignored	-	42	ns
t2	Active Reset Pulse Width (see Note)	150	-	ns

Note:The RESET# line should be held low longer than 150ns to guarantee reset.

7. Commands

7.1 Command Summary

Command	Para-meter	HEX	A0	/CS	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
Power Save	P1	60804	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Power Save Configuration Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Power Save		Bit[1:0] = 00 , PSM0 mode
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[1:0] = 01 , PSM1 mode Bit[1:0] = 1x , NMM mode
Software Reset	P1	60806	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Software Reset Register(Write Only)
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Software Reset	Bit[8] = 0 , no effect in hardware Bit[8] = 1 , all registers are reset to default values
PLL Setting 0	P1	60810	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PLL Setting Register 0
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PLL Bypass	PLL Enable	Bit[0] = 0 , the PLL is disabled Bit[0] = 1 , the PLL enabled Bit[1] = 0 , PLL is selected
		D[15:8]	1	0	0	PLL Lock (RO)	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[1] = 1 , CLKI is selected Bit[15] = 0 , the PLL output is not stable Bit[15] = 1 , the PLL output is stable
PLL Setting 1	P1	60812	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PLL Setting Register 1
	P2	D[7:0]	1	0	0	M-Divider								Bit[9:0] 000h,001h … … 019h,020h : 1:1 ,2:1 … … 33:1(M-Divide Ratio). 021h to 13Fh: Reserved, PFDCLK = CLKI ÷ (M-Divider + 1) Bit[13:10] , must be set to 0000
		D[15:8]	1	0	0	n/a	n/a	N-Counter				M-Divider		
PLL Setting 2	P1	60814	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PLL Setting Register 2
	P2	D[7:0]	1	0	0	L-Counter								Bit[9:0] , must be set between 010h ~ 041h. , and get the M-Divide Ratio
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	L-Counter		from 17:1 to 66:1. POCLK = (L-Counter + 1) x (N-Counter + 1) x PFDCLK
Internal Clock Configuration	P1	60816	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Internal Clock Configuration Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	PCLK Divide Select			Bit[3:0] = 0000b,0001b … … 1110b,1111b : 1:1 ,2:1 … … 16:1(MCLK to
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	PCLK Frequency Ratio)
Panel Setting Miscellaneous	P1	60820	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Panel Setting Miscellaneous Register
	P2	D[7:0]	1	0	0	DE Polarity		PCLK Polarity	n/a	Panel Data Enable	Panel Data Width		Panel Port Enable	Bit[0] = 0 , TFT panel is disable Bit[0] = 1 , TFT panel is enable Bit[2:1] = 01 , TFT 16-bit Bit[2:1] = 10 , TFT 18-bit
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[2:1] = 11 , TFT 24-bit Bit[3] = 0 , panel data is disable Bit[3] = 1 , panel data is enable Bit[5] = 0, the LCD data outputs transition on the rising edge of PCLK Bit[5] = 1 , the LCD data outputs transition on the falling edge of PCLK Bit[7:6] = 00 , DE Polarity Low active Bit[7:6] = 01 , DE Polarity High active Bit[7:6] = 10 , DE Polarity Fixed to Low Bit[7:6] = 11 , DE Polarity Fixed to High
Display	P1	60822	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Display Settings Register

Settings	P2	D[7:0]	1	0	0	TE Status (RO)	TE Function		Display Blank	n/a	Display Blank Polarity	SW Video Invert	Panel Interface Enables	Bit[0] = 0 , HS, VS, DE and PCLK are fixed to H or L and the display pipes are disabled Bit[0] = 1 , enable the panel output and display pipes Bit[1] = 0 , video data is normal Bit[1] = 1 , video data is inverted
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	TE Output Pin Disable	Bit[2] = 0 , the display blank function operates normally Bit[2] = 1 , the display blank function switches polarity Bit[4] = 0 , the LCD data is masked Bit[4] = 1 , all applicable LCD data outputs are forced to zero or one Bit[6:5] = 00b , TE output is disabled and the pin output is low Bit[6:5] = 01b , TE output is high (1) when the display is in the Vertical Non-Display Period (VNDP) and low (0) when the display is in Vertical Display Period (VDISP) Bit[6:5] = 10b , Line Count Bit[6:5] = 11b , Reserved Bit[7] = 0 , the selected condition in not occurring Bit[7] = 1 , the selected condition in not occurring Bit[8] = 0 , TE is output Bit[8] = 1 , TE is not output
HDISP	P1	60824	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Horizontal Display Width Register (HDISP)
	P2	D[7:0]	1	0	0	n/a	Horizontal Display Width							Bit[6:0] = horizontal display width in pixels ÷ 8
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
HNDP	P1	60826	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Horizontal Non-Display Period Register (HNDP)
	P2	D[7:0]	1	0	0	n/a	Horizontal Non-Display Period							Bit[6:0] = horizontal non-display period in PCLK's
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
VDISP	P1	60828	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Vertical Display Height Register (VDISP)
	P2	D[7:0]	1	0	0	Vertical Display Height								Bit[9:0] = vertical display height in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Vertical Display Height		
VNDP	P1	6082A	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Vertical Non-Display Period Register (VNDP)
	P2	D[7:0]	1	0	0	Vertical Non-Display Period								Bit[7:0] = vertical non-display period in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	

Command	Para-meter	HEX	A0	/CS	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
HSW	P1	6082C	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								HS Pulse Width Register (HSW)
	P2	D[7:0]	1	0	0	HS Pulse Polarity	HS Pulse Width							Bit[6:0] = HS pulse width in PCLK's Bit[7] = 0 , the horizontal sync signal is active low Bit[7] = 1 , the horizontal sync signal is active high
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
HPS	P1	6082E	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								HS Pulse Start Position Register (HPS)
	P2	D[7:0]	1	0	0	n/a	HS Pulse Start Position							Bit[6:0] = HS pulse start position in PCLK's
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
VSW	P1	60830	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								VS Pulse Width Register (VSW)
	P2	D[7:0]	1	0	0	VS Pulse Polarity	n/a	VS Pulse Width						Bit[5:0] = VS pulse width in lines Bit[7] = 0 , the vertical sync signal is active low Bit[7] = 1 , the vertical sync signal is active high
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
VPS	P1	60832	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								VS Pulse Start Position Register (VPS)
	P2	D[7:0]	1	0	0	VS Pulse Start Position								Bit[7:0] = VS pulse start position in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
TE Line Count	P1	60834	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								TE Line Count Register
	P2	D[7:0]	1	0	0	TE Line Count								These bits specify the line count value that is compared with the internal vertical line counter
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	TE Line Count		
Main Layer Setting	P1	60840	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Setting Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	Main Layer Rotation Select	Main Layer Color Depth				Bit[2:0] = 000b, RGB 8:8:8 (default) Bit[2:0] = 001b, RGB 5:6:5 Bit[2:0] = 010b/011b/111b, Reserved Bit[2:0] = 100b, 24 bpp + LUT1 Bit[2:0] = 101b, 16 bpp + LUT1 Bit[2:0] = 110b, 8 bpp + LUT1 Bit[4:3] = 00b, 0° (Normal) Bit[4:3] = 01b, 90° Bit[4:3] = 10b, 180° Bit[4:3] = 11b, 270° Bit[8] = 0, Synchronous latching of multi-byte layer registers is enabled Bit[8] = 1, Synchronous latching of multi-byte layer registers is disabled
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Multi-Byte Layer Registers Synchronous Latching Disable	
Main Layer Start Address 0	P1	60842	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Start Address Register 0
	P2	D[7:0]	1	0	0	Main Layer Start Address								Bit[15:0] is Bit[15:0] of Main Layer Start Address ,but Bit[1:0] must be set to 00b
		D[15:8]	1	0	0	Main Layer Start Address								
Main Layer Start Address 1	P1	60844	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Start Address Register 1
	P2	D[7:0]	1	0	0	n/a		n/a	n/a	n/a	Main Layer Start Address			Bit[2:0] is Bit[18:16] of Main Layer Start Address
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	

Main Layer Width	P1	60846	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Width Register
	P2	D[7:0]	1	0	0	Main Layer Width								Read Only
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Main Layer Width		
Main Layer Height	P1	60848	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Main Layer Height Register
	P2	D[7:0]	1	0	0	Main Layer Height								Read Only
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Main Layer Height		
PIP Layer Setting	P1	60850	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Setting Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[2:0] = 000b, RGB 8:8:8 (default) Bit[2:0] = 001b, RGB 5:6:5 Bit[2:0] = 010b/011b/111b, Reserved Bit[2:0] = 100b, 24 bpp + LUT1 Bit[2:0] = 101b, 16 bpp + LUT1 Bit[2:0] = 110b, 8 bpp + LUT1 Bit[4:3] = 00b, 0° (Normal) Bit[4:3] = 01b, 90° Bit[4:3] = 10b, 180° Bit[4:3] = 11b, 270°
		D[15:8]	1	0	0	n/a	n/a	n/a	PIP Layer Rotation Select	PIP Layer Color Depth				
PIP Layer Start Address 0	P1	60852	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Start Address Register 0
	P2	D[7:0]	1	0	0	PIP Layer Start Address								Bit[15:0] is Bit[15:0] of Main Layer Start Address ,but Bit[1:0] must be set to 00b
		D[15:8]	1	0	0	PIP Layer Start Address								
PIP Layer Start Address 1	P1	60854	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Start Address Register 1
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Bit[2:0] is Bit[18:16] of Main Layer Start Address
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	PIP Layer Start Address			
PIP Layer Width	P1	60856	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Width Register
	P2	D[7:0]	1	0	0	PIP Layer Width								Bit[9:] = PIP Layer Horizontal Display Period in number of pixels PIP Layer Horizontal Display Period in number of pixels
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer Width		

Command	Para-meter	HEX	A0	/CS	/WR	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
PIP Layer Height	P1	60858	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Height Register
	P2	D[7:0]	1	0	0	PIP Layer Height								Bit[9:] = PIP Layer Vertical Display Period in number of lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer Height		
PIP Layer X Start Position	P1	6085A	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer X Start Position Register
	P2	D[7:0]	1	0	0	PIP Layer X Start Position								These bits specify X start position of the PIP Layer on the panel, in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer X Start Position		
PIP Layer Y Start Position	P1	6085C	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Layer Y Start Position Register
	P2	D[7:0]	1	0	0	PIP Layer Y Start Position								These bits specify Y start position of the PIP Layer on the panel, in lines
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	PIP Layer Y Start Position		
PIP Enable	P1	60860	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								PIP Enable Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	Blink/ Fade Status (RO)	Blink/Fade Effect			Bit[2:0] = 000b, Blank Bit[2:0] = 001b, Normal Bit[2:0] = 010b, Blink 1 Bit[2:0] = 011b, Blink 2 Bit[2:0] = 100b, Fade Out Bit[2:0] = 101b, Fade In Bit[2:0] = 110b, Fade In/Out Continuous Bit[2:0] = 111b, Reserved Bit[3] = 0b, the PIP layer is not blinking or fading Bit[3] = 1b, the PIP layer is in the process of blinking or fading Bit[15:9] = blink/fade period in frames – 1
		D[15:8]	1	0	0	Blink/Fade Period							n/a	
Alpha Blending	P1	60862	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Alpha Blending Register
	P2	D[7:0]	1	0	0	n/a	Alpha Blending Ratio							Bit[6:0] = 0000000b,0000001b… …0111111b,1000000b : 64:0 (no PIP),63:1 … … 1:63,0:64(full PIP) ; 1000001b ~ 1111111b : Reserved
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	Alpha Blending Step		Bit[9:8] = 00b, 1 Bit[9:8] = 01b, 2 Bit[9:8] = 10b, 4 Bit[9:8] = 11b, 8
Transparency	P1	60864	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Transparency Register
	P2	D[7:0]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	Transparency Enable	Bit[0] = 0b, transparency is disabled Bit[0] = 1b, transparency is enabled
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
Transparency Key Color 0	P1	60866	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Transparency Key Color Register 0
	P2	D[7:0]	1	0	0	Key Color Blue								Bit[15:8] is Key Color Green bits [7:0] Bit[7:0] is Key Color Blue bits [7:0]
		D[15:8]	1	0	0	Key Color Green								
Transparency Key Color 1	P1	60868	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								Transparency Key Color Register 1
	P2	D[7:0]	1	0	0	Key Color Red								Bit[7:0] is Key Color Red bits [7:0]
		D[15:8]	1	0	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	
GPIO Configuration	P1	608D0	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								GPIO Configuration Register
	P2	D[7:0]	1	0	0	GPIO7 Config	GPIO6 Config	GPIO5 Config	GPIO4 Config	GPIO3 Config	GPIO2 Config	GPIO1 Config	GPIO0 Config	Bit[15:0] = 0b (default), the corresponding GPIO pin is configured as an input pin

		D[15:8]	1	0	0	GPIO15 Config	GPIO14 Config	GPIO13 Config	GPIO12 Config	GPIO11 Config	GPIO10 Config	GPIO9 Config	GPIO8 Config	Bit[15:0] = 1b , the corresponding GPIO pin is configured as an output pin
GPIO Status and Control	P1	608D2	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								GPIO Status and Control Register
	P2	D[7:0]	1	0	0	GPIO7 Status	GPIO6 Status	GPIO5 Status	GPIO4 Status	GPIO3 Status	GPIO2 Status	GPIO1 Status	GPIO0 Status	When GPIOx is configured as an output: Bit[15:0] = 0b, GPIOx low Bit[15:0] = 1b, GPIOx high *GPIO2 high, Backlight on; low, Backlight off
		D[15:8]	1	0	0	GPIO15 Status	GPIO14 Status	GPIO13 Status	GPIO12 Status	GPIO11 Status	GPIO10 Status	GPIO9 Status	GPIO8 Status	
GPIO Pull-Down Control	P1	608D4	0	0	0	A[7:0]-> A[15:8] -> A[18:16]								GPIO Pull-Down Control Register
	P2	D[7:0]	1	0	0	GPIO7 Pull-down Control	GPIO6 Pull-down Control	GPIO5 Pull-down Control	GPIO4 Pull-down Control	GPIO3 Pull-down Control	GPIO 2 Pull-down Control	GPIO1 Pull-down Control	GPIO0 Pull-down Control	Bit[15:0] = 0b, the pull-down resistor for the associated GPIO pin is inactive. Bit[15:0] = 1b, the pull-down resistor for the associated GPIO pin is active.
		D[15:8]	1	0	0	GPIO15 Pull-down Control	GPIO14 Pull-down Control	GPIO13 Pull-down Control	GPIO12 Pull-down Control	GPIO11 Pull-down Control	GPIO10 Pull-down Control	GPIO9 Pull-down Control	GPIO8 Pull-down Control	

Note: Access of PLL Setting 0, PLL Setting 1, PLL Setting 2 and Internal Clock Configuration is only possible in Power Save Mode PSM0.
GPIO2 high, Backlight on; low, Backlight off(See register “608D2” for details)

For more information and details please refer to S1D13L01 datasheet.

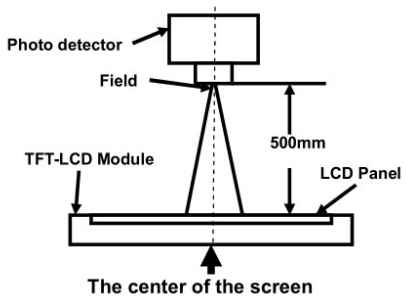
8. Optical Characteristics

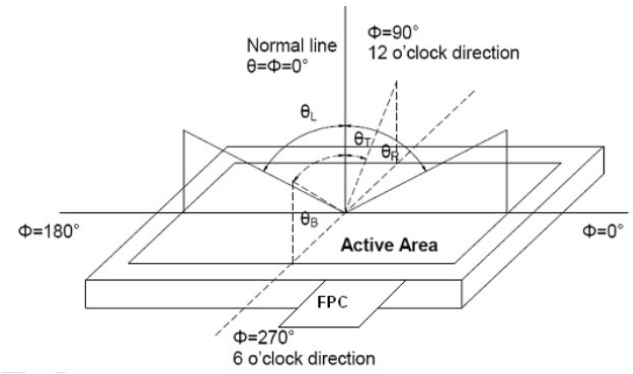
Item		Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle		θ_T	(CR≥10)	40	50	-	degree	Note 2,3
		θ_B		60	70	-		
		θ_L		60	70	-		
		θ_R		60	70	-		
Contrast ratio		CR	θ=0°	500	600	-	-	Note 3
Response Time		T_{on}	25℃	-	20	30	msec	Note 4
		T_{off}					msec	
Chromaticlty	White	X	Backlight is on	0.253	0.303	0.353		Note 1,5
		Y		0.272	0.322	0.372		
	Red	X		0.534	0.584	0.634		
		Y		0.298	0.348	0.398		
	Green	X		0.288	0.338	0.388		
		Y		0.540	0.590	0.640		
	Blue	X		0.100	0.150	0.200		
		Y		0.044	0.094	0.144		
Luminance		L		200	250	-	cd/m^2	Note 7
NTSC				-	50		%	Note 5
Luminance uniformity		U		75	80	-	%	Note 6

Test Conditions:
1. I F = 40 mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80)。



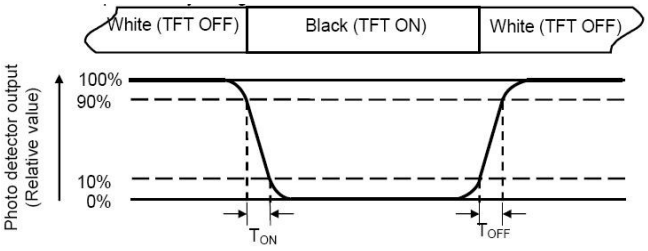


Note 3:
The definition of contrast ratio

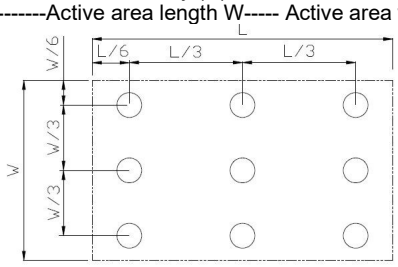
$$\text{Contrast Ratio(CR)} = \frac{\text{Luminance When LCD is at "White" state}}{\text{Luminance When LCD is at "Black" state}}$$

"White state ": The state is that the LCD should drive by Vwhite.
"Black state": The state is that the LCD should drive by Vblack.
Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between "White" state and
"Black" state. Rise time (T ON) is the time between photo detector output intensity changed from 90%
to 10%. And fall time (T OFF) is the time between photo detector output intensity changed from 10%
to 90%.



Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.
Note 6: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer Fig. 2).
Every measuring point is placed at the
center of each measuring area.
Luminance Uniformity (U) = Lmin/ Lmax
L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.
Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:
Measure the luminance of white state at center point.

9. LCD Module Design and Handling Precautions

- Please ensure V0, VCOM is adjustable, to enable LCD module get the best contrast ratio under different temperatures, view angles and positions.

- Normally display quality should be judged under the best contrast ratio within viewable area. Unexpected display pattern may come out under abnormal contrast ratio.

- Never operate the LCD module exceed the absolute maximum ratings.
- Never apply signal to the LCD module without power supply.

- Keep signal line as short as possible to reduce external noise interference.
- IC chip (e.g. TAB or COG) is sensitive to light. Strong light might cause malfunction. Light sealing structure casing is recommended.

- Make sure there is enough space (with cushion) between case and LCD panel, to prevent external force passed on to the panel; otherwise that may cause damage to the LCD and degrade its display result.
- Avoid showing a display pattern on screen for a long time (continuous ON segment).

- LCD module reliability may be reduced by temperature shock.
- When storing and operating LCD module, avoids exposure to direct sunlight, high humidity, high or low temperature. They may damage or degrade the LCD module.
- Never leave LCD module in extreme condition (max./min storage/operate temperature) for more than 48hr.
- Recommend LCD module storage conditions is 0 C~40 C <80%RH.

- LCD module should be stored in the room without acid, alkali and harmful gas.
- Avoid dropping & violent shocking during transportation, and no excessive pressure press, moisture and sunlight.

- LCD module can be easily damaged by static electricity. Please maintain an optimum anti-static working environment to protect the LCD module.(eg. ground the soldering irons properly)
- Be sure to ground the body when handling LCD module.

- Only hold LCD module by its sides. Never hold LCD module by applying force on the heat seal or TAB.
- When soldering, control the temperature and duration avoid damaging the backlight guide or diffuser which might degrade the display result such as uneven display.
- Never let LCD module contact with corrosive liquids, which might cause damage to the backlight guide or the electric circuit of LCD module.
- Only clean LCD with a soft dry cloth, Isopropyl Alcohol or Ethyl Alcohol. Other solvents (e.g. water) may damage the LCD.

- Never add force to components of LCD module. It may cause invisible damage or degrade the module's reliability.
- When mounting LCD module, please make sure it is free from twisting, warping and bending.
- Do not add excessive force on surface of LCD, which may cause the display color change abnormally.
- LCD panel is made with glass. Any mechanical shock (e.g. dropping from high place) will damage the LCD module.
- Protective film is attached on LCD screen. Be careful when peeling off this protective film, since static electricity may be generated.
- Polarizer on LCD gets scratched easily. If possible, do not remove LCD protective film until the last step of installation.
- When peeling off protective film from LCD, static charge may cause abnormal display pattern. The symptom is normal, and it will turn back to normal in a short while.
- LCD panel has sharp edges, please handle with care.
- Never attempt to disassemble or rework LCD module.
- If display panel is damaged and liquid crystal substance leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes promptly wash it off using soap and water.

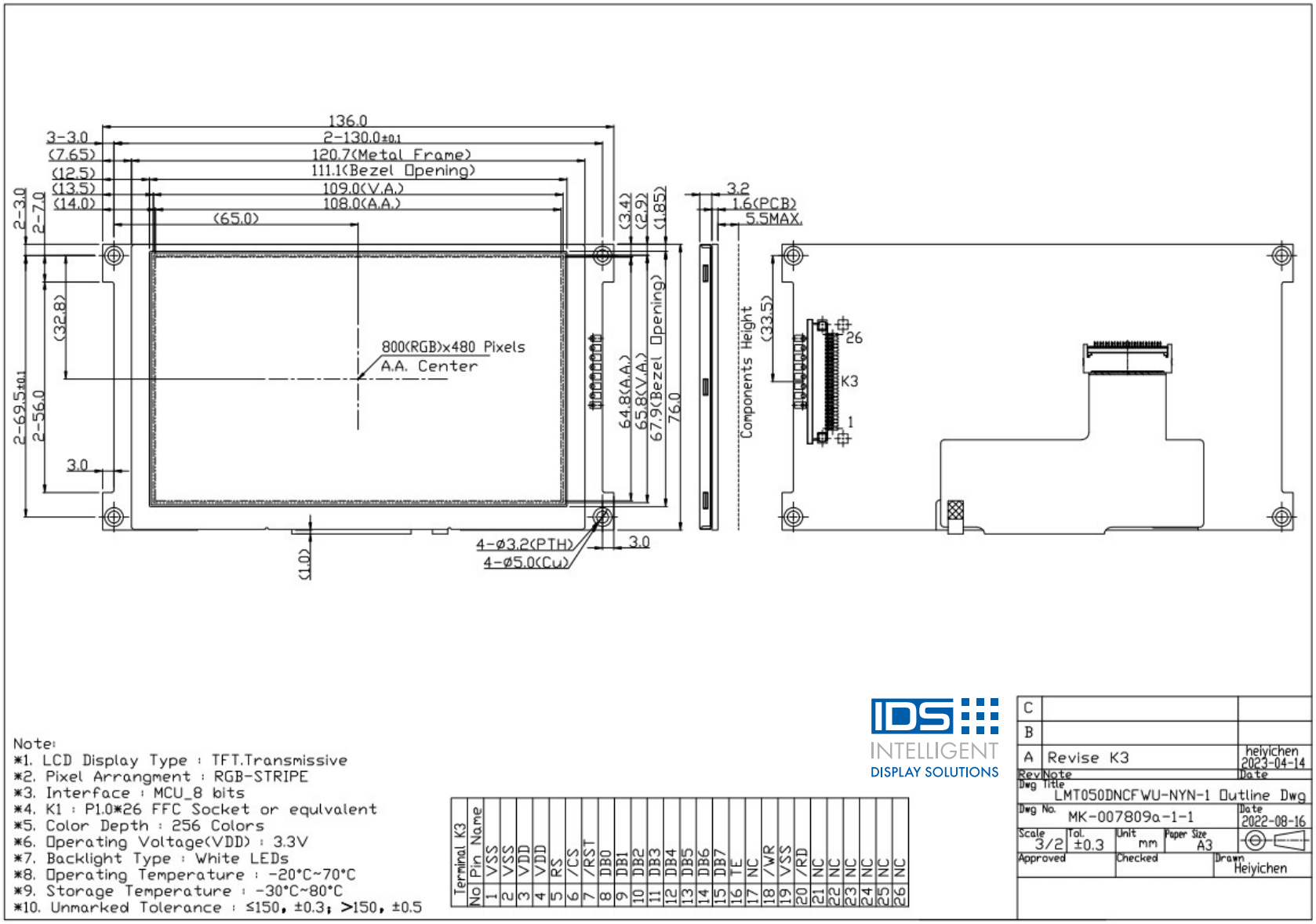
Warranty

This product has been manufactured to our company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct

risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- We cannot accept responsibility for any defect, which may arise form additional manufacturing of the product (including disassembly and reassembly), after product delivery.
- We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
- We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed our company's acceptance inspection procedures.
- When the product is in CCFL models, CCFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
- We cannot accept responsibility for intellectual property of a third part, which may arise through the application of our product to our assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.

10. Outline Drawing



Note:
*1. LCD Display Type : TFT.Transmissive
*2. Pixel Arrangment : RGB-STRIPE
*3. Interface : MCU_8 bits
*4. K1 : P1.0*26 FFC Socket or equlvalent
*5. Color Depth : 256 Colors
*6. Operating Voltage(VDD) : 3.3V
*7. Backlight Type : White LEDs
*8. Operating Temperature : -20°C~70°C
*9. Storage Temperature : -30°C~80°C
*10. Unmarked Tolerance : ≤150, ±0.3; >150, ±0.5

Terminal K3 No	Pin Name
1	VSS
2	VSS
3	VDD
4	VDD
5	RS
6	/CS
7	/RST
8	DB0
9	DB1
10	DB2
11	DB3
12	DB4
13	DB5
14	DB6
15	DB7
16	TE
17	NC
18	/WR
19	VSS
20	/RD
21	NC
22	NC
23	NC
24	NC
25	NC
26	NC

IDS INTELLIGENT DISPLAY SOLUTIONS

Rev	Note	Date
C		
B		
A	Revise K3	heiyichen 2023-04-14

Dwg Title: LMT050DNCFWU-NYN-1 Outline Dwg
Dwg No.: MK-007809a-1-1
Date: 2022-08-16
Scale: 3/2 | Tol.: ±0.3 | Unit: mm | Paper Size: A3
Approved | Checked | Drawn: Heiyichen