X20DMF320

Data sheet
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Translation of the original documentation

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Disclaimer

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1 General information

1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual

1.2 Order data

Order number	Short description	Figure
	Digital inputs/outputs	
X20DMF320	X20 digital mixed module, 16 inputs, 24 VDC, sink, additional functions, 16 digital channels, 24 VDC, 0.5 A, configurable as inputs or outputs, 3x PWM, 2x optional 0.5 or 2 A output, 1-wire connections	
	Required accessories	
	Terminal blocks	
X20TBS1	Terminal block set for X20 I/O module: 2x 16-pin terminal block	
X20TBS2	Terminal block set for X20 I/O module: 8x 4-pin terminal block	

Table 1: X20DMF320 - Order data

1.3 Module description

The module is equipped with 16 inputs and 16 mixed channels, optionally as input or output in 1-wire technology. The outputs are designed for a source output circuit, and the inputs are designed for a sink circuit.

Functions:

- Digital inputs
- Event counter
- Period measurement
- Gate time measurement
- ABR incremental encoder
- Latch function
- Digital outputs
- PWM

Digital inputs

The digital inputs are equipped with an input filter with a configurable input delay.

Event counting / Period measurement / Gate time measurement

The module has 2 channels, which can be used as either event counters or for period duration / gate time measurement.

ABR incremental encoder

2 ABR incremental encoders can be connected to the module. This allows the detection of position (linear) or angular (rotating) changes in ABR encoders.

Latch function

The latch function can be used to latch the current counter values of the event counters or ABR incremental encoders.

Higher nominal output current

Starting with Rev. B1, a nominal output current of 2 A can be set for 2 outputs.

Monitoring status of the digital outputs

The output signal of the digital outputs is monitored for short circuit or overload, as is the state of the power supply.

PWM

The module is equipped with a PWM mode. This can be used to control valves, for example. To prevent the valves from sticking, a dither can be configured exactly according to the specifications of the valve manufacturer.

2 Technical description

2.1 Technical data

Order number	X20DMF320
Short description	
I/O module	16 digital inputs 24 VDC for 1-wire connections 16 mixed channels, 24 VDC input or output for 1-wire connections
General information	
B&R ID code	0x2E86
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Outputs	Yes, using LED status indicator and software (output state)
Power consumption	
Bus	0.04 W
Internal I/O [1]	2.7 W
Additional power dissipation caused by actuators (resistive) [W] [2]	0.312 W
Certifications	
CE	Yes
UKCA	Yes
Digital inputs	
Quantity [3]	6 high-speed inputs, 10 standard inputs 16 mixed channels, configuration as input or output using software
Nominal voltage	24 VDC
Input characteristics per EN 61131-2	Type 1
Input voltage	24 VDC -15% / +20%
Input current at 24 VDC	Channels 1 to 6, high-speed inputs: Typ. 3.2 mA Channels 7 to 16, standard inputs: Typ. 2.4 mA Channels 17 to 32, mixed channel: Typ. 2.4 mA
Input circuit	Sink
Input filter	
Hardware	High-speed inputs: ≤7 µs Standard inputs and mixed channels: ≤100 µs
Software	Default 0 ms, configurable between 0 and 25 ms in 0.1 ms intervals
Connection type	1-wire connections
Input resistance	Channels 1 to 6, high-speed inputs: 7.5 kΩ Channels 7 to 16, standard inputs: 10 kΩ Channels 17 to 32, mixed channels: 10 kΩ
Additional functions	Channels 1 to 6, high-speed digital inputs: 2x 40 kHz event counting, 2x ABR incremental encoder, 2x period measurement, 2x gate time measurement, 2x counter latch function
Switching threshold	
Low	<5 VDC
High	>15 VDC
Insulation voltage between channel and bus	959 VAC
ABR incremental encoder	
Quantity	2
Encoder inputs	24 V, asymmetrical
Counter size	16-bit
Input frequency	40 kHz
Evaluation	4x
Event counters	
Quantity	2
Signal form	Square wave pulse
Evaluation	Rising edge, falling edge or both edges The counter is cyclical.
Input frequency	40 kHz
Counter size	16-bit
Edge detection / Time measurement	
Possible measurements	Period measurement, gate time measurement
Signal form	Square wave pulse
Evaluation	Positive edge - Negative edge
Counter size	16-bit
Counter frequency	
Internal	48 MHz, 24 MHz, 12 MHz, 6 MHz, 3 MHz, 1.5 MHz, 750 kHz, 375 kHz, 187.5 kHz
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs

Table 2: X20DMF320 - Technical data

Technical description

Order number	X20DMF320
Digital outputs	
Quantity	13 standard outputs, 3 high-speed outputs All outputs designed as mixed channels, configurable as inputs or outputs using software
Variant	Current-sourcing FET
Nominal voltage	24 VDC
Switching voltage	24 VDC -15% / +20%
Nominal output current	0.5 A per channel DO 22 and DO 30: Optional 0.5 or 2 A starting with Rev. B1
Total nominal current	8 A
Connection type	1-wire connections
Output circuit	Source
Output protection	Thermal shutdown in the event of overcurrent or short circuit (see value "Short-circuit peak current")
Pulse width modulation	
Period duration	1 to 65 ms
Pulse duration	0 to 100%
Resolution for pulse duration	0.1%
Diagnostic status	Output monitoring with 25 ms delay
Leakage current when the output is switched off	3 µA
$R_{DS(on)}$	78 mΩ
Peak short-circuit current	6.95 A
Switch-on in the event of overload shutdown or short-circuit shutdown	Approx. 3 ms (depends on the module temperature)
Switching delay	
0 → 1	≤300 µs
1 → 0	≤300 µs
Switching frequency	
Resistive load	Standard outputs: Max. 500 Hz High-speed outputs: Max. 1 kHz
Braking voltage when switching off inductive loads	Typ. 53 VDC
Insulation voltage between channel and bus	959 VAC
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.6°C per 100 m
Maximum	4000 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 45°C
Derating	See section "Derating".
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order terminal blocks separately (see section "Order data").
Dimensions	
Width (pitch)	$27.5^{+0.2}$ mm
Height	124 mm
Depth	92 mm

Table 2: X20DMF320 - Technical data

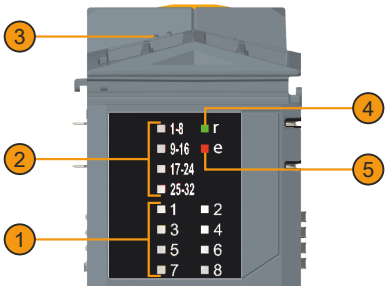
1) The power consumed externally for operating the module discharges via the GND contact of the power supply module and must therefore be taken into account in the power balance of the power supply module.
2) Number of outputs x $R_{DS(on)}$ x Nominal output current^2. For a calculation example, see section "Mechanical and electrical configuration" in the X20 System user's manual.
3) If a mixed channel is used as a digital input, connecting a push-pull is not permitted.

2.2 LED status indicators

LED arrangement

In order to display the status of the 32 channels, they have been combined into 4 groups of 8 channels each. The channel group button is used to switch between groups. The selected group is displayed with the channel group LEDs. The channel LEDs indicate the channel status.

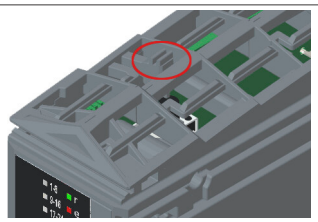
The module status is indicated by LEDs Run and Error.



1	Channel LEDs	2	Channel group LEDs
3	Channel group button	4	LED Run
5	LED Error	-	-

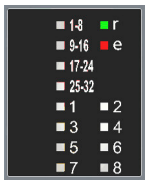
Channel group button

The channel group button is used to switch the 4 channel groups. The channel group button is located on the top of the module. It is marked in red in the following image.



LED description

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	Mode RESET
			Double flash	Mode BOOT (during firmware update)[1]
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	e	Red	Off	Module not supplied with power or everything OK
	e + r	Solid red / Single green flash		Invalid firmware
	1-8, 9-16, 17-24, 25-32	Orange		Selected channel group
	1 - 8	Orange		Input/Output state of the corresponding digital channel

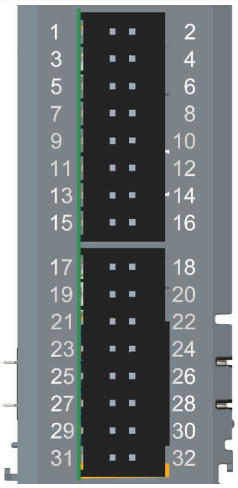
1) Depending on the configuration, a firmware update can take up to several minutes.

2.3 Pinout

Terminal connection

The 32 terminal connections are connected via terminal blocks. Corresponding sets can be ordered from B&R (see "Order data" on page 3).

The following image contains an overview of the 32 terminal connections.



Channel mapping

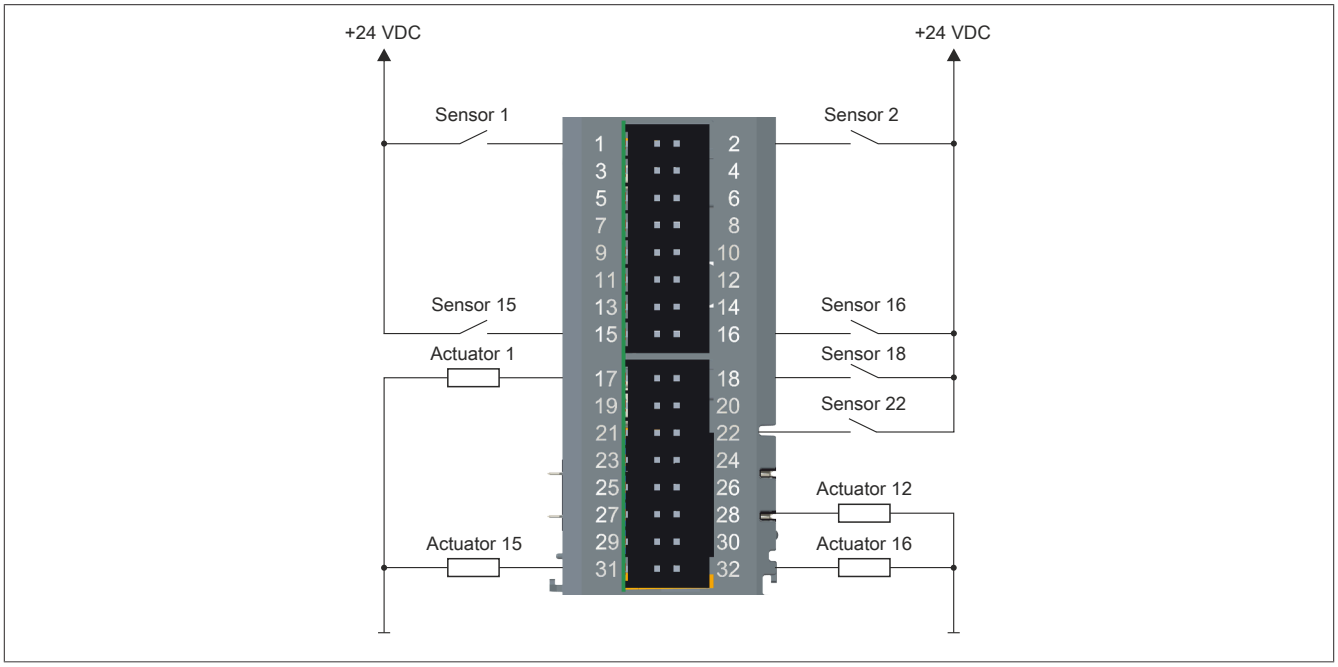
The following overview shows the assignment of terminal connections to the I/O channels and their properties.

The functions of high-speed digital inputs and outputs are described under "Functions of the high-speed digital inputs/outputs" on page 16.

Terminal connection	Channel	Note
1	DI 1	High-speed digital input
2	DI 2	High-speed digital input
3	DI 3	High-speed digital input
4	DI 4	High-speed digital input
5	DI 5	High-speed digital input
6	DI 6	High-speed digital input
7	DI 7	
8	DI 8	
9	DI 9	
10	DI 10	
11	DI 11	
12	DI 12	
13	DI 13	
14	DI 14	
15	DI 15	
16	DI 16	
17	DI/DO 17	
18	DI/DO 18	
19	DI/DO 19	High-speed digital output
20	DI/DO 20	
21	DI/DO 21	
22	DI/DO 22	Optionally 0.5 or 2 A starting with Rev. B1
23	DI/DO 23	
24	DI/DO 24	
25	DI/DO 25	High-speed digital output
26	DI/DO 26	
27	DI/DO 27	
28	DI/DO 28	
29	DI/DO 29	
30	DI/DO 30	Optionally 0.5 or 2 A starting with Rev. B1
31	DI/DO 31	High-speed digital output
32	DI/DO 32	

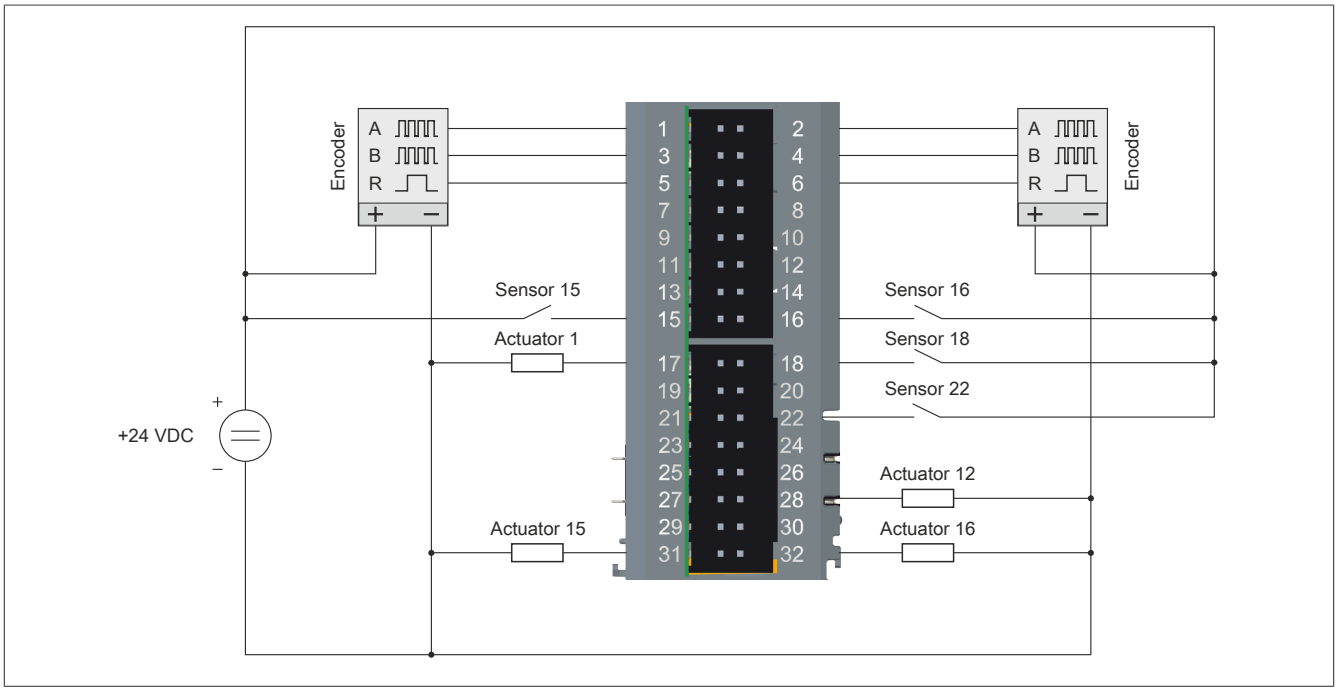
2.4 Connection examples

Digital inputs/outputs



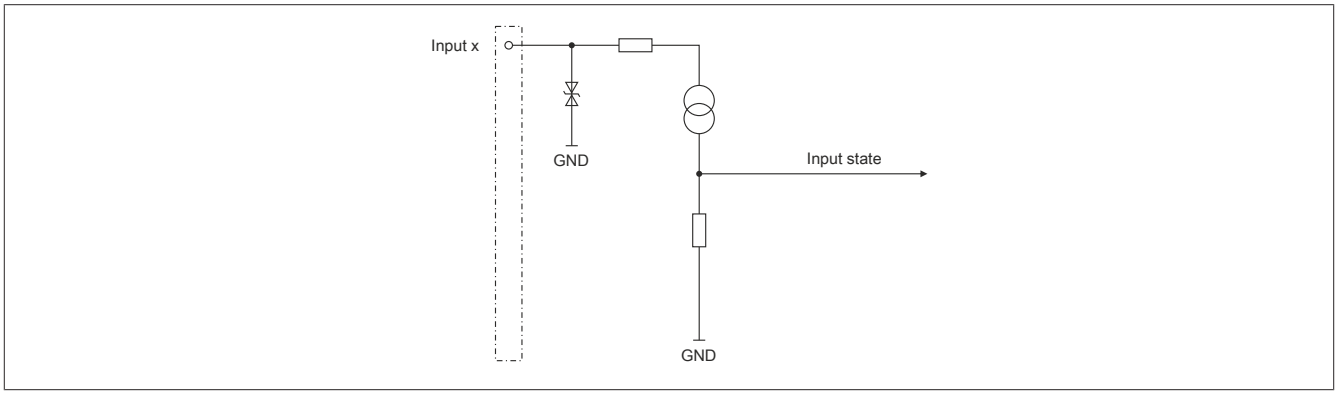
ABR incremental encoder and digital inputs/outputs

Starting with Rev. B1, no shielding is necessary for channels 1 to 6.

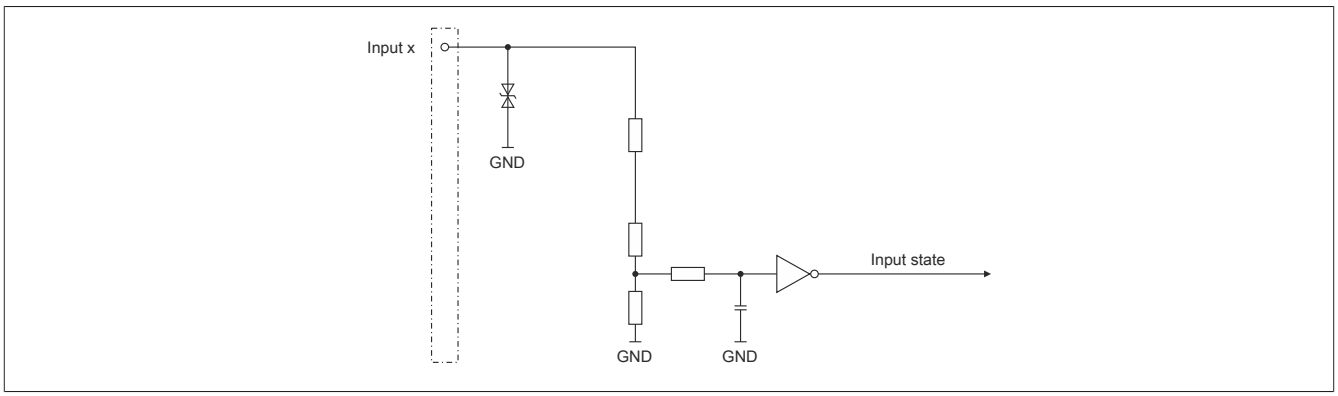


2.5 Input circuit diagram

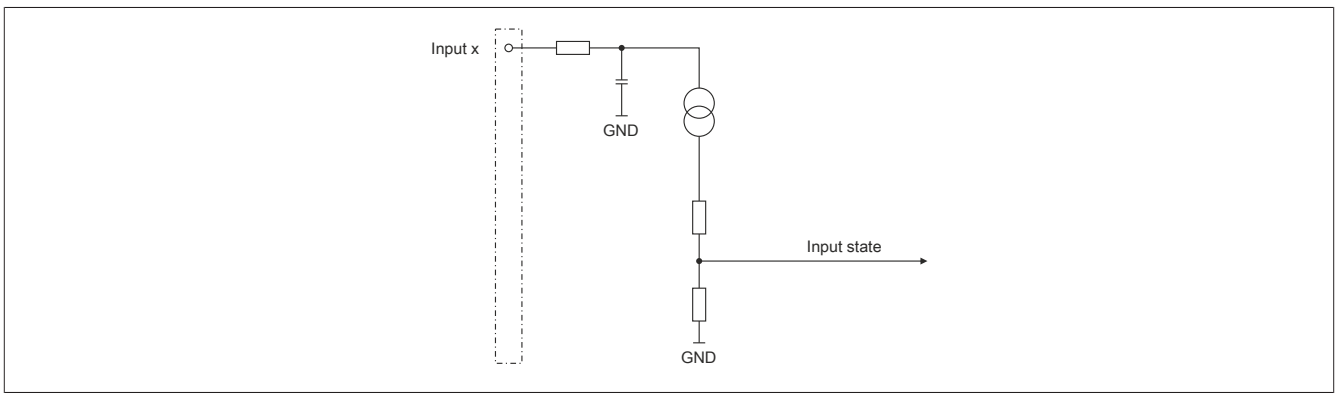
Standard input



High-speed input

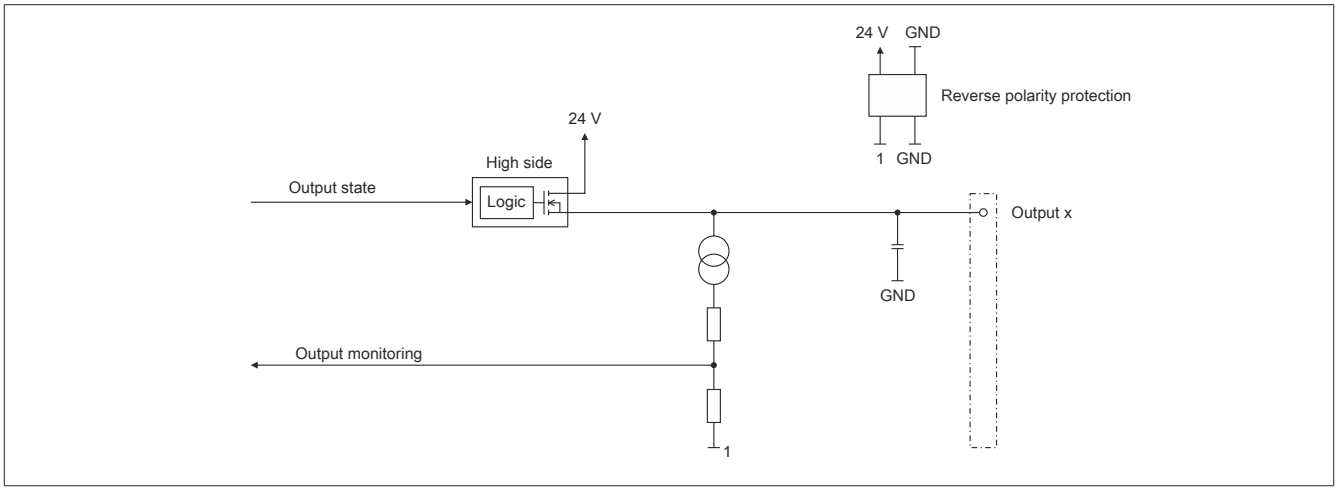


Mixed channel



2.6 Output circuit diagram

Mixed channel



2.7 Mixed channels

The voltage at the digital mixed channels is not permitted to be greater than the supply voltage.

Caution!

Channels 17 to 32 are configured as mixed channels. If one of these channels is being used, it is absolutely essential to ensure that there is no external voltage applied to the I/O channel when the I/O power supply is switched off. Otherwise, power will be regenerated back to the plus terminal of the I/O power supply via the I/O channel. This will result in defective components.

The following solutions are available for preventing power regeneration from occurring:

- **The I/O power supply of the controller is not permitted to be switched off, which allows the reference potential to be maintained.**
- **If the I/O power supply is switched off anyway (e.g. as part of the emergency stop chain), the sensor/actuator power supplies must then also be switched off. This prevents potential power regeneration and protects components from being destroyed.**

2.8 Derating

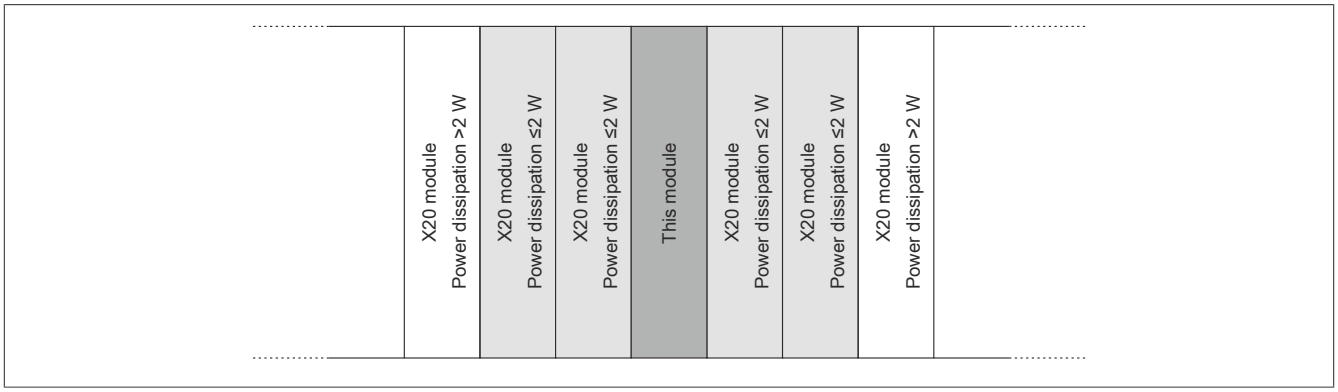
2.8.1 Horizontal mounting orientation

3 derating options are available for the horizontal mounting orientation.

Derating option 1

With a horizontal mounting orientation, derating must be observed starting at an ambient temperature of 55°C.

Starting at 55°C, 2 modules with a maximum power dissipation of 2 W are permitted to be operated next to the module. These modules are marked in light gray in the following image.



Derating option 2

No derating must be observed if the module is supplied with ≤24 VDC.

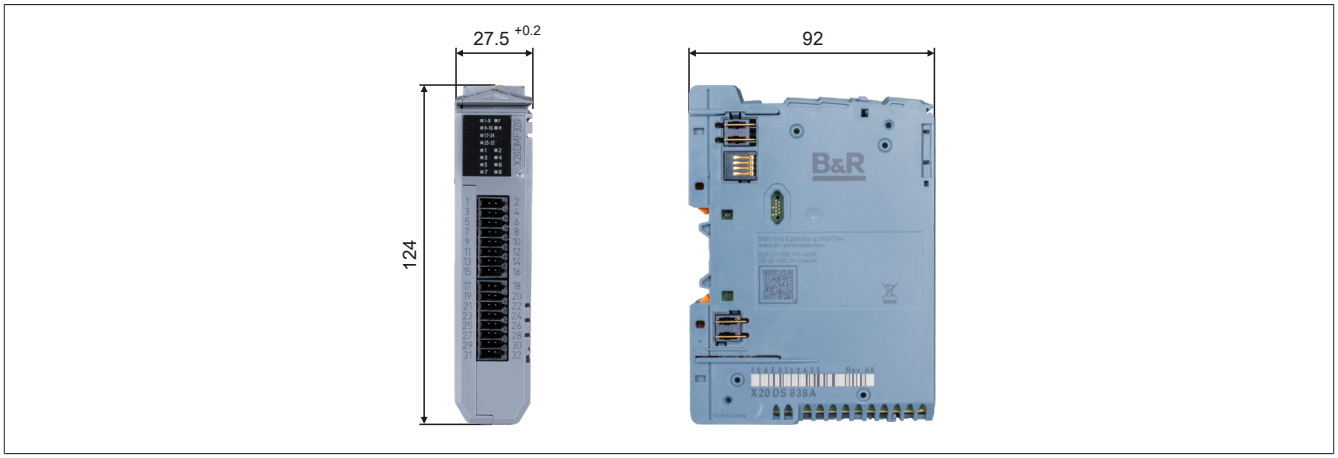
Derating option 3

No derating must be observed if channels 1 to 6 are not used.

2.8.2 Vertical mounting orientation

With a vertical mounting orientation, the maximum ambient temperature is limited to 45°C. No derating must be observed.

2.9 Dimensions



3 Function description

3.1 Digital inputs

The module is equipped with 16 digital input channels and 16 digital mixed channels. By default, the mixed channels are configured as inputs.

3.1.1 Recording the input state

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered state is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering is performed asynchronously to the network in multiples of 100 µs with a network-related jitter of up to 50 µs.

Packed inputs (only function model 0 - Standard)

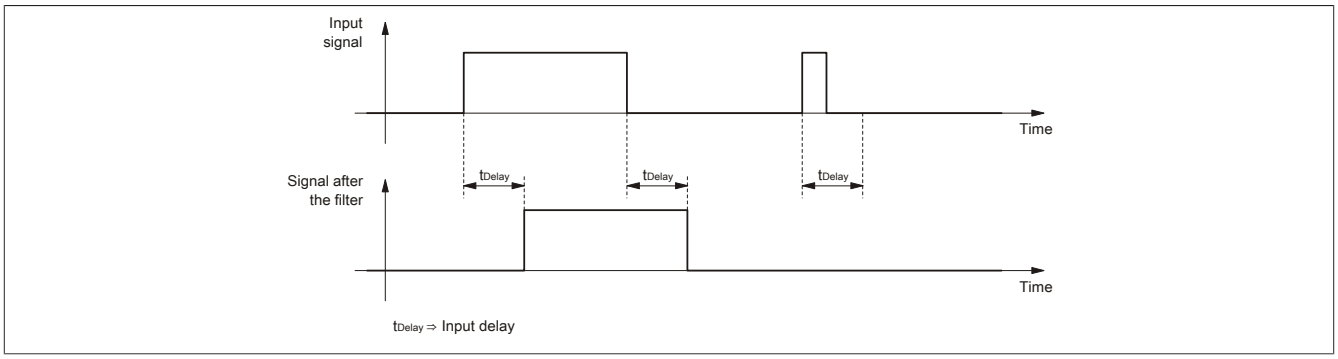
In the Automation Studio I/O configuration, setting "Packed inputs" can be used to determine whether the inputs should be displayed packed or unpacked in the Automation Studio I/O mapping.

Information:

The registers are described in "Digital inputs" on page 25.

3.1.2 Input filter

An input filter is available for each input. Disturbance pulses that are shorter than the input delay are suppressed by the input filter.



The input delay can be set in steps of 100 µs.

Values	Filter
0	No software filter
1	0.1 ms
2	0.2 ms
...	...
250	25 ms - Higher values are limited to this value.

Information:

The register is described in "Digital input filter" on page 25.

3.2 Digital outputs

The module is equipped with 16 digital mixed channels. By default, the mixed channels are configured as inputs. To be able to use one of the channels as an output, it must be defined as an output.

The output state is transferred to the output channels with a fixed offset (<60 µs) in relation to the network cycle (SyncOut).

Packed outputs (only function model 0 - Standard)

In the Automation Studio I/O configuration, setting "Packed outputs" can be used to determine whether the outputs should be displayed packed or unpacked in the Automation Studio I/O mapping.

Information:

The registers are described in "Digital outputs" on page 29.

3.2.1 Outputs with 2 A

Starting with Rev. B1, outputs DO 22 and DO 30 can optionally be operated with a nominal output current of 0.5 or 2 A.

Information:

The register is described in "Configuring an output with 2 A" on page 29.

3.2.2 Monitoring status of the outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read out. A change in the monitoring status is actively transmitted as an error message.

For the PWM outputs, the monitoring status is only calculated in the static state 0 or 100% PWM pulse width.

Supervision status	Description
0	Digital output channel: No error
1	Digital output channel: • Short circuit or overload • Channel switched on and missing I/O power supply • Channel switched off and external voltage applied to channel

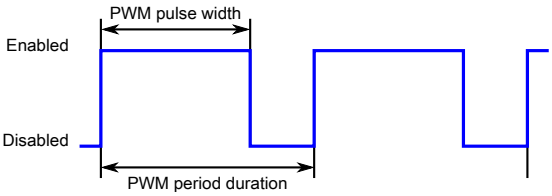
Information:

The registers are described in "Status of the digital outputs" on page 31.

3.3 PWM

The module is equipped with a PWM mode. This can be used to control valves, for example. To prevent the valves from sticking, a dither can be configured exactly according to the specifications of the valve manufacturer.

At the beginning of each period, the output is switched on for the percentage of time set in the PWM pulse width register.



Information:

The registers are described in "Pulse width modulation (PWM)" on page 30.

3.3.1 Dither

When the position setpoint for valves remains constant for a long period of time, especially in fluids, there is a risk that a valve will stick. This is normally prevented using "dithering". When doing so, the value is permitted to slightly oscillate around the position setpoint.

By default, dither is active for all outputs as soon as the following conditions are met:

- Dither amplitude and dither frequency are set to a value greater than 0.
- Pulse width is set to a value greater than 0 and less than 32767.

Dither is enabled or disabled for all outputs together.

3.4 Functions of the high-speed digital inputs/outputs

The module has fast digital inputs/outputs, which can be assigned various functions.

3.4.1 Functions of the high-speed digital inputs

Possible functions

The high-speed digital inputs DI 1 to DI 6 can be configured for the following functions.

Counter/Latch	Counter 1			Counter 2[1)]			Latch
Input	DI 1	DI 3	DI 5	DI 2	DI 4	DI 6	
Event counters	•			•			•
ABR counter	A	B	R	A	B	R	•
Period duration / gate time measurement	•			•			

1) The latch function is only available for counter 1 in "Function model 254 - Bus controller".

Please note

The following points must be taken into account to correctly configure the high-speed digital inputs:

- The counter functions are mutually exclusive. For each input, only one type of counter function can be selected at a time.
- A latch function is available for the event counter and ABR incremental encoder counting functions.

3.4.2 Functions of the high-speed digital outputs

The fast digital outputs DO 19, DO 25 and DO 31 can be configured for pulse width modulation.

3.5 Event counter operation

The edge to detect can be set:

- Rising edge
- Falling edge
- Both edges

The filtering of the input signal can be set:

- Counter inputs filtered using the hardware filter of the counter inputs.
- Counter inputs filtered using the hardware filter and configured software filter of the digital inputs.

The counter value is collected with a fixed offset to the network cycle and transferred in the same cycle.

Information:

The registers are described in "Counter functions" on page 26.

3.6 Period measurement

The time between 2 rising edges of the measurement signal with an internal frequency is recorded. The result is checked for overflow (0xFFFF) and corrected according to the prescaler set. The measurement result is transferred with the next rising edge to the result memory.

The minimum period duration of the measurement signal is 100 µs. This corresponds to a maximum signal frequency of 10 kHz.

Calculating the period measurement

The maximum duration to measure depends on the configured measuring frequency. The higher the measuring frequency, the shorter the measurable period duration.

Formula for converting the counter value into time

$$Time_{ms} = \text{Counter value} * \frac{1000}{\text{Measuring frequency}_{Hz}}$$

Examples

3485 * (1000 / 375000 Hz) = 9.2933 ms

10345 * (1000 / 750000 Hz) = 13.7933 ms

33719 * (1000 / 187500 Hz) = 179.834 ms

55760 * (1000 / 6000000 Hz) = 9.2933 ms

Information:

The registers are described in "Counter functions" on page 26.

3.7 Gate time measurement

The level to measure can be set from the measurement signal:

- High level
- Low level

The time is recorded with an internal frequency.

- High level: From the rising to the falling edge
- Low level: From the falling to the rising edge

The result is checked for overflow (0xFFFF) and corrected according to the prescaler set.

The recovery time between measurements must be greater than 100 µs.

The measurement result is transferred with the falling or rising edge to the result memory.

Calculating the gate time measurement

The maximum duration to measure depends on the configured measuring frequency. The higher the measuring frequency, the shorter the measurable time duration.

Formula for converting the counter value into time

$$Time_{ms} = \text{Counter value} * \frac{1000}{\text{Measuring frequency}_{Hz}}$$

Examples

3485 * (1000 / 375000 Hz) = 9.2933 ms

10345 * (1000 / 750000 Hz) = 13.7933 ms

33719 * (1000 / 187500 Hz) = 179.834 ms

55760 * (1000 / 6000000 Hz) = 9.2933 ms

Information:

The registers are described in "Counter functions" on page 26.

3.8 ABR incremental encoder

The module is equipped with 2 ABR incremental encoders.

3.8.1 General information

Incremental encoders are sensors for detecting position (linear) or angular (rotating) changes that can detect distance and direction of travel or an angular change and direction of rotation.

In contrast to continuously operating measuring systems such as servo-potentiometers, incremental encoders have a measurement scale with repeating periodic graduation lines. The measurement is based on the determined direction and a count. Rotating optical encoders are the most commonly used.

Incremental encoders (in contrast to absolute encoders) may need to be homed after switching on since changes in position are not detected when in the switched-off state.

Typical applications are determining position and speed in automation technology.

3.8.2 Signal evaluation

When a movement is performed, the two sensors emit 2 signals (A and B) with an electrical phase shift of 90°.

The module determines the direction from these 2 signals and counts the pulses. This allows direct conclusions to be drawn about the scale of measurement (path or angle).

3.8.3 Referencing

After switching on the power supply, the incremental encoder only measures changes compared to the switch-on position. For many applications however, knowledge of the absolute position is required. For this reason, most angular encoders output a reference pulse (zero pulse, reference mark) once per revolution on a third output (reference signal R). After switching on, the encoder must be rotated until the reference pulse has been detected. The absolute angle is then available after one revolution at the latest.

Positioning systems with incremental encoders perform "homing procedures" to an external position sensor (e.g. limit switch) after switching on. From this point, the next reference pulse of the incremental encoder is used as an accurate reference point.

3.8.4 Recording the counter value

The counter value of the incremental encoder is displayed as a 16-bit counter value. The counter value can be reset if necessary. The counter is held at zero until the reset command is canceled.

Information:

The registers are described in "Counter functions" on page 26.

3.9 Latch function

If required, the current counter values can be latched. It is important to note the following:

- The latch function is available for the event counter and ABR incremental encoder counter functions.
- The latch function is only available for counter 1 in "Function model 254 - Bus controller".

To use the latch function, the latch mode and the signal channels for triggering the latch procedure must be configured:

Latch mode

- Single shot latch mode:
  The latch function must be enabled/set. After successful latching, which is indicated by the latch event counter, enabling must first be reset or no further latching is possible. If additional latching is desired, enabling must be set again.
- Configuring continuous latch mode:
  The latch function must only be enabled/set as long as latching is desired. The latch event counter counts each time the defined event occurs.

Signal channels

- This configuration determines which channels are linked to create the latch event. All 3 signals of the encoder can be used for the "AND" link.
- To adapt to the physical signals, the "active voltage level" required for the latch procedure can be defined as "High" or "Low".

Information:

The register is described in "Latch event configuration" on page 27.

4 Commissioning

4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

4.1.1 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

5 Register description

5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

5.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
18	CfgInputFilter	USINT				•
20	CfgDiDoMode	UINT				•
22	CfgCurrentMode	USINT				•
25	CfgPwmEnable	USINT				•
26	CfgDitherFrequency	USINT				•
28	CfgDitherAmplitude	USINT				•
40	CfgCounterMode01	USINT				•
42	CfgCounterMode02	USINT				•
52	CfgCounterLatch01	UINT				•
54	CfgCounterLatch02	UINT				•
Output data						
4	DigitalOutput17_24	USINT			•	
	DigitalOutput17	Bit 0				
	...	...				
	DigitalOutput24	Bit 7				
5	DigitalOutput25_32	USINT			•	
	DigitalOutput25	Bit 0				
	...	...				
	DigitalOutput32	Bit 7				
6	PWMOutput19	INT			•	
8	PWMOutput25	INT			•	
10	PWMOutput31	INT			•	
12	PWMPeriod	UINT			•	
19	Counters	USINT			•	
	ResetCounter01	Bit 0				
	ResetCounter02	Bit 1				
	LatchEnable01	Bit 2				
	LatchEnable02	Bit 3				
Input data						
0	DigitalInput01_08	USINT	•			
1	DigitalInput09_16	USINT	•			
2	DigitalInput17_24	USINT	•			
3	DigitalInput25_32	USINT	•			
14	Counter01	UINT / INT	•			
16	Counter02	UINT / INT	•			
30	DigitalOutputStatus17_24	USINT	•			
	StatusDigitalOutput17	Bit 0				
	...	...				
	StatusDigitalOutput24	Bit 7				
31	DigitalOutputStatus25_32	USINT	•			
	StatusDigitalOutput25	Bit 0				
	...	...				
	StatusDigitalOutput32	Bit 7				
44	LatchValue01	UINT / INT	•			
46	LatchValue02	UINT / INT	•			
48	LatchCount01	UINT	•			
50	LatchCount02	UINT	•			
60	DigitalInput01_16	UINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput16	Bit 15				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
62	DigitalInput17_32	UINT	•			
	DigitalInput17	Bit 0				
	...	...				
	DigitalInput32	Bit 15				

5.3 Function model 254 - Bus controller

Register	Offset	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
18	-	CfgInputFilter	USINT				•
20	-	CfgDiDoMode	UINT				•
22	-	CfgCurrentMode	USINT				•
25	-	CfgPwmEnable	USINT				•
26	-	CfgDitherFrequency	USINT				•
28	-	CfgDitherAmplitude	USINT				•
40	-	CfgCounterMode01	USINT				•
42	-	CfgCounterMode02	USINT				•
52	-	CfgCounterLatch01	UINT				•
Output data							
4	0	DigitalOutput17_24	USINT			•	
		DigitalOutput17	Bit 0				
		...	...				
		DigitalOutput24	Bit 7				
5	2	DigitalOutput25_32	USINT			•	
		DigitalOutput25	Bit 0				
		...	...				
		DigitalOutput32	Bit 7				
6	4	PWMOutput19	INT			•	
8	6	PWMOutput25	INT			•	
10	8	PWMOutput31	INT			•	
12	10	PWMPeriod	UINT			•	
19	12	Counters	USINT			•	
		ResetCounter01	Bit 0				
		ResetCounter02	Bit 1				
		LatchEnable01	Bit 2				
Input data							
14	8	Counter01	UINT / INT	•			
16	14	Counter02	UINT / INT	•			
30	4	DigitalOutputStatus17_24	USINT	•			
		StatusDigitalOutput17	Bit 0				
		...	...				
		StatusDigitalOutput24	Bit 7				
31	6	DigitalOutputStatus25_32	USINT	•			
		StatusDigitalOutput25	Bit 0				
		...	...				
		StatusDigitalOutput32	Bit 7				
44	10	LatchValue01	UINT / INT	•			
48	12	LatchCount01	UINT	•			
60	0	Input state of digital inputs 1 to 16	UINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput16	Bit 15				
62	2	Input state of digital inputs 17 to 32	UINT	•			
		DigitalInput17	Bit 0				
		...	...				
		DigitalInput32	Bit 15				

5.4 Digital inputs

5.4.1 Digital input filter

Name:
CfgInputFilter

The filter value for all digital inputs can be configured in this register.

Data type	Values	Filter
USINT	0	No software filter (bus controller default setting)
	1	0.1 ms
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value.

5.4.2 Input states of the digital inputs

There are several ways to read out the states of digital inputs. The following table contains an overview of the registers, in which function model they are available and whether the inputs are packed or unpacked. The data type and the range of values are specified in additional columns.

Register	Function model 0 Standard	Function model 254 Bus controller	Inputs packed	Data type	Values
DigitalInput01_08	•		Yes	USINT	0 to 255
DigitalInput09_16	•		Yes	USINT	0 to 255
DigitalInput17_24	•		Yes	USINT	0 to 255
DigitalInput25_32	•		Yes	USINT	0 to 255
DigitalInput01_16	•		Yes	UINT	0 to 65535
DigitalInput17_32	•		Yes	UINT	0 to 65535
DigitalInput01	•	•	No	BOOL	See Unpacked inputs.
...					
DigitalInput32					

Packed inputs

In function model 0 - Standard, the inputs can be packed (Automation Studio I/O configuration - setting "Packed inputs = On"). The registers, data type and values are shown in the table above.

Unpacked inputs

In the following cases, the inputs are assigned as individual bits in the Automation Studio I/O mapping as data points ("DigitalInput01" to "DigitalInput32"):

- Function model 0 - Standard is set, and the inputs are not packed (Automation Studio I/O configuration - setting "Packed inputs = Off").
- The function model 254 - "Bus controller" is set.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...	...	...	...
15	DigitalInput16	0 or 1	Input state - Digital input 16

Bit	Name	Value	Information
0	DigitalInput17	0 or 1	Input state - Digital input 17
...	...	...	...
15	DigitalInput32	0 or 1	Input state - Digital input 32

5.5 Counter functions

5.5.1 Configuring the counter function

Name:
CfgCounterMode01 to CfgCounterMode02

These registers are used to configure the counters.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	0 Counter function: • Event counters • Counting inputs via hardware filter • Evaluation of the rising edge

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0 - 3	Gate time or period measurement: Setting the counting frequency Event counter: Bits 0 and 1 are used to set the filtering of the input signal.	0	Gate time or period measurement: Counter frequency = 48 MHz Event counter (bus controller default setting): Counter inputs filtered using the hardware filter of the counter inputs.
		1	Gate time or period measurement: Counter frequency = 3 MHz Event counter: Counter inputs filtered using the hardware filter and configured software filter of the digital inputs.
		2	187.5 kHz
		3	24 MHz
		4	12 MHz
		5	6 MHz
		6	1.5 MHz
		7	750 kHz
		8	375 kHz
		9 - 15	Reserved
4 - 5	Gate time measurement: The level to be measured is set from the measurement signal. Event counter: Edge selection	00	Gate time measurement: High level of the measurement signal Event counter: Rising edge (bus controller default setting)
		01	Gate time measurement: Low level of the measurement signal Event counter: Falling edge
		10	Event counter: Both edges
		11	Reserved
6 - 7	Counter function	00	Event counter (bus controller default setting)
		01	Gate time measurement
		10	Period measurement
		11	AB(R) counter

5.5.2 Latch event configuration

Name:
CfgCounterLatch01 to CfgCounterLatch02

These registers define the signal channels and their level for triggering the latch procedure. For details, see "Latch function" on page 20.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Input A high level	0	Disabled
		1	Enabled
1	Input B high level	0	Disabled
		1	Enabled
2	Input R high level	0	Disabled
		1	Enabled
3	Reserved	0	
4	Input A low level	0	Disabled
		1	Enabled
5	Input B low level	0	Disabled
		1	Enabled
6	Input R low level	0	Disabled
		1	Enabled
7	Reserved	0	
8 - 15	Latch mode of the counter	0	Single shot
		1	Continuous
		2 to 254	Reserved
		255	Disabled

5.5.3 Counter value

Name:
Counter01 to Counter02

The current counter values are saved in these registers.

Data type	Values	Information
UINT	0 to 65535	Applies to the following counter functions: • Event counters • Gate time measurement • Period measurement
INT	-32768 to 32767	Applies to AB or ABR counters

5.5.4 Clear counter value and enable/disable latch function

Name:
ResetCounter01
ResetCounter02
LatchEnable01
LatchEnable02

This register is used to clear the counter value with the corresponding bit or to start latching.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	ResetCounter01	0	Do not clear the counter value
		1	Clear the counter value
1	ResetCounter02	0	Do not clear the counter value
		1	Clear the counter value
2	LatchEnable01	0	Do not latch the counter value
		1	Latch the counter value
3	LatchEnable02	0	Do not latch the counter value
		1	Latch the counter value
4 - 7	Reserved	0	

5.5.5 Latched counter value

Name:
LatchValue01 to LatchValue02

As soon as the latch conditions have been met, the contents of the respective counter value are copied to these registers.

Data type	Values	Information
UINT	0 to 65535	Applies to the following counter functions: • Event counters • Gate time measurement • Period measurement
INT	-32768 to 32767	Applies to AB or ABR counters

5.5.6 Number of latch events

Name:
LatchCount01 to LatchCount02

The number of latch events that have occurred is stored in these registers. This allows detection of whether a new latched counter value has been saved.

Data type	Values	Information
UINT	0 to 65535	Number of latch events

5.6 Digital outputs

5.6.1 Configuring a mixed channel as an output

Name:
CfgDiDoMode

This register is used to configure a mixed channel as an output.

Data type	Values	Bus controller default setting[1)]
UINT	See the bit structure.	65535

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput17	0	Disabled
		1	Enabled (bus controller default setting)
...	...	...	...
15	DigitalOutput32	0	Disabled
		1	Enabled (bus controller default setting)

5.6.2 Configuring an output with 2 A

Name:
CfgCurrentMode

Starting with Rev. B1, outputs DO 22 and DO 30 can optionally be operated with a nominal output current of 0.5 or 2 A. The setting is made using this register.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	0

1) The bus controller default setting value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Description	Value	Information
0	DigitalOutput22	0	Nominal output current 0.5 A (bus controller default setting)
		1	Nominal output current 2 A
1	DigitalOutput30	0	Nominal output current 0.5 A (bus controller default setting)
		1	Nominal output current 2 A
2 - 7	Reserved	0	

5.6.3 Switching state of the digital outputs

Name:
DigitalOutput17_24 to DigitalOutput25_32
DigitalOutput17 to DigitalOutput32

This register stores the switching state of digital outputs 17 to 32. The channels must be declared as outputs using register CfgDiDoMode.

Data type	Values	Information[1)]
USINT	0 to 255	Packed outputs = On Data points: "DigitalOutput17_24" and "DigitalOutput25_32"
BOOL	See the bit structure.	Packed outputs = Off or function model ≠ 0 - Standard. Data points: "DigitalOutput17" to "DigitalOutput32"

1) See "Digital outputs" on page 14.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput17	0	Digital output 17 reset
		1	Digital output 17 set
...	...	...	...
7	DigitalOutput24	0	Digital output 24 reset
		1	Digital output 24 set

Bit	Name	Value	Information
0	DigitalOutput25	0	Digital output 25 reset
		1	Digital output 25 set
...	...	...	...
7	DigitalOutput32	0	Digital output 32 reset
		1	Digital output 32 set

5.7 Pulse width modulation (PWM)

3 outputs of the module can be configured as PWM outputs.

5.7.1 Dither frequency

Name:
CfgDitherFrequency

The dither frequency for the PWM outputs is configured in this register.

Data type	Values	Information
USINT	0	Dither switched off
	1 to 250	Dither frequency in Hz

5.7.2 Dither amplitude

Name:
CfgDitherAmplitude

The dither amplitude for the PWM outputs is configured in this register.

Data type	Values	Information
USINT	0	Dither switched off
	1 to 25	Corresponds to 1 to 25% of the PWM period duration

5.7.3 Period duration

Name:
PWMPeriod

In this register, the PWM period duration is specified in microseconds.

Data type	Values	Information
UINT	0	PWM disabled
	1000 to 65535	Period duration in microseconds

5.7.4 Pulse width

Name:
PWMOutput19, PWMOutput25, PWMOutput31

The PWM pulse width is specified in % of the period duration in these registers. At the beginning of each period, the output is switched on for the percentage of time set in this register.

For a detailed description of the pulse width, see "PWM" on page 15.

Data type	Values	Information
INT	0 to 32767	Corresponds to 0 to 100% of the period duration

5.7.5 Enabling the PWM function

Name:
CfgPwmEnable

This register is used to enable the PWM function for the corresponding outputs. The channels must be declared as outputs using register CfgDiDoMode.

Data type	Values	Bus controller default setting[1)]
USINT	See the bit structure.	7

1) The bus controller default value applies only to the register numbers specified in function model 254.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput19	0	PWM function disabled
		1	PWM function enabled (bus controller default setting)
1	DigitalOutput25	0	PWM function disabled
		1	PWM function enabled (bus controller default setting)
2	DigitalOutput31	0	PWM function disabled
		1	PWM function enabled (bus controller default setting)
3 - 7	Reserved	0	

5.8 Status of the digital outputs

Name:
DigitalOutputStatus17_24 to DigitalOutputStatus25_32
StatusDigitalOutput17 to StatusDigitalOutput32

This register contains the state of digital outputs 17 to 32.

Data type	Values	Information[1)]
USINT	0 to 255	Packed outputs = On Data points: "DigitalOutputStatus17_24" and "DigitalOutputStatus25_32"
BOOL	See the bit structure.	Packed outputs = Off or function model ≠ 0 - Standard. Data points: "StatusDigitalOutput17" to "StatusDigitalOutput32"

1) See "Digital outputs" on page 14.

Bit structure:

Bit	Name	Value	Description
0	StatusDigitalOutput17	0	Channel 17: No error
		1	Channel 17: • Short circuit or overload • Channel switched on and missing I/O power supply • Channel switched off and external voltage applied to channel
...	...	...	...
7	StatusDigitalOutput24	0	Channel 24: No error
		1	Channel 24: For an error description, see channel 17.

Bit	Name	Value	Information
0	StatusDigitalOutput25	0	Channel 25: No error
		1	Channel 25: • Short circuit or overload • Channel switched on and missing I/O power supply • Channel switched off and external voltage applied to channel
...	...	...	...
7	StatusDigitalOutput32	0	Channel 32: No error
		1	Channel 32: For an error description, see channel 25.

Information:

For the PWM outputs, the monitoring status is only calculated in the static state 0 or 100% PWM pulse width.

5.9 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Without input filter and without counter functions	200 µs
With input filter or counter functions	250 µs
With input filter and counter functions	300 µs

5.10 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
Equal to the minimum cycle time