PCI1003 PMIC Power Board User Guide

EV69K72A

Introduction

The PCI1003 PMIC Power Board is designed to simplify the evaluation and testing of the PCI1003 Switch's power requirements. It integrates the MCP16701/A PMIC to provide the necessary rails for the PCI1003 Switch and uses an MCP16363 buck converter as a frontend to expand the input voltage range from 5V to 48V (limited to typically 12V because of the passive component ratings).

The MCP16701 and MCP16701A are Power Management Integrated Circuits (PMICs) designed for high-performance, high-accuracy power delivery for FPGA, high-end MPU and PCI-Express Switch applications. Both devices are functionally identical for the purposes of this board, with the only difference being the configuration: the MCP16701A comes factory programmed specifically for the PCI1003, while the MCP16701 comes unprogrammed and it is custom programed when the board is assembled.

The MCP16701/A integrates eight parallelable DC-DC buck regulators, four auxiliary LDOs and one low-input/low-output voltage LDO Controller that uses an external MOSFET.

The buck channels support loads up to 1.5A. All low-voltage bucks are 100% duty cycle capable. They can be operated either independently or paralleled in groups of four to support higher currents.

Four 300 mA LDOs are provided to support sensitive analog loads. The LDOs can also be cascaded (in groups of two) to the output of a DC-DC channel, thus improving overall conversion efficiency.

The MCP16701/A power management settings allow for the implementation of low-power mode commanded by a GPIO pin (MODE input of MCP16701). Any channel can also be selectively and permanently set in Auto PFM or FPWM.

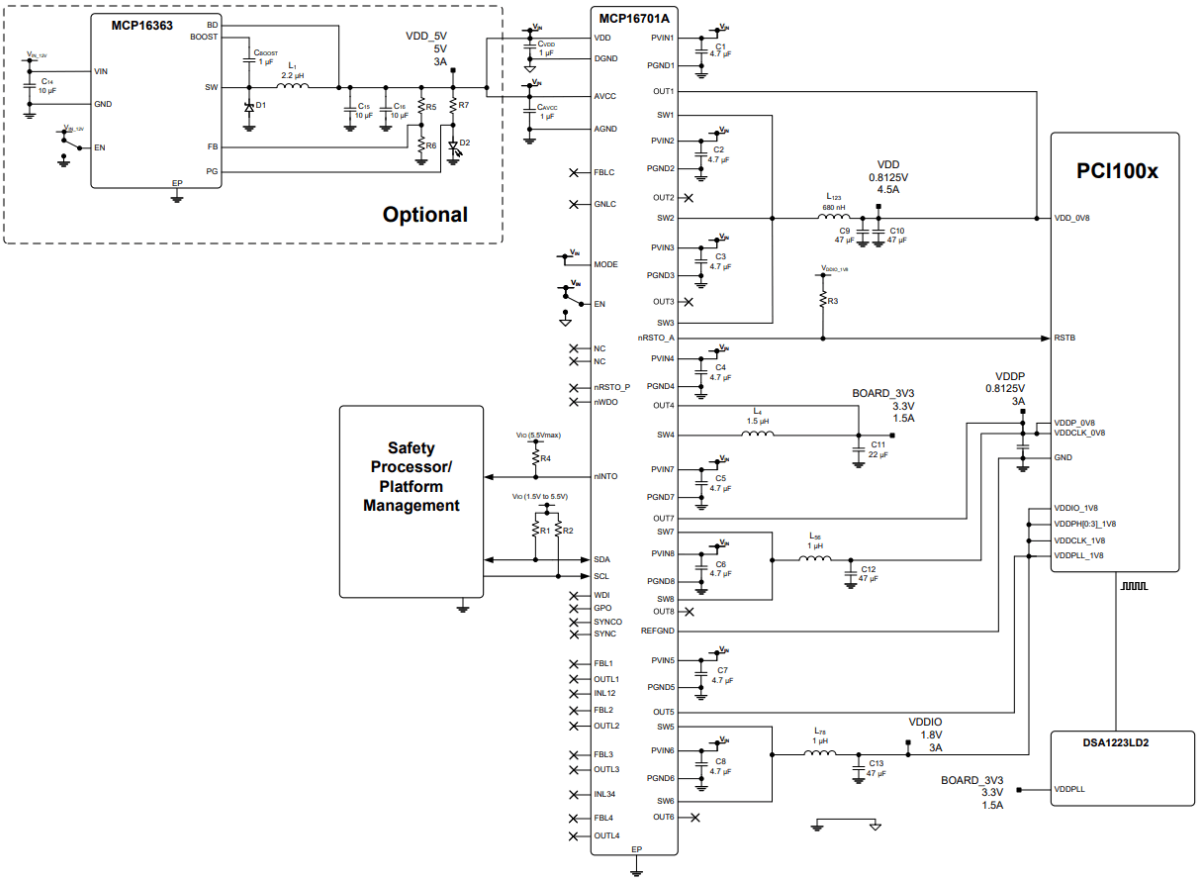
Active discharge resistors are provided on each output. All Buck channels and LDOs support soft start-up.

The PMIC supports advanced power sequencing, soft start-up, active discharge resistors, and programmable thermal and fault management. It is suitable for powering multi-rail systems such as MPU, network switches and FPGAs, with flexible configuration via a GUI or direct I2C commands.

The MCP16701/A is available in a 64-pin, 8 mm x 8 mm VQFN package with an operating junction temperature range from -40°C to +105°C.

For a full list of features and registry configuration for the MCP16701A, please see the MCP16701/A Datasheet.

Figure 1. Typical Application With MCP16701A and Buck Frontend for Powering PCI100x



Board Features

The PCI1003 PMIC Power Board (EV69K72A) has the following features:

- Input Voltage Range: 12V Nominal (13V Maximum)
- Output Rails:
  - VDDAUX: 3.3V, 1.5A
  - VDDIO: 1.8V, 3A
  - VDDP_0V8: 0.8125V, 3A
  - VDD_0V8: 0.8125V, 4.5A
  - VDD5V_PMIC: 5V, 3A (Intermediate Rail)
- Sequenced Startup for Proper Power-up of the PCI1003 Switch
- 2.33 MHz Switching Frequency (MCP16701A PMIC Rails, Forced PWM Mode)
- 2.2 MHz Switching Frequency (MCP16363 Rail, With Dithering for Improved EMI)
- Fault Management via nRSTO and nINTO Pins With LED Indicators
- Thermal and Overcurrent Protection for Both Power Devices
- Reverse Battery and Overvoltage Protection

Note: The PCI1003 PMIC Power Board (EV69K72A), supports both MCP16701 and MCP16701A PMICs.

Integration:

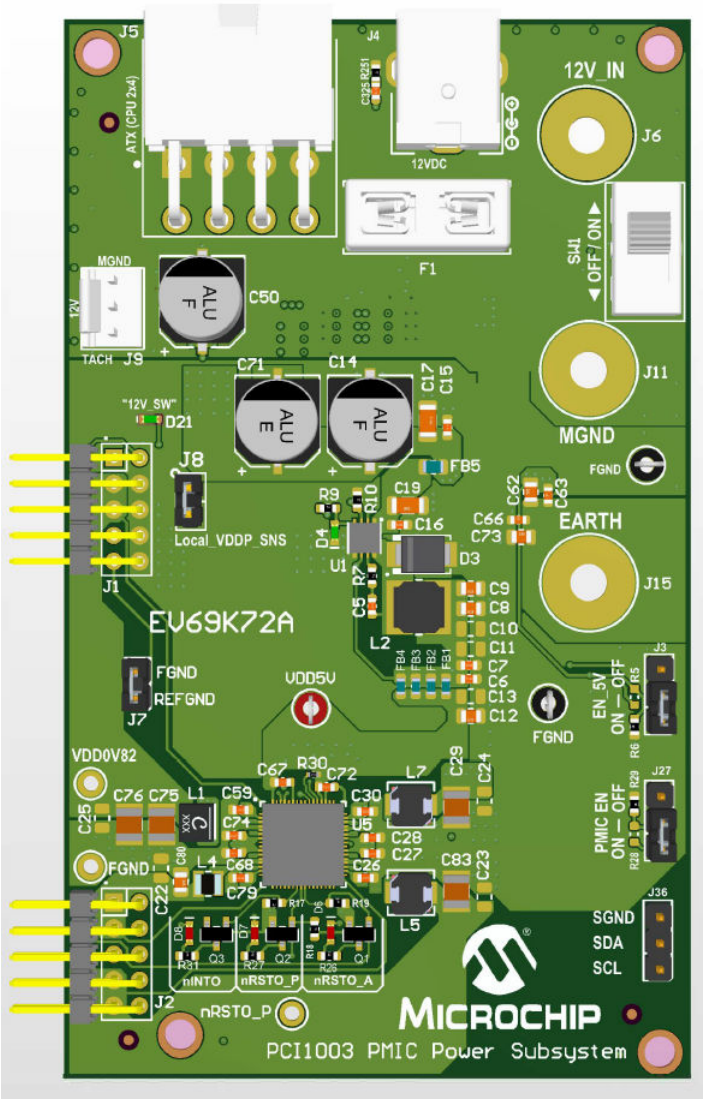
The board is intended for use with the EVB-PCI1003 Rev. D Evaluation Kit, providing all required power rails and protection features for reliable operation in commercial and industrial applications.

Kit Contents

The PCI1003 PMIC Power Board (EV69K72A) kit includes:

- PCI1003 PMIC Power Board (Fully Assembled and Tested)
- Important Information Sheet
- Accessories (Connectors, Jumpers, etc.)

Figure 2. PCI1003 PMIC Power Board (EV69K72A)

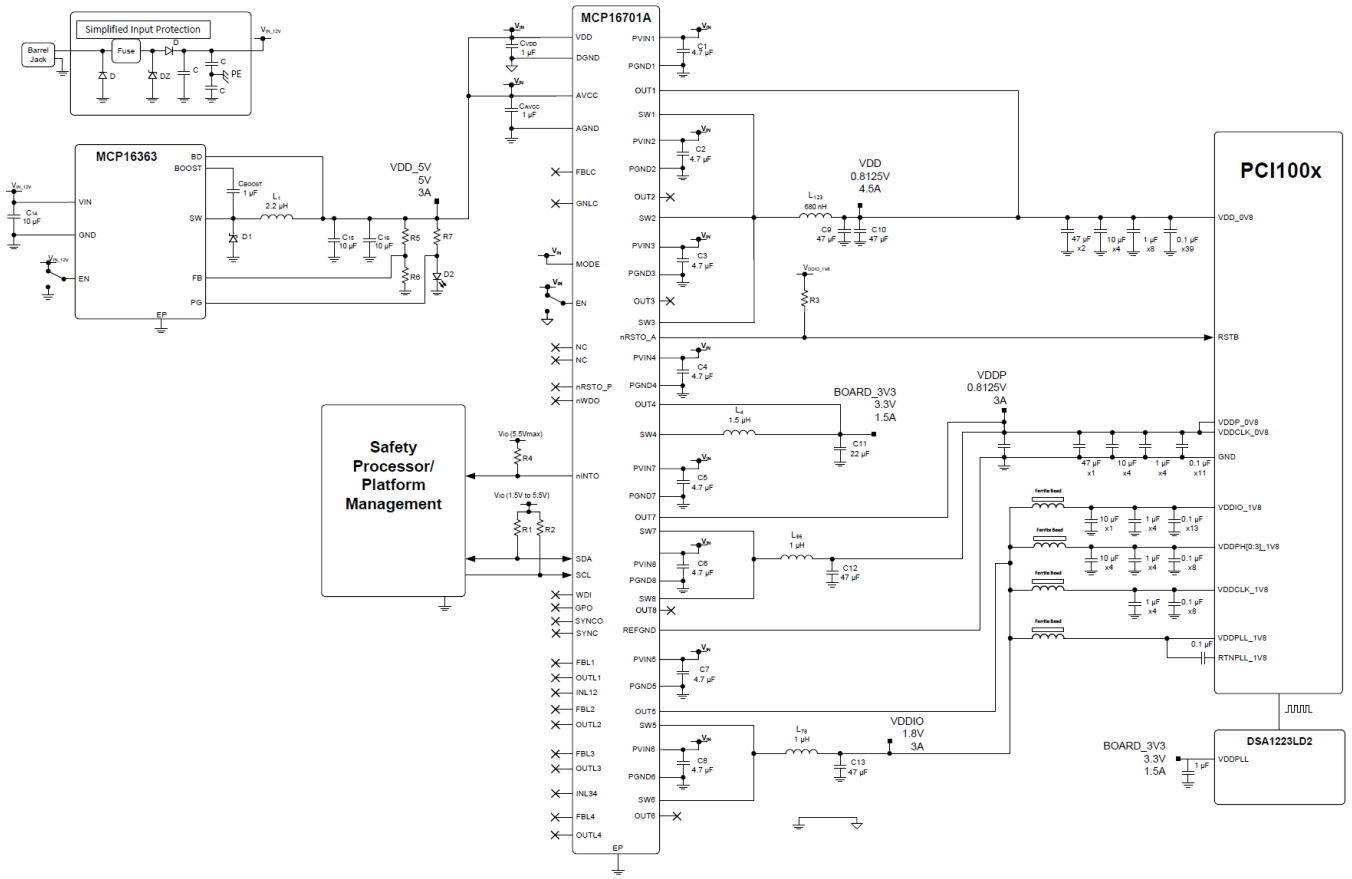


1. Installation and Operation

1.1. Introduction

This section provides instructions for installing and operating the PCI1003 PMIC Power Board (EV69K72A). The board is designed to deliver sequenced, protected power rails to the PCI1003 Switch and is intended for use with the EVB-PCI1003 Rev. D Evaluation Kit. It can also be used as a standalone board, by populating the appropriate jumpers. The following sections describe the board's features, initial setup, layout considerations and circuit description.

Figure 1-1. PCI1003 PMIC Power Board (EV69K72A) Simplified Schematic



1.2. Features

The PCI1003 PMIC Power Board offers the following features:

- **Input Voltage Range:**
  - 12V typical (13V maximum), expanded by MCP16363 front-end buck converter
- **High Accuracy Output Voltages:**
  - VDDAUX: 3.3V, 1.5A
  - VDDIO: 1.8V, 3A
  - VDDP_0V8: 0.8125V, 3A
  - VDD_0V8: 0.8125V, 4.5A
  - VDD5V_PMIC: 5V, 3A (Intermediate Rail)

- **Sequenced Rails Startup:** Ensures proper power-up of the PCI1003 Switch
- **Switching Frequency:**
  - 2.33 MHz forced PWM mode for MCP16701A PMIC rails (low-ripple output)
  - 2.2 MHz for MCP16363 rail with dithering for improved EMI
- **Fault Management:**
  - nRSTO and nINTO pins with LED indicators
  - Global and user-defined RESET with programmable de-assertion delay
- **Thermal Protection:**
  - Programmable thermal early warning and thermal shutdown for both power devices
- **Overcurrent Protection:**
  - Hiccup-mode current limit for buck channels (can be disabled)
  - Overcurrent protection for both power devices
- **Reverse Battery and Overvoltage Protection:**
  - Safeguards against incorrect supply connections
- **On-Die Programmable NVM:**
  - NVM write password protection (e.g., voltage setting)
  - Reconfigurable during runtime
- **I2C Interface:**
  - 3.4 MHz I2C interface for configuration and monitoring
  - Compatible with I2C Monitor GUI when using the MCP2221A Breakout Board USB C (BB62Z76A)
- **Test Points and Headers:**
  - For all available outputs and input
  - Ease of access to all digital signals
- **LED Visual Indicators:**
  - For fault and status monitoring
- **Board Compatibility:**
  - Fully assembled and tested for use with EVB-PCI1003 Rev. D Evaluation Kit

1.3. Getting Started

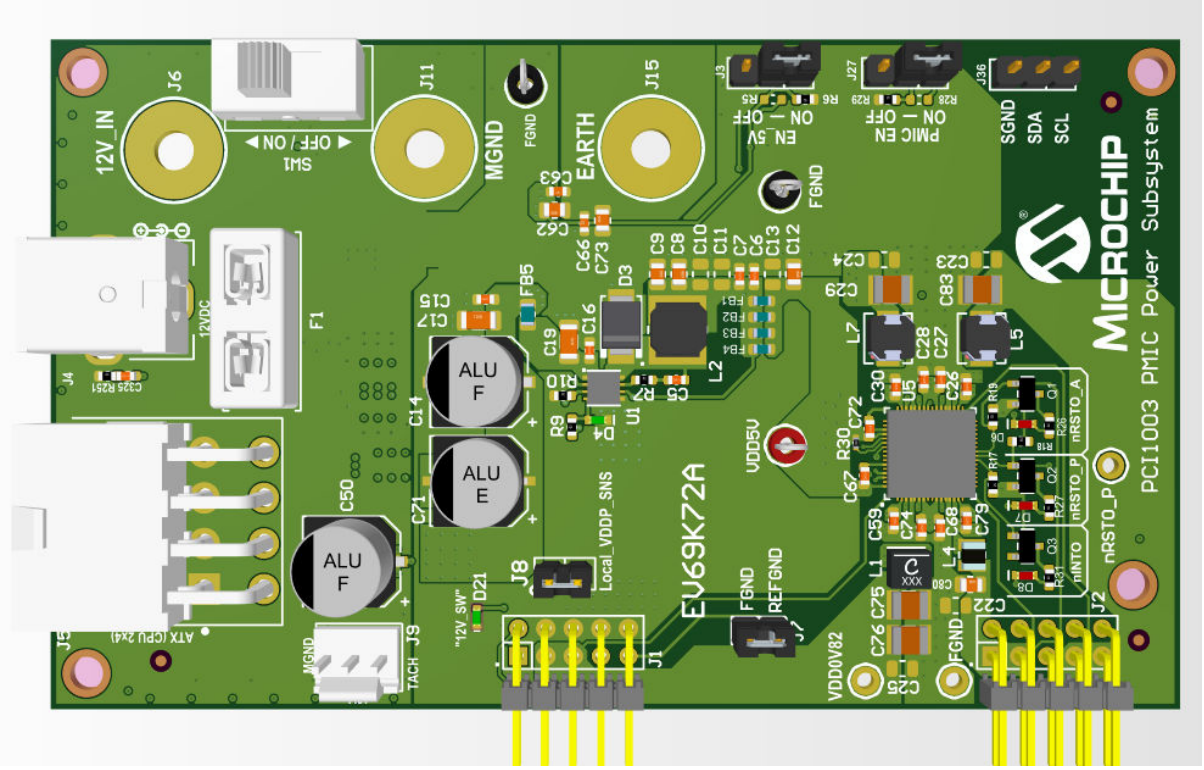
The PCI1003 PMIC Power Board is fully assembled and tested. To begin evaluation, follow these steps:

1.3.1. Power Input and Output Connections

1. Connect a power supply to the input terminals (recommended 12V, up to 13V maximum). Ensure that the supply can deliver sufficient current for the intended load. The power supply should have a power output of at least 20W to allow the PCI1003 PMIC Power Board to perform at full load.

   Connect the 12V power supply to the barrel jack (J4), or use the terminal block by connecting the positive wire to 12V_IN and the negative wire to MGND.

Figure 1-2. PCI1003 PMIC Power Board (EV69K72A) Connections



2. Connect the output rails to the EVB-PCI1003 Rev. D Evaluation Kit or other target system. The board provides the following rails:

Table 1-1. Rail Configuration

Rail	Voltage	Maximum Current	Connection
VDDAUX	3.3V	1.5A	J2 pins 1+3
VDDIO	1.8V	3A	J2 pins 7+9
VDDP_0V8	0.8125V	3A	J1 pin 1
VDD_0V8	0.8125V	4.5A	J1 pins 3+5
VDD5V_PMIC	5V	3A	TP2 (VDD5V)

Note: All voltage measurements shall be made in reference to **FGND** (J1 pins 4+6+8+10 or J2 pins 2+4+6+8+10).

3. If desired, connect an ammeter between the input supply and the board to monitor current consumption.
   Note: If the PMIC Power Board is tested stand-alone (without PCI1003 board) then external loads can be connected via J1 and J2 output pins with J7 (Local REFGND sense) and J8 (Local VDDP sense) jumpers that must be present. Power resistors or electronic loads can be used but take care to enable the electronic load after powering the board. Please take care not to exceed the maximum current output for each rail.
4. Keep the power supply disabled until all connections are made.
5. Configure the jumper connections on the board: Set jumpers J3 and J27 to the ON position. For local use (stand-alone, without the EVB-PCI1003 board) please set jumpers J7 and J8. When using together with the EVB-PCI1003 board, please remove jumpers J7 and J8 for best performance.
6. Enable the power supply input, by setting the SW1 switch to the ON position, then verify that the board powers up and the output rails are within specification. LED D4 will be ON signaling the 5V Buck frontend is functioning correctly. If LED D4 is OFF, please check the input power

supply connections, check that LED D21 is ON and measure the input voltage to be over the 11V minimum. After the PMIC completes the start-up sequence, under normal operation, the LEDs signaling nINTO, nRSTO_A and nRSTO_P must be all OFF.

Note: By default, the board is preconfigured with the correct registry settings, with the Buck regulators enabled and LDOs disabled.

1.3.2. Fault Management

The board features fault management through nRSTO and nINTO pins, with LED indicators for visual status. In case of overcurrent, overvoltage, or thermal fault, the board will signal the fault and may shut down affected rails to protect the system.

1.3.3. Layout Considerations

The MCP16701/A PMIC requires at least 25 vias from the ICs Exposed Pad to the ground (GND) plane to dissipate the generated heat. The size of the GND plane can be increased or decreased based on the ambient temperature, air flow or other devices that generate heat. As a rule of thumb, the GND plane should be as large as possible. The MCP16701/A also features Power Ground (PGND) pins that must be connected to the power components (power input and output capacitors) and to a low-impedance return path, such as a dedicated plane or copper pour. It is also recommended to connect the input and output capacitors GND connections, as well as the PGND pins on the same layer (thus, avoiding via inductance) and the same continuous copper plane for optimal performance.

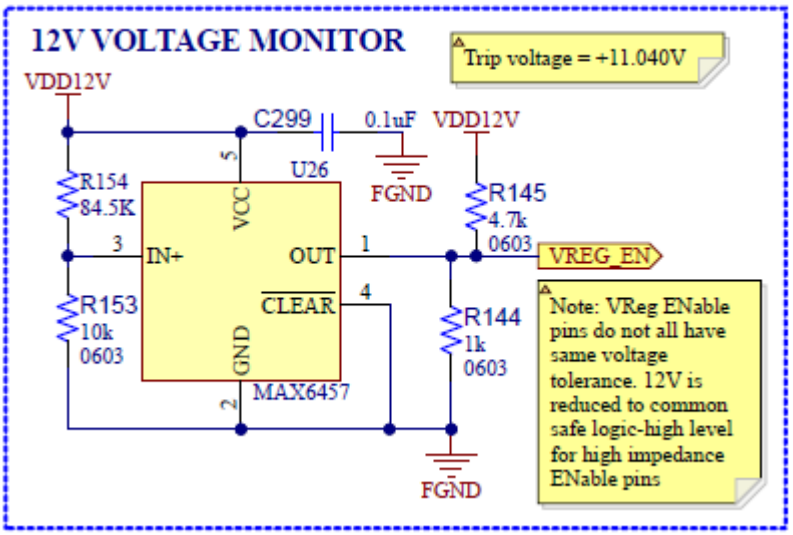
For low Electromagnetic Interference (EMI) emissions, routing the switching node of the Buck regulators on an internal plane is recommended, surrounded or enclosed by input supply voltage distribution or GND planes. The REFGND is a reference to all the regulators and gives better performance to the rail that it is tied close to, but the others have a slight disadvantage. The high current core rail is the most important; it is recommended that the REFGND go directly to the core supply GND.

Proper PCB layout is essential for optimal performance of the PCI1003 PMIC Power Board. Consider the following guidelines:

- Minimize the length and resistance of power traces to reduce voltage drop and improve efficiency.
- Place input and output capacitors as close as possible to the PMIC and buck converter ICs.
- Use wide copper pours for power and ground connections to improve current handling and thermal performance.
- Ensure adequate thermal vias and copper area for heat dissipation, especially under the PMIC and buck converter.
- Follow best practices for EMI reduction, including proper grounding and shielding where necessary.

1.3.4. The 12V Voltage Monitor Block

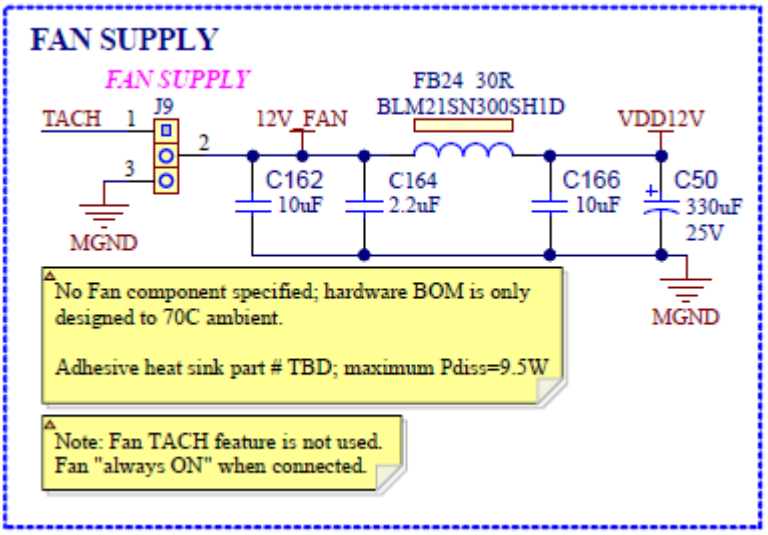
The 12V Voltage Monitor block is responsible for continuously monitoring the main 12V supply (VDD12V) on the PCI1003 PMIC Power Board. It uses a voltage monitor IC, which is configured to detect when the 12V rail drops below a specific threshold (trip voltage set at approximately 11.04V). If the voltage falls below this level, the output of the monitoring IC changes state, which will disable the 5V Buck regulator. The output (VREG_EN) is used to enable or disable the 5V Buck frontend regulator.



1.3.5. Fan Supply

The Fan Supply block provides a dedicated, filtered 12V power rail for an external cooling fan. The 12V_FAN output is routed through a ferrite bead (FB24) and shunted by several capacitors (C162, C164, C166, C50) to filter out noise and provide stable supply voltage. This design helps maintain reliable fan operation and reduces electrical noise that could affect other parts of the board.

The fan connector (J9) includes a TACH pin for fan speed monitoring, but this feature is not used in the current design. The fan is always powered ON when connected, ensuring continuous cooling. The hardware is specified to operate at ambient temperatures up to 70°C, and the maximum power dissipation for the system is 9.5W. The specific fan component and adhesive heat sink part will be determined based on final system requirements.

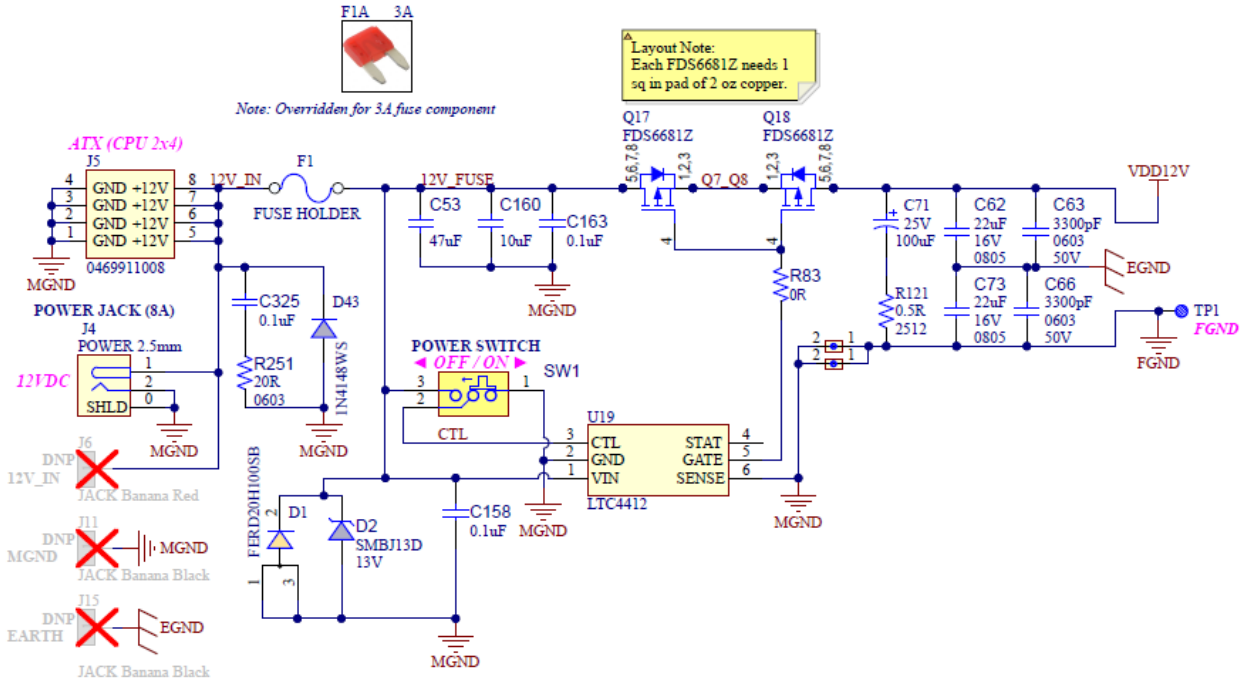


1.3.6. The 12V Supply Block

The 12V supply block provides the main power input and protection for the PCI1003 PMIC Power Board. It accepts 12V input from multiple sources, such as an ATX connector, DC power jack, or banana jacks. Key components include a fuse (F1) for overcurrent protection, reverse polarity protection diode (D1) and a transient voltage suppressor (D2) for surge protection.

A manual power switch (SW1) allows the user to turn the board on or off, while the U19 load switch controller manages the power MOSFETs (Q17, Q18) for efficient and safe switching of the 12V supply. The output is filtered by several capacitors (C53, C160, C163, C71, C62, C73, C63, C66) to ensure a clean and stable VDD12V rail. This block ensures that only protected, filtered and reliable 12V power is delivered to the buck frontend regulator, which generates the 5V rail for the PMIC.

Figure 1-3. 12V Supply Block Layout



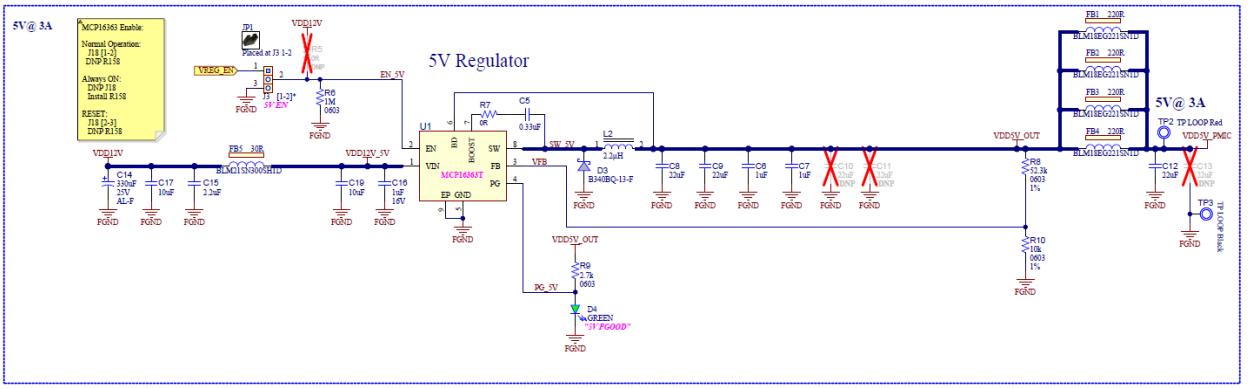
1.3.7. Buck Frontend 5V Regulator

This 5V Buck regulator circuit from the PCI1003 PMIC Power Board is designed to convert a 12V DC input into a stable 5V output capable of supplying up to 3A of current. The MCP16363 can operate with a maximum input voltage of 48V but in this design the nominal input value is 12V and should not exceed 13V. An overvoltage at the input will cause the transient protection diode D2 to conduct and it can blow fuse F1.

The input voltage is filtered by a combination of capacitors and a ferrite bead to reduce noise before reaching the MCP16363T switching regulator IC. The enable pin of the MCP16363T can be configured for normal operation, always-on, or reset mode using jumper J3 and resistor R5.

The output from the regulator is further filtered by several capacitors and ferrite beads to ensure low noise and stable voltage, making it suitable for sensitive electronic loads. A Power Good indicator circuit, consisting of a resistor and a green LED, provides a visual confirmation that the 5V output is within specification. Test points are provided for easy measurement of the 5V output and ground.

Figure 1-4. 5V Buck Regulator Schematic



Configuration Options

The enable logic for the MCP16363T can be set as follows:

- **Normal Operation:** J3 [1-2] installed, R5 not populated.
- **Always ON:** J3 not installed, R5 installed.
- **Reset:** J3 [2-3] installed, R5 not populated.

2. Graphical User Interface (GUI) Installation and Operation

In order to install, use and evaluate the product, several software and hardware tools are required.

Required Software

- I^2C Monitor Graphical User Interface (9.0 or higher)
- Microsoft®.NET Framework 4.5 or higher
- Adobe® Acrobat Reader®
- Windows® 10 or later

Required Hardware

- PCI1003 PMIC Power Board (EV69K72A)
- USB cable - USB type A Plug to USB type C plug
- MCP2221A Breakout Board USB C (BB62Z76A)

2.1. Graphical User Interface Installation

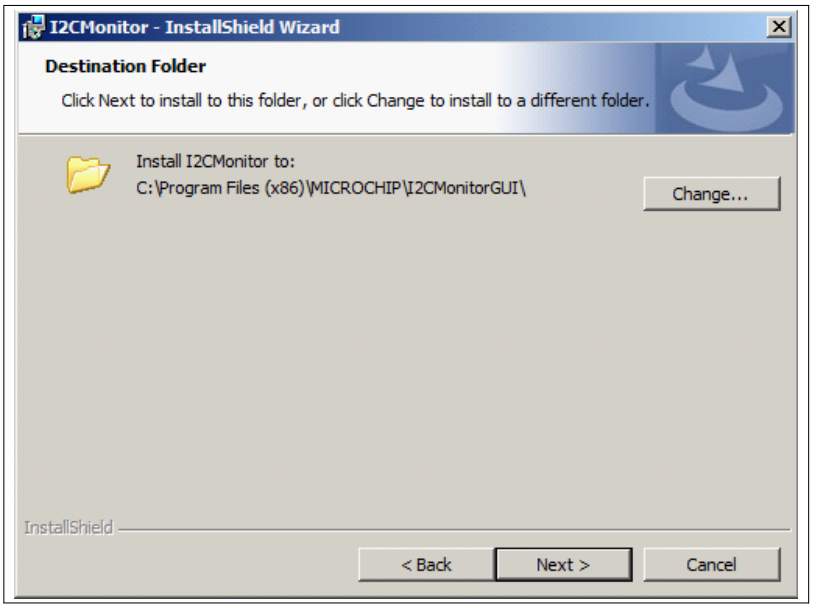
The following steps describe how to install the I^2C Monitor Graphical User Interface:

1. If Microsoft®.NET Framework is already installed, go to Step 3. If not, download Microsoft®.NET Framework from www.microsoft.com and follow the installation instructions.
2. If Adobe Acrobat Reader is already installed, go to Step 3. If not, download Adobe Acrobat Reader from http://get.adobe.com/reader/ and follow the installation instructions.
3. Download the I^2C Monitor Graphical User Interface archive from the product web page under **Documentation**.
4. Unzip the I^2C Monitor Graphical User Interface archive, which contains the `setup.exe` file.
   Note: If an older version or a corrupted version of the current I^2C Monitor Graphical User Interface is already installed on the computer, please see I2C Monitor Graphical User Interface Uninstall before proceeding with the installation.
5. Double click the `setup.exe` file to open the InstallShield Wizard window and wait for the extraction to complete. If required, the installation can be stopped by pressing the **Cancel** button.
6. In the **Welcome to the InstallShield Wizard for I2CMonitor** window, click the **Next** button to start the installation.

Figure 2-1. Starting the I²C Monitor Graphical User Interface Installation

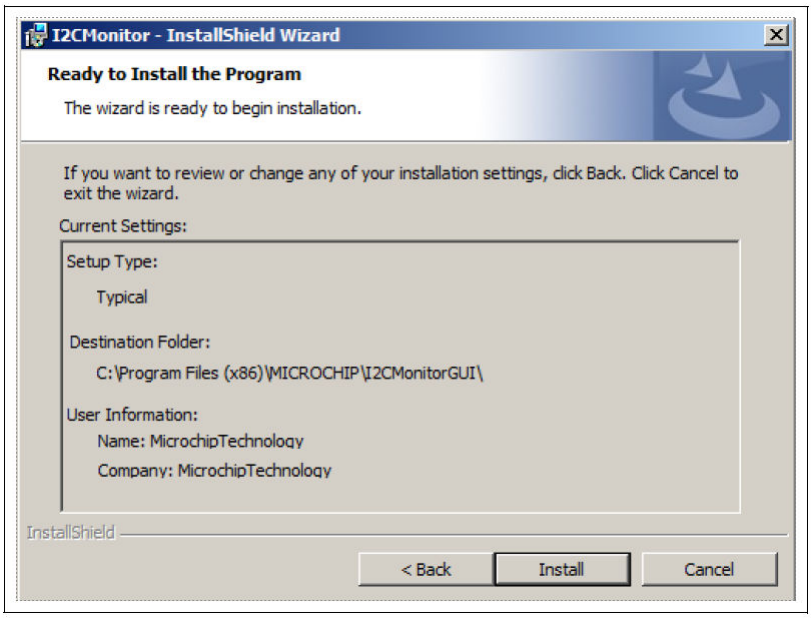
7. The installation path can be changed, although it is recommended to keep the default path. Click the **Next** button to continue.

Figure 2-2. Selecting the Destination Folder



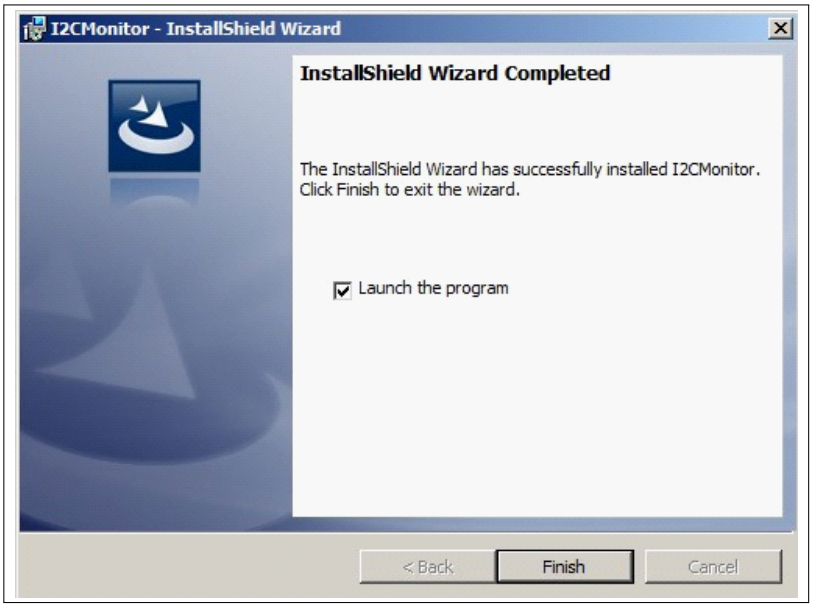
8. In the **Ready to Install the Program** window, click the **Install** button and wait for the application to proceed with the installation.

Figure 2-3. Installing the I²C Monitor Graphical User Interface



9. Once the installation is complete, leave the **Launch the program** box checked to automatically start the I2C Monitor GUI, or deselect this check box to start the GUI at a later stage. Click the **Finish** button to end the installation.
   To start the GUI at a later stage, either click the desktop icon or browse to *Windows Start>All Programs>Microchip>I2C Monitor*.

Figure 2-4. The Installation Complete Window

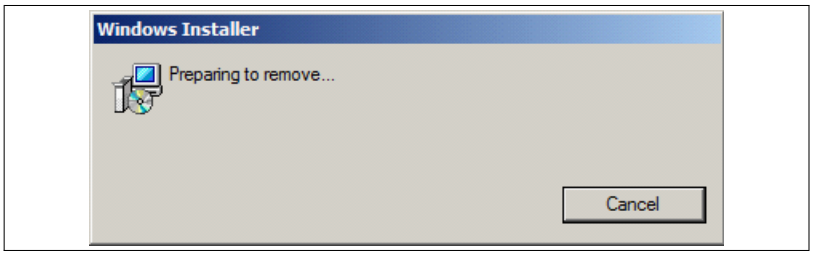


2.2. I²C Monitor Graphical User Interface Uninstall

In order to install a new version of the I²C Monitor Graphical User Interface, any previous version or corrupted version should be removed from the computer.

To uninstall, go to *Windows Start>Control Panel>Uninstall a program>I2CMonitor*. The I²C Monitor GUI will automatically close once the uninstallation process is complete.

Figure 2-5. *Uninstalling the I²C Monitor Graphical User Interface*



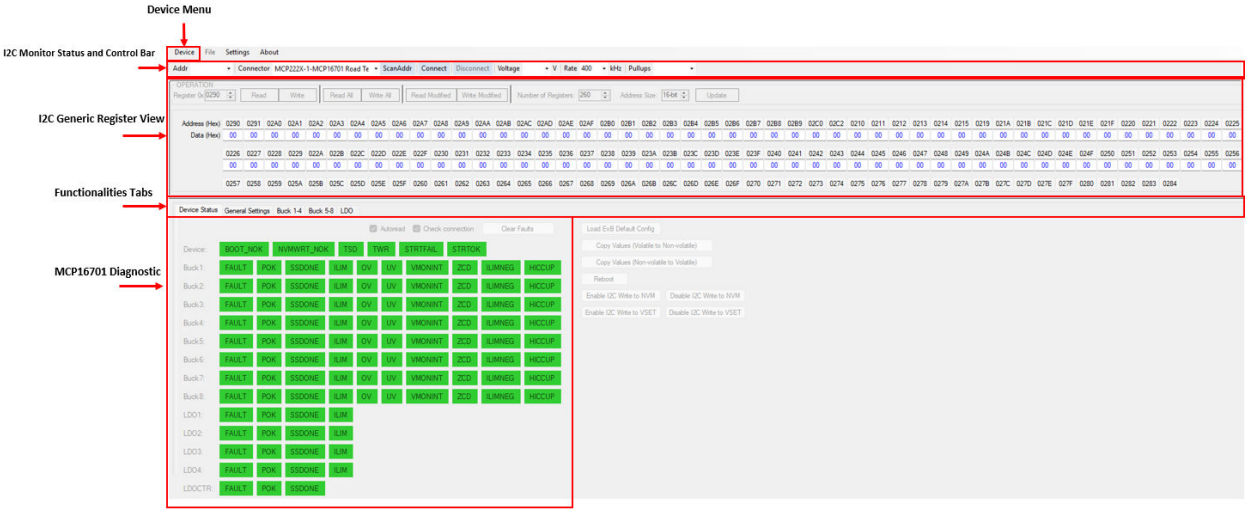
3. GUI Description

3.1. Introduction

This section describes how to use the I2C Monitor Graphical User Interface with the PCI1003 PMIC Power Board.

NOTICE This section provides information regarding the use of the GUI in the case of the MCP16701/A. For other devices using the I2C Monitor Graphical User Interface, see their specific Data Sheets and User Guides.

Figure 3-1. I²C Monitor Graphical User Interface Main Window - MCP16701/A View



All the changes to register values are made in the Volatile Register Map. For these changes to be present after a re-power of the PMIC, follow these steps:

1. Enable I2C Write to both VSET and NVM by pressing the corresponding buttons.
2. Copy the values (Volatile to Non-Volatile) by pressing the corresponding button.
3. Write all registers values by pressing the corresponding button.

3.2. The Graphical User Interface

The following sections describe the items in the Graphical User Interface (GUI).

3.2.1. Device Menu

The Device drop-down menu allows the user to select the device to be evaluated.

3.2.2. I2C Monitor Status and Control

The “Status and Control” bar contains the items described in Table 3-1.

Figure 3-2. I²C Monitor Status and Control Bar

Table 3-1. Monitor Status and Control Bar

Item	Description
Addr	This drop-down menu shows the address of the available devices.
Connector	This drop-down menu shows the type of connector used to connect the board.
ScanAddr	This button is used to scan for a valid address.
Connect/Disconnect	These buttons are used to connect/disconnect the current selected device.
Voltage	This drop-down menu is used to select the voltage level of the communication when using PICkit™ Serial Analyzer.
Rate	This drop-down menu is used to select the corresponding communication rate for the device.
Pull Ups	This drop-down menu is used to activate the internal pull ups from the PICkit Serial Analyzer.

In the "Status and Control" bar the user can choose the hardware tool for the communication with the device and the settings it should allow.

In order to connect to a device, the user must follow the steps described in Getting Started. After connecting the USB cable, the user must scan for a valid address. Once a valid address is detected, clicking the **Connect** button will initialize the connection with the device and the registers will be available for read and write operations.

3.2.3. I²C Generic Register View

The I²C Generic Register View area contains the items in Figure 3-3. This section of the I²C Monitor GUI is common for any device evaluated.

Figure 3-3. Generic Register View Area

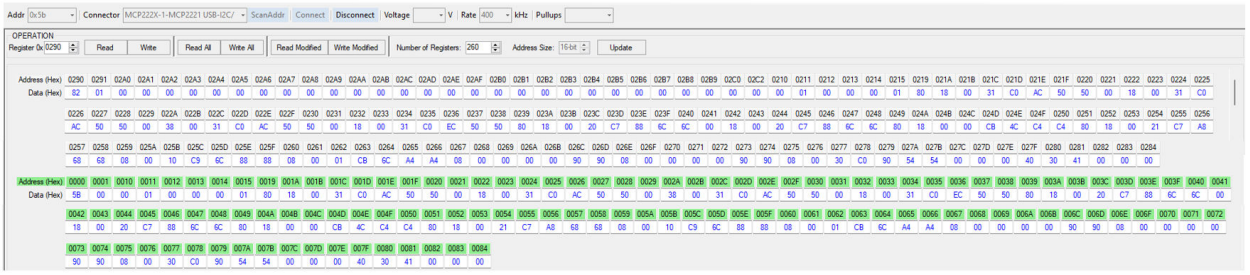


Table 3-2. I²C Generic Register View Items

Panel	Item	Description
Operation	**Register**	This section shows the registers available for read/write operations.
	Read/Write	These buttons are used for single register read/write operations.
	ReadAll/WriteAll	These buttons are used for reading/writing all the available registers.
	Number of Registers	In this section, the user can set the number of available registers for read/write operations.
	Address Size	In this section, the user can set the registers Address size.
	Update	This button sets the number of available registers for read/write operations in the Register Area.
Register Area		This section shows the current status of the registers address and their content.

The specific registers for MCP16701/A are described in the MCP16701/A Data Sheet.

3.2.4. MCP16701/A I²C Diagnostic

The MCP16701/A I²C Diagnostic part of the GUI resumes the information contained in the STATUS register.

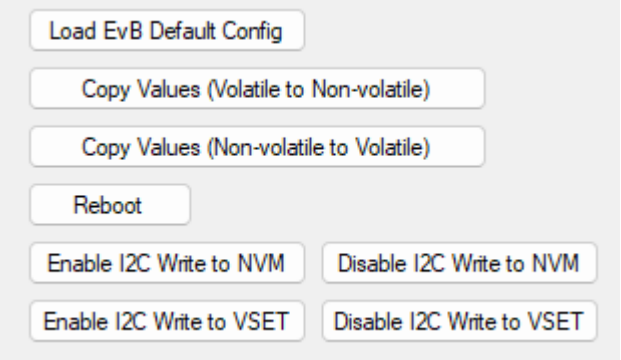
Figure 3-4. I²C Diagnostic Area

This region marks the status and faults of each corresponding bits in the registers. For the SSDONE, STRTOK and POK status flags, green signals a '1' condition and red signals a '0' condition. For the TSD, TWR, BOOT_NOK, NVMWRT_NOK, VMONINT, FAULT, HICCUP, ZCD, OV, UV, STRTFAIL, ILIM, Fault flags, green signals a '0' condition and red signals a '1' condition an active Fault.

If the "Autoread" box is checked, all the information is refreshed automatically. All Fault flags are reset on read, so the GUI memorizes the apparition of a Fault. To clear them from the GUI, the **Clear Faults** button must be clicked.

3.2.5. MCP16701/A Special Commands

Figure 3-5. Special Commands



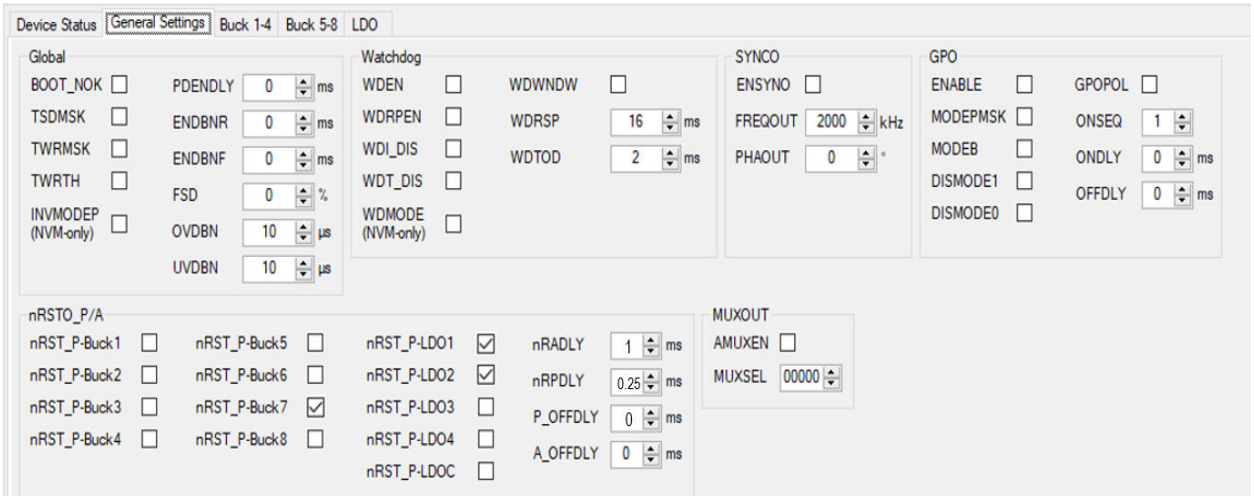
MCP16701/A has a list of special commands:

- Load EvB Default Config will load the typical application registry settings for the evaluation board. After loading the config, click the **Write All** button to make the changes effective.
- REBOOT is equivalent to a device turn-off. It reloads all values from the EEPROM content to volatile registers, followed by a new start-up sequence.
- Enable I2C Write to NVM is required to change the settings of the registers located in the non-volatile memory. Disable I2C Write to NVM revokes write access in the non-volatile memory.
- To change the output voltages, Enable I2C Write to VSET is required; otherwise, any changes to VSET settings will not be taken into account. Disable I2C Write to VSET revokes write access to VSET settings to avoid accidental changes in the VOUT settings.

3.2.6. MCP16701/A I²C General Settings

This area of the GUI allows the user to modify the General related features of the PMIC.

Figure 3-6. General Settings



nRSTO_P is an individual POK monitor; it has to be enabled for each channel that needs to be monitored at start-up/shutdown. For the PCI1003 PMIC Power Board, the monitored channels are BUCK7, LDO1 and LDO2 because these have VOUT set for I/O rails. When all the I/O rails have successfully powered on (POK threshold is reached), the monitored rails are fully working.

nRSTO_A is the global Reset; it will deassert after all regulators have started correctly.

3.2.6.1. MCP16701/A Global

The MCP16701 Global area in General Settings contains the items in Table 3-3.

Figure 3-7. Global Settings

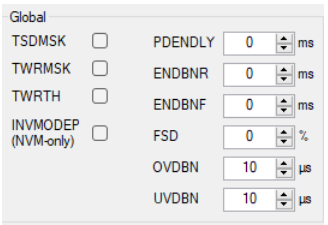


Table 3-3. Global

Panel	Item	Description
Global	TSDMSK	If the TSDMSK box is ticked, nINTO assertion at Thermal Shutdown is masked.
	TWRMSK	If the TWRMSK box is ticked, nINTO assertion during Thermal Early Warning is masked.
	TWRTH	If the TWRTH box is ticked, Thermal Early Warning Threshold is set to 1.
	INVMODEP (NVM-only)	If the INVMODEP box is ticked, MODE polarity is inverted.
	PDENDLY	This spin box allows Power-Down Enable Delay for Enable L-to-H transition to be ignored until the delay has expired.
	ENDBNR	This spin box allows for debounce time for L-to-H transition of Enable.
	ENDBINF	This spin box allows for debounce time for H-to-L transition of Enable.
	FSD	This spin box allows for Switching Frequency Displacement.
	OVDBN	This spin box allows for Overvoltage comparator debouncing delay.
	UVDBN	This spin box allows for Undervoltage comparator debouncing delay.

3.2.6.2. MCP16701/A Watchdog

The MCP16701/A Global area in General Settings contains the items in Table 3-4.

Figure 3-8. Watchdog Settings

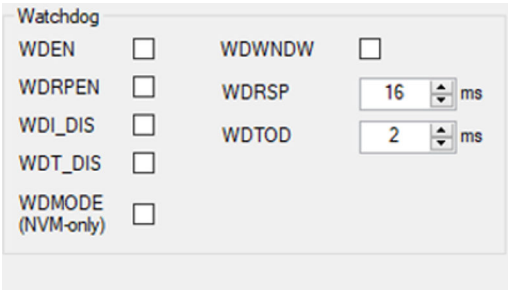


Table 3-4. Watchdog

Panel	Item	Description
Watchdog	WDEN	If the WDEN box is ticked, the Watchdog is enabled.
	WDRPEN	If the WDRPEN box is ticked, the Watchdog is enabled on nRSTO_P deassertion.
	WDI_DIS	If the WDI_DIS box is ticked, the Watchdog counter will not be incremented during H-to-L transitions.
	WDT_DIS	If the WDT_DIS box is ticked, the Watchdog counter will not be incremented during Watchdog Timer timeout.
	WDMODE (NVM-only)	If the WDMODE box is ticked, the Watchdog is in MODE 1.
	WDWNDW	If the WDWNDW box is ticked, the Watchdog is windowed.
	WDRSP	This spin box allows the change of Watchdog pulse width.
	WDTOD	This spin box allows for different time-out delays for the Watchdog.

3.2.6.3. MCP16701/A SYNCO

The MCP16701/A SYNCO area in General Settings contains the items in Table 3-5.

Figure 3-9. SYNCO Settings

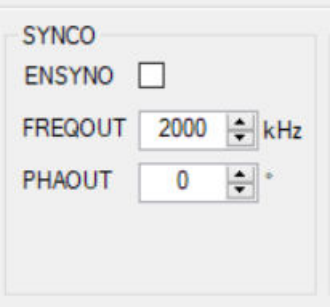


Table 3-5. SYNCO

Panel	Item	Description
SYNCO	ENSYNO	If the ENSYNO box is ticked, Syncronization Output is enabled.
	FREQOUT	This spin box allows for different division ratio for external syncronization.
	PHAOUT	This spin box allows for the syncronization signal to have a different phase.

3.2.6.4. MCP16701/A GPO

The MCP16701/A GPO area in General Settings contains the items in Table 3-6.

Figure 3-10. GPO Settings

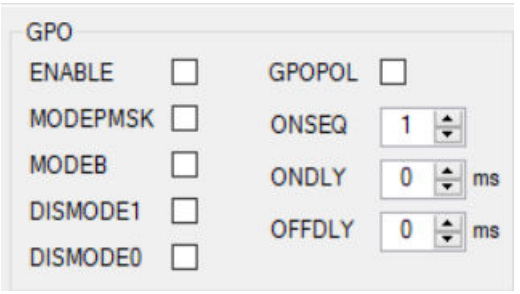


Table 3-6. GPO

Panel	Item	Description
GPO	ENABLE	If the ENABLE box is ticked, GPO is enabled during start-up.
	MODEPMSK	If the MODEPMSK box is ticked, MODE pin is masked.
	MODEB	If the MODEB box is ticked, MODE pin value is irrelevant.
	DISMODE1	If the DISMODE1 box is ticked, the channel will be disabled when MODE is 1 even if ENABLE is 1
	DISMODE0	If the DISMODE0 box is ticked, the channel will be disabled when MODE is 0, even if ENABLE is 1.
	GPOPOL	If the GPOPOL box is ticked, the polarity of GPO is inverted.
	ONSEQ	This spin box assigns GPO to a certain ON sequence step.
	ONDLY	This spin box programs the delay between the end of the previous sequence and assertion of GPO.
	OFFDLY	This spin box programs the delay between the deassertion of ENABLE and the deassertion of GPO.

3.2.6.5. MCP16701/A nRSTO_P/A

The MCP16701/A nRSTO_P/A area in General Settings contains the items in Table 3-7.

Figure 3-11. nRSTO_P/A Settings

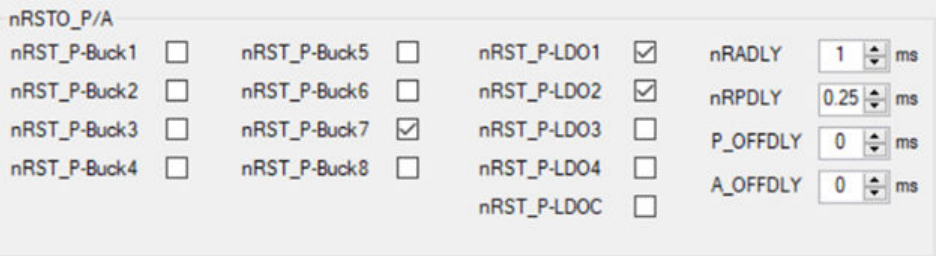


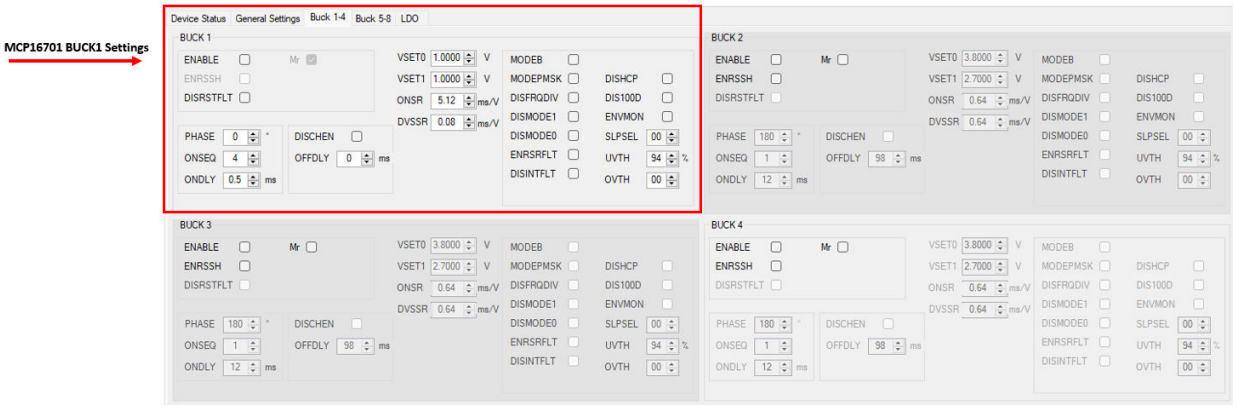
Table 3-7. nRTSTO_P/A

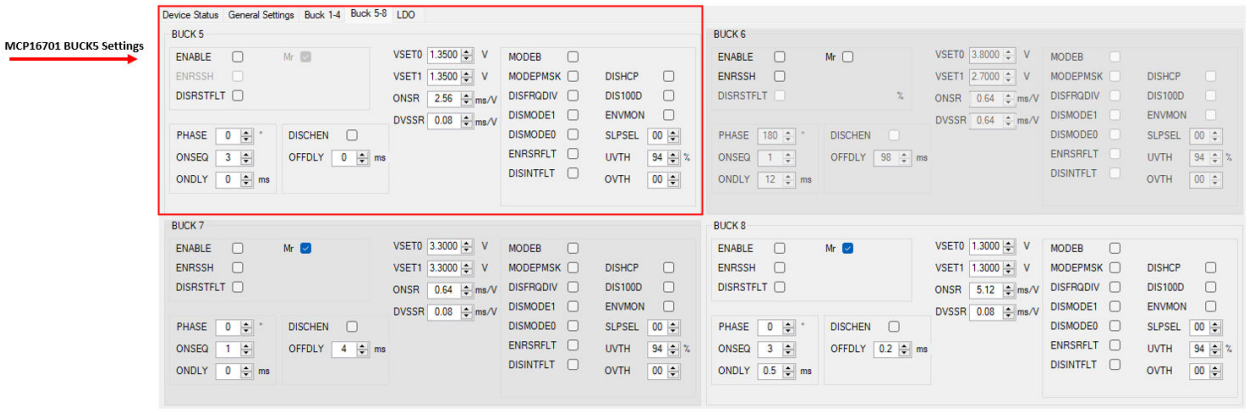
Panel	Item	Description
nRTSTO_P/A	nRST_P BUCKs 1-to-8	If the nRST_P for BUCKS 1-to-8 box is ticked, the channel will be taken into consideration for nRSTO_P deassertion.
	nRST_P LDOs 1-to-4 and LDOC	If the nRST_P for LDOs 1-to-4 and LDOC box is ticked, the channel will be taken into consideration for nRSTO_P deassertion.
	nRADLY	This spin box sets the delay of deassertion of nRSTO_A.
	nRPDLY	This spin box sets the delay of deassertion of nRSTO_P.
	P_OFFDLY	This spin box sets the delay between the deassertion of ENABLE input and the assertion of nRSTO_P.
	A_OFFDLY	This spin box sets the delay between the deassertion of ENABLE input and the assertion of nRSTO_A.

3.2.7. MCP16701/A I²C Buck Channel Settings

This area of the GUI allows the user to modify the Buck-related features individually for each of the eight Buck channels. There are two tabs for the Buck Channels, the first one is for Bucks 1 to 4 and the second one for Bucks 5 to 8.

Figure 3-12. I²C Buck Channel Settings





3.2.7.1. MCP16701/A Bucks 1-to-8 General

The MCP16701/A General area in BUCKS 1-to-8 contains the items in Table 3-8.

Figure 3-13. General Buck Channel Settings

Table 3-8. General

Panel	Item	Description
General	ENABLE	If the ENABLE box is ticked, the channel will activate at start-up.
	DISRSTFLT	If the DISRSTFLT box is ticked, nRSTO_A/P will not deassert upon channel Fault during runtime.
	ENRSSH	If the ENRSSH box is ticked, a replica channel is disabled with the ENABLE bit.
	Mr	If the Mr box is ticked, the channel will be set to Main. BUCKs 1 and 5 are always Main, cannot be replica.
	VSET0	This spin box changes the output voltage of the channel when MODE is '0'.
	VSET1	This spin box changes the output voltage of the channel when MODE is '1'.

3.2.7.2. MCP16701/A Bucks 1-to-8 Start-Up, Shutdown and Dynamic Voltage Scaling

The MCP16701/A Start-Up, Shutdown and Dynamic Voltage Scaling area in BUCKS 1-to-8 contains the items in Table 3-9.

Figure 3-14. Start-up, Shutdown and Dynamic Voltage Scaling Settings for Buck Channels

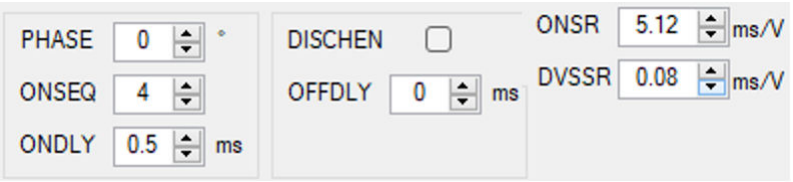


Table 3-9. Start-Up, Shutdown and Dynamic Voltage Scaling

Panel	Item	Description
Start-Up, Shutdown and DVSR	PHASE	This spin box sets the phase displacement of the Buck converter switch turn-on edge.
	ONSEQ	This spin box assigns the Buck to a certain ON sequence.
	ONDLY	This spin box sets the delay between the end of the previous sequence and the beginning of the converter turn-on.
	DISCHEN	If the DISCHEN box is ticked, the discharge resistor is enabled at turn-off.
	OFFDLY	This spin box sets the delay between the deassertion of ENABLE and the converter turn-off.
	DVSSR	This spin box set the slew-rate for DVS transitions.

3.2.7.3. MCP16701/A Bucks 1-to-8 Features

The MCP16701/A Features area in Bucks 1-to-8 contains the items in Table 3-10.

Figure 3-15. Features Settings of Buck Channels

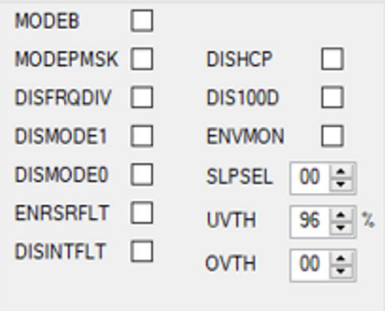


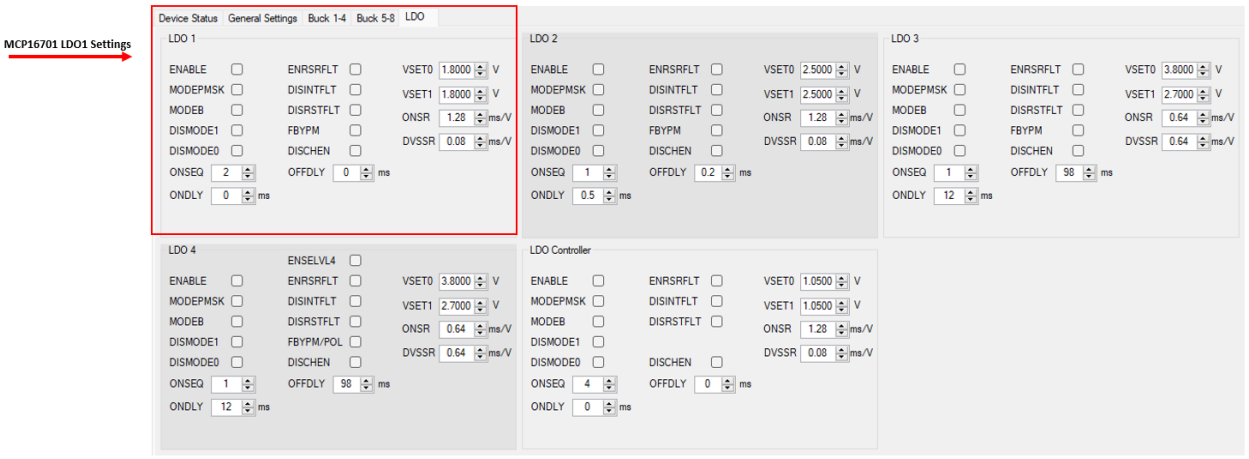
Table 3-10. Features

Panel	Item	Description
Features	MODEB	If the MODEB box is ticked when MODEMSK = 1, the MODE pin is irrelevant and only MODEB value is taken into account.
	MODEPMSK	If the MODEMSK box is ticked, the MODE pin is not taken into consideration for a MODE change.
	DISFRQDIV	If the DISFRQDIV box is ticked, the frequency division algorithm in light-load efficiency is disabled.
	DISMODE1	If the DISMODE1 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 1.
	DISMODE0	If the DISMODE0 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 0.
	ENRSRFLT	If the ENRSRFLT box is ticked, when a channel has a Fault, an automatic restart will be invoked after 100 ms.
	DISINTFLT	If the DISINTFLT box is ticked, nINTO will not deassert upon channel Fault during runtime.
	DISHCP	If the DISHCP box is ticked, hiccup mode overcurrent protection is disabled for the channel.
	DIS100D	If the DIS100D box is ticked, duty cycle of the channel will be limited to 75%.
	ENVMON	If the ENVMON box is ticked, nINTO will deassert when an OV/UV condition is detected.
	SLPSEL	This spin box changes the slope compensation.
	UVTH	This spin box changes the threshold of undervoltage monitoring.
	OVTH	This spin box changes the threshold of overvoltage monitoring.

3.2.8. MCP16701/A I^2C Buck Channel Settings

This area of the GUI allows the user to modify the LDO related features individually for each of the four LDO channels and LDO Controller.

Figure 3-16. I²C LDO Channel Settings



3.2.8.1. MCP16701/A LDOs 1-to-4 and LDO Controller General

The MCP16701/A General area in in LDO contains the items in Table 3-11.

Figure 3-17. General Settings for the LDOs

Table 3-11. General

Panel	Item	Description
General	ENABLE	If the ENABLE box is ticked, the channel will activate at Start-Up.
	MODEPMSK	If MODEMSK box is ticked, MODE pin is not taken into consideration for a MODE change.
	ENRSRFLT	If ENRSRFLT box is ticked, when a channel has a Fault, an automatic restart will be invoked after 100 ms.
	DISINTFLT	If DISINTFLT box is ticked, nINTO will not deassert upon channel Fault during runtime.
	VSET0	This spin box changes the output voltage of the channel when MODE is 0.
	VSET1	This spin box changes the output voltage of the channel when MODE is 1.
	ENSELVL4 (LDO4 only)	If ENSELVL4 box is ticked, it enables SELVL4 to control LDO4 voltage between 1.8V and 3.3V.

3.2.8.2. MCP16701/A LDOS 1-to-4 and LDO Controller Start-Up, Shutdown and Dynamic Scaling

The MCP16701/A LDOs 1-to-4 and LDO Controller Start-Up, Shutdown and Dynamic Voltage Scaling area contains the items in Table 3-12.

Figure 3-18. Start-up, Shutdown and Dynamic Voltage Scaling for LDOs

Table 3-12. Start-Up, Shutdown and Dynamic Voltage Scaling

Panel	Item	Description
Start-Up, Shutdown and DVSR	ONSEQ	This spin box assigns the LDO to a certain ON sequence.
	ONDLY	This spin box sets the delay between the end of the previous sequence and the beginning of the LDO turn-on.
	DISCHEN	If the DISCHEN box is ticked, the discharge resistor is enabled at turn-off.
	OFFDLY	This spin box sets the delay between the deassertion of ENABLE and the LDO turn-off.
	ONSR	This spin box sets the slew-rate for Soft-Start ramp.
	DVSSR	This spin box set the slew-rate for DVS transitions.

3.2.8.3. MCP16701/A LDOs 1-to-4 and LDO Controller Features

The MCP16701/A LDOs 1-to-4 and LDO Controller Features area contains the items in Table 3-13.

Figure 3-19. Features Settings for LDOs

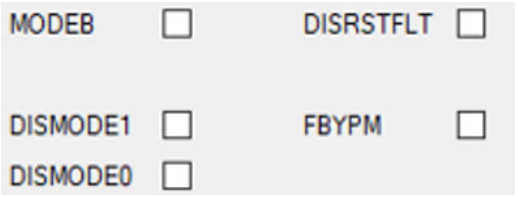


Table 3-13. Features

Panel	Item	Description
Features	MODEB	If the MODEB box is ticked when MODEMSK = 1, the MODE pin is irrelevant and only the MODEB value is taken into account.
	DISRSTFLT	If the DISRSTFLT box is ticked, nRSTO_A/P will not deassert upon channel Fault during runtime.
	DISMODE1	If the DISMODE1 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 1.
	DISMODE0	If the DISMODE0 box is ticked, when a channel is ENABLED, it will be disabled when MODE = 0.
	FBYPM/POL	(FBYPM exclusive LDOs 1-to-4) Forces LDOs in Load-Switch Mode.
		(POL LDO4 only) If this box is ticked and ENSELVL4 = 1, it selects the polarity of SELVL4 logic.

3.2.9. Status Bar

The status bar provides information on the status of the device connected to the PC.

Figure 3-20. Status Bar

Table 3-14. Status Bar Items

Item	Description
Status Label	The label shows if there is any device connected to the board. Refer to Table 3-15 for a list of possible labels.
Progress Bar	This bar shows the level of completion for a given command.

Table 3-15. Status Labels

Status Label	Description
STATUS: Connected!	This message is shown when the GUI connects to a device.
STATUS: Disconnected!	This message is shown when the GUI does not detect a connected device.

The specific settings for all control areas are detailed in the register map available in the MCP16701/A data sheet.

4. Board Design

This section contains the following schematic and layouts for the PCI1003 PMIC Power Board (EV69K72A):

- Board - Schematic 1
- Board - Schematic 2
- Board - Schematic 3
- Board - Schematic 4
- Board - Top Silk
- Board - Top Copper and Silk
- Board - Top Copper
- Board - Bottom Copper
- Board - Bottom Copper and Silk
- Board - Bottom Silk

4.1. Schematic

Figure 4-1. Board - Schematic 1

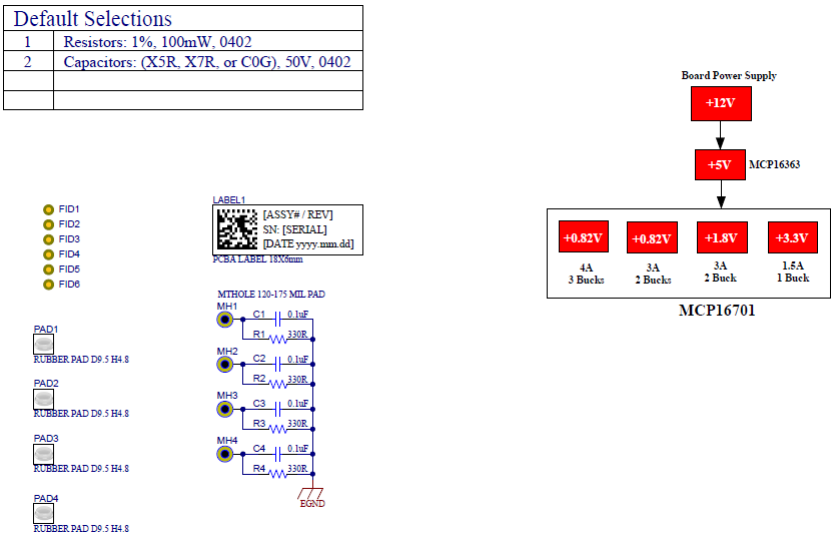


Figure 4-2. Board - Schematic 2

12V Supply

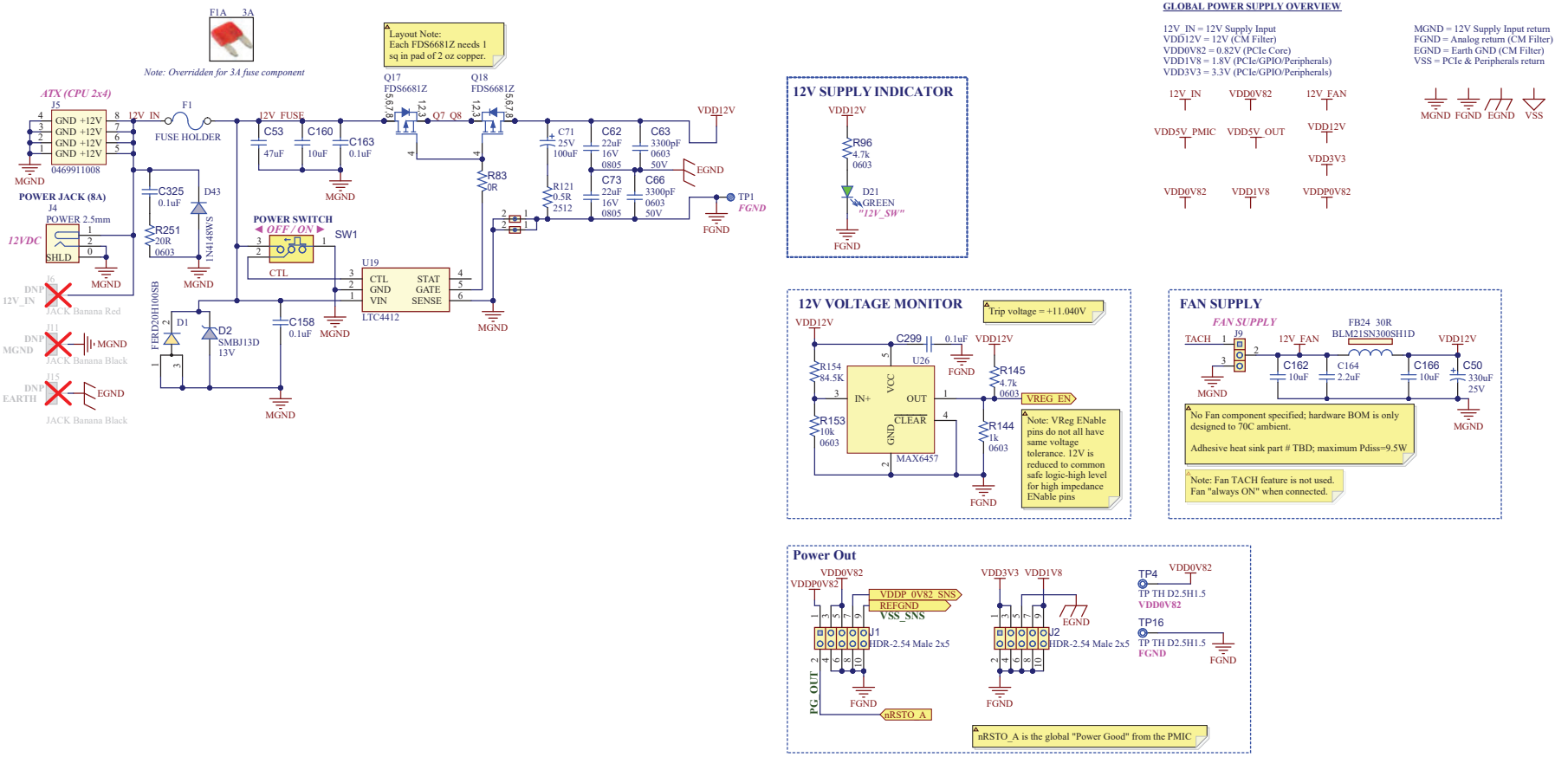


Figure 4-3. Board - Schematic 3

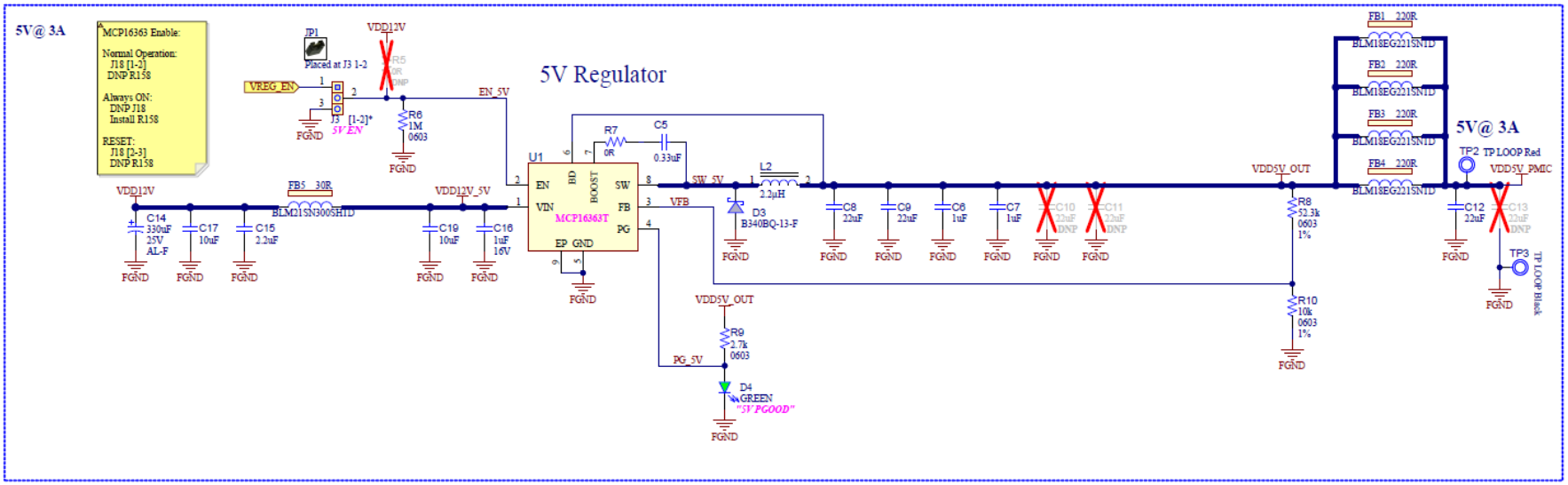
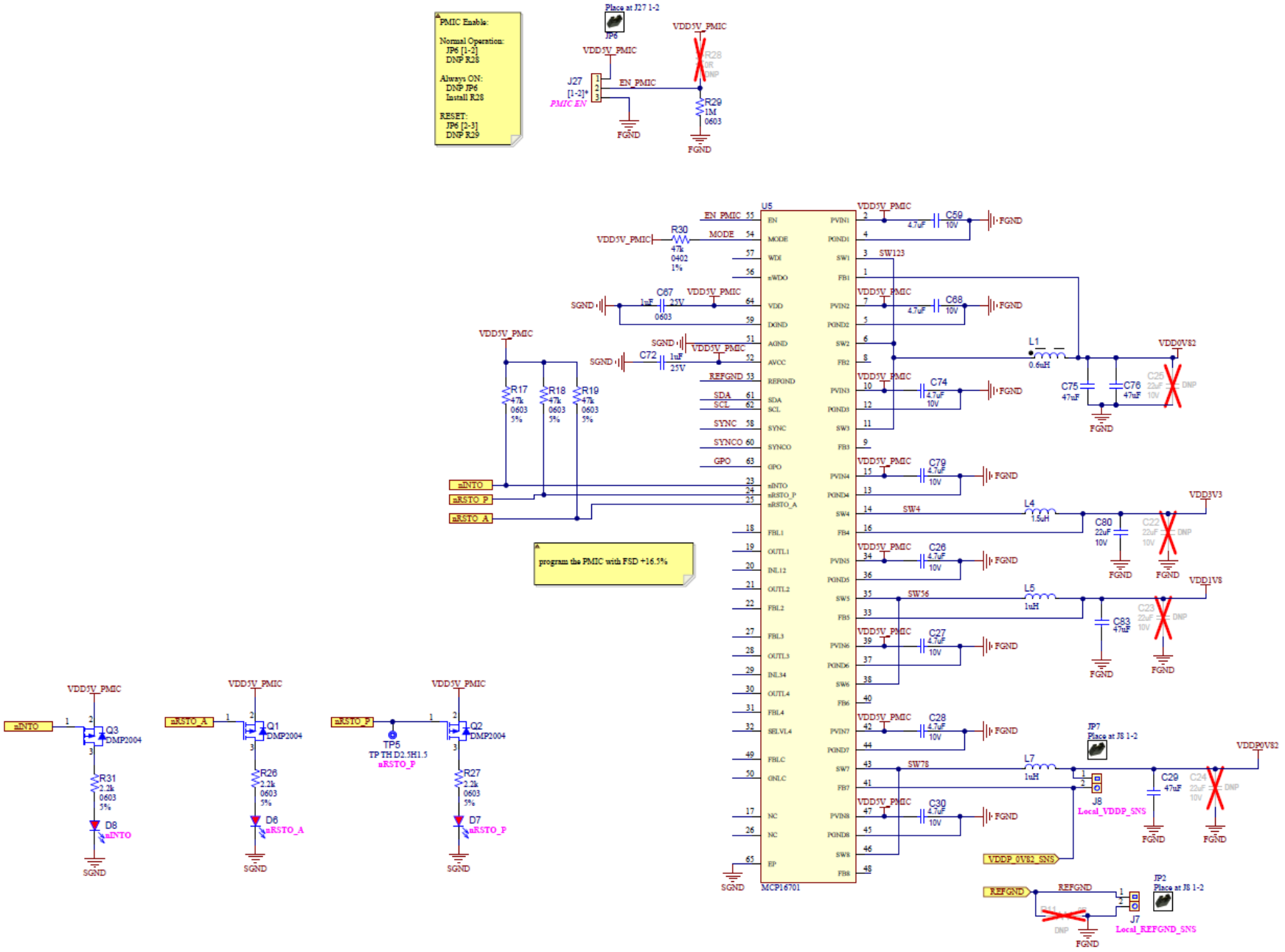


Figure 4-4. Board - Schematic 4



4.2. Layout

Figure 4-5. Board - Top Silk

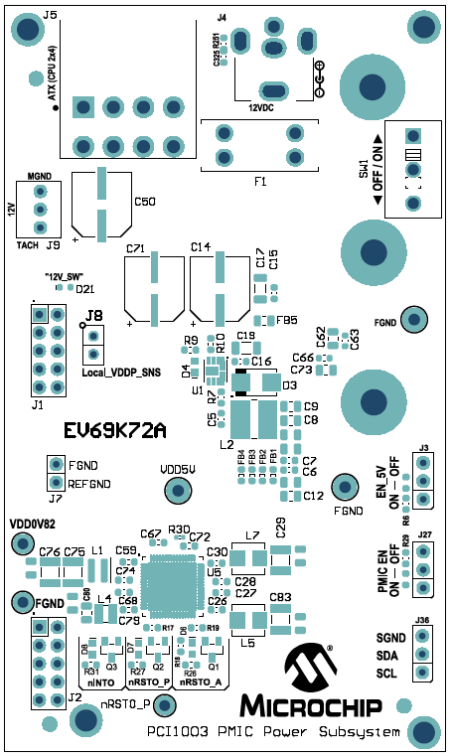


Figure 4-6. Board - Top Copper and Silk

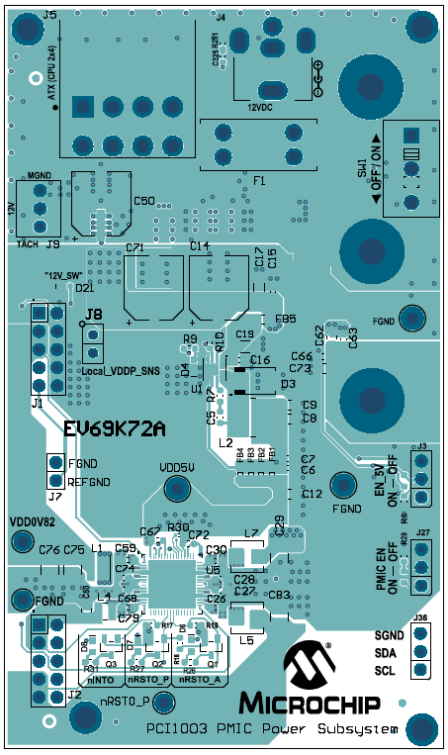


Figure 4-7. Board - Top Copper

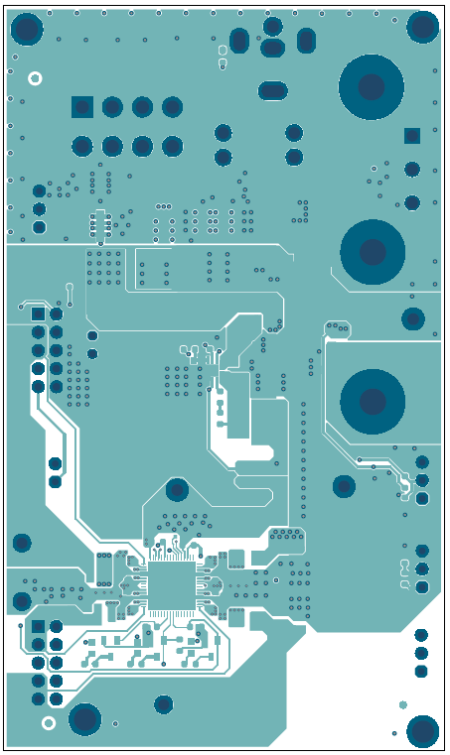


Figure 4-8. Board - Bottom Copper

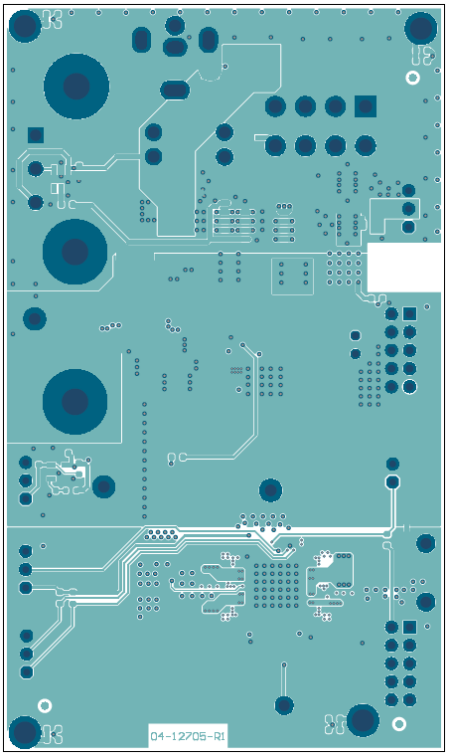


Figure 4-9. Board - Bottom Copper and Silk

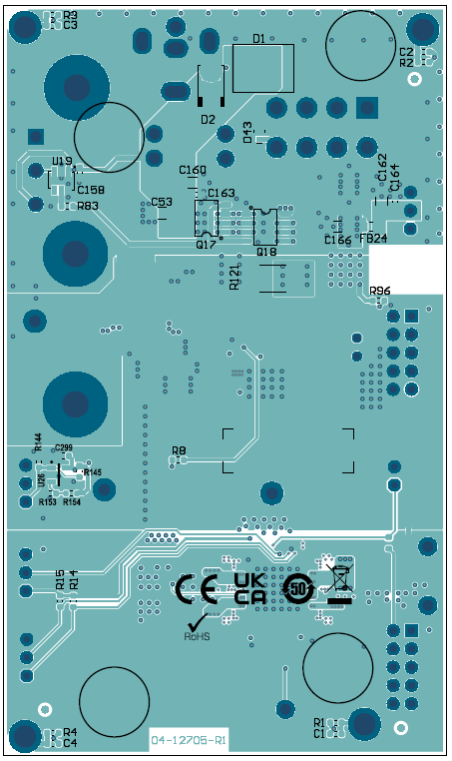
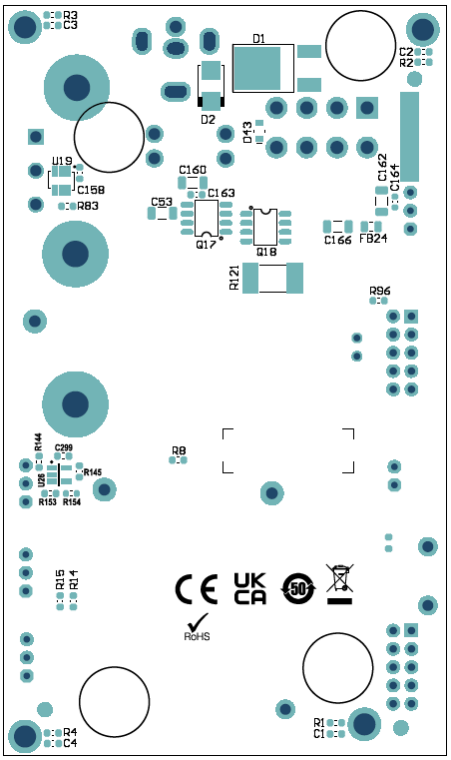


Figure 4-10. Board - Bottom Silk



5. Bill of Materials (BOM)

Table 5-1. Bill of Materials (BOM)

Qty.	Reference	Description	Manufacturer	Part Number
8	C1, C2, C3, C4, C158, C163, C299, C325	Capacitor, Ceramic, 0.1 µF, 50V, 10%, X7R, SMD, 0603, AEC-Q200	Vishay Intertechnology, Inc.	GA0603Y104KXAAC31G
1	C5	Capacitor, Ceramic, 0.33 µF, 50V, 20%, X7R, SMD, 0603, AEC-Q200	TDK Corporation	CGA3E3X7R1H334K080AB
3	C6, C7, C16	Capacitor, Ceramic, 1 µF, 16V, 10%, X7R, SMD, 0603	Kyocera AVX	0603YC105KAT2A
5	C8, C9, C12, C62, C73	Capacitor, Ceramic, 22 µF, 16V, 20%, X5R, SMD, 0805 AEC-Q200	Murata Manufacturing Co., Ltd.	GRT21BR61C226ME13L
2	C14, C50	Capacitor, Aluminum, 330 µF, 25V, 20%, X5R, SMD, F	Nichicon Corporation	UWT1E331MNL1GS
2	C15, C164	Capacitor, Ceramic, 2.2 µF, 25V, 10%, X5R, SMD, 0603	Murata Manufacturing Co., Ltd.	GRM188R61E225KA12D
5	C17, C19, C160, C162, C166	Capacitor, Ceramic, 10 µF, 50V, 10%, X5R, SMD, 1206 AEC-Q200	Murata Manufacturing Co., Ltd.	GRT31CR61H106KE01L
8	C26, C27, C28, C30, C59, C68, C74, C79	Capacitor, Ceramic, 4.7 µF, 10V, 10%, X7S, SMD, 0603	TDK Corporation	C1608X7S1A475K080AC
4	C29, C75, C76, C83	Capacitor, Ceramic, 4.7 µF, 10V 10%, X7R, SMD, 1210	Murata Manufacturing Co., Ltd.	GRM32ER71A476KE15L
1	C53	Capacitor, Ceramic, 47 µF, 25V 20%, X5R, SMD, 1206	TDK Corporation	C3216X5R1E476M160AC
2	C63, C66	Capacitor, Ceramic, 3300 pF, 50V, 10%, X7R, SMD, 0603, AEC-Q200	KEMET	C0603C332K5RACAUTO
2	C67, C72	Capacitor, Ceramic, 1 µF, 25V, 10%, X7R, SMD, 0603	TDK Corporation	C1608X7R1E105K080AB
1	C71	Capacitor, Aluminum, 100 µF, 25V, 20%, SMD, E	Panasonic® - ECG	EEE-FP1E101AP
1	C80	Ceramic, Ceramic, 22 µF, 10V, 20%, X7S, SMD, 0805	TDK Corporation	C2012X7S1A226M125AC
1	D1	Diode, Rectifier, 100V, 20A, DPAK	STMicroelectronics	FERD20H100SB-TR
1	D2	Diode, TVS, 13V, 21.2V, 600W, SMD, DO-214AA	Vishay Intertechnology, Inc.	SMBJ13D-M3/I
1	D3	Diode, Schottky, B340, 40V, 3A, DO-214AA, SMB AEC-Q101	Diodes Incorporated	B340BQ-13-F
2	D4, D21	Diode, LED, Green, 2.2V, 25 mA, 18 mcd, Diffuse, SMD, 0603	Lumex® Inc.	SML-LX0603GW-TR
3	D6, D7, D8	Diode, LED, Red, 1.9V, 20 mA, 60 mcd, Clear ,SMD, 0603	Wurth Elektronik	150060SS75000
1	D43	Diode, Rectifier, 1.25V, 150 mA, 75V, SOD-323	Diodes Incorporated®	1N4148WS-7-F
4	FB1, FB2, FB3, FB4	Ferrite, 220R@100MHz, 2A, SMD, 0603	Murata Manufacturing Co., Ltd.	BLM18EG221SN1D
2	FB5, FB24	Ferrite 30R@100MHz, 8.5A, AEC-Q200, SMD, 0805	Murata Manufacturing Co., Ltd.	BLM21SN300SH1D
2	J1, J2	Connector, HDR-2.54, Male, 2x5 Gold, 5.84 MH, Through Hole, Right Angle	Samtec, Inc.	TSW-105-08-F-D-RA

Note: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Table 5-1. Bill of Materials (BOM) (continued)

Qty.	Reference	Description	Manufacturer	Part Number
3	J3, J27, J36	Connector, HDR-2.54, Male, 1x3, Gold, 5.84 MH, Through Hole, Vertical	FCI	68000-103HLF
1	J4	Connector, Power, 2.5 mm, 5.5 mm, Through Hole, Right Angle	Same Sky	PJ-063BH
1	J5	Connector, HDR-4.2, Female, 2x4 Tin, Through Hole, Right Angle	Molex, LLC	0469911008
2	J7, J8	Connector, HDR-2.54, Male, 1x2, Gold, 5.84 MH, Through Hole, Vertical	FCI	77311-118-02LF
1	J9	Connector, HDR-2.54, Male, 1x3, Tin Lock, 7.49 MH, Through Hole, Vertical	TE Connectivity	640456-3
1	L1	Inductor, 0.6 µH, 10.8A, 20%, 0.006R, SMD, L3.2, W3.6, H3	Coilcraft	XGL3530-601MEC
1	L2	Inductor, 2.2 µH, 4.54A, 20%, SMD, 2020, AEC-Q200	Wurth Elektronik	78404054022
1	L4	Inductor, 1.5 µH, 3.5A, 20%, SMD, 1008	Murata Manufacturing Co., Ltd.	DFE252012P-1R5M=P2
2	L5, L7	Inductor, 1 µH, 8A, 20%, SMD, L4.2, W4, H3.0	TDK Corporation	SPM4030T-1R0M
3	Q1, Q2, Q3	Transistor, FET, P-Channel, 20V, 0.6A, 0.9R, 0.55W, SOT-23-3	Diodes Incorporated®	DMP2004K-7
2	Q17, Q18	Transistor, FET, P-Channel, 30V, 20A, 0.0046R, 2.5W SOIC-8	ON Semiconductor®	FDS6681Z
4	R1, R2, R3, R4	Resistor, Thick Film, 330R, 5%, 1/10W, SMD, 0603	Stackpole Electronics, Inc.	RMCF0603JT330R
2	R6, R29	Resistor, Thick Film, 1M, 5%, 1/10W, SMD, 0603 AEC-Q200	Panasonic® - ECG	ERJ-3GEYJ105V
2	R7, R83	Resistor, Thick Film, 0R, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3GSY0R00V
1	R8	Resistor, Thick Film, 52.3k, 1%, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3EKF5232V
1	R9	Resistor, Thick Film, 2.7k, 1%, 1/10W, SMD, 0603, AEC-Q200	Vishay Intertechnology, Inc.	CRCW06032K70FKEA
2	R10, R153	Resistor, Thin Film, 10k, 1%, 1/8W, SMD, 0603	Stackpole Electronics, Inc.	RNCP0603FTD10K0
2	R14, R15	Resistor, Thick Film, 2.2k, 1%, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3EKF2201V
3	R17, R18, R19	Resistor, Thick Film, 47k, 5%, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3GEYJ473V
3	R26, R27, R31	Resistor, Thick Film, 2.2k, 5%, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3GEYJ222V
1	R30	Resistor, Thick Film, 47k, 1%, 1/16W, SMD, 0402	Yageo Corporation	RC0402FR-0747KL
1	R96	Resistor, Thick Film, 4.7k, 5%, 1/10W, SMD, 0603	Yageo Corporation	RC0603JR-074K7L
1	R121	Resistor, Metal Film, 0.5R, 1%, 2W, SMD, 2512	Vishay Intertechnology, Inc.	WSL2512R5000FEA
1	R144	Resistor, Thick Film, 1k, 5%, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3GEYJ102V
1	R145	Resistor, Thick Film, 4.7k, 1%, 1/16W, SMD, 0603	TE Connectivity	CRG0603F4K7

Note: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Table 5-1. Bill of Materials (BOM) (continued)

Qty.	Reference	Description	Manufacturer	Part Number
1	R154	Resistor, Thick Film, 84.5k, 1%, 1/10W, SMD, 0603	Yageo Corporation	RC0603FR-0784K5L
1	R251	Resistor, Thick Film, 20R, 1%, 1/10W, SMD, 0603, AEC-Q200	Panasonic® - ECG	ERJ-3EKF20R0V
1	SW1	Switch, Slide, Single Pole Double Throw, 120V, 6A, Through Hole	C&K Components	1101M2S3CQE2
2	TP1, TP3	Connector, Test Point, LOOP, Black, 3.18 x 5.59, Through Hole	Keystone® Electronics Corp.	5006
1	TP2	Connector, Test Point, LOOP, Red, Through Hole	Keystone® Electronics Corp.	5010
1	U19	IC, Power, Power OR Switch, TSOT-23-6	Analog Devices Inc.	LTC4412ES6#TRMPBF
1	U26	IC, Power, Voltage Monitor, SOT23-5	Maxim Integrated Products	MAX6457UKD0B+T
1	PCB	Printed Circuit Board	Microchip Technology Inc.	04-12705-R1

Note: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Table 5-2. Bill of Materials (BOM) – Microchip Parts

Qty.	Reference	Description	Manufacturer	Part Number
1	U1	Analog Switcher Buck 4V to 48V, VDFN-8	Microchip Technology Inc.	MCP16363T-E/NMX
1	U5	Analog PMIC Switcher Buck, Adj, VQFN-64	Microchip Technology Inc.	MCP16701T-I/KCX

Note: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Table 5-3. Bill of Materials (BOM) – Mechanical Parts

Qty.	Reference	Description	Manufacturer	Part Number
1	F1	Mechanical, Headers & Wires, Fuse Holder, Blade, PCB	Keystone® Electronics Corp.	3568
1	F1A	Mechanical, Headers & Wires, Fuse, 3A 32VAC, Fast Blow, Mini Blade	Littelfuse, Inc.	0297003.WXNV
4	JP1, JP2, JP6, JP7	Mechanical, Headers & Wires, Jumper, 2.54 mm, 1x2, Gold	Oupiin America Inc.	2006-BBB
1	LABEL1	Label, PCBA, 18x6 mm, Datamatrix Assy#/Rev/Serial/Date	ACT Logimark AS	505462
4	PAD1, PAD2, PAD3, PAD4	Mechanical, Headers & Wires, Rubber Pad, Cylindrical, Flat Top, D9.5, H4.8, Clear	Bumper Specialties, Inc.	BS35CL01X02RP

Note: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Table 5-4. Bill of Materials (BOM) – Do not Populate Parts

Qty.	Reference	Description	Manufacturer	Part Number
0	C10, C11, C13	Capacitor, Ceramic, 22 µF, 16V, 20%, X5R, SMD, 0805, AEC-Q200	Murata Manufacturing Co., Ltd.	GRT21BR61C226ME13L
0	C22, C23, C24, C25	Capacitor, Ceramic, 22 µF, 10V, 20%, X7S, SMD, 0805	TDK Corporation	C2012X7S1A226M125AC
0	J6	Connector, Jack, Banana, Red, 3.66 mm, Female, Through Hole, Vertical	Keystone® Electronics Corp.	7006

Table 5-4. Bill of Materials (BOM) – Do not Populate Parts (continued)

Qty.	Reference	Description	Manufacturer	Part Number
0	J11, J15	Connector, Jack, Banana, Black, 3.66 mm, Female, Through Hole, Vertical	Keystone® Electronics Corp.	7007
0	R5, R11, R28	Resistor, Thick Film, 0R, 1/10W, SMD, 0603	Panasonic® - ECG	ERJ-3GSY0R00V

Note: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

6. References

Table 6-1. Recommended Reading

Source	Document Title	Literature Number	Available
Microchip Technology, Inc.	MCP16701 Data Sheet	DS20006993	www.microchip.com/en-us/product/MCP16701
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7. Revision History

Revision	Date	Section	Comments
A	4/2026		Initial release of this document.

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