

SOP-8

Pin Definition:

- | | |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate | 5. Drain |

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
-30	14 @ $V_{GS} = -10V$	-11
	20 @ $V_{GS} = -4.5V$	-8.5

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

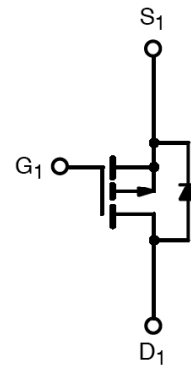
Application

- Load Switches
- Notebook PCs
- Desktop PCs

Ordering Information

Part No.	Package	Packing
TSM4425CS RLG	SOP-8	2.5Kpcs / 13" Reel

Note: "G" denotes for Halogen- and Antimony-free as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds

Block Diagram


P-Channel MOSFET

Absolute Maximum Rating ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	-11	A
Pulsed Drain Current	I_{DM}	-50	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	-2.1	A
Maximum Power Dissipation	P_D	$T_a = 25^\circ C$	2.5
		$T_a = 75^\circ C$	1.6
Operating Junction Temperature	T_J	+150	$^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ C$

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Foot Thermal Resistance	$R_{\theta JF}$	18	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	52.5	$^\circ C/W$

Notes:

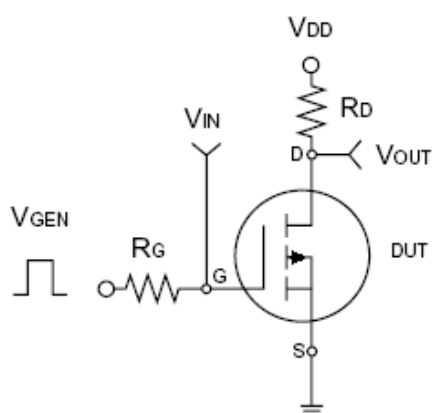
- Pulse width limited by the Maximum junction temperature
- Surface Mounted on FR4 Board, $t \leq 10$ sec.

Electrical Specifications (T_C = 25°C unless otherwise noted)

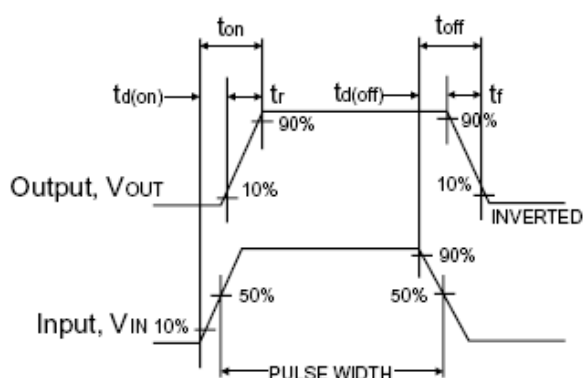
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	BV _{DSS}	-30	--	--	V
Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	V _{GS(TH)}	-1	--	-3	V
Gate Body Leakage	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V _{DS} = -30V, V _{GS} = 0V	I _{DSS}	--	--	-1.0	μA
On-State Drain Current ^a	V _{DS} = -5V, V _{GS} = -10V	I _{D(ON)}	-50	--	--	A
Drain-Source On-State Resistance ^a	V _{GS} = -10V, I _D = -11A	R _{DS(ON)}	--	10	12	mΩ
	V _{GS} = -4.5V, I _D = -8.5A		--	15	19	
Forward Transconductance ^a	V _{DS} = -15V, I _D = -11A	g _{fs}	--	23	--	S
Diode Forward Voltage	I _S = -2.1A, V _{GS} = 0V	V _{SD}	--	--	-1.3	V
Dynamic^b						
Total Gate Charge	V _{DS} = -15V, I _D = -11A, V _{GS} = -10V	Q _g	--	64	--	nC
Gate-Source Charge		Q _{gs}	--	11	--	
Gate-Drain Charge		Q _{gd}	--	25	--	
Input Capacitance	V _{DS} = -8V, V _{GS} = 0V, f = 1.0MHz	C _{iss}	--	3680	--	pF
Output Capacitance		C _{oss}	--	930	--	
Reverse Transfer Capacitance		C _{rss}	--	620	--	
Switching^c						
Turn-On Delay Time	V _{DD} = -15V, R _L = 15Ω, I _D = -1A, V _{GEN} = -10V, R _G = 6Ω	t _{d(on)}	--	15	--	ns
Turn-On Rise Time		t _r	--	13	--	
Turn-Off Delay Time		t _{d(off)}	--	100	--	
Turn-Off Fall Time		t _f	--	53	--	

Notes:

- a. pulse test: PW ≤ 300μs, duty cycle ≤ 2%
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.



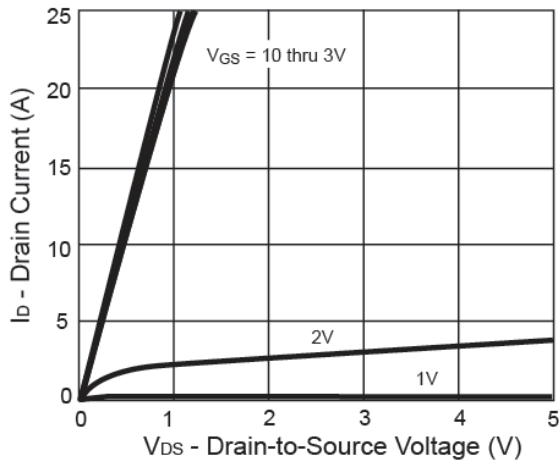
Switching Test Circuit



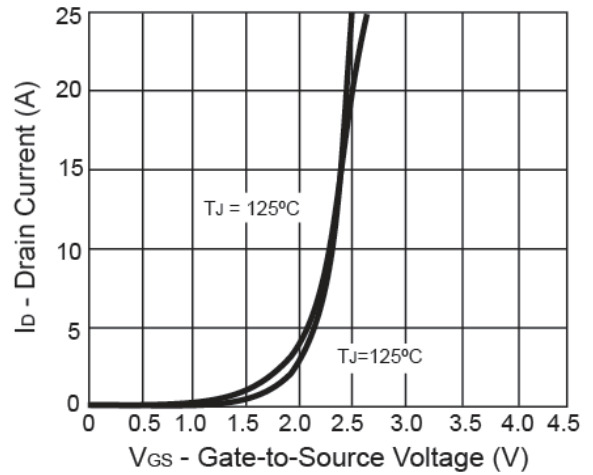
Switchin Waveforms

Electrical Characteristics Curve

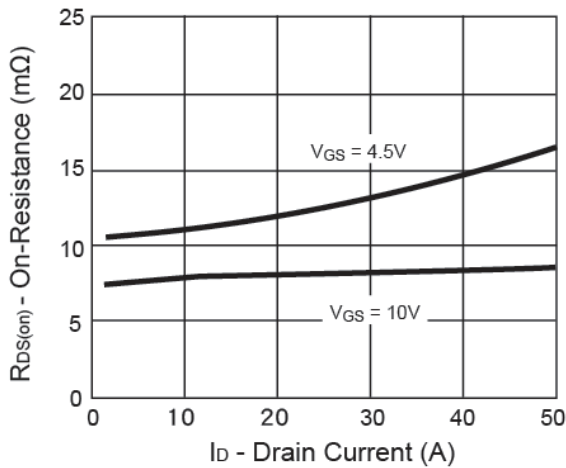
Output Characteristics



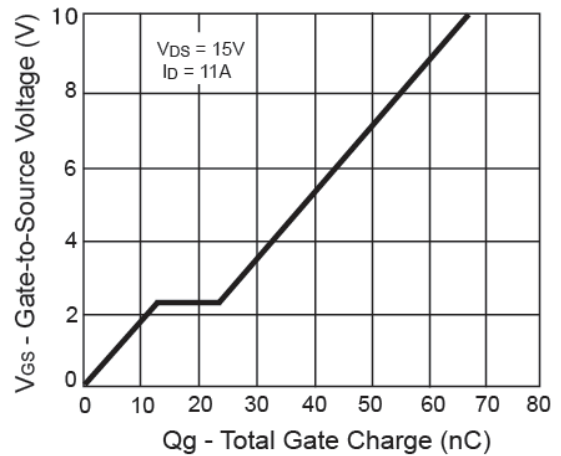
Transfer Characteristics



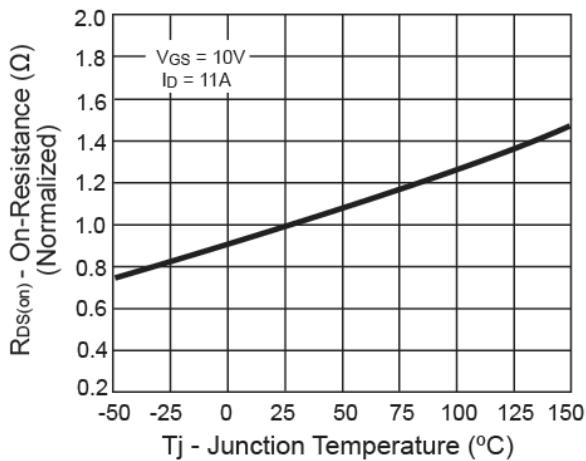
On-Resistance vs. Drain Current



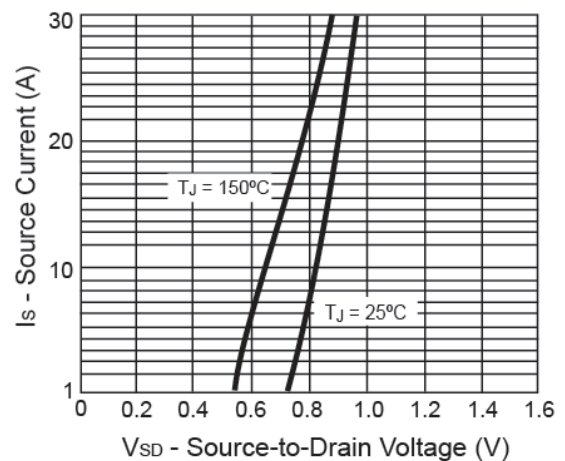
Gate Charge



On-Resistance vs. Junction Temperature

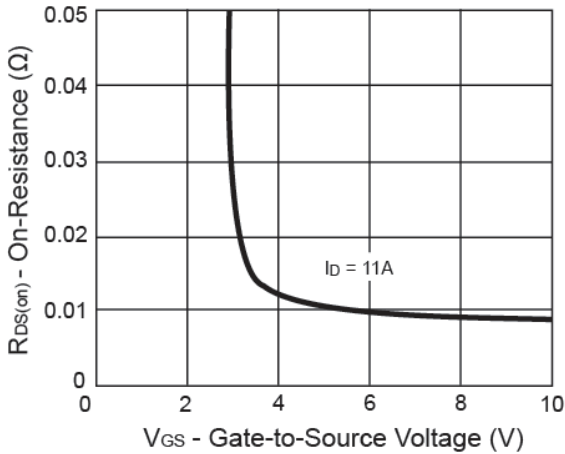


Source-Drain Diode Forward Voltage

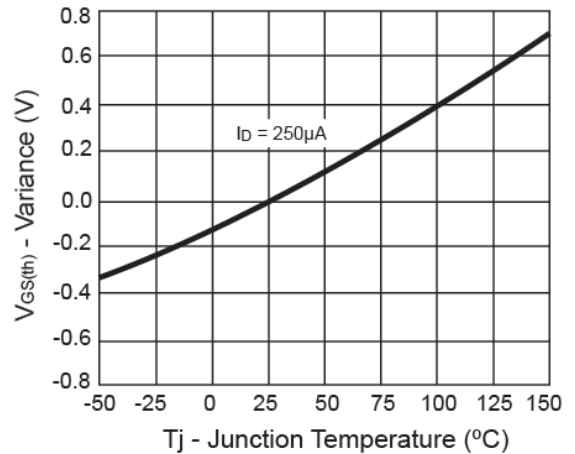


Electrical Characteristics Curve

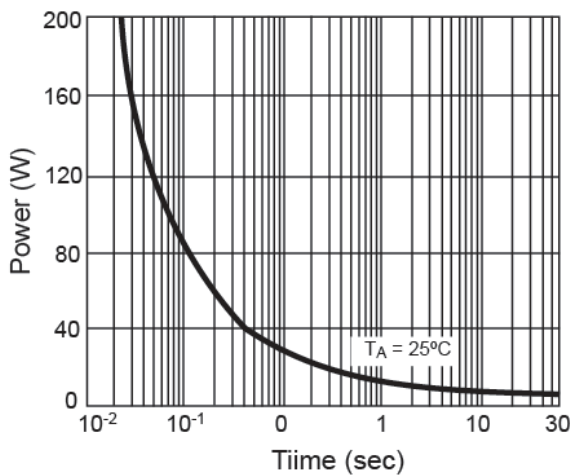
On-Resistance vs. Gate-Source Voltage



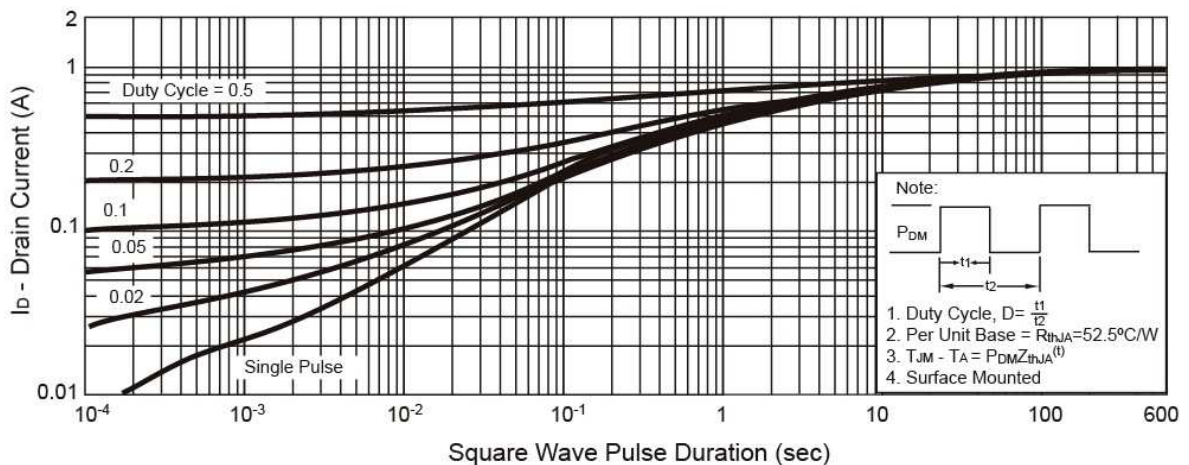
Threshold Voltage



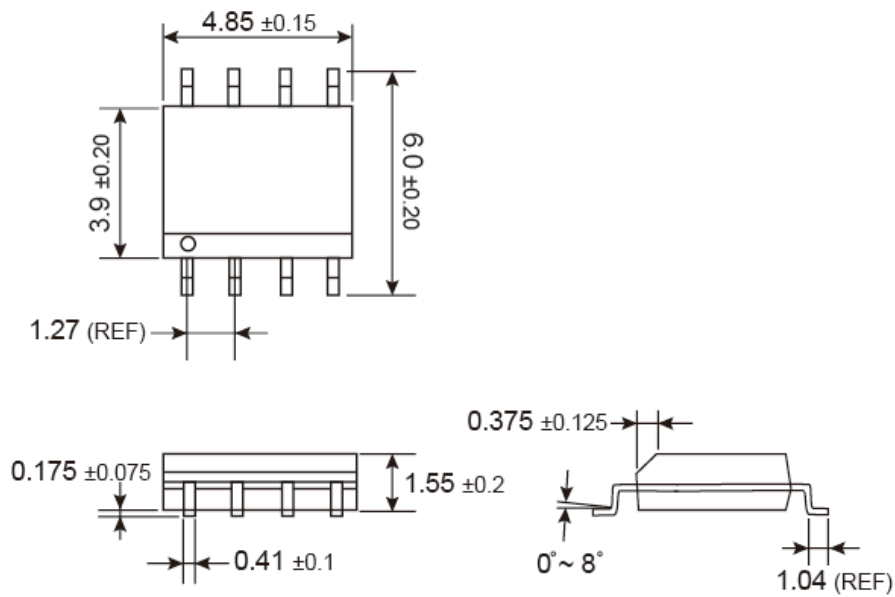
Single Pulse Power



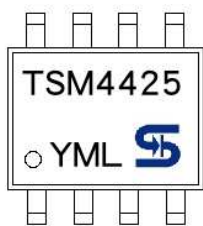
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOP-8 Mechanical Drawing



Marking Diagram



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan **P** =Feb **Q** =Mar **R** =Apr

S =May **T** =Jun **U** =Jul **V** =Aug

W =Sep **X** =Oct **Y** =Nov **Z** =Dec

L = Lot Code



TSM4425

30V P-Channel MOSFET

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