



EVB-PCI11414

Evaluation Kit

User's Guide

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ISBN: 979-8-3371-0027-2

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NOTES:

Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXXA”, where “XXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-PCI11414 Evaluation Kit User's Guide. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [Warranty Registration](#)
- [The Microchip Web Site](#)
- [Development Systems Customer Change Notification Service](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

This document describes how to use the EVB-PCI11414 Evaluation Kit as a demonstration platform optimized for portable applications. The manual layout is as follows:

- **Chapter 1. “Overview”** – This chapter shows a brief description of the EVB-PCI11414 Evaluation Kit.
- **Chapter 2. “Getting Started”** – This chapter provides information about the set-up and operation of the EVB-PCI11414 Evaluation Kit.
- **Chapter 3. “Hardware Configuration”** – This chapter includes information about the hardware configuration of the EVB-PCI11414 Evaluation Kit.
- **Appendix A. “Schematics”** – This appendix shows the schematic drawings of the EVB-PCI11414 Evaluation Kit.
- **Appendix B. “Bill of Materials”** – This appendix details the EVB-PCI11414 Evaluation Kit's bill of materials.
- **Appendix C. “PCB Silk Screens”** – This chapter shows the silk screen images of the EVB-PCI11414 Evaluation Kit.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	<i>MPLAB® IDE User's Guide</i>
	Emphasized text	...is the <i>only</i> compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	<u><i>File>Save</i></u>
Bold characters	A dialog button	Click OK
	A tab	Click the Power tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	#define START
	Filenames	autoexec.bat
	File paths	c:\mcc18\h
	Keywords	_asm, _endasm, static
	Command-line options	-Opa+, -Opa-
	Bit values	0, 1
	Constants	0xFF, 'A'
Italic Courier New	A variable argument	file.o, where <i>file</i> can be any valid filename
Square brackets []	Optional arguments	mcc18 [options] file [options]
Curly brackets and pipe character: { }	Choice of mutually exclusive arguments; an OR selection	errorlevel {0 1}
Ellipses...	Replaces repeated text	var_name [, var_name...]
	Represents code supplied by user	void main (void) { ... }

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- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICKit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICKit 2 and 3.

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- Technical Support

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Technical support is available through the web site at:

<http://www.microchip.com/support>

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003598B (11-14-24)	Section 2.2 “Kit Contents”	Removed “PCIe slot retention clip (installed)” from the list.
	All	Removed the “Preliminary - NDA Required” marking.
DS50003598A (11-24-23)	Initial release	

Chapter 1. Overview

1.1 EVALUATION BOARD OVERVIEW

The EVB-PCI11414 is a demonstration and evaluation platform that provides the necessary requirements and interface options for evaluating the PCI11414, a single-chip PCIe[®] switch with an integrated USB 3.2 Gen 2 host controller and programmable I/O options (I²C/SPI/UART/GPIO), on a six-layer RoHS-compliant Printed Circuit Board (PCB). This kit allows the user to gain an understanding of the product and accelerate the integration of the PCI11414 into the user's design.

The evaluation platform includes four USB-IF compliant downstream USB host ports: One (1) USB Type-C[®] at USB 3.2 Gen 2 SuperSpeed+ port and three (3) USB Type-A at USB 2.0 High-Speed.

This evaluation platform also includes 1 downstream PCIe Gen 3 switch port (1 lane * 8 GT/s), and an on-board KSZ9131RNX Ethernet transceiver (10/100/1000 Mbps) implements 4 channels of RS-232/485 connectivity.

The EVB-PCI11414 demonstrates its PCIe, USB Host, and I²C/SPI/UART/GPIO driver compatibility in Linux[®] and Microsoft[®] Windows[®] 10.

See [Section 1.2 “Features”](#) for more information.

Note: 12V/48 Watt supply is required for maximal use of all interfaces of this evaluation hardware.
--

1.2 FEATURES

The EVB-PCI11414 Evaluation Kit has the following features:

- The EVB-PCI11414 in a 132-pin Dual-row QFN (DQFN) RoHS compliant package
- Four USB-IF-compliant Downstream USB host ports:
 - One USB Type-C[®] 3.2 Gen 2 SuperSpeed+ downstream port
 - Three USB Type-A 2.0-only downstream ports
- One downstream PCIe Gen 4 (1 lane * 8GT/s) port on a PCIe x4 slot connector
- Four channels of RS-232/485
- Two banks of programmable I/Os
- On-board I²C serial EEPROM for EVB system configuration and function customization
- One optional I²C or SPI target configuration bus
- Operates from a single voltage (+12.0 V, regulated) external power supply
- On-board 25 MHz crystal
- Single on-board +5 V, regulator
- Single on-board +3.3 V, regulator
- Single on-board +1.1 V, regulator
- USB Port Power LED indicators
- Reset LED indicator
- Regulator LED indicators for 5V, 3.3V, and 1.1V outputs

- ### 1.3 BLOCK DIAGRAM

FIGURE 1-1: EVB-PCI11414 BLOCK DIAGRAM



- *PCI11414 PCIe Switch with Integrated USB 3.2 Gen 2 Host Controller, Ethernet MAC & Programmable I/O Data Sheet*
- *AN5190 PCI1xxxx Windows Driver Installation Guide*

Table 1-1 lists the terms and acronyms used in this document:

Acronym	Definition
DFP	Downstream Facing Port
EVB	Evaluation Board
OTP	One Time Programmable memory
Type-C	USB-IF standard reversible 24-pin USB Connector
USB-IF	USB Integrators Forum. Collection of corporate sponsored members responsible for developing USB specifications.
Gen 2	USB Specification 3.2 Gen 2

Chapter 2. Getting Started

2.1 INTRODUCTION

The Microchip EVB-PCI11414 is designed for flexible configuration solutions. It can be configured via external EEPROM (the EVB-PCI11414 configuration resides in EEPROM), internal One-Time-Programmable (OTP) memory, and/or external I²C/SPI controller (optional).

To modify the functionality of the EVB-PCI11414, Microchip provides a software programming tool, MPLAB[®] Connect Configurator, for configuring PCI11414 functions or registers.

For additional information on the MPLABCC programming tool, refer to Software Libraries at www.microchip.com.

Note: Older SPI documentation uses the terminologies “master” and “slave.” The equivalent Microchip terminologies used in this document are “controller” and “target,” respectively.

2.2 KIT CONTENTS

The EVB-PCI11414 Evaluation Kit includes the basic equipment necessary for evaluation. The item included in the kit is:

1. EVB-PCI11414 Evaluation Board

2.3 RECOMMENDED EQUIPMENT

The following are the recommended hardware for the EVB-PCI11414 Evaluation Kit:

- **12V DC Power Supply:** The EVB-PCI11414 includes a 5.5x2.5x12 mm DC barrel jack, which is compatible with AC/DC adapters including the Cincon TRH70A120-12E01-Level-VI.
- **PCIe Riser Cable:** This evaluation board is best used on an electronics bench-top for ease of access to its interfaces and headers. It is recommended to attach a PCIe riser cable between the PC motherboard add-in-card slot and the EVB-PCI11414 PCIe edge connector to provide enough distance from desktop PC chassis:
 - 0.25m cable: Samtec PCIEC-064-0250-EC-EM-P-85
 - 0.5m cable: Samtec PCIEC-064-0500-EC-EM-P-85
- **DE-9 Male to 10-pin (2x5) IDC Adapter Cable:** This evaluation board includes two (2) UART transceivers which may be configured for RS-232 or RS-485 connectivity. The RS-232 signals are available on a 10-pin header compatible with commercial-off-the-shelf adapters for DE-9 interface including, CablesOnline DB9 Male to 10-Pin (2x5) IDC Female Motherboard Header RS232 Serial Adapter Cable, AD-I01.

2.4 QUICK START

Perform the following steps to quickly start using the board:

1. Ensure that your Host PC is powered OFF before proceeding.
2. Configure jumpers according to default settings described in [Section 3.1.4 “Jumper Settings and Defaults”](#).
3. Connect the recommended PCIe riser cable from P1, to the PCIe card slot in Host PC.
4. Connect +12 VDC power supply to one of the three (3) power input connectors: J15, J27, or J30.
5. Enable the +12 VDC power supply output.
6. Set the Power mode select switch SW1 into position [1-2] for PCIe-Connected mode.
7. Power ON the Host PC.

Note: With Power Mode Select Switch SW1 in position [1-2], the EVB-PCI11414 becomes powered, in sync with the Host PC.

8. If not already installed, install the following drivers for your OS (See *AN5190 PCIxxxx Windows Driver Installation Guide*):
 - Microchip PCI11414 Ethernet driver
 - Microchip PCI11414 GPIO peripheral drivers.
 - Microchip PCI11414 I²C peripheral drivers.
 - Microchip PCI11414 SPI peripheral drivers.
 - Microchip PCI11414 UART peripheral drivers.
9. Verify complete EVB-PCI11414 PCIe function enumeration by checking lspci (or equivalent) command output and confirming if the Vendor/Device IDs combinations in [Table 2-1](#) are present.

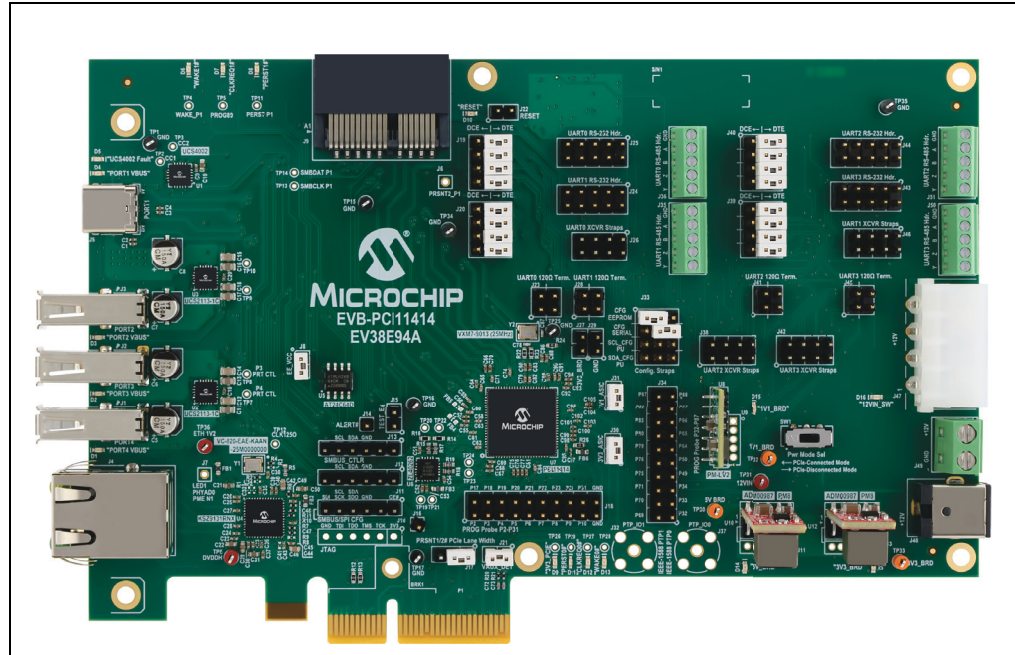
TABLE 2-1: EVB-PCI11414 SUBSYSTEM VENDOR (VID) AND DEVICE (DID) IDENTIFIERS

Endpoint	Vendor ID(Hex) : Device ID (Hex)
xHCI Controller	0x1055:0xA030
I ² C Controller	0x1055:0xA033
SPI Controller	0x1055:0xA034
GPIO/OTP/EEPROM Multifunction Module	0x1055:0xA035
PCIe Switch Ports	0x1055:[0xA038-0xA03C]

Chapter 3. Hardware Configuration

3.1 HARDWARE CONFIGURATION OPTIONS

FIGURE 3-1: EVB-PCI11414 REV B (TOP-SIDE)



3.1.1 Power Input Options

The EVB-PCI11414 is intended to be powered from one of three (3) external +12 VDC power supply connections:

1. J47 – 4-pin ATX Peripheral Power connector
2. J48 – AC/DC barrel jack
3. J49 – 2-pin screw terminal

Note: Connect and enable one (1) power supply input at a time only.

3.1.2 Power Mode Select Switch

The EVB-PCI11414 has a Power Mode Select switch SW1 with two (2) modes, which must be chosen prior to applying power to the board. See [Table 3-1](#).

TABLE 3-1: POWER MODE SELECT OPTIONS

SW1 Position	Power Mode
1-2	PCIe-connected mode
2-3	PCIe-disconnected mode

3.1.2.1 PCIE-CONNECTED MODE

The EVB-PCI11414 on-board voltage regulators will be automatically switched on in synchronization with when the +12 VDC power is enabled in the Host PC's PCIe add-in-card slot.

Perform the following steps to use this power mode:

1. Set SW1 to position [1-2].
2. Ensure that the Host PC is powered OFF, then connect EVB-PCI11414's P1 connector to the Host PCIe slot.
3. Connect external +12 VDC power supply (powered-OFF) to one of the three power input options.
4. Enable external +12 VDC power supply output and observe whether LED D16 is illuminated. This external power supply will remain isolated from EVB-PCI11414 main circuitry until the Host PC PCIe power is enabled. Now the EVB-PCI11414 shall become fully powered by the external power supply in synchronization with the Host PC's PCIe power being enabled.

Note: This mode is intended to allow the EVB-PCI11414 to be entirely self-powered for the highest power integrity and compatibility with most host systems and PCIe riser cables.

3.1.2.2 PCIE-DISCONNECTED MODE

This mode can be selected when the EVB-PCI11414 is used independently or without a PCIe connection (e.g. for I²C EEPROM programming).

The evaluation board power can be manually controlled via SW1 and/or the external +12 VDC power supply.

Perform the following steps to use this power mode:

1. Ensure that there is no PCIe connection to EVB-PCI11414's P1 connector.
2. Set SW1 to position [2-3].
3. Connect external +12 VDC power supply (powered OFF) to one of the three power input options.
4. Enable external +12 VDC power supply output and observe whether LED D16 is illuminated. Now the EVB-PCI11414 shall become fully powered by the external power supply.

Note: In this mode, the evaluation board power can be controlled by either the +12 VDC power supply's enable control or by switching SW1 back into position [1-2].

3.1.3 Board Reset

The evaluation board does not include a momentary Reset switch. Instead, it includes a Reset jumper.

Note: Resetting of EVB-PCI11414 during the runtime operation of the evaluation board when connected to a Host PC's PCIe slot is not supported. Therefore, all intentional Reset actions shall occur via installation of jumper J22.

When the EVB-PCI11414 is reset via J22 during runtime operation, the PCIe-dependent functions of the PCI11414 are not expected to function normally afterwards.

Reset of EVB-PCI11414 shall normally occur prior to PCIe enumeration, as the EVB-PCI11414's on-board 3.3V voltage regulator output becomes stable.

3.1.4 Jumper Settings and Defaults

This section describes the functionality of the multiple jumpers included in EVB-PCI11414. The jumper graphics indicate the intended default positions of the jumpers as they would appear with the board oriented with the Microchip logo upright from the user's perspective.

Note: Two-pin jumper headers are not graphically shown in [Table 3-3](#).

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS

Reference	Jumper Function	Default Position	Description
J22	Board Reset	Open [1-2]	Install [1-2] to assert Reset for the PCI11414, KSZ9131 Ethernet transceiver, and MAX3161 RS-232/485 transceivers. Open [1-2] to deassert Reset for PCI11414, KSZ9131 Ethernet transceiver, and MAX3161 RS-232/485 transceivers.
J30	PCI11414 3.3V Power Measurement	Install [1-2]	Install [1-2] to connect 3.3V power (3V3_BRD) to the PCI11414 ASIC 3.3V power pins (3V3_ASIC) Open [1-2] to connect an ammeter across the jumper pins, and perform measurement of PCI11414 ASIC 3.3V power consumption.
J31	PCI11414 1.1V Power Measurement	Install [1-2]	Install [1-2] to connect 1.1V power (1V1_BRD) to the PCI11414 ASIC 1.1V power pins (1V1_ASIC) Open [1-2] to connect an ammeter across the jumper pins, and perform the measurement of PCI11414 ASIC 1.1V power consumption.

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J33	PCI11414 Configuration Straps	Install [1-2] [5-6] Open [7-8-9] [10-11-12]	Note that with the default jumper positions, PCI11414 will load its configuration from EEPROM. Install [1-2] to assert PCI11414 CONFIG_EEPROM strap and allow I²C EEPROM configuration to be loaded. Install [2-3] to deassert PCI11414 CONFIG_EEPROM strap and prevent I²C EEPROM configuration from being loaded. Install [4-5] to assert PCI11414 CONFIG_SERIAL strap and allow configuration via either the SMBus or SPI target interface. Note that when jumper [4-5] is installed, PCI11414 will enable its SPI Target bus when the SMBUS_TGT_SCL/SPI_TGT_CLK and SMBUS_TGT_SDA/SPI_TGT_SDO pins are both detected as logic LOW upon exiting Reset state. Otherwise, when those pins are detected as logic high upon exiting Reset state, PCI11414 will enable its SMBus target interface. Install [5-6] to deassert PCI11414 CONFIG_SERIAL strap and prevent configuration via either the SMBus or SPI target interface. To enable PCI11414 configuration via SPI interface, install [8-9] and [11-12] to connect 100 kΩ pull-downs to the PCI11414 SMBUS_TGT_SCL and SMBUS_TGT_SDA pins respectively. Note that when jumpers [4-5], [7-8], and [10-11] are each installed, the PCI11414 will await configuration from SMBus target interface. To enable PCI11414 configuration via SMBus interface, install [7-8] and [10-11] to connect 1 kΩ pull-ups to the PCI11414 SMBUS_TGT_SCL and SMBUS_TGT_SDA pins, respectively.
J8	I ² C EEPROM VCC Power Enable	Install [1-2]	Install [1-2] to connect 3.3V power to the I²C EEPROM device. Open [1-2] to disconnect 3.3V power to the I²C EEPROM device.
J15	PCI11414 JTAG TAP Enable	Open [1-2]	Install [1-2] to force PCI11414 into Test mode with JTAG TAP enabled (prevents normal system operation of PCI11414). Open [1-2] to operate PCI11414 in normal, Non-test mode with JTAG TAP disabled.

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J17	PCIe PRSNT# Lane Width Selection	Install [1-2]	Install [1-2] to identify the EVB-PCI11414 as a 4-lane/x4 add-in-card. Install [2-3] to identify the EVB-PCI11414 as a 1-lane/x1 add-in-card. Note that leaving this EVB jumper position open may cause host system not to detect the presence of the EVB-PCI11414. It is recommended to always keep the jumper installed in J17 into one of its positions.
J21	PCIe VAUX_DET	Install [1-2]	Install [1-2] to allow PCI11414 to detect PCIe 3.3Vaux presence (e.g. for implementing a PCIe Warm Reset capability, or supporting PME from PCIe D3cold state) Open [1-2] to decline support for PME from PCIe D3cold state.
J19	UART0 DTE/DCE Mode Selection	Install [2-3] [5-6] [8-9] [11-12]	This jumper set is for re-routing of UART signals to the appropriate DE-9 connector pins for either a "DTE" (Data Terminal Equipment) or "DCE" (Data Communications Equipment) implementation. The default jumper settings are for a "DTE" implementation. See schematic for explicit detail of signals routing for the two (2) jumper options. This jumper set shall be configured only in one of the following ways: • DTE implementation: Install [1-2], [4-5], [7-8], and [10-11]. • DCE implementation: Install [2-3], [5-6], [8-9], and [11-12].

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J26	UART0 Transceiver Configuration	Open [1-2] [3-4] [7-8] Install [5-6]	This jumper set is for the pin strap configuration of Analog Devices MAX3161 RS-232/485 Transceiver. Install [1-2] to force MAX3161 into SHDN state. Install [3-4] to configure MAX3161 into FAST mode; disables slew rate limiting. Install [5-6] to configure MAX3161 into RS-232 mode. Install [7-8] to configure MAX3161 into Half-duplex mode. Open [1-2] to force MAX3161 into normal operational state. Open [3-4] to configure MAX3161 into normal mode; enables slew rate limiting. Open [5-6] to configure MAX3161 into RS-485 mode. Open [7-8] to configure MAX3161 into Full-duplex mode. Consult the Analog Devices <i>MAX3161 Data-Sheet</i> for complete details regarding these settings.
J23	UART0 RS-485 Terminations	Open [1-2] [3-4]	This jumper set is to connect discrete 120Ω terminations onto the RS-485 bus. Install [1-2] to connect 120Ω termination between the "A" and "B" RS-485 bus signals. Install [1-2] to connect 120Ω termination onto the "Y" and "Z" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination between the "A" and "B" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination onto the "Y" and "Z" RS-485 bus signals.

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J20	UART1 DTE/DCE Mode Selection	Install [2-3] [5-6] [8-9] [11-12]	This jumper set is for re-routing of UART signals to the appropriate DE-9 connector pins for either a "DTE" (Data Terminal Equipment) or "DCE" (Data Communications Equipment) implementation. The default jumper settings are for a "DTE" implementation. See schematic for explicit detail of signals routing, for the two (2) jumper options. This jumper set shall be configured only in one of the following ways: • DTE implementation: Install [1-2], [4-5], [7-8], and [10-11]. • DCE implementation: Install [2-3], [5-6], [8-9], and [11-12].
J46	UART1 Transceiver Configuration	Open [1-2] [3-4] [7-8] Install [5-6]	This jumper set is for the pin strap configuration of Analog Devices MAX3161 RS-232/485 Transceiver. Install [1-2] to force MAX3161 into SHDN state. Install [3-4] to configure MAX3161 into FAST mode; disables slew rate limiting. Install [5-6] to configure MAX3161 into RS-232 mode. Install [7-8] to configure MAX3161 into Half-duplex mode. Open [1-2] to force MAX3161 into normal operational state. Open [3-4] to configure MAX3161 into normal mode; enables slew rate limiting. Open [5-6] to configure MAX3161 into RS-485 mode. Open [7-8] to configure MAX3161 into Full-duplex mode. Consult the Analog Devices <i>MAX3161Data Sheet</i> for complete details regarding these settings.

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J28	UART1 RS-485 Terminations	Open [1-2] [3-4]	This jumper set is to connect discrete 120Ω terminations onto the RS-485 bus. Install [1-2] to connect 120Ω termination between the "A" and "B" RS-485 bus signals. Install [1-2] to connect 120Ω termination onto the "Y" and "Z" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination between the "A" and "B" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination onto the "Y" and "Z" RS-485 bus signals.
J40	UART2 DTE/DCE Mode Selection	Install [2-3] [5-6] [8-9] [11-12]	This jumper set is for rerouting of UART signals to the appropriate DE-9 connector pins for either a "DTE" (Data Terminal Equipment) or "DCE" (Data Communications Equipment) implementation. The default jumper settings are for a "DTE" implementation. See schematic for explicit detail of signals routing, for the two (2) jumper options. This jumper set shall be configured only in one of the following ways: • DTE implementation: Install [1-2], [4-5], [7-8], and [10-11]. • DCE implementation: Install [2-3], [5-6], [8-9], and [11-12].

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J38	UART2 Transceiver Configuration	Open [1-2] [3-4] [7-8] Install [5-6]	This jumper set is for the pin strap configuration of Analog Devices MAX3161 RS-232/485 Transceiver. Install [1-2] to force MAX3161 into SHDN state. Install [3-4] to configure MAX3161 into FAST mode; disables slew rate limiting. Install [5-6] to configure MAX3161 into RS-232 mode. Install [7-8] to configure MAX3161 into Half-duplex mode. Open [1-2] to force MAX3161 into normal operational state. Open [3-4] to configure MAX3161 into normal mode; enables slew rate limiting. Open [5-6] to configure MAX3161 into RS-485 mode. Open [7-8] to configure MAX3161 into Full-duplex mode. Consult the Analog Devices <i>MAX3161 Data Sheet</i> for complete details regarding these settings.
J41	UART2 RS-485 Terminations	Open [1-2] [3-4]	This jumper set is to connect discrete 120Ω terminations onto the RS-485 bus. Install [1-2] to connect 120Ω termination between the "A" and "B" RS-485 bus signals. Install [1-2] to connect 120Ω termination onto the "Y" and "Z" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination between the "A" and "B" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination onto the "Y" and "Z" RS-485 bus signals.

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J39	UART3 DTE/DCE Mode Selection	Install [2-3] [5-6] [8-9] [11-12]	This jumper set is for re-routing of UART signals to the appropriate DE-9 connector pins for either a "DTE" (Data Terminal Equipment) or "DCE" (Data Communications Equipment) implementation. The default jumper settings are for a "DTE" implementation. See schematic for explicit details of signal routing for the two (2) jumper options. This jumper set shall be configured only in one of the following ways: - DTE implementation: Install [1-2], [4-5], [7-8], and [10-11]. - DCE implementation: Install [2-3], [5-6], [8-9], and [11-12].
J42	UART3 Transceiver Configuration	Open [1-2] [3-4] [7-8] Install [5-6]	This jumper set is for the pin strap configuration of Analog Devices MAX3161 RS-232/485 Transceiver. Install [1-2] to force MAX3161 into SHDN state. Install [3-4] to configure MAX3161 into FAST mode; disables slew rate limiting. Install [5-6] to configure MAX3161 into RS-232 mode. Install [7-8] to configure MAX3161 into Half-duplex mode. Open [1-2] to force MAX3161 into normal operational state. Open [3-4] to configure MAX3161 into normal mode; enables slew rate limiting. Open [5-6] to configure MAX3161 into RS-485 mode. Open [7-8] to configure MAX3161 into Full-duplex mode. Consult the Analog Devices <i>MAX3161 Data Sheet</i> for complete details regarding these settings.

TABLE 3-3: JUMPER SETTINGS AND DEFAULTS (CONTINUED)

Reference	Jumper Function	Default Position	Description
J45	UART3 RS-485 Terminations	Open [1-2] [3-4]	This jumper set is to connect discrete 120Ω terminations onto the RS-485 bus. Install [1-2] to connect 120Ω termination between the "A" and "B" RS-485 bus signals. Install [1-2] to connect 120Ω termination onto the "Y" and "Z" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination between the "A" and "B" RS-485 bus signals. Open [1-2] to disconnect 120Ω termination onto the "Y" and "Z" RS-485 bus signals.

3.1.5 Interface Connectors

3.1.5.1 P1 – PCIE UPSTREAM (MALE EDGE CONNECTOR)

The “upstream” connection towards the PCIe Root Complex is implemented as a standard 4-lane/x4 PCIe add-in-card male edge connector (64 positions).

The design of EVB-PCI11414 is intended to prioritize hands-on or board-on-benchtop use and may not be mechanically compatible with all PCIe host systems. Therefore, a 0.25m to 0.5m PCIe riser cable is strongly recommended to be connected between connector P1 and the upstream platform's PCIe add-in-card slot.

The upstream platform's 12V and 3.3V power rails are routed to the EVB-PCI11414 via this P1 connector. However, EVB-PCI11414 is designed not to substantially load these power rails as it includes options for external 12V power supplies to become “self-powered”.

Note: The “self-powered” capability of the EVB-PCI11414 is meant to accommodate PCIe->M.2 adapters where 12V is not available and ensure enough power availability for all four USB ports to be operated.

SMBus connectivity to PCI11414's SMBus target interface is available via the P1 PCIe upstream connector by default, with the following 0Ω resistors installed:

- R12 – SMBUS SCL
- R13 – SMBUS SDA

Optional JTAG connectivity to PCI11414 is available via P1, when the following 0Ω resistors are installed:

- R128 – JTAG TCK
- R140 – JTAG TDI
- R139 – JTAG TDO
- R133 – JTAG TMS

3.1.5.2 J9 – PCIE DOWNSTREAM (FEMALE ADD-IN-CARD SLOT)

The “downstream” connection towards an external PCIe device is implemented as a standard 1-lane/x1 PCIe add-in-card female receptacle (36 positions). PCIe Hot Plug is not implemented on this PCIe Downstream connector.

Both the PCIe 3.3V and 3.3 Vaux power pins are sourced from the EVB-PCI11414 3V3_BRD regulator.

3.1.5.3 J5 – USB 3.2 (10 GBPS) USB TYPE-C® (PORT 1)

J5 is a USB-IF certified (TID=5200000514) USB Type-C® receptacle associated with Port 1 of the PCI11414's xHCI Host Controller.

The USB Type-C implementation is a source-only downstream-facing port which is capable of sourcing 5V at 3A VBUS via a dual-channel UCS2113 5V current limiting switch. The USB 3.2 data connections are routed directly to the PCI11414 to utilize its "internal mux" in achieving the reversibility of USB Type-C. Likewise, the CC1 and CC2 pins are also routed directly to PCI11414's integrated USB Type-C controller.

VCONN power of up to 1W can be sourced from this USB Type-C port in to accommodate USB 3.2 active redriver cables.

The presence of 5V VBUS power on J5 is indicated by LED D4.

3.1.5.4 J3 – USB 2.0 (480 MBPS) USB TYPE-A (PORT 2)

J3 is a USB-IF certified (TID=63000197) USB Type-A receptacle associated with Port 2 of the PCI11414's xHCI Host Controller.

The USB Type-A implementation is a source-only downstream-facing port, which is capable of sourcing 5V at 3A VBUS via a dual-channel UCS2113 5V current limiting switch.

The presence of 5V VBUS power on J3 is indicated by LED D3.

3.1.5.5 J2 – USB 2.0 (480 MBPS) USB TYPE-A (PORT 3)

J2 is a USB-IF certified (TID=63000197) USB Type-A receptacle associated with Port 3 of the PCI11414's xHCI Host Controller.

The USB Type-A implementation is a source-only downstream-facing port which is capable of sourcing 5V at 500 mA VBUS via a dual-channel UCS2113 5V current limiting switch.

The presence of 5V VBUS power on J2 is indicated by LED D2.

3.1.5.6 J1 – USB 2.0 (480 MBPS) USB TYPE-A (PORT 4)

J1 is a USB-IF certified (TID=63000197) USB Type-A receptacle associated with Port 4 of the PCI11414's xHCI Host Controller.

The USB Type-A implementation is a source-only downstream-facing port which is capable of sourcing 5V at 500 mA VBUS via a dual-channel UCS2113 5V current limiting switch.

The presence of 5V VBUS power on J1 is indicated by LED D1.

3.1.5.7 J4 ETHERNET (10/100/1000BASE-T) RJ-45

This RJ-45 receptacle is a "magjack"-style connector which includes the necessary magnetic coupling for the 10/100/1000BASE-T KSZ9131 transceiver, as well as the dual link status/activity and collision LEDs.

3.1.5.8 J25 – UART0 RS-232 DE-9 ADAPTER HEADER

This connector is for the RS-232 mode of connectivity associated with U23 MAX3161 RS-232/485 transceiver.

To use this DE-9 connector for RS-232 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J19 must have jumpers installed into either the DTE, or DCE positions. See J19

detailed description in [Section 3.1.4 “Jumper Settings and Defaults”](#).

- J26 must have jumper installed in position [5-6] to configure MAX3161 into RS-232 mode.

Connect IDC-10 DE-9 adapter cable to J25 to interface with this UART using common RS-232 cables.

3.1.5.9 J36 – UART0 RS-485 HEADER

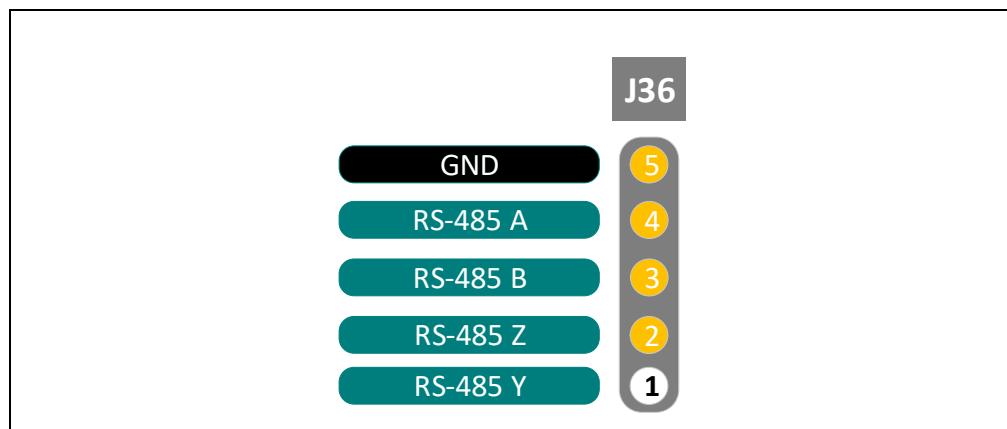
This header is for the RS-485 mode of connectivity associated with U23 MAX3161 RS-232/485 transceiver.

To use this header for RS-485 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J26 must be open in position [5-6] to configure MAX3161 into RS-485 mode.
- J23 must be jumpered according to the RS-485 bus topology's requirements.

[Figure 3-2](#) shows the J36 signal pinout.

FIGURE 3-2: J36 SIGNAL PINOUT



3.1.5.10 J24 – UART1 RS-232 DE-9 ADAPTER HEADER

This connector is for the RS-232 mode of connectivity associated with U15 MAX3161 RS-232/485 transceiver.

To use this DE-9 connector for RS-232 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J20 must have jumpers installed into either the DTE or DCE position. See detailed description on J20 in [Section 3.1.4 “Jumper Settings and Defaults”](#).
- J46 must have a jumper installed in position [5-6] to configure MAX3161 into RS-232 mode.

3.1.5.11 J35 – UART1 RS-485 HEADER

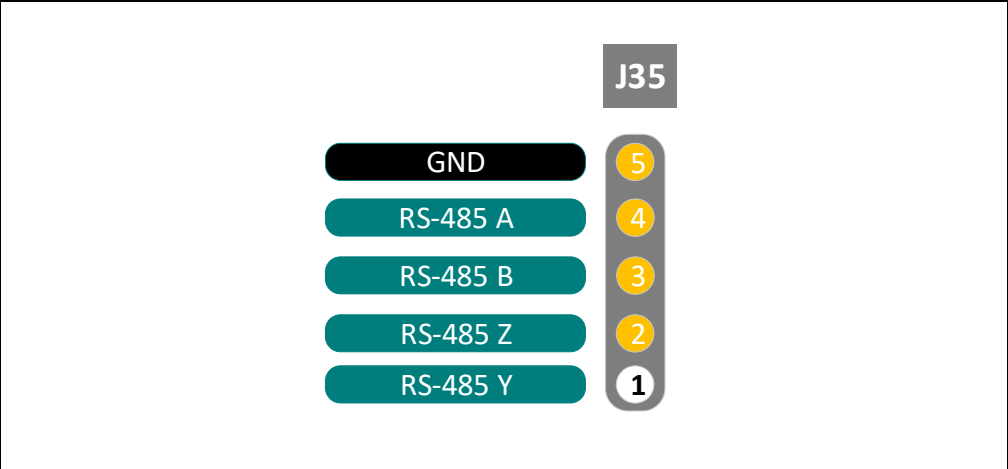
This header is for the RS-485 mode of connectivity associated with U15 MAX3161 RS-232/485 transceiver.

To use this header for RS-485 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J46 must be open in position [5-6] to configure MAX3161 into RS-485 mode.
- J28 must be jumpered according to the RS-485 bus topology's requirements.

[Figure 3-3](#) shows the J35 the signal pinout.

FIGURE 3-3: J35 SIGNAL PINOUT



3.1.5.12 J44 – UART2 RS-232 DE-9 ADAPTER HEADER

This connector is for the RS-232 mode of connectivity associated with U16 MAX3161 RS-232/485 transceiver.

To use this DE-9 connector for RS-232 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J40 must have jumpers installed into either the DTE, or DCE positions. See J40 detailed description in [Section 3.1.4 “Jumper Settings and Defaults”](#).
- J38 must have jumper installed in position [5-6] to configure MAX3161 into RS-232 mode.

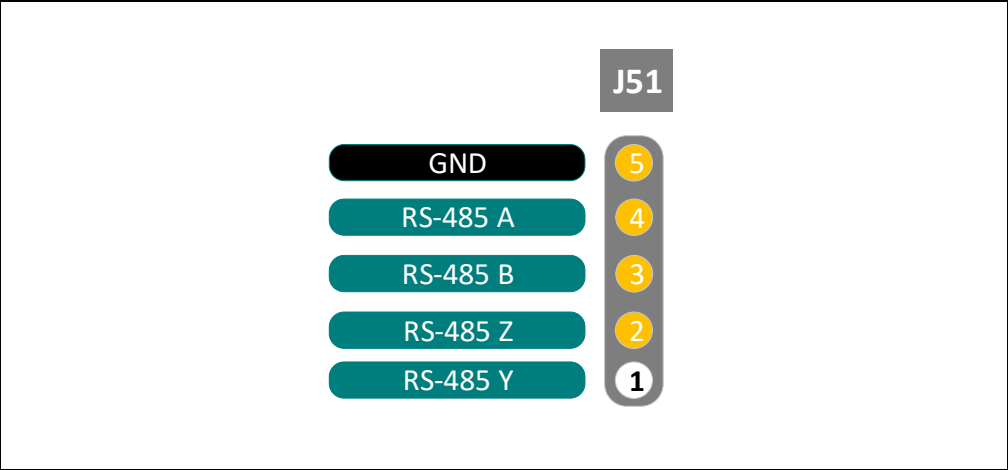
3.1.5.13 J51 – UART2 RS-485 HEADER

This header is for the RS-485 mode of connectivity associated with U16 MAX3161 RS-232/485 transceiver.

To use this header for RS-485 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J38 must be open in position [5-6] to configure MAX3161 into RS-485 mode.
- J41 must be jumpered according to the RS-485 bus topology's requirements.

FIGURE 3-4: J51 SIGNAL PINOUT



3.1.5.14 J43 – UART3 RS-232 DE-9 ADAPTER HEADER

This connector is for the RS-232 mode of connectivity associated with U14 MAX3161 RS-232/485 transceiver.

To use this DE-9 connector for RS-232 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J39 must have jumpers installed into either the DTE, or DCE positions. See J39 detailed description in [Section 3.1.4 “Jumper Settings and Defaults”](#).
- J42 must have jumper installed in position [5-6] to configure MAX3161 into RS-232 mode.

J43 signal pinout is aligned to standardized RS-232 pinout on DE-9 for either DTE, or DCE depending upon the configuration of J39.

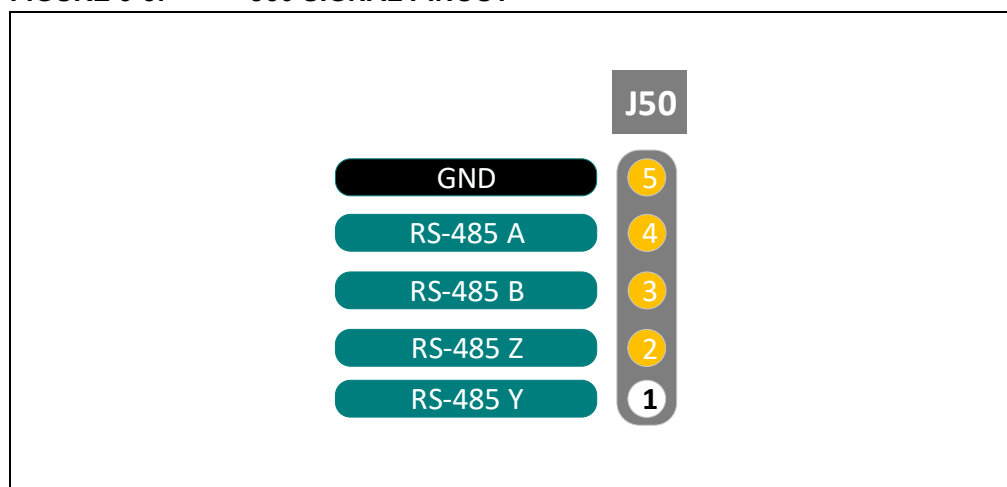
3.1.5.15 J50 – UART3 RS-485 HEADER

This header is for the RS-485 mode of connectivity associated with U14 MAX3161 RS-232/485 transceiver.

To use this header for RS-485 connectivity, ensure that the corresponding configuration jumpers are set appropriately:

- J42 must be open in position [5-6] to configure MAX3161 into RS-485 mode.
- J45 must be jumpered according to the RS-485 bus topology's requirements.

FIGURE 3-5: J50 SIGNAL PINOUT



3.1.5.16 J11 – SMBUS/SPI TARGET (PICKIT™ SERIAL)

This PICKIT™ Serial-compatible connector provides access to either the SMBus Target, or SPI Target configuration bus of PCI11414, depending upon how the J33 PCI11414 Configuration Straps are configured (See J33 in [Section 3.1.4 “Jumper Settings and Defaults”](#) for details.).

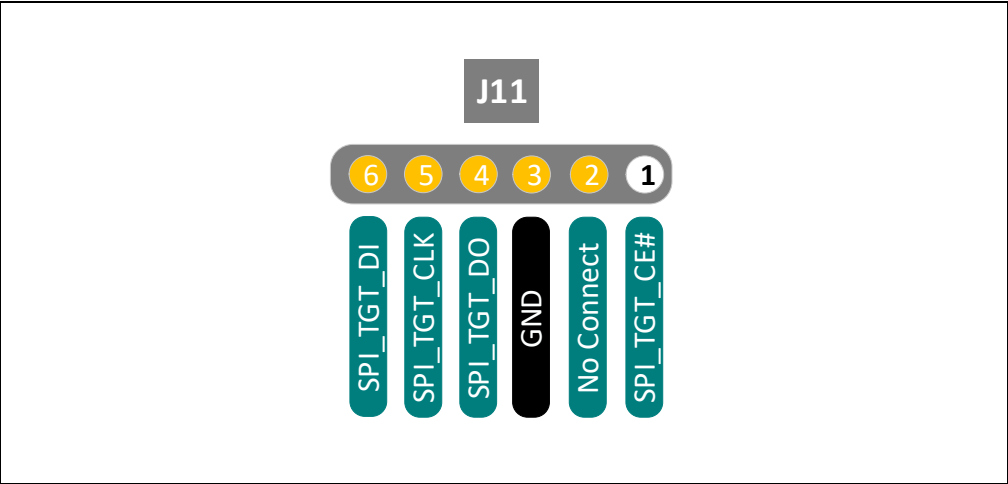
When J33 is configured to enable SMBus Target, J11 signal pinout appears as illustrated in [Figure 3-6](#).

FIGURE 3-6: J11 SIGNAL PINOUT (SMBUS TARGET)



When J33 is configured to enable SPI Target, J11 signal pinout becomes the one shown in [Figure 3-7](#).

FIGURE 3-7: J11 SIGNAL PINOUT (SPI TARGET)



3.1.5.17 J13– I²C/SMBUS EEPROM CONTROLLER (PICKIT SERIAL)

This PICKit Serial-compatible connector provides access to the I²C/SMBus EEPROM Controller bus of PCI11414. This bus will only be enabled when J33 PCI11414 Configuration Straps are configured to assert the CONFIG_EEPROM setting. (See J33 in [Section 3.1.4 “Jumper Settings and Defaults”](#).) Refer to [Figure 3-8](#).

FIGURE 3-8: J13 SIGNAL PINOUT

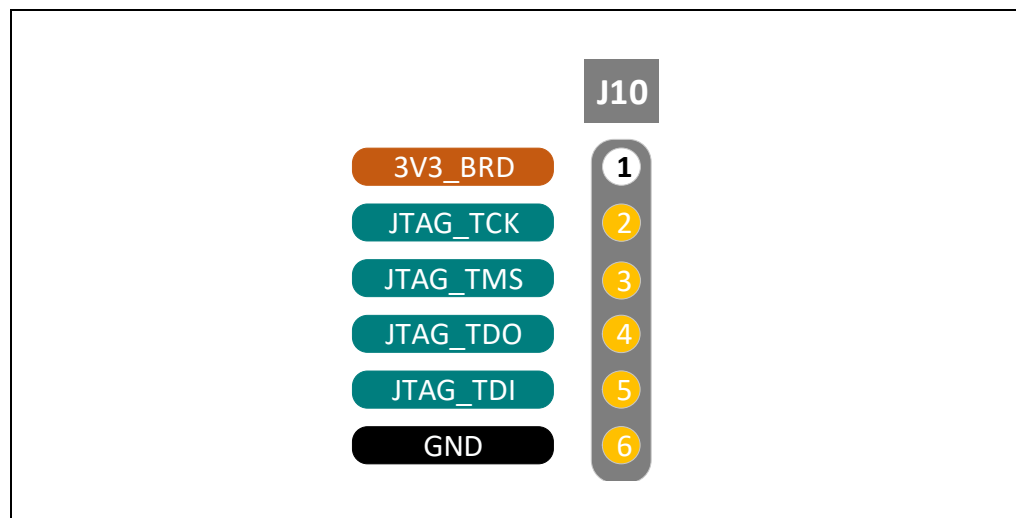


3.1.5.18 J10 – JTAG

The PCI11414 JTAG TAP interface becomes enabled only when PCI11414 is powered-on into Test mode by installing jumper J15 and resetting the evaluation board.

An optional 1x6 header position is provided in order to fly-wire into any JTAG adapter of choice. See [Figure 3-9](#).

FIGURE 3-9: J10 SIGNAL PINOUT



3.1.5.19 J37 – IEEE-1588 PTP_IO0

The IEEE-1588 Precision Timing Protocol I/O Channel 1 is available upon a through-hole SMA connector footprint to connect external hardware for event capture, Local Time Target Compare Event output, or Pulse Per Second (PPS) output.

3.1.5.20 J32 – IEEE-1588 PTP_IO1

The IEEE-1588 Precision Timing Protocol I/O Channel 2 is available upon a through-hole SMA connector footprint to connect external hardware for event capture, Local Time Target Compare Event output, or Pulse Per Second (PPS) output.

3.1.5.21 J18 – PROGRAMMABLE PIN PROBE HEADER 1

The majority of programmable pins available in PCI11414 are exposed across two Programmable Pin Probe Headers to facilitate signal measurement and testing of non-default use-cases of EVB-PCI11414. Each programmable pin position is labeled in silkscreen adjacent to its probe pin, e.g. “P2” is for probing pin “PROG2”. See [Table 3-4](#).

TABLE 3-4: PINOUT OF J18 PROGRAMMABLE PIN PROBE HEADER 1

Pin Number	Signal
Pin 1	PROG2
Pin 2	PROG17
Pin 3	PROG3
Pin 4	PROG18
Pin 5	PROG4
Pin 6	PROG19
Pin 7	PROG5
Pin 8	PROG20
Pin 9	PROG6
Pin 10	PROG21
Pin 11	PROG7
Pin 12	PROG22
Pin 13	PROG8
Pin 14	PROG23
Pin 15	PROG9
Pin 16	PROG24
Pin 17	PROG10
Pin 18	PROG31
Pin 19	GND
Pin 20	GND

3.1.5.22 J34 – PROGRAMMABLE PIN PROBE HEADER 2

This header exposes the second set of programmable pins for ease of probing access. See [Table 3-5](#).

TABLE 3-5: PINOUT OF J34 PROGRAMMABLE PIN PROBE HEADER 2

Pin Number	Signal
Pin 1	PROG32
Pin 2	PROG69
Pin 3	PROG33
Pin 4	PROG70
Pin 5	PROG34
Pin 6	PROG71
Pin 7	PROG49
Pin 8	PROG75
Pin 9	PROG50
Pin 10	PROG76
Pin 11	PROG64

TABLE 3-5: PINOUT OF J34 PROGRAMMABLE PIN PROBE HEADER 2

Pin Number	Signal
Pin 12	PROG79
Pin 13	PROG65
Pin 14	PROG80
Pin 15	PROG66
Pin 16	PROG85
Pin 17	PROG67
Pin 18	PROG86
Pin 19	PROG68
Pin 20	PROG87

3.1.6 Evaluation Board LED Indicators

Table 3-6 describes the LED indicators included on the EVB-PCI11414.

TABLE 3-6: LED INDICATOR DESCRIPTIONS

Reference	Signal Name	Description
D10	RESET#	Lit when PCI11414 Reset pin is asserted.
D16	12VIN_SW	Lit when there is voltage present upon one of the 12V input power connectors.
D14	5V_BRD	Lit when the on-board 5V regulator is outputting voltage.
D17	3V3_BRD	Lit when the on-board 3.3V regulator is outputting voltage.
D15	1V1_BRD	Lit when the on-board 1.1V regulator is outputting voltage.
D9	3V3_PCIE	Lit when the upstream PCIe host connection (at P1) is sourcing 3.3V power for EVB-PCI11414.
D11	PERST0#	Lit when the upstream PCIe host connection (at P1) has asserted PERST#.
D12	CLKREQ0#	Lit when PCI11414 has asserted CLKREQ# for its upstream PCIe connection.
D13	WAKE0#	Lit when PCI11414 has asserted WAKE# for its upstream PCIe connection.
D8	PERST1#	Lit when either PERST#0 or RESET# are asserted
D7	CLKREQ1#	Lit when external downstream PCIe device (at J9) has asserted its CLKREQ# signal (ready to receive PCIe REF-CLK)
D6	WAKE1#	Lit when external downstream PCIe device (at J9) has signaled a wake event.
D4	USB Port 1 VBUS	Lit when 5V VBUS power has been enabled onto the Port 1 USB-C receptacle.
D3	USB Port 2 VBUS	Lit when 5V VBUS power has been enabled onto the Port 2 USB-A receptacle.
D2	USB Port 3 VBUS	Lit when 5V VBUS power has been enabled onto the Port 3 USB-A receptacle.
D1	USB Port 4 VBUS	Lit when 5V VBUS power has been enabled onto the Port 4 USB-A receptacle.
D5	USC4002 FAULT# (Port 1)	Lit when the USB-C protection + VCONN source UCS4002 has experienced a Fault condition.

3.1.7 Evaluation Board Test Points

Table 3-7 describes the test points available on EVB-PCI11414.

TABLE 3-7: EVB-PCI11414 TEST POINTS

Reference	Signal Name	Remarks
TP31	12VIN	At the power-OR node
TP30	5V_BRD	—
TP33	3V3_BRD	—
TP32	1V1_BRD	—
TP28	PCIE_WAKE_P0_N	—
TP29	PCIE_PERST_P0_N	—
TP27	PCIE_CLKREQ0_N	—
TP19	PCIE_REFCLK_P	PCIe REFCLK from upstream PCIe connection, which inputs to clock buffer U6 (differential)
TP21	PCIE_REFCLK_N	PCIe REFCLK from upstream PCIe connection, which inputs to clock buffer U6 (differential)
TP20	PCIE_REFCLK_IN_P	PCIe REFCLK output from clock buffer U6, which inputs to PCI11414 (differential)
TP22	PCIE_REFCLK_IN_N	PCIe REFCLK output from clock buffer U6, which inputs to PCI11414 (differential)
TP24	PCIE_REFCLK_P1_P	PCIe REFCLK output from clock buffer U6, which inputs to external PCIe device at J9 (differential)
TP2	USB Port 1 Receptacle CC1	USB Type-C CC1 signal for Port 1
TP3	USB Port 1 Receptacle CC2	USB Type-C CC2 signal for Port 1
TP9	VB_PRT_CTL_P1/OCS_P1	—
TP10	VB_PRT_CTL_P2/OCS_P2	—
TP7	VB_PRT_CTL_P3/OCS_P3	—
TP8	VB_PRT_CTL_P4/OCS_P4	—
TP12	KSZ9131RX/CLK123_NDO/ LED_MODE	Ethernet PHY sideband signal test point
TP16	GND	Ground reference near U4
TP17	GND	Ground reference near P1

Appendix A. Schematics

A.1 INTRODUCTION

This appendix shows the EVB-PCI11414 Evaluation Kit's schematics.

Board Power & Resets

Power Inputs, Switch and Voltage Regulators

Power Inputs, Switch and Voltage Regulators

Note: 12V ATX supply (12V_PCE) can range 11.4-12.6V

Note: VS-12CWQ03FN-M3
D18 V_I = 0.47V @ 6A (25C)
D19 V_F = 0.315V @ 5A (25C)

Note: For PCIe downstream port power,
12VIN valid range is 11.04-12.96V

SW1: Board Power Mode Select Switch
[1-2] → PCIe-CONNECTED MODE:
Board power is synchronized to PCIe Host power presence
[2-3] → PCIe-DISCONNECTED MODE:
Board power is enabled/disabled by SW1

Alternate 12V-5V Regulator
Layout: Place to overlap PM8 footprint.

5V@8A
U10
TP LOOP Orange TP30

Alternate 12V-3.3V Regulator
Layout: Place to overlap PM8 footprint.

3.3V@8A
U12
TP LOOP Orange TP33

VIN(12V) to 3.3VDC

Alternate 12V-3.3V Regulator
Layout: Place to overlap PM8 footprint.

Note: Install RTRIM=430 Ohm 1% for 3.3V output from Alternate Regulator

5VDC to 1.1VDC

Alternate 5V-1.1V Regulator
Layout: Place to overlap PMLV2 footprint.

Note: Install RTRIM=2.32kOhm 1% for 1.1V output from Alternate Regulator

Board Reset

RESET tree connections
Pull-ups located near to each resettable function

PCIE Port# PERST# is pulled-up by host system 3.3V

PCIE PERST P0 N U24 5 A VCC

PCIE PERST P1 N U24 6 7

PCIE CLKREQ N U21 4 6

PCIE PERST P1 N U21 3

UART RESETS N U20 12

MICROCHIP	
Project Owner: Josh Avery	Project Title: Variant: [No Variations]
PCB Layout Contact: Mick Davis	Part Number: EV38E94A
Sheet Title: Bridgeport PC11T14 EVB	Rev: 1
Board Power and Resets Size: ICSH # 02-090608 Rev: 1 Date: 8/21/2023 Tabloid: PCB # 04-17100 Rev: 1 Sheet 2 of 12 File: evb38e94a_04-down.schdoc	
Designed with Altium	

FIGURE A-2: PCI11414 POWER

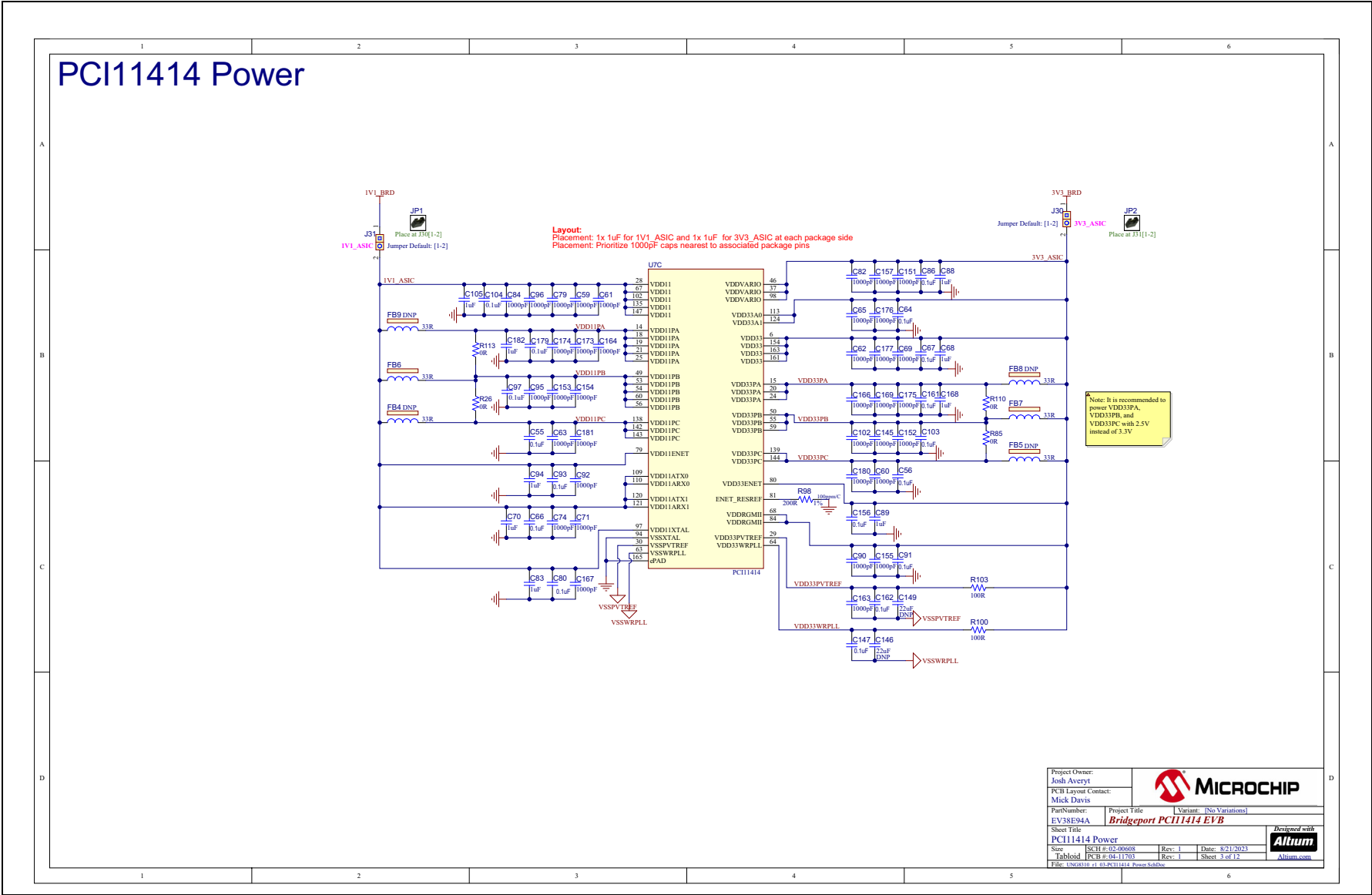


FIGURE A-3: PCI11414 I/O

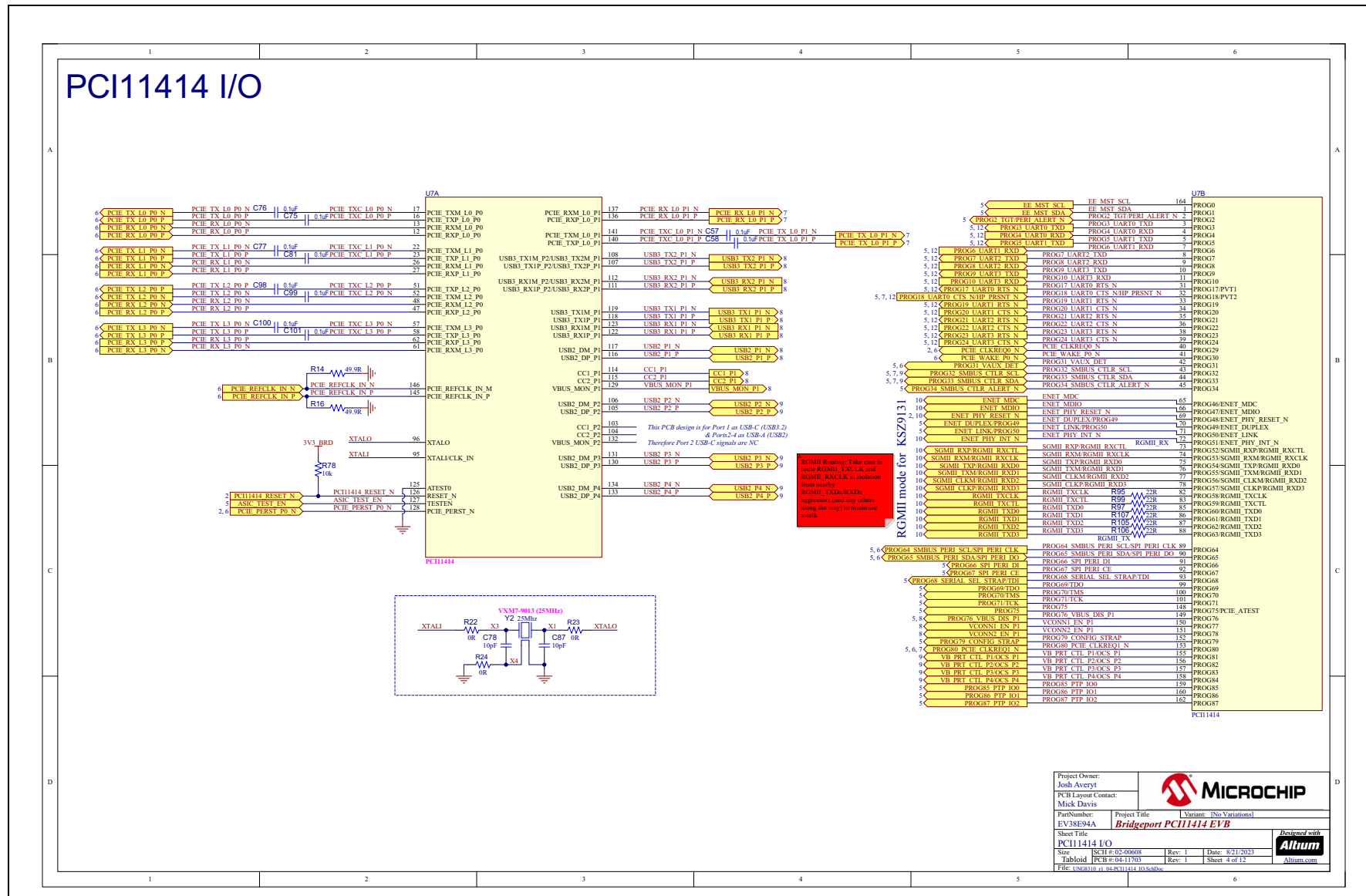


FIGURE A-4: CONFIGURATION INTERFACES AND I/O BREAKOUTS

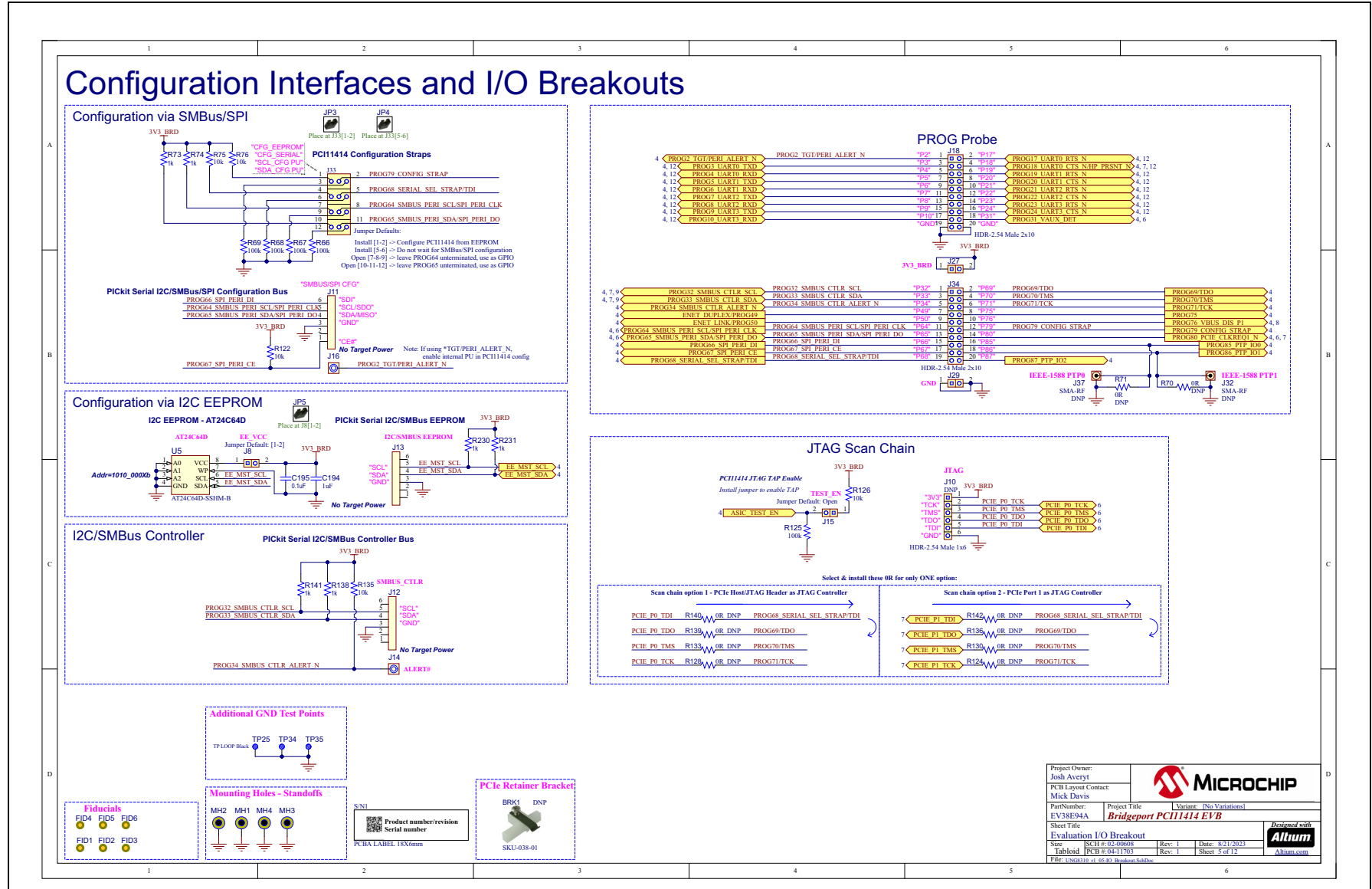
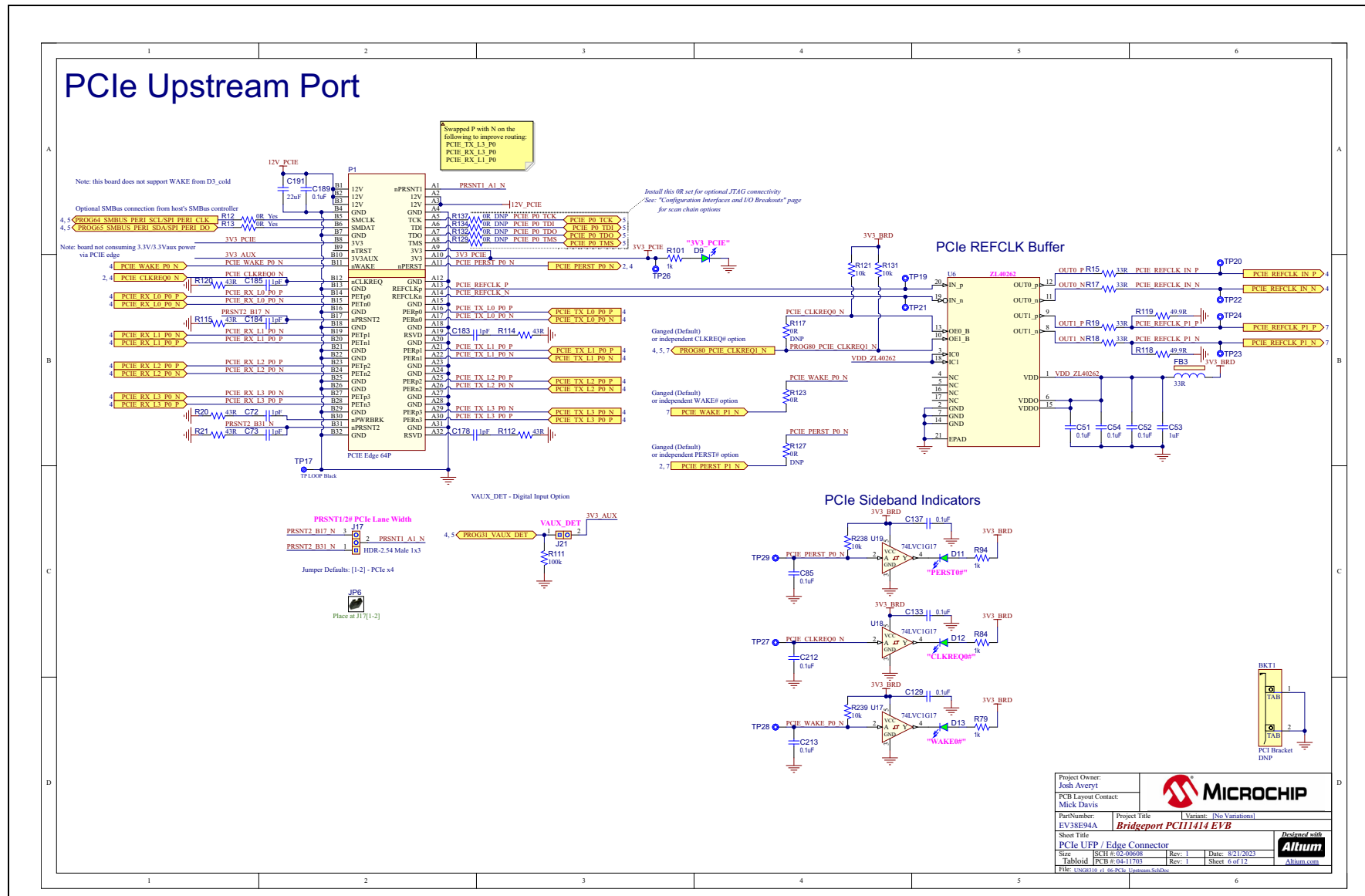


FIGURE A-5: PCIE UPSTREAM PORT



PCIe Downstream Switch Port



FIGURE A-7: USB3.2 GEN 2 HOST PORT 1

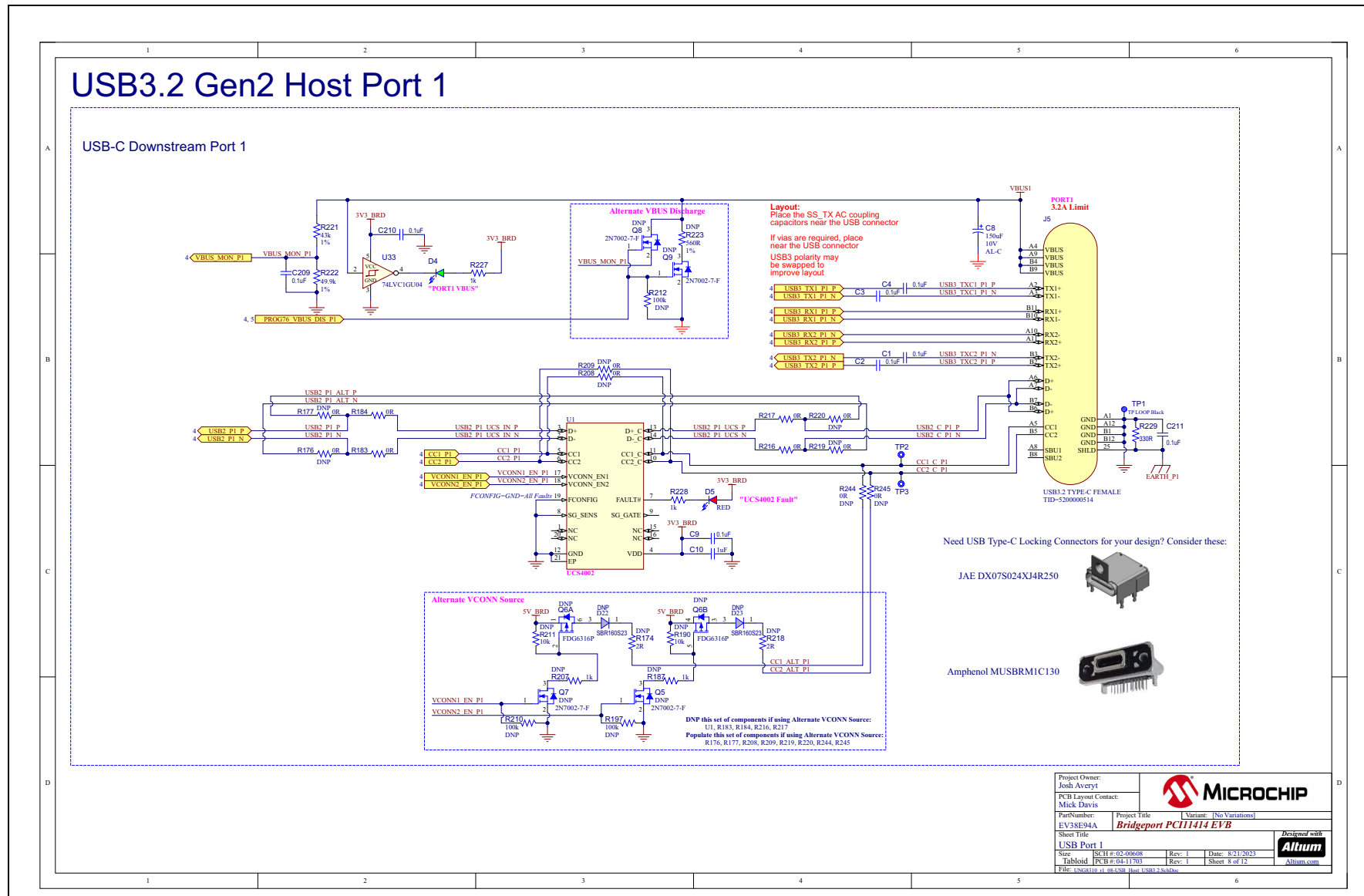


FIGURE A-8: USB2.0 HOST PORTS AND 5 VBUS POWER

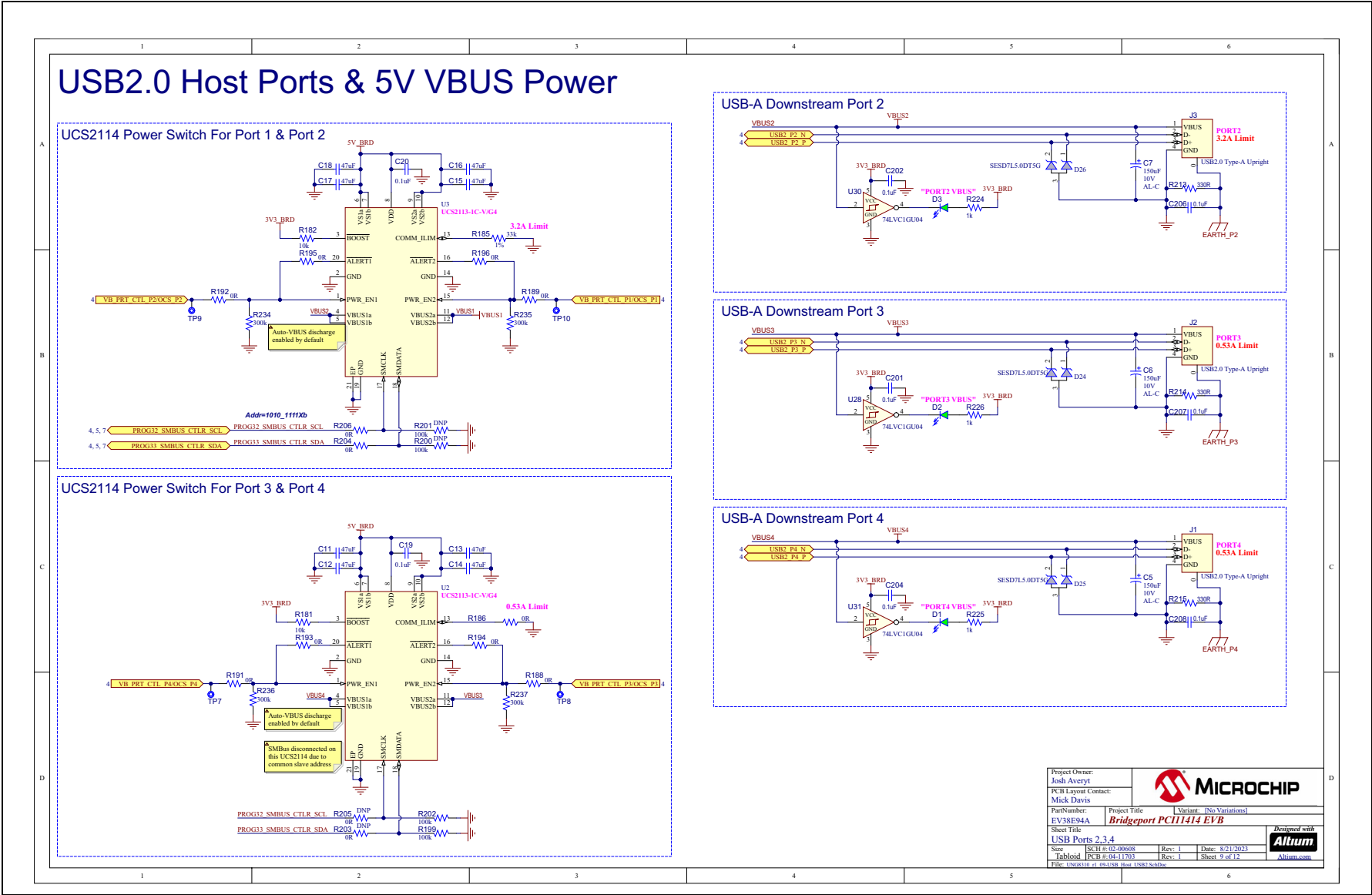


FIGURE A-9: ETHERNET

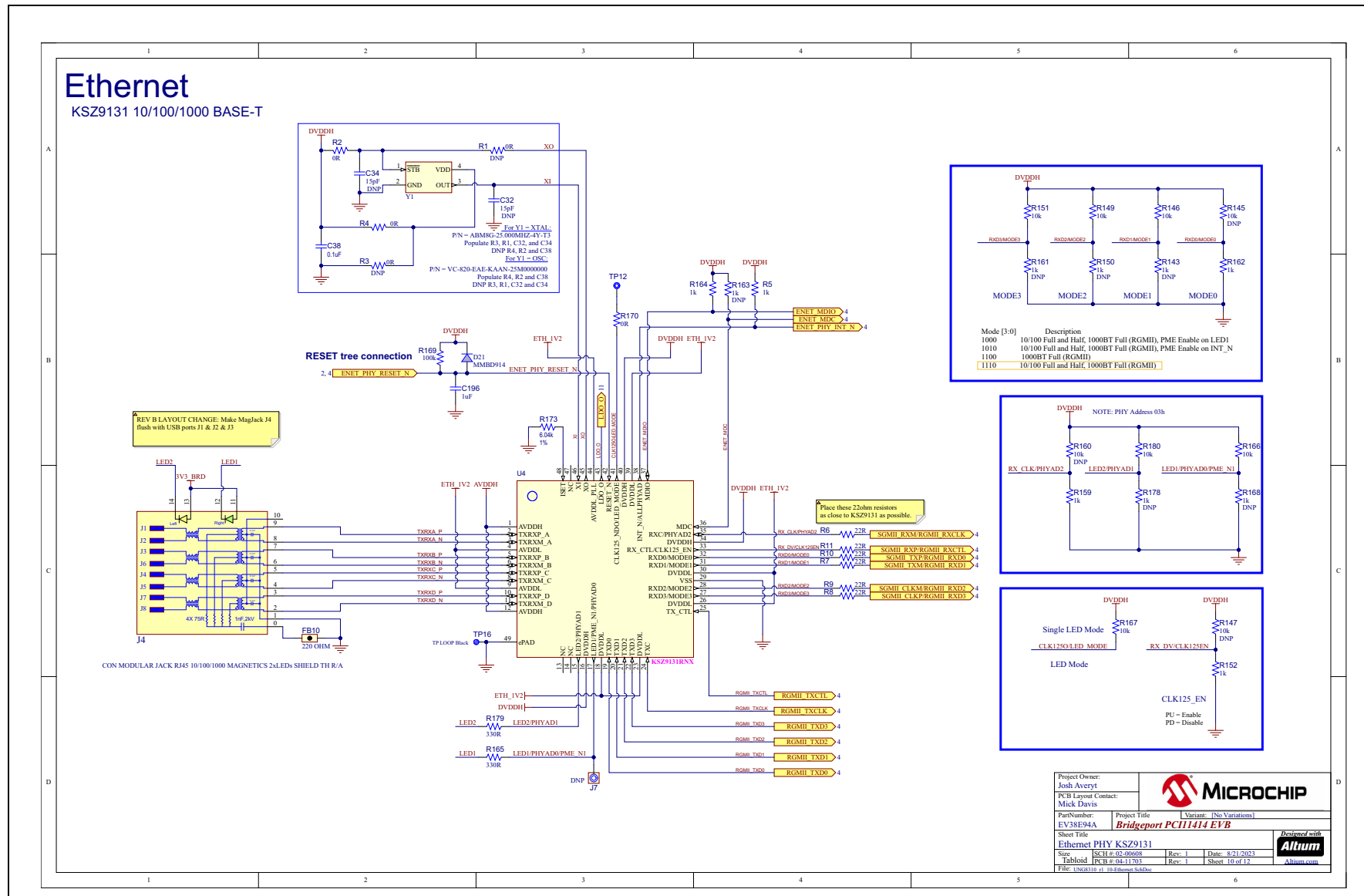


FIGURE A-10: ETHERNET POWER

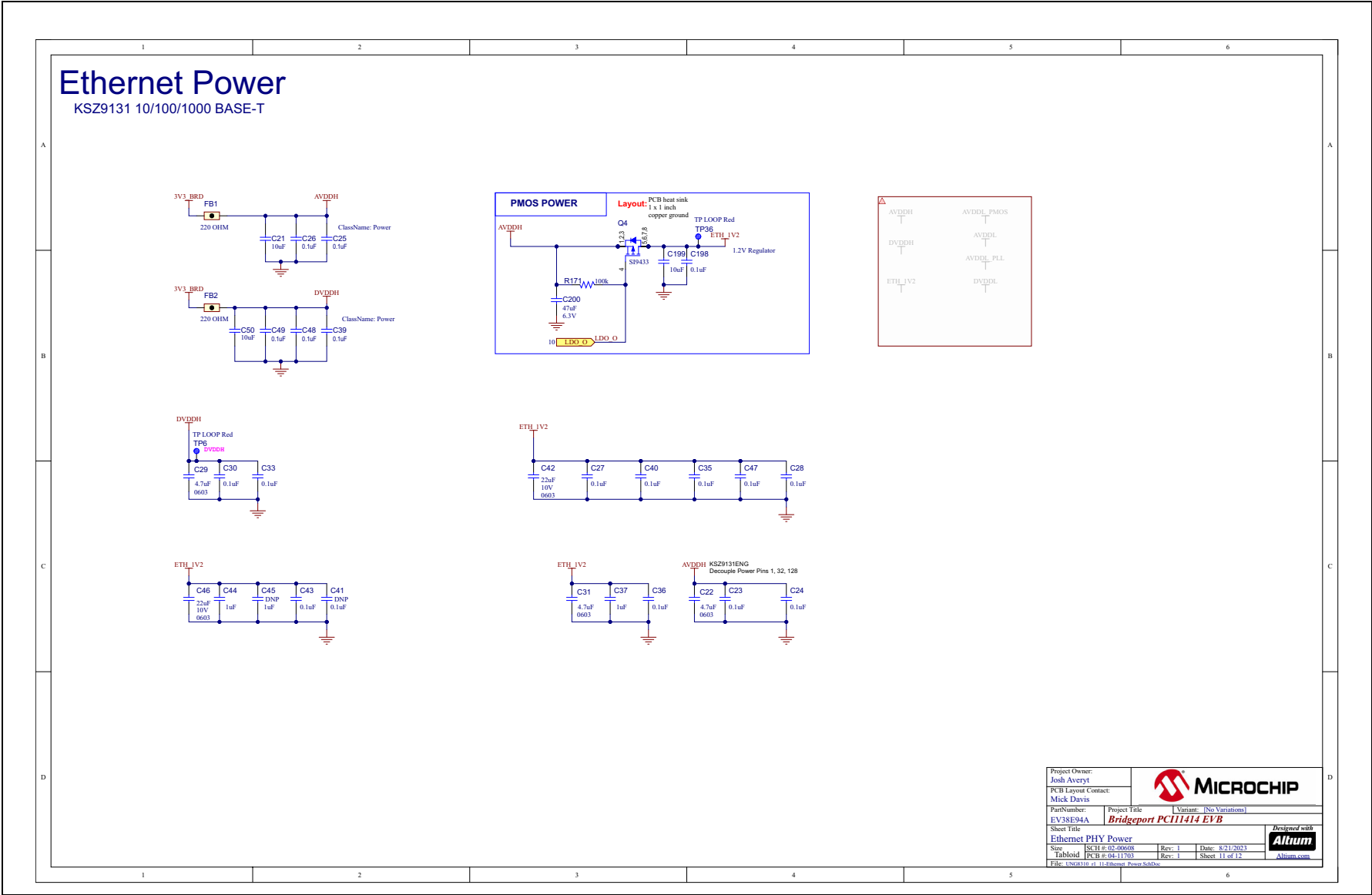
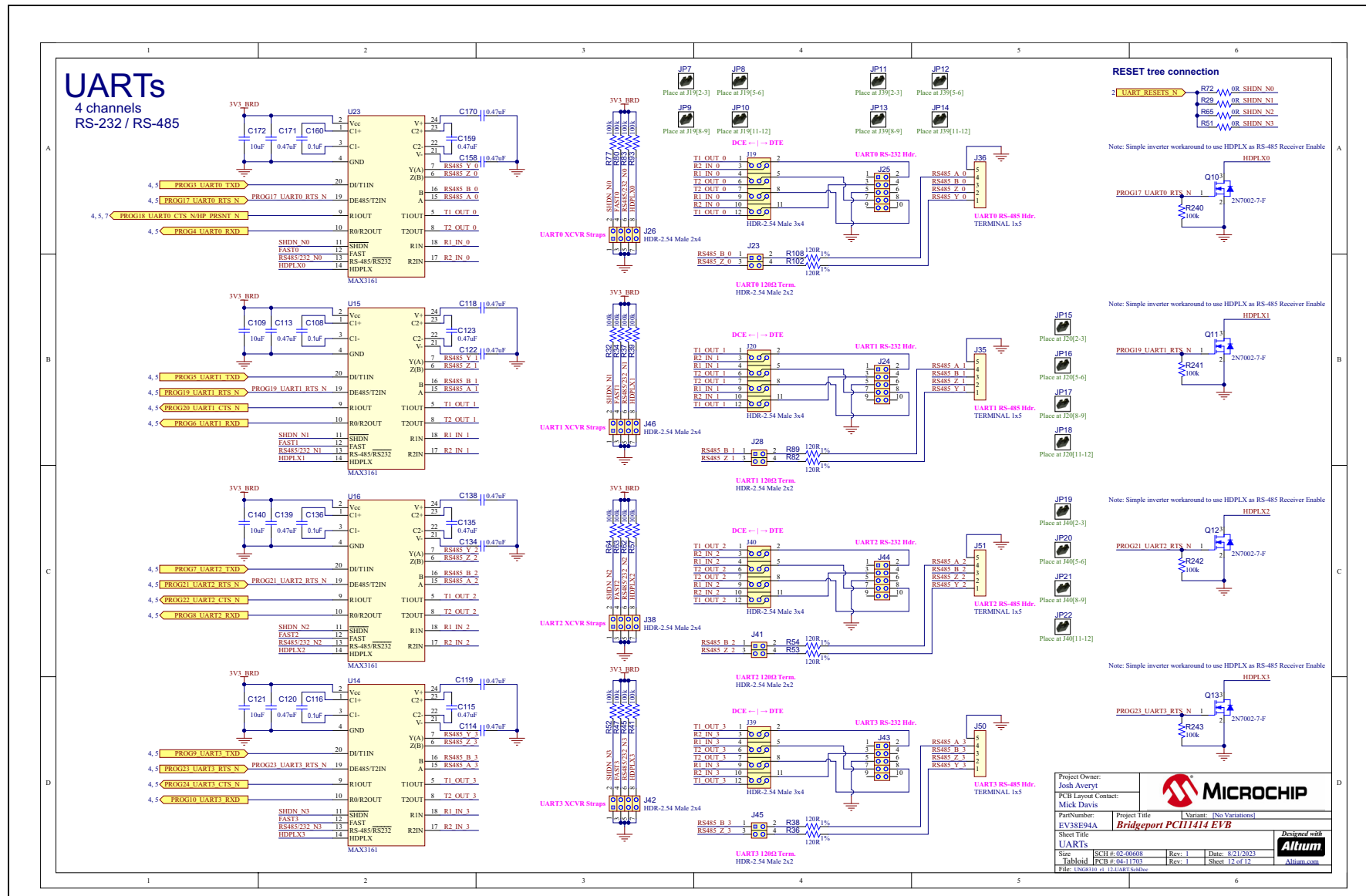


FIGURE A-11: UARTS



Appendix B. Bill of Materials

B.1 INTRODUCTION

This appendix contains the EVB-PCI11414 Evaluation Kit's Bill of Materials.

TABLE B-1: BILL OF MATERIALS (INSTALLED COMPONENTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
1	64	C1, C2, C3, C4, C9, C51, C52, C54, C55, C56, C57, C58, C64, C66, C67, C75, C76, C77, C80, C81, C85, C86, C91, C93, C98, C99, C100, C101, C103, C108, C112, C116, C129, C133, C136, C137, C141, C142, C143, C144, C147, C150, C156, C160, C161, C162, C165, C187, C188, C189, C192, C193, C195, C197, C203, C205, C209, C210, C211, C212, C213, C214, C215, C216	CAP CER 0.1uF 35V 10% X7R SMD 0402	TDK Corporation	CGA2B3X7R1V104K050BB
2	4	C5, C6, C7, C8	CAP ALU 150uF 10V 20% SMD C	Panasonic Electronic Components	EEE-FT1A151AR
3	2	C10, C196	CAP CER 1uF 16V 10% X5R SMD 0603	AVX	0603YD105KAT2A
4	8	C11, C12, C13, C14, C15, C16, C17, C18	CAP CER 47uF 6.3V 20% X5R SMD 0805	Taiyo Yuden	JMK212BJ476MG-T
5	7	C19, C20, C97, C104, C106, C107, C179	CAP CER 0.1uF 16V 10% X7R SMD 0402	Wurth Electronics Inc, KEMET	885012205037, C0402C104K4RACAUTO
6	6	C21, C50, C109, C121, C140, C172	CAP CER 10uF 10V 10% X5R SMD 0603	Samsung Electro-Mechanics	CL10A106KP8NNNC
7	3	C22, C29, C31	CAP CER 4.7uF 10V 10% X5R SMD 0603	KEMET	C0603C475K8PACTU
8	19	C23, C24, C25, C26, C27, C28, C30, C33, C35, C36, C38, C39, C40, C43, C47, C48, C49, C130, C198	CAP CER 0.1uF 50V 10% X7R SMD 0402	TDK Corporation, Taiyo Yuden	C1005X7R1H104K050BB, UMK105B7104KV-FR
9	14	C37, C44, C53, C68, C70, C83, C88, C89, C94, C105, C148, C168, C182, C194	CAP CER 1uF 35V 10% X5R SMD 0402	Murata Electronics North America	GRM155R6YA105KE11D
10	2	C42, C46	CAP CER 22uF 10V 20% X5R SMD 0603	TDK Corporation	C1608X5R1A226M080AC
11	37	C59, C60, C61, C62, C63, C65, C69, C71, C74, C79, C82, C84, C90, C92, C95, C96, C102, C126, C145, C151, C152, C153, C154, C155, C157, C163, C164, C166, C167, C169, C173, C174, C175, C176, C177, C180, C181	CAP CER 1000pF 50V 5% NP0 SMD 0402 AEC-Q200	Murata Electronics	GCM1555C1H102JA16J
12	6	C72, C73, C178, C183, C184, C185	CAP CER 1pF 50V C0G/NP0 SMD 0402 AEC-Q200	Murata Electronics North America	GCM1555C1H1R0CA16J
13	2	C78, C87	CAP CER 10pF 50V 5% NP0 SMD 0402	Murata	GJM1555C1H100JB01D
14	9	C110, C111, C117, C125, C127, C128, C186, C190, C191	CAP CER 22uF 25V 20% X5R SMD 0805	Yageo	CC0805MKX5R8BB226
15	16	C113, C114, C115, C118, C119, C120, C122, C123, C134, C135, C138, C139, C158, C159, C170, C171	CAP CER 0.47uF 16V 10% X7R SMD 0603	Murata	GRM188R71C474KA88D
16	1	C124	CAP CER 4.7uF 10V 10% X5R SMD 0603	KEMET	C0603C475K8PACTU

TABLE B-1: BILL OF MATERIALS (INSTALLED COMPONENTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
17	1	C132	CAP CER 47pF 5% 50V C0G/NP0 SMD 0402 AEC-Q200	Murata Electronics North America	GCM1555C1H470JA16D
18	1	C199	CAP CER 10uF 25V 20% X5R SMD 0603	Murata Electronics North America	GRM188R61E106MA73D
19	1	C200	CAP CER 47uF 6.3V 20% X5R SMD 0805	Taiyo Yuden	JMK212BJ476MG-T
20	6	C201, C202, C204, C206, C207, C208	CAP CER 0.1uF 35V 10% X7R SMD 0402	TDK Corporation	CGA2B3X7R1V104K050BB
21	3	D1, D2, D3	DIO LED GREEN 2V 30mA 35mcd Clear SMD 0603	Lite-On Inc	LTST-C191KGKT
22	12	D4, D6, D7, D8, D9, D11, D12, D13, D14, D15, D16, D17	DIO LED GREEN 2V 30mA 35mcd Clear SMD 0603	Lite-On Inc	LTST-C191KGKT
23	2	D5, D10	DIO RED 2V 20mA 54mcd CLEAR SMD 0603	Lite-On Inc.	LTST-C191KRKT
24	1	D18	DIO SCTKY ARRAY VS-12CWQ03FN-M3 0.37V 6A SMD DPAK	Vishay Semiconductor Diodes Division	VS-12CWQ03FN-M3
25	1	D19	DIO SCTKY PMEG3050EP 315mV 5A 30V SOD-128	NXP Semiconductors	PMEG3050EP
26	1	D20	DIO TVS SMBJ13D-M3/I 13V 21.2V 600W SMD DO-214AA	Vishay Semiconductor Diodes Division	SMBJ13D-M3/I
27	1	D21	DIO RECT MMBD914LT1G 1V 10mA 100V SMD SOT-23-3	ON Semiconductor	MMBD914LT1G
28	2	D22, D23	DIO SBAR SBR160S23-7 SBR 530mV 900mA 60V SMD SOT23-3	Diodes Incorporated	SBR160S23-7
29	3	D24, D25, D26	DIO TVS ARRAY SESD7L5.0DT5G 5V AEC-Q101 SMD SOT-723	ON Semiconductor	SESD7L5.0DT5G
30	3	FB1, FB2, FB10	FERRITE 500mA 220R SMD 0603	Murata Electronics North America	BLM18AG221SN1D
31	1	FB3	FERRITE 33R@100MHz 3A SMD 0603	Murata	BLM18PG330SN1D
32	2	FB6, FB7	FERRITE 33R@100MHz 3A SMD 0603	Murata	BLM18PG330SN1D
33	6	FID1, FID2, FID3, FID4, FID5, FID6	FIDUCIAL		
34	3	J1, J2, J3	USB2.0 STD-A FEMALE UPRIGHT	Amphenol FCI	73725-0110BLF
35	1	J4	CONN MAGJACK 1PORT 1000 BASE-T	Pulse Electronics Network	JD1-0001NL
36	1	J5	CON USB3.1 TID TYPE-C Female SMD R/A	Amphenol Commercial Products	12401610E4#2A
37	7	J8, J15, J21, J27, J29, J30, J31	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	FCI	68001-202HLF
38	1	J9	CON EDGE PCIe 1mm 36P Female TH R/A	Samtec Inc.	PCIE-036-02-F-D-RA
39	3	J11, J12, J13	CON HDR-2.54 Male 1x6 Tin 5.84MH TH VERT	WURTH ELEKTRONIK	61300611121
40	2	J14, J16	CON HDR-2.54 Male 1x1 Gold 5.84MH TH VERT	Samtec	TSW-101-07-G-S
41	1	J17	CON HDR-2.54 Male 1x3 Tin 5.84MH TH VERT	Samtec	TSW-103-07-T-S
42	2	J18, J34	CON HDR 2.54 MALE 2x10 3u" GOLD IN CONTACT AREA MATTE TIN ON TAIL 5.84MH TH VERT	Samtec	TSW-110-07-F-D
43	5	J19, J20, J33, J39, J40	CON HDR-2.54 Male 3x4 Gold 5.84MH TH VERT	Samtec Inc.	TSW-104-07-G-T
44	1	J22	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	FCI	77311-118-02LF
45	4	J23, J28, J41, J45	CON HDR-2.54 Male 2x2 Gold 5.84MH TH VERT	Wurth Electronics Inc	61300421121
46	4	J24, J25, J43, J44	CON HDR-2.54 Male 2x5 0.100" (2.54mm) TH VERT	Samtec	TSW-105-07-G-D

TABLE B-1: BILL OF MATERIALS (INSTALLED COMPONENTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
47	4	J26, J38, J42, J46	CON HDR-2.54 Male 2x4 Gold 5.84MH TH VERT	Würth Electronics Inc	61300821121
48	4	J35, J36, J50, J51	CON TERMINAL 2.54mm 1x5 Female 20-30AWG 6A TH R/A	Phoenix Contact	1725685
49	1	J47	CON HDR-5.08 Male 1x4 Tin SHROUD 12.32MH TH R/A	TE Connectivity	641737-1
50	1	J48	CON POWER 2.5mm 5.5mm TH R/A	CUI Inc.	PJ-063BH
51	1	J49	CON TERMINAL 5.08mm 1X2 Female 16-30AWG 13.5A TH RA	TE Connectivity	282836-2
52	1	L1	RES TKF 0R 1/8W SMD 0805	Panasonic	ERJ-6GEY0R00V
53	1	Q1	TRANS FET P-CH SI4435 30V 12.6A 4.8W 0.019R SOIC-8	Vishay / Siliconix	SI4435FDY-T1-GE3
54	7	Q2, Q5, Q7, Q10, Q11, Q12, Q13	TRANS FET N-CH 2N7002-7-F 60V 170mA 370mW SOT-23-3	Diodes Inc	2N7002-7-F
55	1	Q3	TRANS BJT NPN MMBT3904 40V 200mA 310mW SOT-23-3	NXP Semiconductors	PMBT3904,215
56	1	Q4	TRANS FET P-CH SI9433 20V 4.5A 1.3W 0.040R SOIC-8	Vishay	SI9433BDY-T1-GE3
57	1	Q6	TRANS FET DUAL P+P FDG6316P 12V 0.7A 0.270R 0.3R SC-88	ON Semiconductor	FDG6316P
58	2	R2, R4	RES TKF 0R 1/16W SMD 0402	Yageo	RC0402JR-070RL
59	8	R5, R55, R96, R152, R159, R162, R164, R228	RES TKF 1k 5% 1/10W SMD 0603	Panasonic	ERJ-3GEYJ102V
60	12	R6, R7, R8, R9, R10, R11, R95, R97, R99, R105, R106, R107	RES TKF 22R 1% 1/20W SMD 0402	Panasonic Electronic Components	ERJ-2RKF22R0X
61	37	R12, R13, R22, R23, R24, R26, R29, R49, R51, R65, R72, R85, R90, R91, R92, R110, R113, R123, R144, R148, R154, R170, R183, R184, R186, R188, R189, R191, R192, R193, R194, R195, R196, R204, R206, R216, R217	RES TKF 0R 1/10W SMD 0603	Stackpole Electronics Inc	RMCF0603ZT0R00
62	4	R14, R16, R118, R119	RES TKF 49.9R 1% 1/10W SMD 0603	ROHM	MCR03EZPFX49R9
63	4	R15, R17, R18, R19	RES TKF 33R 5% 1/10W SMD 0603	Panasonic	ERJ-3GEYJ330V
64	6	R20, R21, R112, R114, R115, R120	RES TKF 43R 1% 1/10W SMD 0402	Panasonic Electronic Components	ERJ-2RKF43R0X
65	21	R25, R59, R66, R67, R68, R69, R81, R86, R87, R88, R111, R125, R171, R197, R199, R202, R210, R240, R241, R242, R243	RES TF 100k 1% 1/8W SMD 0603	Vishay	MCT06030C1003FP500
66	4	R27, R213, R214, R215	RES TKF 330R 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF3300V
67	1	R28	RES TKF 20R 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF20R0V
68	17	R30, R44, R46, R75, R76, R121, R122, R131, R135, R181, R182, R190, R211, R232, R233, R238, R239	RES TKF 10k 1% 1/10W SMD 0603	Vishay, ROHM	CRCW060310K0FKEA, MCR03EZPFX1002
69	2	R31, R33	RES TF 2.2k 1% 1/8W SMD 0603	Vishay Beyschlag	MCT06030C2201FP500

TABLE B-1: BILL OF MATERIALS (INSTALLED COMPONENTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
70	17	R32, R34, R37, R39, R41, R45, R47, R52, R57, R62, R63, R64, R77, R80, R83, R93, R169	RES TKF 100k 5% 1/16W SMD 0402	Yageo	RC0402JR-07100KL
71	20	R35, R73, R74, R79, R84, R94, R101, R138, R141, R172, R175, R187, R198, R207, R224, R225, R226, R227, R230, R231	RES TKF 1k 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF1001V
72	8	R36, R38, R53, R54, R82, R89, R102, R108	RES TKF 120R 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF1200V
73	1	R40	RES TKF 20R 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF20R0V
74	1	R42	RES TKF 4.42k 1% 1/10W SMD 0603	Vishay Dale	CRCW06034K42FKEA
75	1	R43	RES TKF 30k 1% 1/10W SMD 0603	Stackpole Electronics Inc	RMCF0603FT30K0
76	2	R48, R58	RES TKF 680R 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF6800V
77	1	R60	RES TF 8.98k 0.5% 1/10W SMD 0603 AEC-Q200	KOA Speer	RN73R1JTDD8981D100
78	1	R61	RES TKF 2.7k 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF2701V
79	4	R78, R104, R109, R126	RES TF 10k 1% 1/10W SMD 0402 AEC-Q200	Vishay Beyschlag	MCS0402MC1002FE000
80	1	R98	RES TKF 200R 1% 1/10W SMD 0603 AEC-Q200	Vishay / Dale	CRCW0603200RFKEA
81	2	R100, R103	RES TKF 100R 5% 1/10W SMD 0603	Vishay	CRCW0603100RJNEA
82	6	R146, R149, R151, R166, R167, R180	RES TKF 10k 5% 1/10W SMD 0603	Panasonic	ERJ-3GEYJ103V
83	2	R165, R179	RES TKF 330R 5% 1/10W SMD 0603	Panasonic	ERJ-3GEYJ331V
84	1	R173	RES TKF 6.04k 1% 1/10W SMD 0603	Yageo	9T06031A6041FBHFT
85	2	R174, R218	RES TKF 2R 5% 0.5W SMD 0805 AEC-Q200	Panasonic - ECG	ERJ-6DQJ2R0V
86	1	R185	RES TKF 33k 1% 1/10W AEC-Q200 SMD 0603	Vishay	CRCW060333K0FKEA
87	1	R221	RES TKF 43k 1% 1/10W SMD 0603	Yageo	9C06031A4302FKHFT
88	1	R222	RES TKF 49.9k 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF4992V
89	1	R229	RES TKF 330R 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF3300V
90	4	R234, R235, R236, R237	RES TKF 300k 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF3003V
91	1	SW1	SWITCH SLIDE DPDT 6V 300MA JS202011CQN TH	C&K Components	JS202011CQN
92	7	TP1, TP15, TP16, TP17, TP25, TP34, TP35	MISC, TEST POINT MULTI PURPOSE MINI BLACK	Keystone	5001
93	3	TP6, TP31, TP36	MISC, TEST POINT MULTI PURPOSE MINI RED	Keystone	5000
94	3	TP30, TP32, TP33	CON TP LOOP Orange TH	Keystone Electronics	5003
95	4	U14, U15, U16, U23	IC TRANSCEIVER MAX3161EE FULL RS-232/RS-485/RS-422 SSOP-24	Maxim Integrated	MAX3161EEAG+
96	6	U17, U18, U19, U27, U29, U32	IC BUFFER 74LVC1G17 NON-INVERT SC-74A	Nexperia	74LVC1G17GV,125
97	3	U20, U21, U22	IC BUFFER MC74VHC1G07 NON-INVERT SOT-23	onsemi	MC74VHC1G07DTT1G

TABLE B-1: BILL OF MATERIALS (INSTALLED COMPONENTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
98	1	U24	IC LOGIC MC74VHC1G09 AND GATE SOT-23-5	onsemi	MC74VHC1G09DTT1G
99	1	U26	74LVC1G14GW,125 SCHMITT-TRG INVERTER	NXP	74LVC1G14GW,125
100	4	U28, U30, U31, U33	IC LOGIC 74LVC1GU04 NON-BUFF INV SOT-23	Texas Instruments	SN74LVC1GU04DBVR

TABLE B-2: BILL OF MATERIALS (MICROCHIP PARTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
1	1	U1	MCHP INTERFACE USB TYPE-C PORT PROTECT UCS4002 QFN-20 AECQ100	Microchip Technology	UCS4002-E/6N
2	2	U2, U3	MCHP INTERFACE USB PWR Controller with Auto Discharge UCS2113-1C-V/G4 QFN-20	Microchip Technology	UCS2113-1C-V/G4
3	1	U4	MCHP INTERFACE KSZ9131RNX 10/100/1000BASE-T QFN-48	Microchip Technology	kSZ9131RNXC
4	1	U5	MCHP MEMORY SERIAL EEPROM 64Kb I2C AT24CS64-SSHM-B SOIC-8	Microchip Technology	AT24C64D-SSHM-B
5	1	U6	MCHP CLOCK DISTRIBUTION 1:2 UPI/QPI fanout buffer 0-400MHz ZL40262 QFN-20	Microchip Technology	ZL40262LDG1
6	1	U7	MCHP INTERFACE PCI Switch USB 3.2 Host Controller Ethernet PCI11414 DQFN-164 VQFN-132	Microchip Technology	PCI11414

TABLE B-3: BILL OF MATERIALS (DO-NOT-POPULATE COMPONENTS)

Item	Qty.	Reference	Description	Manufacturer	Manufacturer Part Number
1	1	BKT1	PCI Bracket, Global G5452	Global	
2	1	BRK1	MECH HW MISC PCIe Board Retainer	Amfeltec Corporation	SKU-038-01
3	2	C32, C34	CAP CER 15pF 5% 50V C0G/NP0 SMD 0402 AEC-Q200	Murata Electronics North America	GCM1555C1H150JA16D
4	2	C41, C131	CAP CER 0.1uF 50V 10% X7R SMD 0402	TDK Corporation, Taiyo Yuden	C1005X7R1H104K050BB, UMK105B7104KV-FR
5	1	C45	CAP CER 1uF 35V 10% X5R SMD 0402	Murata Electronics North America	GRM155R6YA105KE11D
6	2	C146, C149	CAP CER 22uF 6.3V 20% X6S SMD 0603	Murata Electronics	GRM188C80J226ME15D
7	4	FB4, FB5, FB8, FB9	FERRITE 33R@100MHz 3A SMD 0603	Murata	BLM18PG330SN1D
8	2	J6, J7	CON HDR-2.54 Male 1x1 Gold 5.84MH TH VERT	Samtec	TSW-101-07-G-S
9	1	J10	CON HDR-2.54 Male 1x6 Tin 5.84MH TH VERT	WURTH ELEKTRONIK	61300611121
10	2	J32, J37	CON RF Coaxial SMA Female 2P SMD VERT	Cinch Connectivity Solutions Johnson	142-0701-201
11	2	Q8, Q9	TRANS FET N-CH 2N7002-7-F 60V 170mA 370mW SOT-23-3	Diodes Inc	2N7002-7-F
12	2	R1, R3	RES TKF 0R 1/16W SMD 0402	Yageo	RC0402JR-070RL
13	1	R50	RES TKF 30k 1% 1/10W SMD 0603	Stackpole Electronics Inc	RMCF0603FT30K0
14	1	R56	RES TKF 2.32k 1% 1/10W SMD 0603	Panasonic	ERJ-3EKF2321V
15	31	R70, R71, R117, R124, R127, R128, R129, R130, R132, R133, R134, R136, R137, R139, R140, R142, R153, R155, R156, R157, R158, R176, R177, R203, R205, R208, R209, R219, R220, R244, R245	RES TKF 0R 1/10W SMD 0603	Stackpole Electronics Inc	RMCF0603ZT0R00
16	3	R116, R200, R201	RES TF 100k 1% 1/8W SMD 0603	Vishay	MCT06030C1003FP500
17	6	R143, R150, R161, R163, R168, R178	RES TKF 1k 5% 1/10W SMD 0603	Panasonic	ERJ-3GEYJ102V
18	3	R145, R147, R160	RES TKF 10k 5% 1/10W SMD 0603	Panasonic	ERJ-3GEYJ103V
19	1	R212	RES TKF 100k 5% 1/16W SMD 0402	Yageo	RC0402JR-07100KL
20	1	R223	RES TKF 560R 1% 1/10W SMD 0603	Yageo	RC0603FR-07560RL
21	1	U9	MOD DC-DC OKR-T/3-W12-C 6V 15W	Murata Electronics North America	OKR-T/3-W12-C
22	2	U11, U13	MOD DC-DC OKR-T/6-W12-C 6V 30W	Murata Power Solutions Inc.	OKR-T/6-W12-C

NOTES:

Appendix C. PCB Silk Screens

C.1 INTRODUCTION

This appendix shows the top and bottom silk screens of the EVB-PCI11414 Evaluation Kit.

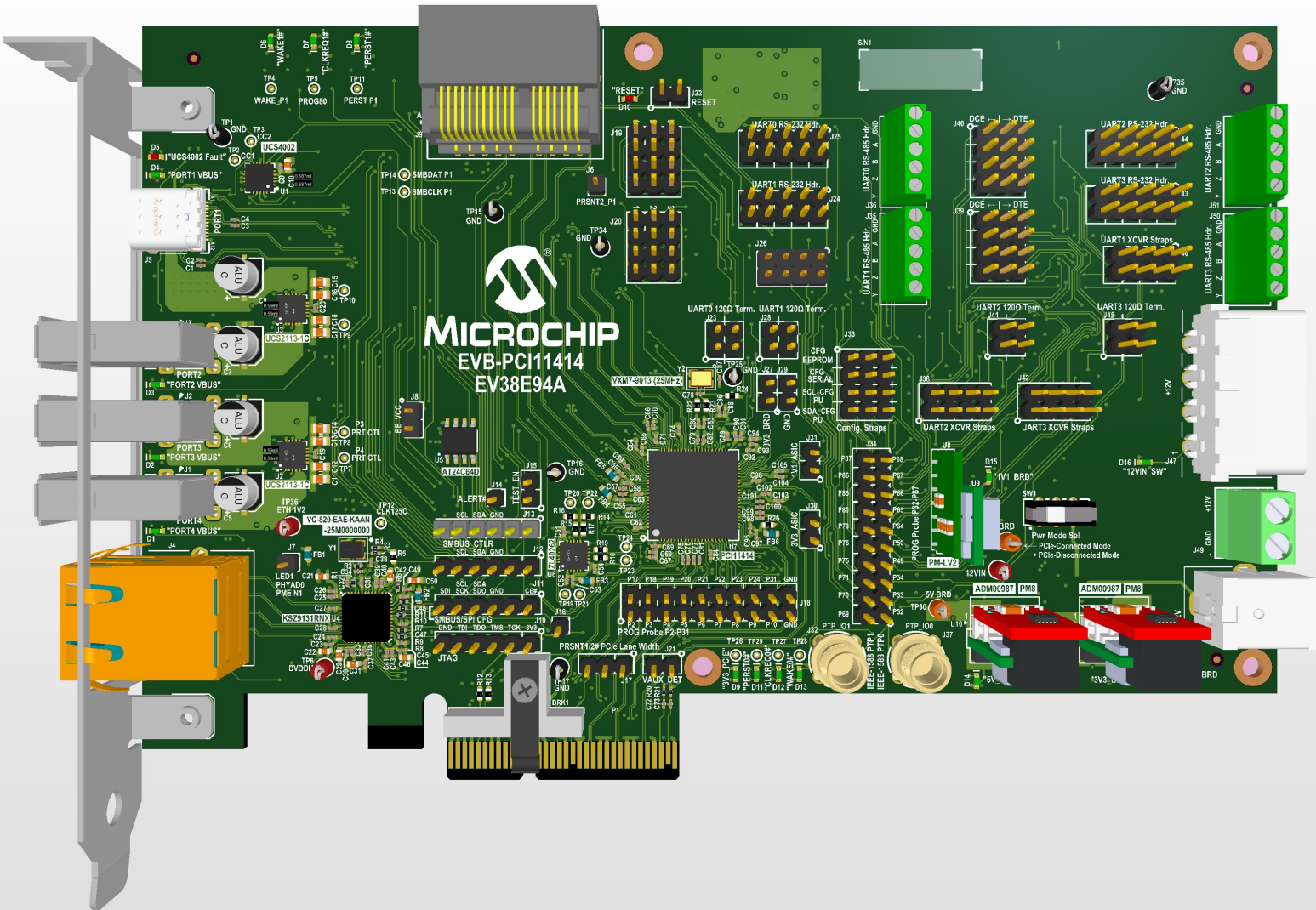
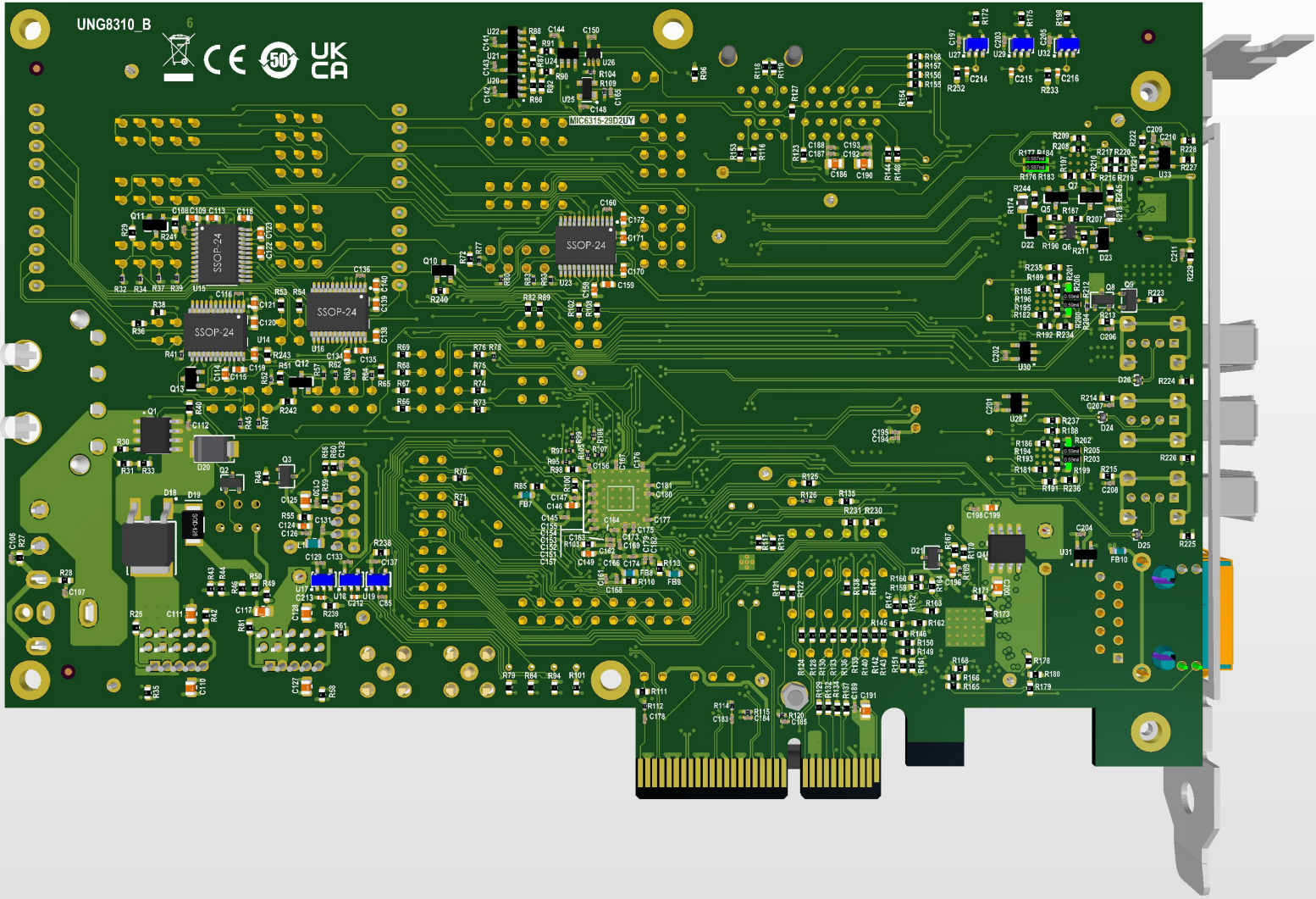


FIGURE C-2: EVB-PC111414 BOTTOM SILK SCREEN IMAGE



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