ADVANCED POWER COMPONENTS

Commercial and Industrial Electronic Components

SERIALVIEW LDDB0
NETVIEW LDDB1

LCD controller for Text & Graphics Display

DATE	DESCRIPTION OF CHANGE

APC-Hero Div., Advanced Power Components plc, Phoenix House, 2 Phoenix Park, Eaton Socon, St. Neots, PE19 8EP England
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LDDBx is part of the **VIEW BY WIRE**™ range of display driver boards aimed at enabling small to medium monochrome and colour displays to be driven from either a low cost serial interface or an optional Ethernet interface.

LDDBx Features

- Epson display controller with 80K byte of embedded SRAM.
- Drives active matrix TFT and Passive single and dual scan displays. Up to 640 x 480 resolution. Direct connection for Sharp's LQ038Q5DR01 320x240 TFT and LM038QC1T10 CSTN.
- 1/2/4/8 bit-per-pixel (bpp) colour depth support.
  640x480 at 2bpp
  640x240 at 4bpp
  320x240 at 8bpp
- Up to 16 shades of grey on monochrome panels.
- Hardware portrait mode enabling direct hardware 90º rotation of display image.
- 3.3V and 5V panel support.
- RS232 and Ethernet interfaces (LDDB1 has the Ethernet option).
- LCD VEE voltage generation on board with contrast adjustment.
- 128K byte of E^2prom on board for picture storage.
- Optional onboard CCFL inverter.
- Character set built in to microcontroller flash memory.
- Character size 8x8 and 8x16 available.
- Foreground and background character colour attributes.
- Direct write and character write modes.
- Block transfer of graphics data from E^2 memory to display memory.
- Stand alone slide show capability.
- Storage of Display controller set-up registers and look-up table in microcontroller internal E^2 memory enabling automatic display initialisation on power up.
- On board flash based in circuit programmable microcontroller for easy updates and customisation. (Interface directly to MPLAB® ICD via CN2).

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Link 7 and 8
Operation:

LK7 1&2
LK8 1&2
RS232 Input to board via CN1.

LK7 2&3
LK8 2&3
RS232 Input directed to Xport. (LDDB1 option)

LK7 3&4
LK8 3&4
Xport Input to board via Ethernet. (LDDB1 option)

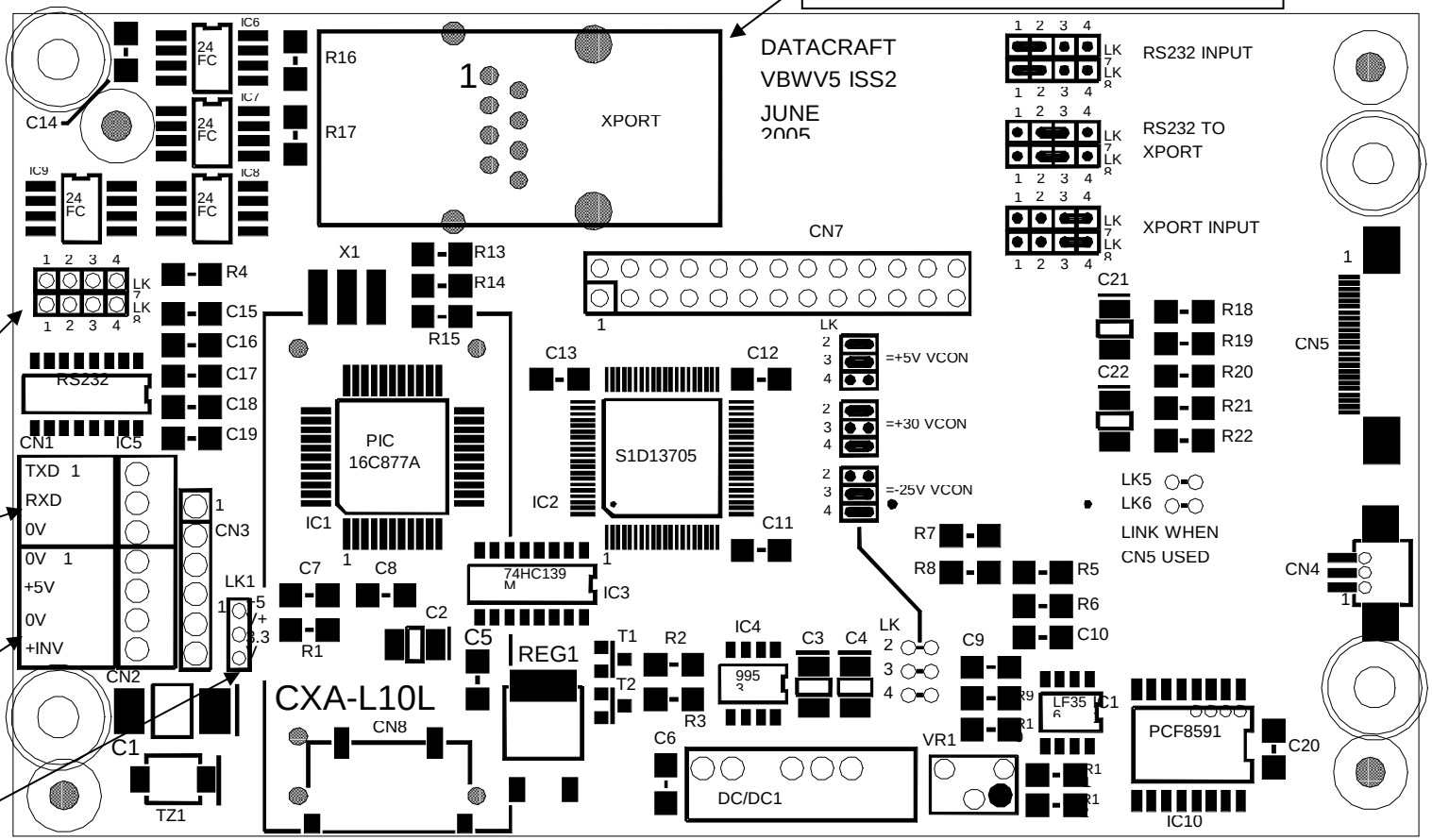
CN1
RS232 Input.

CN2
Power Input.

LK1 set to 3.3V for LQ038 Display

Ethernet connection
(LDDB1 OPTION ONLY)

IP=192.168.0.11
Submask=255.255.255.0
Port=3001



!HIGH VOLTAGE!
LQ038 Display Back Light Connection.

Connect LQ038 Display to CN6 on back of board.

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Interconnection details

CN1 Interface connection Molex 22-05-1032	
PIN	SIGNAL
1	TXD RS232
2	RXD RS232
3	0V

CN2 Power connection Molex 22-05-1042	
PIN	SIGNAL
1	0V
2	+5V
3	0V
4	+INV (BACKLIGHT)

CN3 Programming interface for firmware updates. 0.1" Header	
PIN	SIGNAL
1	PGM
2	PGC
3	PGD
4	0V
5	+5V
6	VPP

CN4 Backlight inverter interface Molex 53261-0390	
PIN	SIGNAL
1	+INV Safe (switched via LCDPWR pin.) Origin = CN2 pin 4
2	0V
3	+5V Safe (switched via LCDPWR pin.)

CN5 CSTN Interface. (LM038Qxxx compatible) 0.5mm pitch FFC	
PIN	SIGNAL
1	VSS
2	FPLINE
3	VDD
4	FPD0
5	FPD1
6	FPD2
7	FPD3
8	Vc
9	DISP/OFF
10	VSS
11	FPSHIFT
12	Vbl
13	FPD4
14	FPD5
15	FPD6
16	FPD7
17	Vbh
18	M
19	FPFRAME
20	Vsh
21	VSS
22	Vsl
23	NC
24	NC

CN6 TFT interface. (LQ038Q5 compatible) JAE KX15-40K4-D1			
PIN	SIGNAL	PIN	SIGNAL
1	VSS	2	VCC
3	FPLINE	4	FPD5 (G3)
5	T0	6	FPD4 (G4)
7	T1	8	FPD3 (G5)
9	HVR (0V)	10	VSS
11	VSS	12	FPD11 (B0)
13	FPSHIFT	14	FPD11 (B1)
15	VSS	16	FPD8 (B2)
17	FPD9 (R0)	18	VSS
19	FPD9 (R1)	20	FPD8 (B3)
21	FPD2 (R2)	22	FPD7 (B4)
23	VSS	24	FPD6 (B5)
25	FPD2 (R3)	26	VSS
27	FPD1 (R4)	28	FPFRAME
29	FPD0 (R5)	30	TEST
31	VSS	32	TEST
33	FPD10 (G0)	34	TEST
35	FPD10 (G1)	36	TEST
37	FPD5 (G2)	38	DRDY
39	VCC	40	VSS

CN7 General Purpose Display Connection 26 Way IDC			
PIN	SIGNAL	PIN	SIGNAL
1	VEE+	2	VEE-
3	VEECON	4	+12V Safe
5	+5V/3.3V	6	+5V/3.3V
7	0V	8	FPSHIFT
9	0V	10	LCDPWR
11	M/DRDY	12	FPFRAME
13	FPLINE	14	FPD0
15	FPD1	16	FPD2
17	FPD3	18	FPD4
19	FPD5	20	FPD6
21	FPD7	22	FPD8
23	FPD9	24	FPD10
25	FPD11	26	GPIO

Jumper Link details

LK1 2mm jumper Link.	
LINK	SIGNAL
1&2	+5V Display
2&3	3.3VDisplay

LK1 sets the operating voltage to either 5V or 3.3V.
For LM038Q and LQ038Q5 displays link 2&3 for 3.3V.

LK2-6 2mm Jumper Link two only	
LINK	SIGNAL
2 & 3	For +5V VEECON
2 & 4	For +30V VEECON
3 & 4	For -25V VEECON
5 & 6	Link for LM038Q only.

LK2-4 sets the LCD VEE voltage level. These affect the VEE+ VEE- and VEECON levels as shown in the table.
Note: link only the combinations shown. These voltages assume a +/- 15V DC/DC converter.
For LM038Q link LK4, LK5 and LK6 only.
For LQ038Q5 leave links LK2 to LK6 open.

LK7 & 8 2mm jumper Link.	
LINK	SIGNAL
LK7 1&2 LK8 1&2	RS232 input to board via CN1.
LK7 2&3 LK8 2&3	RS232 input directed to Xport.
LK7 3&4 LK8 3&4	Xport input to board via Ethernet.

LK7 and LK8 select the various options for communication with the SerialView or NetView boards.

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Stx=02h Etx=03h Data=00h to ffh Ack=06h Nak=15h Dc4=14h Null=00h

Command	Hex	Sequence
Graphics mode.	10	Stx,address,10,data---data,etx,etx
External EE memory mode.	11	Stx,address,11,data---data,etx,etx
Set writing address to Display.	12	Stx,address,12, address0-7, address8-15, address16, etx,etx
Set writing address to EE mem.	13	Stx,address,13, address0-7, address8-15, address16-24, etx,etx
Transfer block from EE mem to display.	14	Stx,address,14, width0-7, width8-15, height0-7, height8-15, etx,etx
Read internal EE memory.	15	Stx,address,15,address,address,----,etx,etx
Write 1375 set-up data to internal EE memory.	16	Stx,address,16, address, data---data, etx,etx
Initialise 1375 registers.	17	Stx,address,17, etx,etx
Character mode.	18	Stx,address,18, data---data, etx,etx
Set writing position.	19	Stx,address,19, x-data, y-data, etx,etx
Set character attribute.	1A	Stx,address,1A, size-data, foreground-colour-data, background-colour-data, etx,etx
Clear all display memory	1B	Stx,address,1B, etx,etx
Transfer compressed block from EE mem to display.	1C	Stx,address,1C, width0-7, width8-15, height0-7, height8-15, etx,etx
Set contrast voltage.	1D	Stx,address,1D, contrast, etx,etx

Protocol description

Data is sent to the LDDBx board in packets framed with Stx (02h) and Etx Etx (03h 03h). The Byte following the Stx character is the board address 00 to FFh, this enables several boards to be on one bus. Sending address 00 will access all boards regardless of their address value. The Byte following the address defines the command. To prevent false end of packet sequences occurring in data being sent the following action should be taken: If Etx (03h) occurs in the data, the transmitter should send a Null (00h) character after it, the receiver then detects this 03h 00h sequence removes the 00h and writes 03h as data. This ensures genuine end of packet sequences and general data are distinguishable.
After the end of packet sequence Etx Etx an Ack(06h) character is transmitted to confirm success. If an error occurred then a Nak(15h) character is transmitted.

Command description

Graphics Mode 10h
After the 10h command any amount of data can be sent which will be stored in display memory starting at the address set by command 12h. The address is auto-incremented after each write.

External E^2 Memory Mode 11h
After the 11h command any amount of data can be sent which will be stored in external E^2 memory starting at the address set by command 13h. The address is auto-incremented after each write. Also after every 64 writes a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

Set writing address to Display 12h
The three bytes following the 12h command define the display memory writing address. In the order Address0_7, Address8_15, Address16. Note only the first bit in byte three is used as the address range is A0 to A16.

Set writing address to E^2 Memory 13h
The three bytes following the 13h command define the E^2 memory writing address. In the order Address0_7, Address8_15, Address16-24. Note Address16-24 is included for future increases in memory size.

Transfer block from E^2 memory to Display memory 14h
The four bytes following the 14h command define the width and height of the block to be transferred as follows: The first two bytes width0_7 and width8_15 define the block width in bytes -1, ie. At 4bpp a width value of 23 will give a pixel width of 48. The second two bytes height0_7 and height8_15 define the block height in pixels-1. Ie. A height value of 47 will give a height of 48 pixels.
Before executing this command the set writing address commands 12h and 13h should be set. After completion, a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

Read internal E^2 memory 15h
The command 15h enables data to be read from the Microcontroller internal E^2 memory. Address bytes following the command are replied to with the data at that address. Etx,etx ends the command

Initialise controller registers 17h
The command 17h initialises the controller registers and look up table, from the Microcontroller internal E^2 memory, a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

Character Mode 18h
After this command 18h data is accepted as ASCII character data and characters are written to the display. Back space 08h, Carriage return 0Dh and Line feed 0Ah are also interpreted. After each character a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure. The character set is stored in the Microcontroller flash memory and can easily be modified. Please contact supplier for more details.

Set character writing position 19h
The two bytes following the 19h command define the X and Y positions in characters (8x8) where the next character will be written. (0,0 = top left).

Set character attributes 1Ah
The three bytes following the 1Ah command define the character attributes as follows: Character size 0 for 8x8 and 1 for 8x16. Foreground colour byte. Background colour byte. Default is 00h, 0Fh, 00h.

Clear all display memory 1Bh
All display memory is filled with 00h, a DC4 (14h) character is transmitted to confirm success or Nak (15h) for failure.

Transfer compressed block from E^2 memory to Display memory 1Ch
This command operates the same as command 14h except the transfer routine assumes compressed image data (8 bit RLE used). For certain types of image where there are large blocks of the same colour compression improves both speed and memory space used.

Adjust contrast voltage 1Dh
This command allows adjustment of the contrast voltage around the voltage set by VR1. 00= minimum and FFh = maximum contrast value.

Write controller set-up data to internal E^2 memory 16h

The command 16h enables data to be written to the Microcontroller internal E^2 memory. This memory holds display register, colour look up table, interface set-up and slide show information. This is used to configure the board on power-up or after command 17h. The first byte following the command defines the address, which is then followed by data. The address auto-increments after each write and a DC4 (14h) character is transmitted after each byte to confirm success.

The correspondence between the internal E^2 memory and display controller registers are defined in the following table:

Internal E^2 memory address	Display controller register value	Example value for 320 x 240 colour STN at 4 Bpp (16 colours)	Register description.
00h	01h	27h	Mode register 0
01h	02h	90h	Mode register 1
02h	03h	03h	Mode register 2
03h	04h	27h	Horizontal panel size register = (width in pixels/8)-1
04h	05h	Efh	Vertical panel size (lsb) –1
05h	06h	00h	Vertical panel size (msb)
06h	07h	00h	Fpline start position.
07h	08h	00h	Horizontal non-display period.
08h	09h	00h	Fpframe start position.
09h	0Ah	03h	Vertical non-display period.
0Ah	0Bh	00h	Mod rate register.
0Bh	0Ch	00h	Screen1 start address register (lsb).
0Ch	0Dh	00h	Screen1 start address register (msb).
0Dh	0Eh	00h	Screen2 start address register (lsb).
0Eh	0Fh	00h	Screen2 start address register (msb).
0Fh	10h	00h	Screen1 start address register overflow (A16).
10h	11h	00h	Memory address offset register.
11h	12h	FFh	Screen1 vertical size register (lsb).
12h	13h	03h	Screen1 vertical size register (msb).
13h	18h	00h	GPIO configuration control register.
14h	19h	00h	GPIO status / control register.
15h	1Ah	00h	Scratch pad register.
16h	1Bh	00h	Swivel view mode register.
17h	1Ch	00h	Swivel view line byte count register.
18h,19h,1Ah	17h	00h,00h,00h	Look up table RGB index value 00 (black).
1Bh,1Ch,1Dh	17h	80h,00h,00h	Look up table RGB index value 01 (dark red).
1Eh,1Fh,20h	17h	00h,80h,00h	Look up table RGB index value 02 (dark green).
21h,22h,23h	17h	80h,80h,00h	Look up table RGB index value 03 (dark yellow).
24h,25h,26h	17h	00h,00h,80h	Look up table RGB index value 04 (dark blue).
27h,28h,29h	17h	80h,00h,80h	Look up table RGB index value 05 (dark magenta).
2Ah,2Bh,2Ch	17h	00h,80h,80h	Look up table RGB index value 06 (dark cyan).
2Dh,2Eh,2Fh	17h	B0h,B0h,B0h	Look up table RGB index value 07 (light grey).
30h,31h,32h	17h	70h,70h,70h	Look up table RGB index value 08 (dark gray).
33h,34h,35h	17h	F0h,00h,00h	Look up table RGB index value 09 (light red).
36h,37h,38h	17h	00h,F0h,00h	Look up table RGB index value 10 (light green).
39h,3Ah,3Bh	17h	F0h,F0h,00h	Look up table RGB index value 11 (light yellow).
3Ch,3Dh,3Eh	17h	00h,00h,F0h	Look up table RGB index value 12 (light blue).
3Fh,40h,41h	17h	F0h,00h,F0h	Look up table RGB index value 13 (light magenta).
42h,43h,44h	17h	00h,F0h,F0h	Look up table RGB index value 14 (light cyan).
45h,46h,47h	17h	F0h,F0h,F0h	Look up table RGB index value 15 (white).

Note: For displays requiring 8Bpp (256 colour) the remainder of the look up table will need to be loaded via the serial interface, directly into the display controller.

Internal E^2 memory address	Display controller register value	Example value for 320 x 240 colour STN at 4 Bpp (16 colours)	Register description.
48h	Na	9Fh	Display block on power up width0-7
49h	Na	00h	Display block on power up width8-15
4Ah	Na	EFh	Display block on power up height0-7
4Bh	Na	00h	Display block on power up height0-15
4Ch	Na	53h	Software identification low byte (Checksum used)
4Dh	Na	C8h	Software identification high byte (Checksum used)
4Eh	Na	04h	Serial Baud rate 0=9600, 1=19200, 2=38400, 3=57600, 4=115200.
4Fh	Na	01h	I^2C rate 0=normal (LC chips) 1=fast (FC chips)
50h	Na	00h	Board address. 00 to FFh. (Avoid address 03h)
51h	Na	05h	Slide show time between slides in seconds.
53h, 52h	Na	2710h	Slide show E^2 memory spacing between images.
55h, 54h	Na	009Fh	Slide show block width slide 1.
57h, 56h	Na	00Efh	Slide show block height slide 1.
59h, 58h	Na	009Fh	Slide show block width slide 2.
5Bh, 5Ah	Na	00Efh	Slide show block height slide 2.
5Dh, 5Ch	Na	009Fh	Slide show block width slide 3.
5Fh, 5Eh	Na	00Efh	Slide show block height slide 3.
61h, 60h	Na	009Fh	Slide show block width slide 4.
63h, 62h	Na	00Efh	Slide show block height slide 4.
65h, 64h	Na	009Fh	Slide show block width slide 5.
67h, 66h	Na	00Efh	Slide show block height slide 5.
69h, 68h	Na	009Fh	Slide show block width slide 6.
6Bh, 6Ah	Na	00Efh	Slide show block height slide 6.
6Dh, 6Ch	Na	009Fh	Slide show block width slide 7.
6Fh, 6Eh	Na	00Efh	Slide show block height slide 7.
71h, 70h	Na	009Fh	Slide show block width slide 8.
73h, 72h	Na	00Efh	Slide show block height slide 8.
75h, 74h	Na	009Fh	Slide show block width slide 9.
77h, 76h	Na	00Efh	Slide show block height slide 9.
79h, 78h	Na	009Fh	Slide show block width slide 10.
7Bh, 7Ah	Na	00Efh	Slide show block height slide 10.
81h	Na	80h	Contrast setting.

If the address 48h has any value other than FFh then a transfer compressed block command is carried out on power-up using the width and height values in the internal E^2 memory from 48h to 4Bh. Assumes the image is stored at external E^2 memory address 000000.

Address 4Ch and 4Dh contain the PIC software checksum for identification purposes.

Address 4Eh contains the serial baud rate set at power-up, 0=9600, 1=19200, 2=38400, 3=57600, 4=115200.

Address 4Fh contains the I^2C rate set at power-up, 0=normal (LC chips) 1=fast (FC chips).

Address 50h contains the board address. The board will respond to commands when the address sent corresponds to the value storred at this location or the address sent is 00h. Avoid using address 03h as it can conflict with the end of packet character.

To set-up the slide show first down load your compressed images into the E^2 memory spaced at a fixed address boundary. I.e. every 10000 (2710h) .
Set address 51h to the time delay between slides in seconds i.e. 05h.
Set the image spacing into addresses 53h and 52h. i.e. 53h=27h 52h=10h.
Set the block width and height for each slide, if there are less than 10 slides then set the remaining block widths and heights to FFh. When the software encounters FFh it loops back to the first image. If no slide show is required fill all the block widths and heights with FFh.
Once the LDDBx internal E^2 memory is written to then the slide show will start immediately.

Please note whilst the LDDBx is communicating over the serial interface the slide show timer is stopped Some errors may occur if communication is tried whilst the LDDBx slide show is updating the screen.

RS232 Interface

Format:
Baud rate: 19200 (default)
Data: 8 bits
Parity: None
Stop bits: 1

Ethernet Interface

The Ethernet interface is via an Xport Ethetnet to RS232 converter. This enables the board to operate in the same way as with the RS232 interface except via a network.

Optional CCFL inverter

The LDDBx has the ability to mount a CXA-L10L inverter on board that can be used to power the LQ038Q5 display backlight.

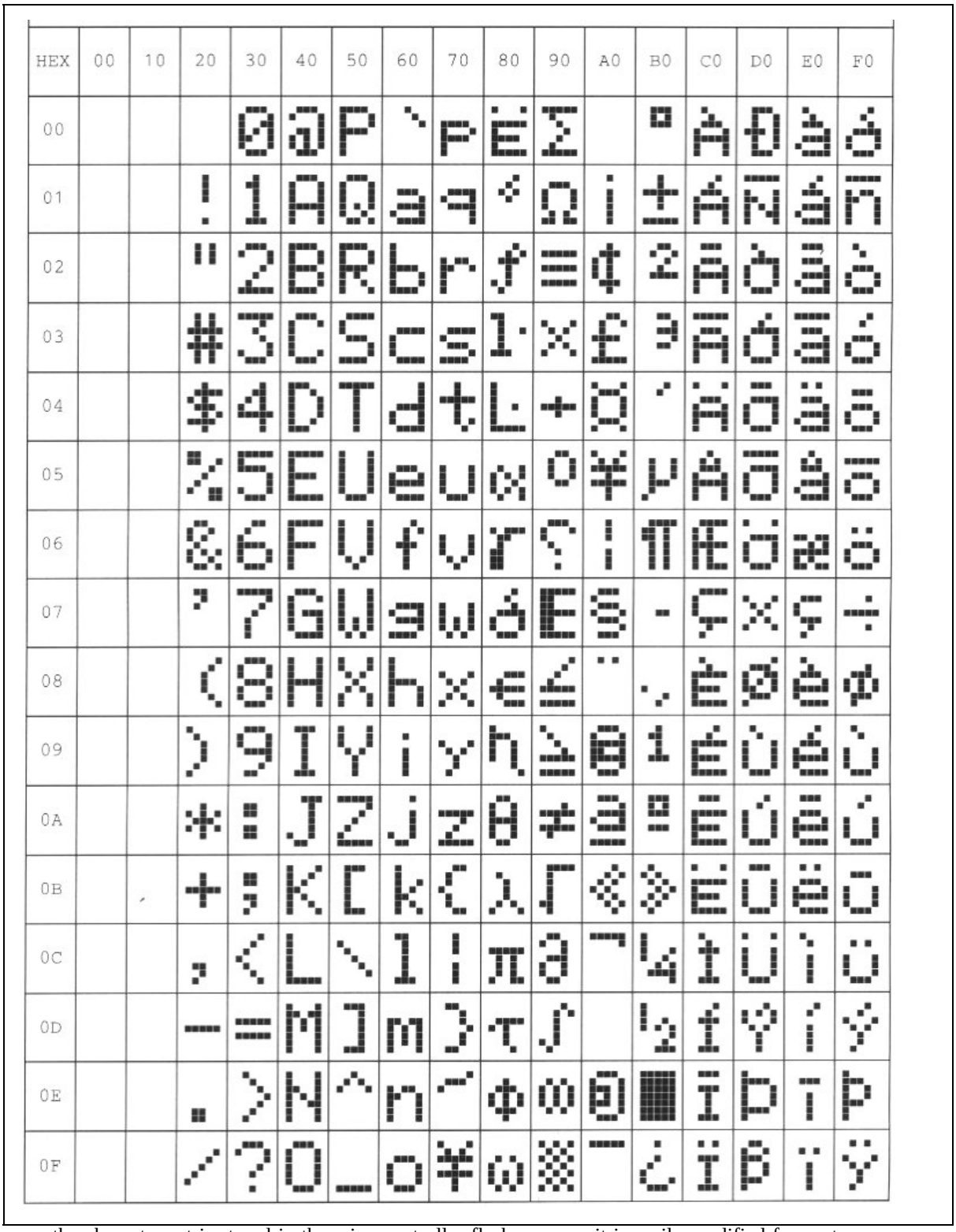
Electrical specification

SYMBOL	PARAMITER	MIN	TYP	MAX	UNIT
VCC in	LogicSupply voltage	4.5	5.0	5.5	V
+INV in	Back light inverter supply voltage	0.0	12.0	15.0	V
VDD Safe out	Switched +5V out	VCC	VCC	VCC	V
IDD Safe out				1.0	A
VEE +/-	LCD Bias voltage	-25		+30	V
IEE +/-				30	mA
VEECON	LCD Contrast voltage.	-24		+29	V
+INV Safe out	Switched +INV out to back light inverter.	0.0 in	+12V in	+15V in	V
+INVI Safe out				1.0	A
Top	Operating temperature	0		+70	^{o}C
Tstg	Storage temperature	-40		+125	^{o}C

Further information

For further details of the display controller please refer to the Epson S1D13705 Specification.
For further details of the Xport Ethernet to RS232 converter please refer to www.lantronix.com.

Character set



s the character set is stored in the microcontroller flash memory it is easily modified for custom characters. Please contact APC-Hero for further details.