

75V, Synchronous Buck Controller Featuring Adaptive On-Time Control with External Soft Start

Features

- Hyper Speed Control[®] Architecture Enables:
 - High Input to Output Voltage Conversion Ratio Capability
 - Any Capacitor[™] Stable
 - Ultra-Fast Load Transient Response
- Wide 4.5V to 75V Input Voltage Range
- Adjustable Output Voltage from 0.6V to 30V
- 270 kHz to 800 kHz Programmable Switching Frequency
- Built-in 5V Regulator for Single-Supply Operation
- Auxiliary Bootstrap LDO for Improving System Efficiency
- Internal Bootstrap Diode
- Adjustable Soft-Start Time
- Enable Input and Power Good Output
- Programmable Current Limit
- Hiccup Mode Short-Circuit Protection
- Internal Compensation and Thermal Shutdown
- Supports Safe Start-Up into a Prebiased Output

Applications

- Networking/Telecom Equipment
- Base Station, Servers
- Distributed Power Systems
- Industrial Power Supplies

General Description

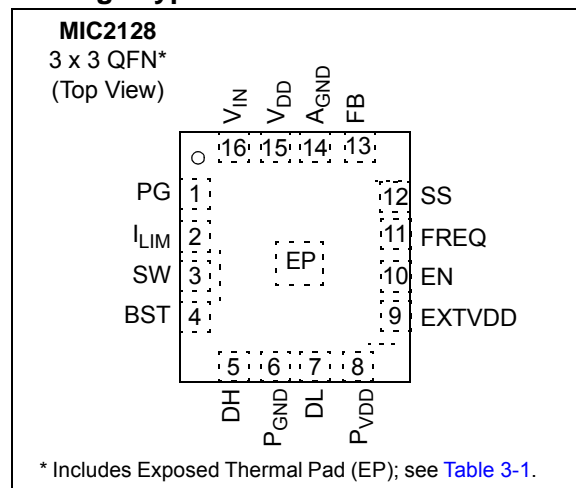
The MIC2128 is a constant-frequency synchronous buck controller featuring a unique adaptive on-time control architecture with external soft start. The MIC2128 operates over an input voltage range from 4.5V to 75V. The output voltage is adjustable down to 0.6V with a guaranteed accuracy of $\pm 1\%$. The device operates with programmable switching frequency from 270 kHz to 800 kHz.

The MIC2128 features an external soft-start pin (SS) which allows the user to adjust output soft-start time to reduce inrush current from mains during start-up. The MIC2128 features an auxiliary bootstrap LDO which improves the system efficiency by supplying the MIC2128 internal circuit bias power and gate drivers from output of the converter. A logic level enable (EN) signal can be used to enable or disable the controller. The MIC2128 can start-up monotonically into a prebiased output. The MIC2128 features an open drain power good signal (PG) which signals when the output is in regulation and can be used for simple power supply sequencing purpose.

The MIC2128 offers a full suite of protection features to ensure protection of the IC during Fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, "hiccup" mode short-circuit protection and thermal shutdown.

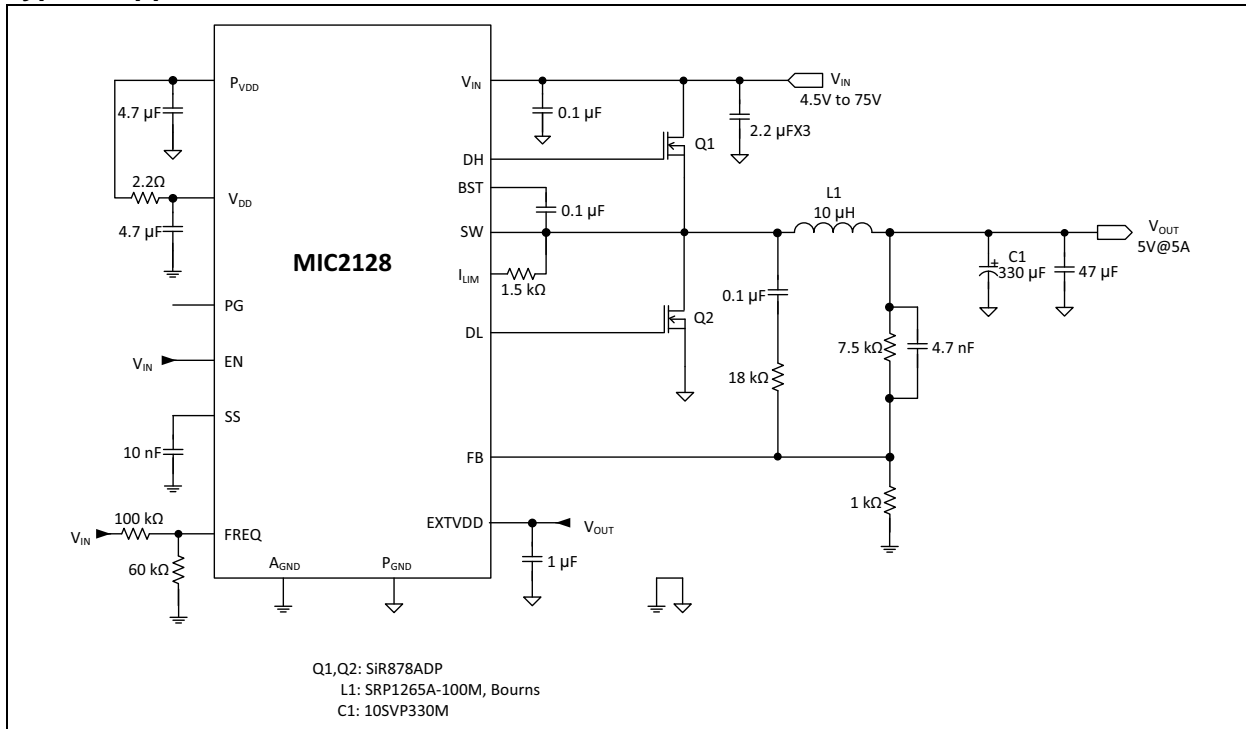
The MIC2128 is available in a 16-pin 3 mm x 3 mm QFN package, with an operating junction temperature range from -40°C to $+125^{\circ}\text{C}$.

Package Types

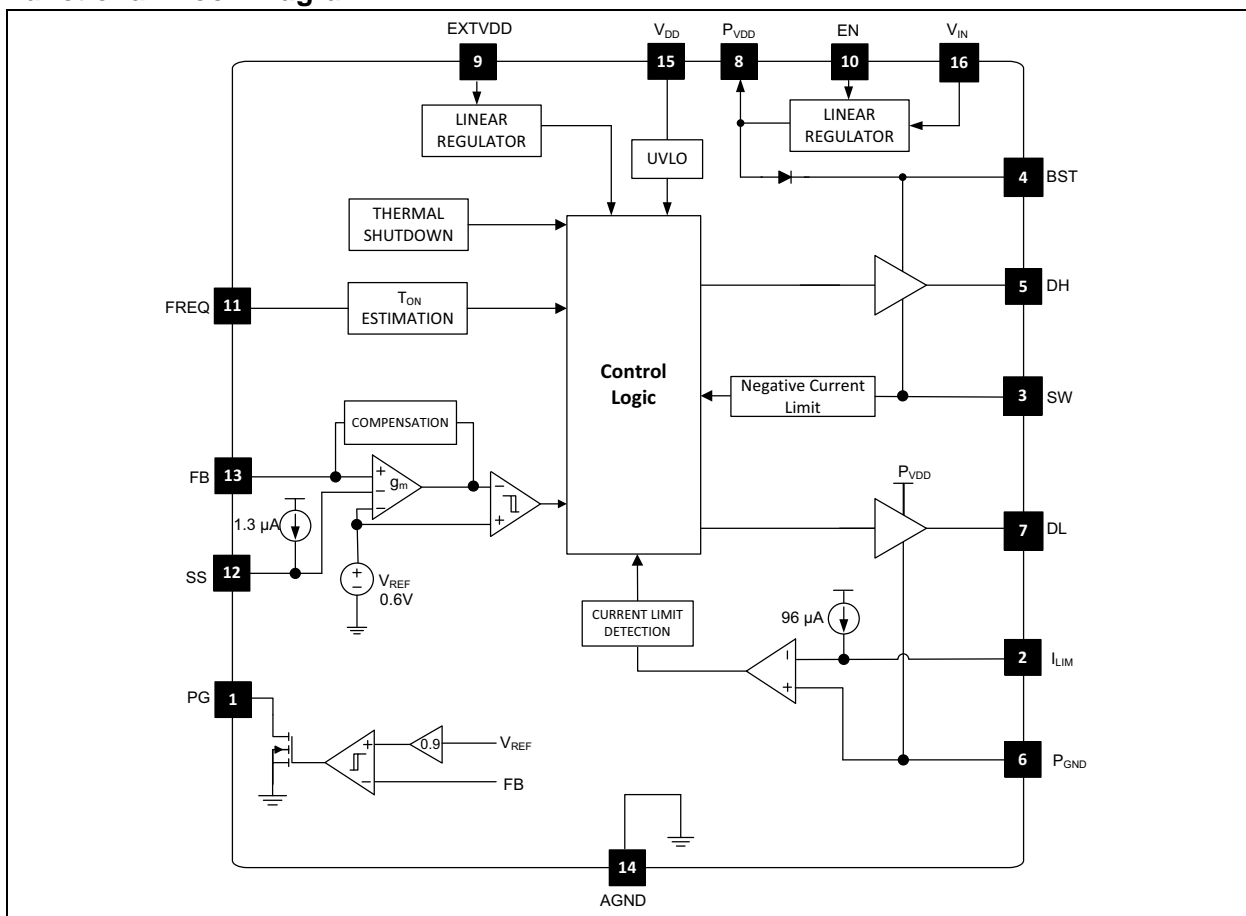


MIC2128

Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} , FREQ, I_{LIM} , SW to P_{GND}	-0.3V to +76V
V_{DD} , P_{VDD} , FB, PG, SS to A_{GND}	-0.3V to +6V
EXTVDD to A_{GND}	-0.3V to +16V
BST to SW	-0.3V to +6V
BST to A_{GND}	-0.3V to +82V
EN to A_{GND}	-0.3V to (V_{IN} +0.3V)
DH, DL to A_{GND}	-0.3V to (V_{DD} +0.3V)
P_{GND} to A_{GND}	-0.3V to +0.3V
Junction Temperature	+150°C
Storage Temperature (T_S)	-65°C to +150°C
Lead Temperature (soldering, 10s)	260°C
ESD Rating ⁽¹⁾	1000V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 k Ω in series with 100 pF.

Operating Ratings⁽¹⁾

Supply Voltage (V_{IN})	4.5V to 75V
SW, FREQ, I_{LIM} , EN	0V to V_{IN}
Junction Temperature (T_J)	-40°C to +125°C
Package Thermal Resistance (3 mm × 3 mm QFN-16)	
Junction to Ambient (θ_{JA})	50.8°C/W
Junction to Case (θ_{JC})	25.3°C/W

Note 1: The device is not ensured to function outside the operating range.

MIC2128

ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, $V_{IN} = 12V$, $V_{OUT} = 1.2V$; $V_{BST} - V_{SW} = 5V$, $T_A = +25^\circ C$. **Boldface** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$ (Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Power Supply Input						
Input Voltage Range	V_{VIN}	4.5	—	5.5	V	P_{VDD} and V_{DD} shorted to V_{IN} ($V_{PVDD} = V_{VIN} = V_{VDD}$)
		5.5	—	75		
Quiescent Supply Current	I_Q	—	1.4	1.8	mA	$V_{FB} = 1.5V$, no switching
Shutdown Supply Current	$I_{VIN(SHDN)}$	—	0.1	5	μA	EN = Low
		—	30	60	μA	EN = Low, $V_{IN} = V_{DD} = 5.5V$
PVDD, VDD and EXTVD						
P_{VDD} Output Voltage	V_{PVDD}	4.8	5.1	5.4	V	$V_{VIN} = 7V$ to $75V$, $I_{PVDD} = 10$ mA
V_{DD} UVLO Threshold	$V_{VDD_UVLO_Rise}$	3.7	4.2	4.5	V	V_{DD} rising
V_{DD} UVLO Hysteresis	$V_{VDD_UVLO_Hys}$	—	600	—	mV	V_{DD} falling
EXTVD Bypass Threshold	V_{EXTVD_Rise}	4.4	4.6	4.85	V	EXTVD rising
EXTVD Bypass Hysteresis	V_{EXTVD_Hys}	—	200	—	mV	
EXTVD Dropout Voltage		—	250	—	mV	$V_{EXTVD} = 5V$, $I_{PVDD} = 25mA$
Reference						
Feedback Reference Voltage	V_{REF}	0.597	0.6	0.603	V	$T_J = 25^\circ C$
		0.594	0.6	0.606	V	$-40^\circ C \leq T_J \leq 125^\circ C$
FB Bias Current	I_{FB}	—	50	500	nA	$V_{FB} = 0.6V$
Enable Control						
EN Logic Level High	V_{EN_H}	1.6	—	—	V	
EN Logic Level Low	V_{EN_L}	—	—	0.6	V	
EN Hysteresis	V_{EN_Hys}	—	150	—	mV	
EN Bias Current	I_{EN}	—	6	30	μA	$V_{EN} = 12V$
ON Timer						
Switching Frequency	f_0	—	800	—	kHz	$V_{FREQ} = V_{VIN}$, $V_{VIN} = 12V$
		230	270	300		$V_{FREQ} = 33\%$ of V_{VIN} , $V_{VIN} = 12V$
Maximum Duty Cycle	D_{MAX}	—	85	—	%	$V_{FREQ} = V_{VIN} = 12V$
Minimum Duty Cycle	D_{MIN}	—	0	—	%	$V_{FB} > 0.6V$
Minimum ON Time	$t_{ON(MIN)}$	—	80	—	ns	
Minimum OFF Time	$t_{OFF(MIN)}$	150	230	350	ns	
Soft-Start						
Soft-Start Current Source	I_{SS}	—	1.3	—	μA	
Current Limit						
Current-Limit Comparator Offset	V_{OFFSET}	-15	0	15	mV	$V_{FB} = 0.59V$
I_{LIM} Source Current	I_{CL}	80	96	110	μA	$V_{FB} = 0.59V$
I_{LIM} Source Current Tempco		—	0.3	—	$\mu A/^\circ C$	
Negative Current Limit Comparator Threshold	—	—	48	—	mV	

Note 1: Specification for packaged product only.

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH} .

ELECTRICAL CHARACTERISTICS (Note 1)

Electrical Specifications: unless otherwise specified, $V_{IN} = 12V$, $V_{OUT} = 1.2V$; $V_{BST} - V_{SW} = 5V$, $T_A = +25^\circ C$. **Boldface** values indicate $-40^\circ C \leq T_J \leq +125^\circ C$ (Note 2).

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
FET Drivers						
DH On-Resistance, High State	$R_{DH(PULL-UP)}$	—	2	3	Ω	
DH On-Resistance, Low State	$R_{DH(PULL_DOWN)}$	—	2	4	Ω	
DL On-Resistance, High State	$R_{DL(PULL-UP)}$	—	2	4	Ω	
DL On-Resistance, Low State	$R_{DL(PULL_DOWN)}$	—	0.36	0.6	Ω	
SW, VIN and BST Leakage						
BST Leakage	—	—	—	30	μA	
V_{IN} Leakage	—	—	—	50	μA	
SW Leakage	—	—	—	50	μA	
Power Good (PG)						
PG Threshold Voltage	V_{PG_Rise}	85	—	95	$\%V_{OUT}$	V_{FB} rising
PG Hysteresis	V_{PG_Hys}	—	6	—	$\%V_{OUT}$	V_{FB} falling
PG Delay Time	PG_R_DLY	—	100	—	μs	V_{FB} rising
PG Low Voltage	V_{OL_PG}	—	70	200	mV	$V_{FB} < 90\% \times V_{NOM}$, $I_{PG} = 1\text{ mA}$
Thermal Protection						
Overtemperature Shutdown	T_{SHDN}	—	150	—	$^\circ C$	Junction temperature rising
Overtemperature Shutdown Hysteresis	T_{SHDN_Hys}	—	15	—	$^\circ C$	

Note 1: Specification for packaged product only.

2: The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH} .

MIC2128

2.0 TYPICAL CHARACTERISTIC CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{VIN} = 12V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

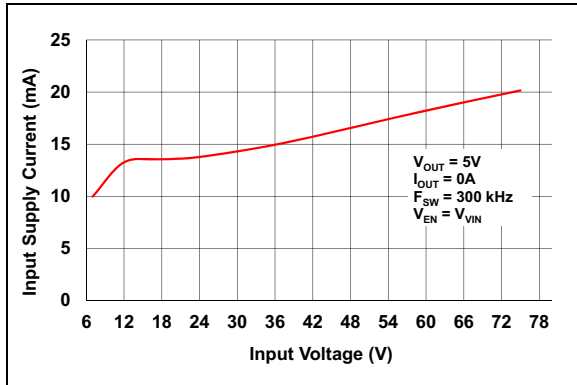


FIGURE 2-1: Input Supply Current vs. Input Voltage.

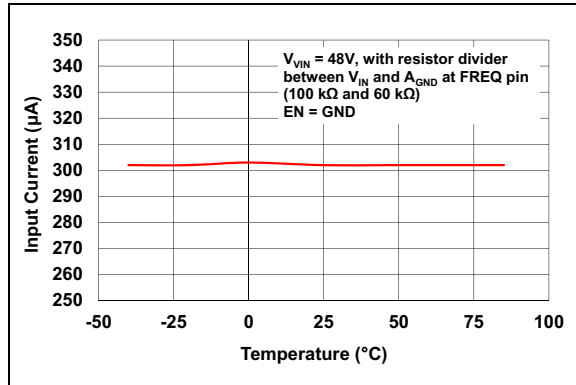


FIGURE 2-4: Input Shutdown Current vs. Temperature.

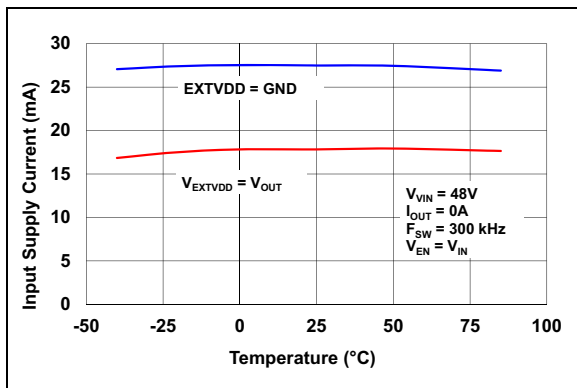


FIGURE 2-2: Input Supply Current vs. Temperature.

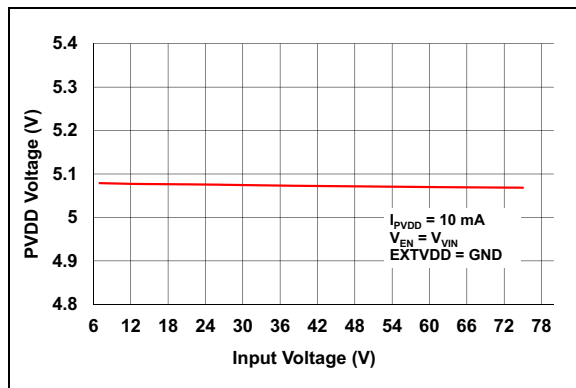


FIGURE 2-5: PVDD Line Regulation

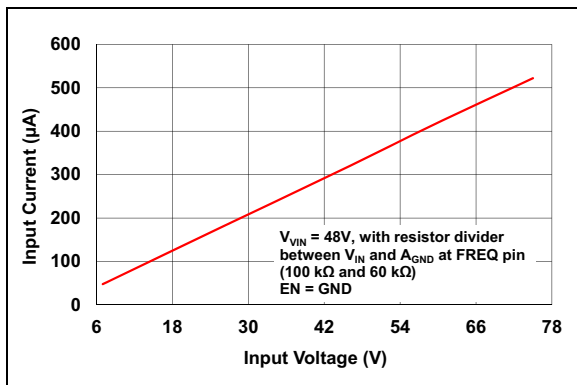


FIGURE 2-3: Input Shutdown Current vs. Input Voltage.

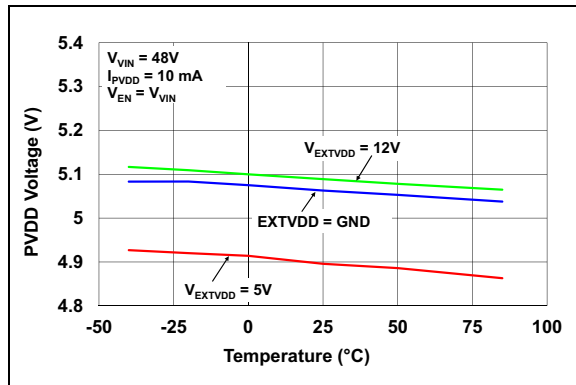


FIGURE 2-6: PVDD Voltage vs. Temperature.

Note: Unless otherwise indicated, $V_{VIN} = 12V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

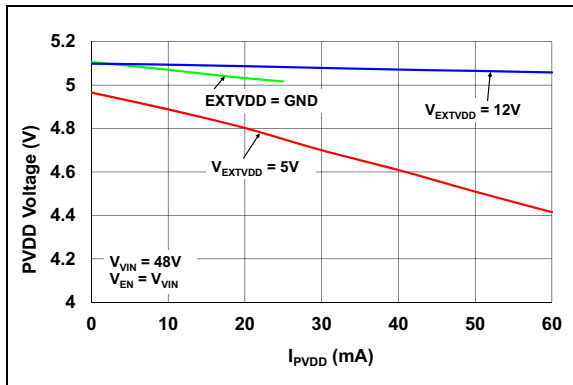


FIGURE 2-7: PVDD Load Regulation.

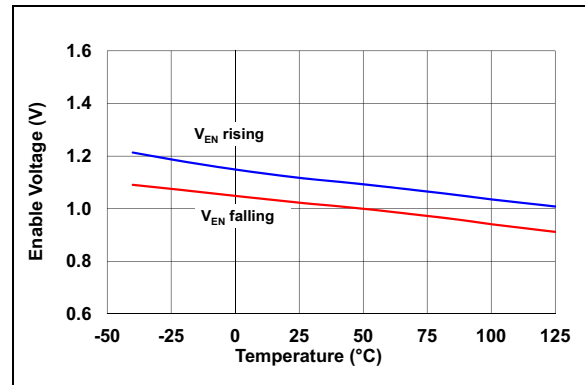


FIGURE 2-10: Enable Threshold vs. Temperature.

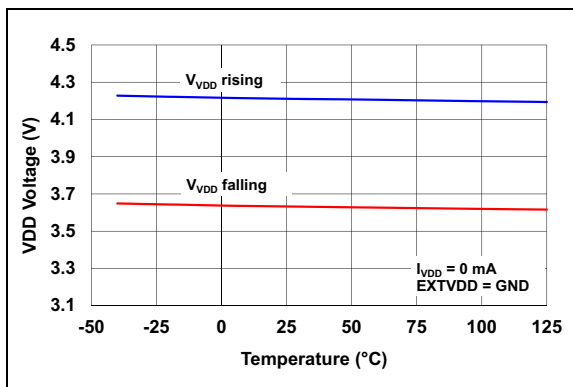


FIGURE 2-8: VDD UVLO Threshold vs. Temperature.

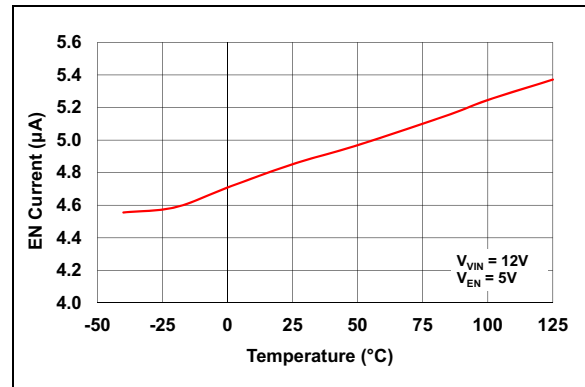


FIGURE 2-11: Enable Bias Current vs. Temperature

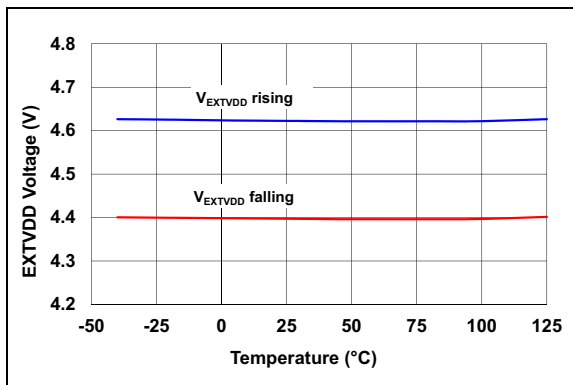


FIGURE 2-9: EXT_VDD Threshold vs. Temperature.

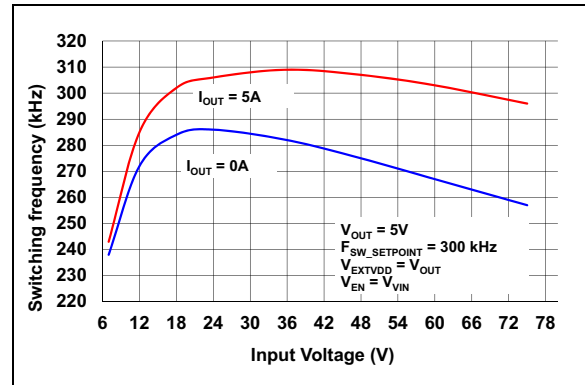


FIGURE 2-12: Switching Frequency vs. Input Voltage.

MIC2128

Note: Unless otherwise indicated, $V_{VIN} = 12V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

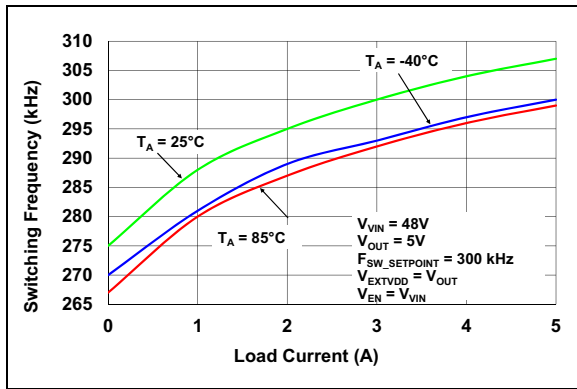


FIGURE 2-13: Switching Frequency vs. Load Current.

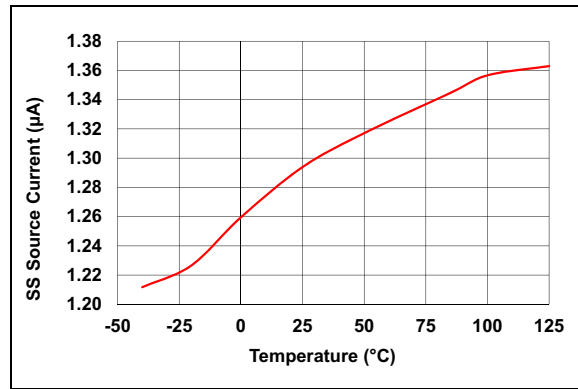


FIGURE 2-16: SS Source Current vs. Temperature.

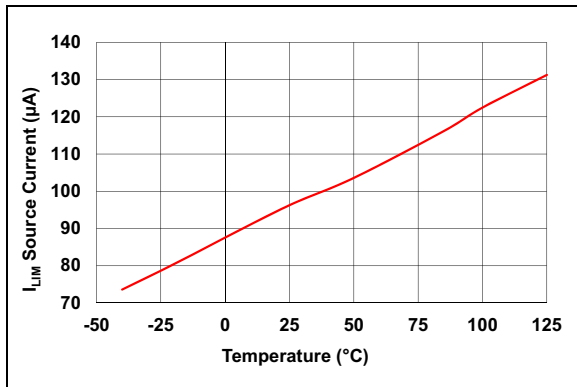


FIGURE 2-14: I_{LIM} Source Current vs. Temperature.

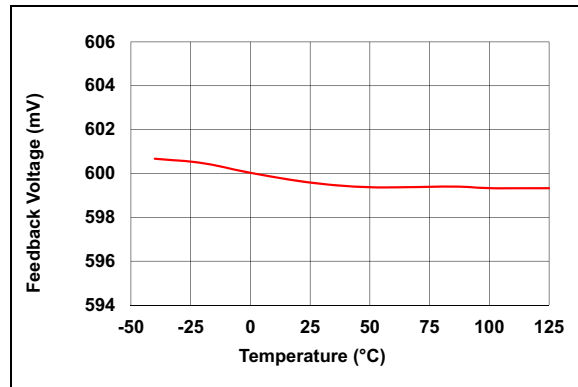


FIGURE 2-17: Feedback Voltage vs. Temperature.

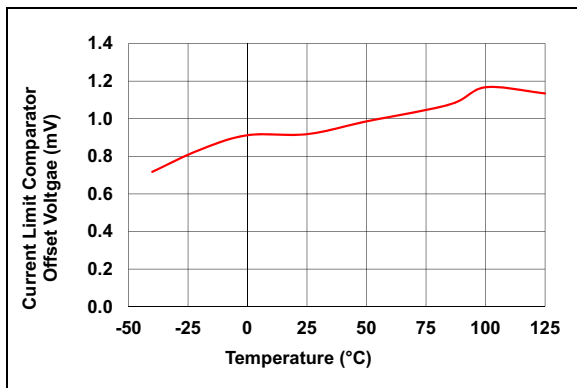


FIGURE 2-15: Current Limit Comparator Offset vs. Temperature.

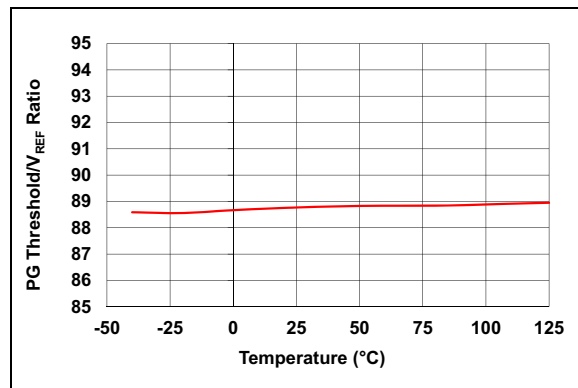


FIGURE 2-18: PG Threshold/ V_{REF} Ratio vs. Temperature.

Note: Unless otherwise indicated, $V_{VIN} = 12V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

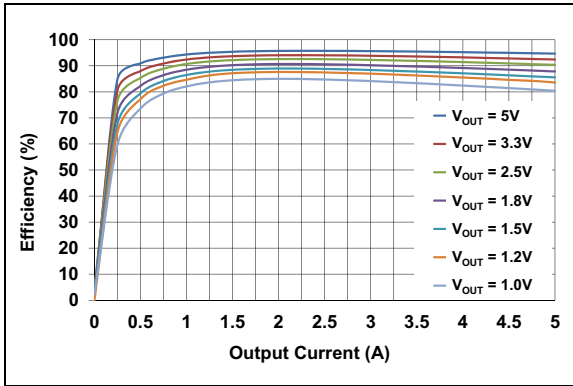


FIGURE 2-19: Efficiency vs. Output Current (Input Voltage=12V).

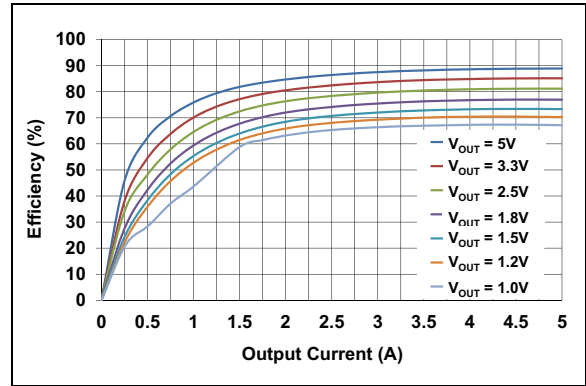


FIGURE 2-22: Efficiency vs. Output Current (Input Voltage = 48V).

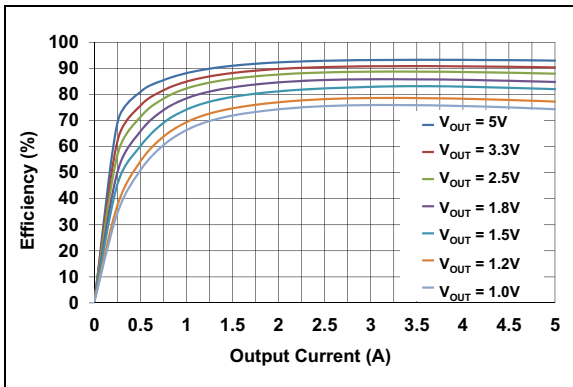


FIGURE 2-20: Efficiency vs. Output Current (Input Voltage = 24V).

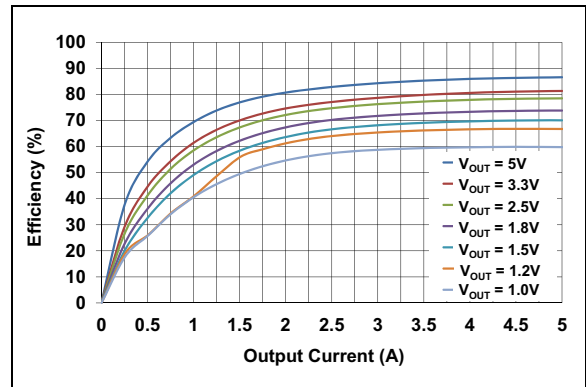


FIGURE 2-23: Efficiency vs. Output Current (Input Voltage = 60V).

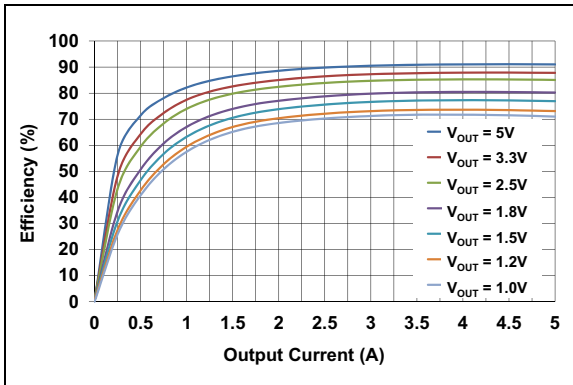


FIGURE 2-21: Efficiency vs. Output Current (Input Voltage = 36V).

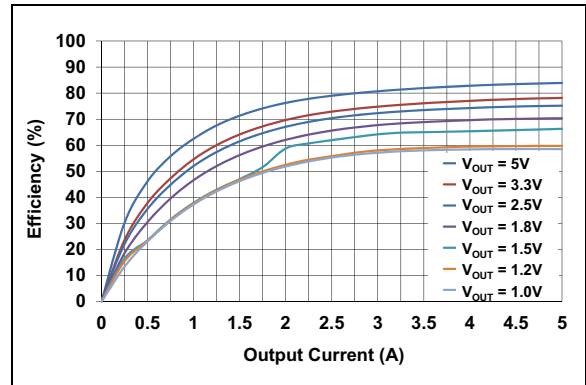


FIGURE 2-24: Efficiency vs. Output Current (Input Voltage = 75V).

MIC2128

Note: Unless otherwise indicated, $V_{VIN} = 12V$, $f_{SW} = 300\text{ kHz}$, $R_{ILIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

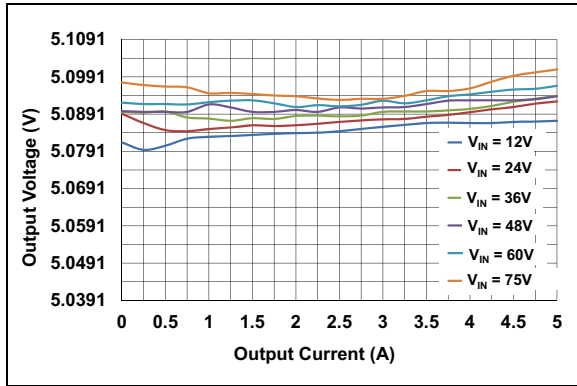


FIGURE 2-25: Load Regulation ($V_{OUT} = 5V$).

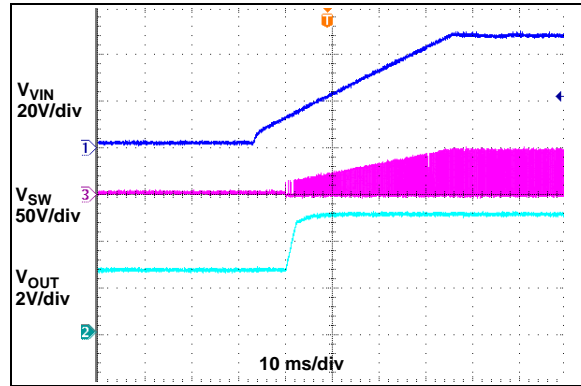


FIGURE 2-28: V_{VIN} Turn-On with Pre-biased Output.

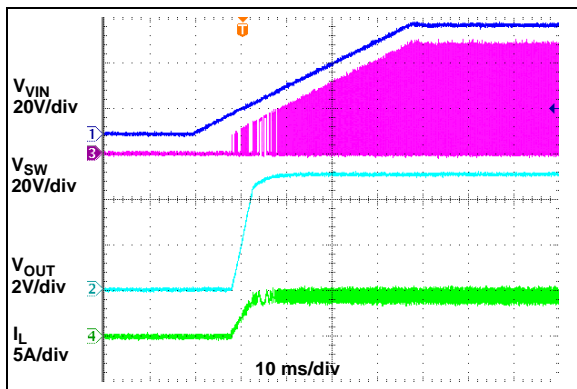


FIGURE 2-26: V_{VIN} Turn-On.

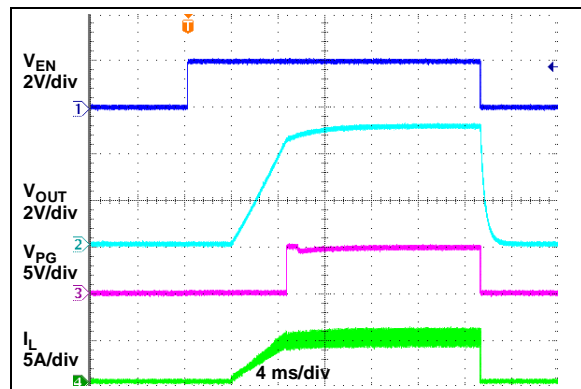


FIGURE 2-29: EN Turn-On/Turn-Off.

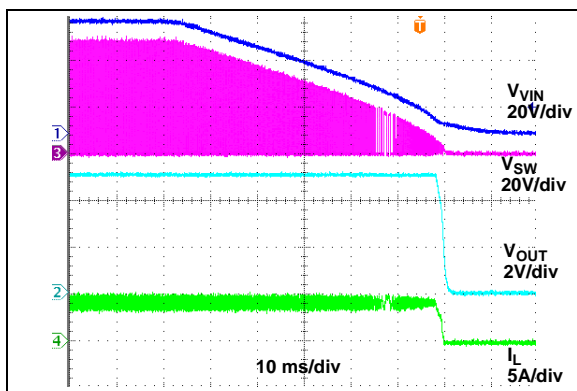


FIGURE 2-27: V_{VIN} Turn-Off.

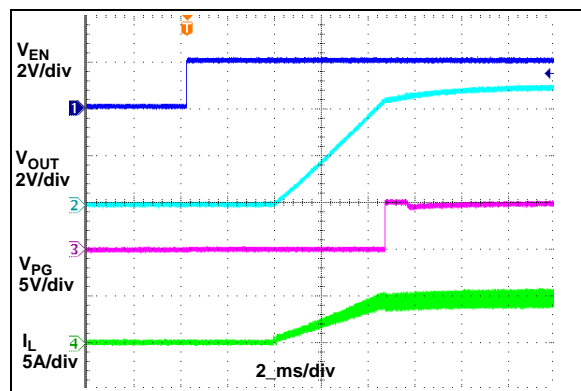


FIGURE 2-30: EN Turn-On Delay.

Note: Unless otherwise indicated, $V_{VIN} = 48V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

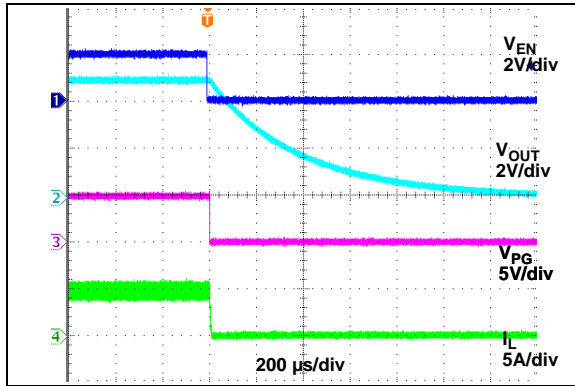


FIGURE 2-31: EN Turn-Off Delay.

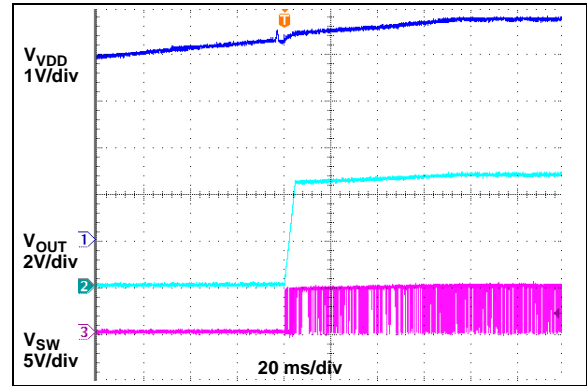


FIGURE 2-34: VDD UVLO Threshold-Rising.

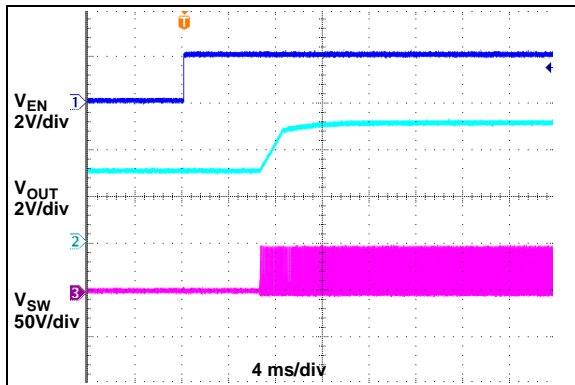


FIGURE 2-32: EN Turn-On with Prebiased Output.

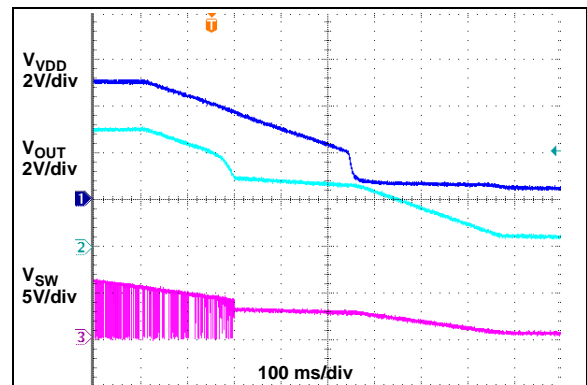


FIGURE 2-35: VDD UVLO Threshold-Falling.

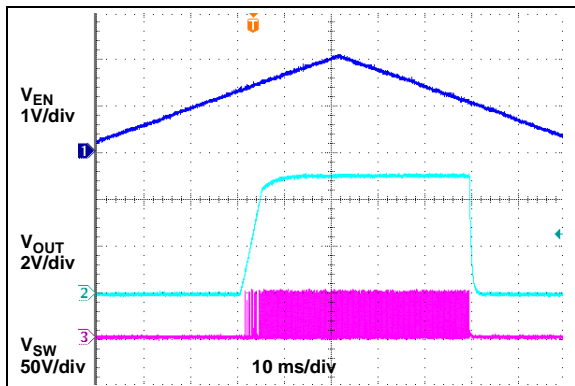


FIGURE 2-33: Enable Thresholds.

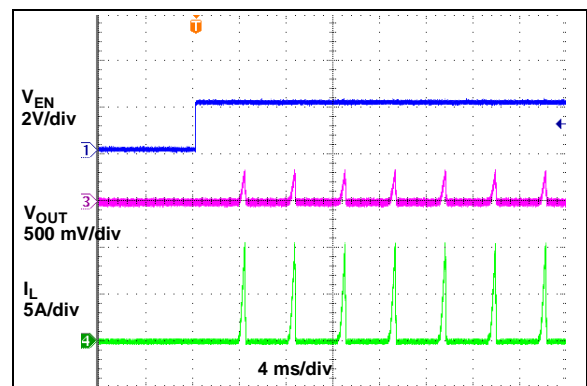


FIGURE 2-36: Enable into Output Short.

MIC2128

Note: Unless otherwise indicated, $V_{VIN} = 48V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

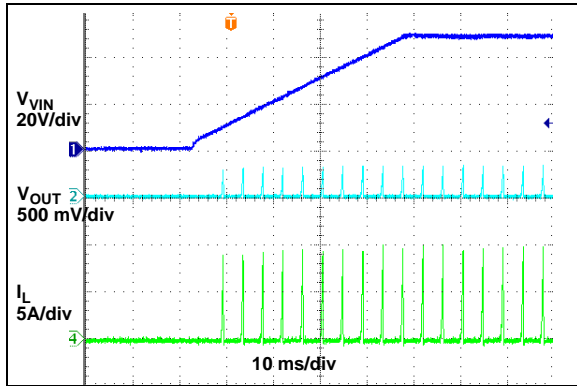


FIGURE 2-37: Power-Up into Output Short.

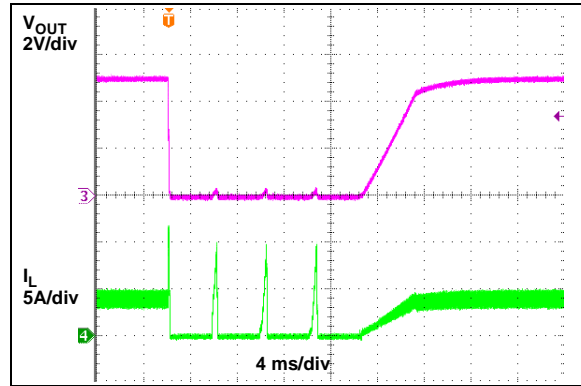


FIGURE 2-40: Recovery from Output Short Circuit.

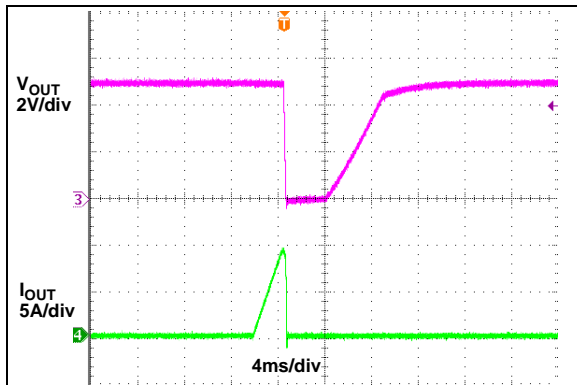


FIGURE 2-38: Output Current Limit Threshold.

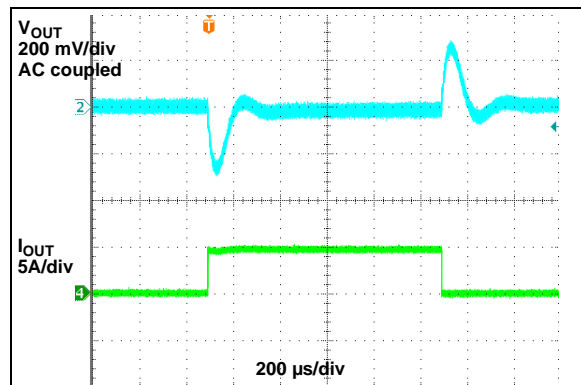


FIGURE 2-41: Load Transient Response ($I_{OUT} = 0A$ to $5A$).

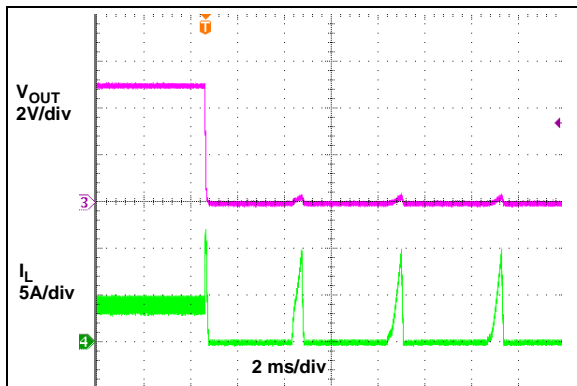


FIGURE 2-39: Output Short Circuit.

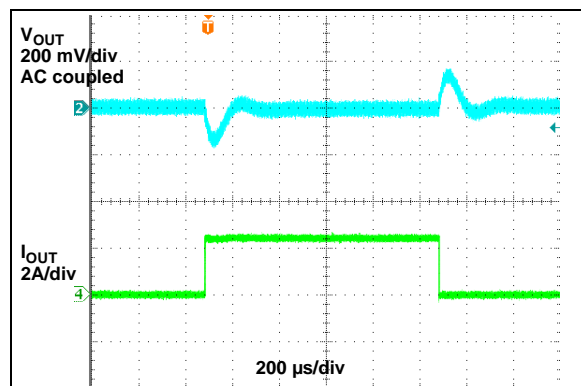


FIGURE 2-42: Load Transient Response ($I_{OUT} = 0A$ to $2.5A$).

Note: Unless otherwise indicated, $V_{VIN} = 48V$, $f_{SW} = 300\text{ kHz}$, $R_{LIM} = 1.5\text{ k}\Omega$, $L = 10\text{ }\mu\text{H}$, $V_{EXTVDD} = V_{OUT}$, $T_A = +25^\circ\text{C}$ (refer to the [Typical Application](#) circuit).

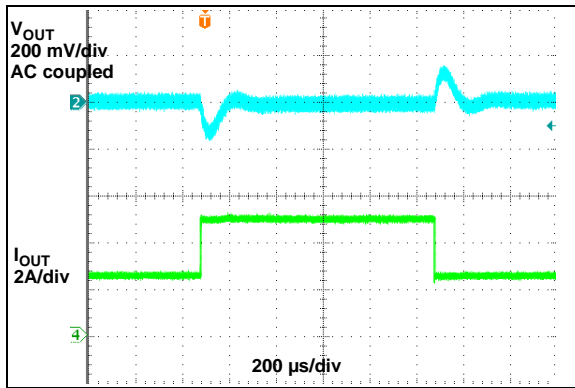


FIGURE 2-43: Load Transient Response ($I_{OUT} = 2.5A$ to $5A$).

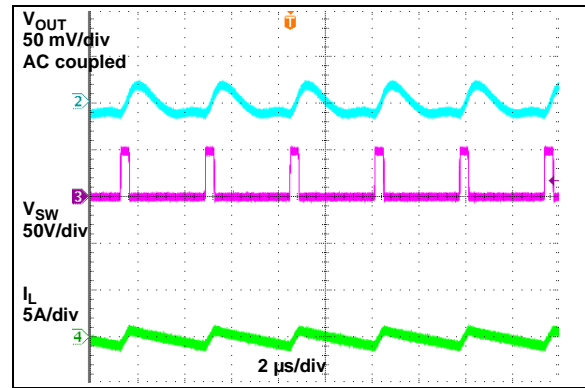


FIGURE 2-46: Switching Waveform at No Load.

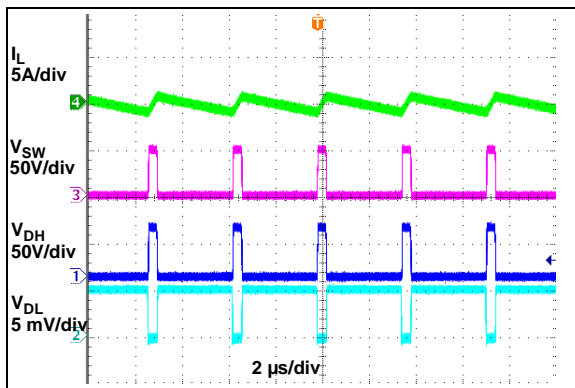


FIGURE 2-44: Switching Waveform at No Load.

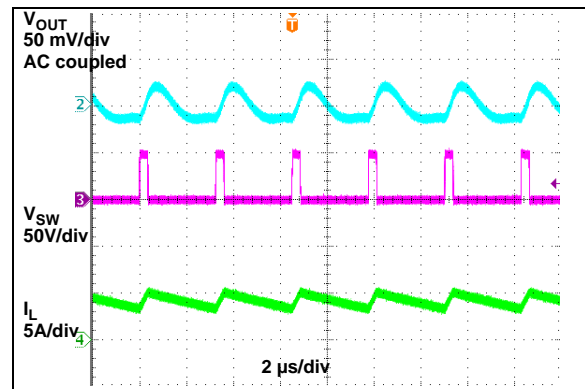


FIGURE 2-47: Switching Waveform at Full Load.

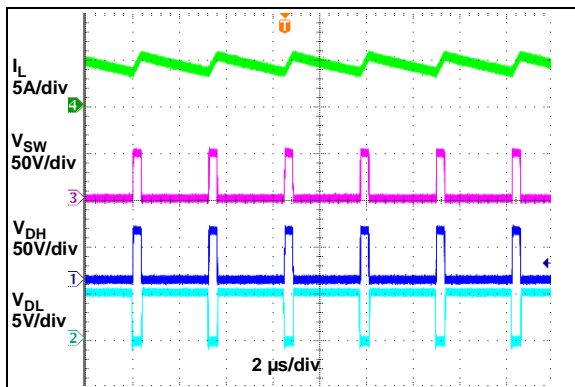


FIGURE 2-45: Switching Waveform at Full Load.

MIC2128

3.0 PIN DESCRIPTION

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

MIC2128	Symbol	Pin Function
1	PG	Open-drain Power Good Output pin
2	I_{LIM}	Current Limit setting resistor connection pin
3	SW	Switch Pin and Current Sense Input for negative current limit
4	BST	Bootstrap Capacitor Connection Pin
5	DH	High-side N-MOSFET gate driver Output
6	P_{GND}	Power Ground
7	DL	Low-side N-MOSFET gate driver output.
8	P_{VDD}	Internal high voltage LDO Output of the MIC2128
9	EXTVDD	Supply to the internal low voltage LDO
10	EN	Enable Input
11	FREQ	Switching Frequency Programming Input
12	SS	Soft-Start time setting capacitor connection pin
13	FB	Feedback Input
14	A_{GND}	Analog ground
15	V_{DD}	Supply for the MIC2128 internal analog circuits
16	V_{IN}	Supply Input for the internal high voltage LDO
17	EP	Exposed Pad

3.1 Power Good Output Pin (PG)

Connect PG to V_{DD} through a pull up resistor. PG is low when the FB voltage is 10% below the 0.6V reference voltage.

3.2 Current Limit Pin (I_{LIM})

Connect a resistor from I_{LIM} to SW to set current limit. Refer to [Section 4.3 “Current Limit \(ILIM\)”](#) for more details.

3.3 Switch Pin (SW)

SW pin provides return path for the high-side N-MOSFET gate driver when DH is low and is also used to sense low-side MOSFET current by monitoring the SW node voltage for negative current limit function.

Connect SW to the pin where high-side MOSFET source and the low-side MOSFET drain terminal are connected together.

3.4 Bootstrap Capacitor Pin (BST)

BST capacitor acts as supply for the high-side N-MOSFET driver. Connect a minimum of 0.1 μ F low ESR ceramic capacitor between BST and SW. Refer to [Section 4.5 “High-Side MOSFET Gate Drive \(DH\)”](#) section for more details.

3.5 High-Side N-MOSFET Gate Driver Output Pin (DH)

High-side N-MOSFET gate driver Output. Connect DH to the gate of external high-side N-MOSFET.

3.6 Power Ground Pin (P_{GND})

P_{GND} provides return path for the internal low-side N-MOSFET gate driver output and also acts as reference for current limit comparator. Connect P_{GND} to the external low-side N-MOSFET source terminal and to the return terminal of P_{VDD} bypass capacitor.

3.7 Low-Side N-MOSFET Gate Driver Output Pin (DL)

Low-side N-MOSFET gate driver output. Connect to the gate terminal of the external low-side N-MOSFET.

3.8 Internal High Voltage LDO Output Pin (P_{VDD})

Internal high voltage LDO Output of the MIC2128. P_{VDD} is the supply for the low-side MOSFET driver and for floating high-side MOSFET driver. Connect a minimum of 4.7 μ F low ESR ceramic capacitor from P_{VDD} to P_{GND} .

3.9 EXTVDD

Supply to the internal low voltage LDO. Connect EXTVDD to the output of the Buck converter if it is between 4.7V to 14V to improve system efficiency. Bypass EXTVDD with a minimum of 1 μ F low ESR ceramic capacitor.

3.10 Enable Input Pin (EN)

EN is a logic input. Connect to logic high to enable the converter and connect to logic low to disable the converter.

3.11 Switching Frequency Programming Input Pin (FREQ)

Switching Frequency Programming Input. Connect to mid-point of the resistor divider formed between V_{IN} and A_{GND} to set switching frequency of the converter. Tie FREQ to V_{IN} to set the switching frequency to 800 kHz. Refer to [Section 5.1 “Setting the Switching Frequency”](#) for more details.

3.12 Soft-Start Time Setting Capacitor Connection Pin (SS)

Soft-Start time setting capacitor connection pin. Connect a ceramic capacitor from SS to A_{GND} to set the output Soft-Start time. Refer to [Section 5.3 “Setting the Soft-Start Time”](#) section for further details.

3.13 Feedback Input Pin (FB)

FB is input to the transconductance amplifier of the control loop. The control loop regulates the FB voltage to 0.6V. Connect FB node to mid-point of the resistor divider between output and A_{GND} .

3.14 Analog Ground Pin (A_{GND})

A_{GND} is reference to the analog control circuits inside the MIC2128. Connect A_{GND} to P_{GND} at one point on PCB.

3.15 Bias Voltage Pin (V_{DD})

Supply for the MIC2128 internal analog circuits. Connect V_{DD} to P_{VDD} of the MIC2128 through a low pass filter. Connect a minimum of 4.7 μ F low ESR ceramic capacitor from V_{DD} to A_{GND} for decoupling.

3.16 Input Voltage Pin (V_{IN})

Supply Input to the internal high voltage LDO. Connect to the main power source and bypass to P_{GND} with a minimum of 0.1 μ F low ESR ceramic capacitor.

3.17 Exposed Pad (EP)

Connect to A_{GND} copper plane to improve thermal performance of the MIC2128.

MIC2128

4.0 FUNCTIONAL DESCRIPTION

The MIC2128 is an adaptive on-time synchronous buck controller designed to cover a wide range of input voltage applications ranging from 4.5V to 75V. An adaptive on-time control scheme is employed to get fast transient response and to obtain high voltage conversion ratios at constant switching frequency. Overcurrent protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$ which eliminates lossy current sense resistor. The device features external soft-start, enable input, UVLO, power good output (PG), secondary bootstrap LDO and thermal shutdown.

4.1 Theory of Operation

The MIC2128 is an adaptive on-time synchronous buck controller which operates based on ripple at feedback node. The output voltage is sensed by the MIC2128 feedback pin (FB) and is compared to a 0.6V reference voltage (V_{REF}) at the low-gain transconductance error amplifier (gm) as shown in the [Functional Block Diagram](#). [Figure 4-1](#) shows the MIC2128 control loop timing during steady-state operation.

The error amplifier behaves as short circuit for the ripple voltage frequency on the FB pin which causes the error amplifier output voltage ripple to follow the feedback voltage ripple. When the transconductance error amplifier output (V_{gm}) is below the reference voltage of the comparator, which is same as the error amplifier reference (V_{REF}), the comparator triggers and generates an on-time event. The on-time period is predetermined by the fixed t_{ON} estimator circuitry which is given by the following [Equation 4-1](#):

EQUATION 4-1:

$$t_{ON(ESTIMATED)} = \frac{V_{OUT}}{V_{VIN} \times f_{SW}}$$

Where:
 V_{OUT} = Output voltage
 V_{VIN} = Power stage input voltage
 f_{SW} = Switching frequency

At the end of the ON time, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF time of the high-side MOSFET depends on the feedback voltage. When the feedback voltage decreases, the output of the gm amplifier (V_{gm}) also decreases. When the output of the gm amplifier (V_{gm}) is below the reference voltage of the comparator (which is same as the error amplifier reference (V_{REF})) the OFF time ends and ON time is triggered. If the OFF time determined by the feedback voltage is less than the minimum OFF time ($t_{OFF(MIN)}$) of the MIC2128, which is about 230 ns (typical), the MIC2128 control logic applies the $t_{OFF(MIN)}$ instead.

The maximum duty cycle can be calculated using the following [Equation 4-2](#):

EQUATION 4-2:

$$D_{MAX} = \frac{t_{SW} - t_{OFF(MIN)}}{t_{SW}} = 1 - \frac{230ns}{t_{SW}}$$

Where:
 t_{SW} = Switching period, equal to $1/f_{SW}$

It is not recommended to use the MIC2128 with an OFF time close to $t_{OFF(MIN)}$ during steady-state operation.

The adaptive on-time control scheme results in a constant switching frequency over wide range of input voltage and load current. The actual ON time and resulting switching frequency varies with the different rising and falling times of the external MOSFETs. The minimum controllable ON time ($t_{ON(MIN)}$) results in a lower switching frequency than the target switching frequency in high V_{IN} to V_{OUT} ratio applications.

The equation below shows the output-to-input voltage ratio, below which the MIC2128 lowers the switching frequency in order to regulate the output-to-set value.

EQUATION 4-3:

$$\frac{V_{OUT}}{V_{IN}} = t_{ON(MIN)} \times f_{SW}$$

Where:
 V_{OUT} = Output voltage
 V_{IN} = Input voltage
 f_{SW} = Switching frequency
 $t_{ON(MIN)}$ = Minimum controllable ON time (80 ns typ.)

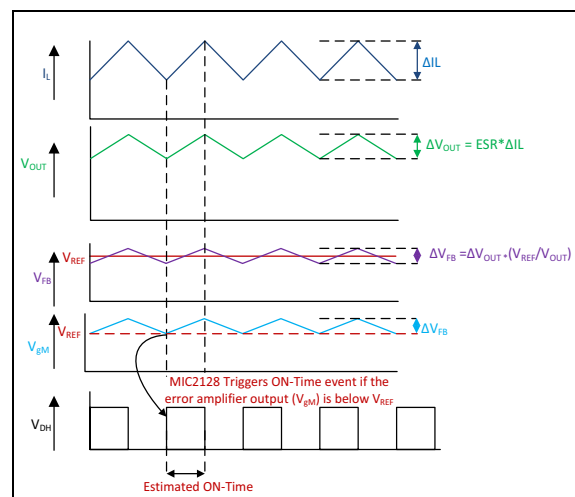


FIGURE 4-1: MIC2128 Control Loop Timing.

Figure 4-2 shows operation of the MIC2128 during load transient. The output voltage drops due to a sudden increase in load, which results in the error amplifier output (V_{GM}) falling below V_{REF} . This causes the comparator to trigger an on-time event. At the end of the ON time, a minimum OFF time $t_{OFF(MIN)}$ is generated to charge the bootstrap capacitor. The next ON time is triggered immediately after the $t_{OFF(MIN)}$ if the error amplifier output voltage (V_{GM}) is still below V_{REF} due to the low feedback voltage. This operation results in higher switching frequency during load transients. The switching frequency returns to the nominal set frequency once the output stabilizes at new load current level. The output recovery time is fast and the output voltage deviation is small in the MIC2128 converter due to the varying duty cycle and switching frequency.

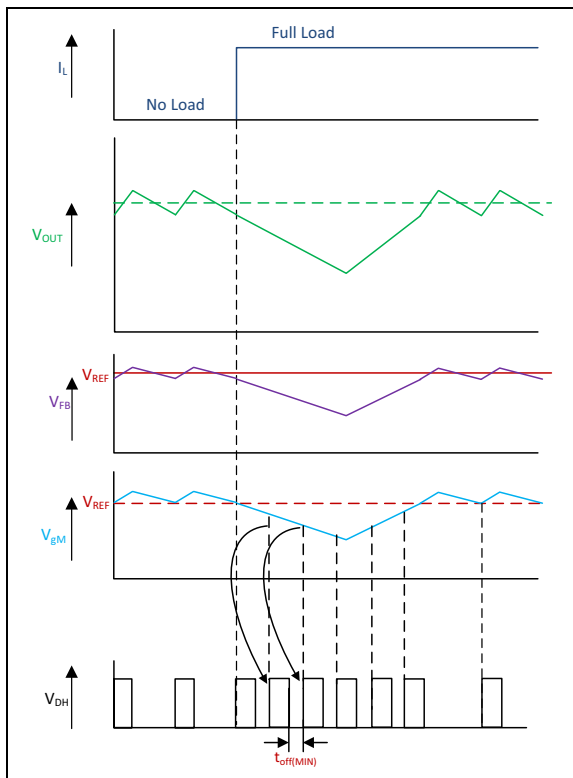


FIGURE 4-2: MIC2128 Load Transient Response.

Unlike true current-mode control, the MIC2128 uses the output voltage ripple to trigger an on-time event. In order to meet the stability requirements, the MIC2128 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the internal error amplifier. The recommended feedback voltage ripple is 20 mV~100 mV over the full input voltage range. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the internal error amplifier. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor

current ripple if the ESR of the output capacitor is very low. For these applications, ripple injection is required to ensure proper operation. Refer to [Section 5.8 “Ripple Injection”](#) for details about the ripple injection technique.

4.2 Soft Start (SS)

Soft Start reduces the power supply inrush current at start-up by controlling the output voltage rise time. The MIC2128 features SS pin which allows the user to set the soft-start time by connecting a capacitor from the SS pin to A_{GND} . An internal current source of 1.3 μA charges this capacitor and generates a linear voltage which is used as the reference for the internal error amplifier during Soft Start. Once the voltage on this SS capacitor is above the internal fixed reference of 0.6V, the error amplifier uses the fixed 0.6V as reference instead of the voltage on the external SS capacitor.

4.3 Current Limit (I_{LIM})

The MIC2128 uses the low-side MOSFET $R_{DS(ON)}$ to sense inductor current. In each switching cycle of the MIC2128 converter, the inductor current is sensed by monitoring the voltage across the low-side MOSFET during the OFF period of the switching cycle during which low-side MOSFET is ON. An internal current source of 96 μA generates a voltage across the external current limit setting resistor R_{CL} as show in the [Figure 4-3](#).

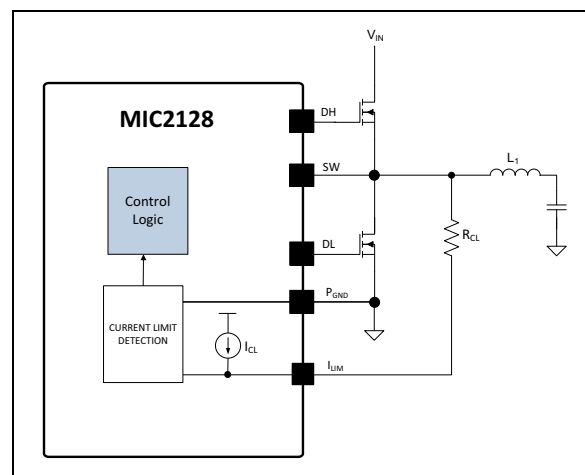


FIGURE 4-3: MIC2128 Current Limiting Circuit.

The I_{LIM} pin voltage (V_{ILIM}) is the difference of the voltage across the low-side MOSFET and the voltage across the resistor (V_{CL}). The sensed voltage V_{ILIM} is compared with the power ground (P_{GND}) after a blanking time of 150 ns.

If the absolute value of the voltage drop across the low-side MOSFET is greater than the absolute value of the voltage across the current setting resistor (V_{CL}), the MIC2128 triggers the current limit event. Consecutive

MIC2128

eight current limit events trigger the hiccup mode. Once the controller enters into hiccup mode, it initiates a soft-start sequence after a hiccup timeout of 4 ms (typical). Both the high-side and low-side MOSFETs are turned off during hiccup timeout. The hiccup sequence including the soft start reduces the stress on the switching FETs and protects the load and supply from severe short conditions.

The current limit can be programmed by using the following [Equation 4-4](#).

EQUATION 4-4:

$$R_{CL} = \frac{\left(I_{CLIM} + \frac{\Delta I_{LPP}}{2}\right) \times R_{DS(ON)} + V_{OFFSET}}{I_{CL}}$$

Where:

I_{LIM}	= Load current limit
$R_{DS(ON)}$	= On-resistance of low-side power MOSFET
ΔI_{LPP}	= Inductor peak-to-peak ripple current
V_{OFFSET}	= Current-limit comparator offset (15 mV max.)
I_{CL}	= Current-limit source current (96 μ A typ)

Since MOSFET $R_{DS(ON)}$ varies from 30% to 40% with temperature, it is recommended to consider the $R_{DS(ON)}$ variation while calculating R_{CL} in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

To improve the current limit variation, the MIC2128 adjusts the internal current limit source current (I_{CL}) at a rate of 0.3 μ A/ $^{\circ}$ C when the MIC2128 junction temperature changes to compensate the $R_{DS(ON)}$ variation of external low-side MOSFET. The effectiveness of this method depends on the thermal gradient between the MIC2128 and the external low-side MOSFET. The lower the thermal gradient, the better the current limit variation.

A small capacitor (C_{CL}) can be connected from the I_{LIM} pin to PGND to filter the switch node ringing during the Off-time allowing a better current sensing. The time constant of R_{CL} and C_{CL} should be less than the minimum off time.

4.4 Negative Current Limit

The MIC2128 implements negative current limit by sensing the SW voltage when the low-side FET is ON. If the SW node voltage exceeds 48 mV typical, the device turns off the low-side FET for 500 ns. Negative current limit value is shown in [Equation 4-5](#).

EQUATION 4-5:

$$I_{NLIM} = \frac{48mV}{R_{DS(ON)}}$$

Where:

I_{NLIM}	= Negative current limit
$R_{DS(ON)}$	= On-resistance of low-side power MOSFET

4.5 High-Side MOSFET Gate Drive (DH)

The MIC2128's high-side drive circuit is designed to switch an N-Channel external MOSFET. The MIC2128 Functional Block diagram shows a bootstrap diode between PVDD and BST pins. This circuit supplies energy to the high-side drive circuit. A low ESR ceramic capacitor should be connected between BST and SW pins (refer Typical Application Circuit). The capacitor between BST and SW pins, C_{BST} , is charged while the low-side MOSFET is on. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. A minimum of 0.1 μ F low ESR ceramic capacitor is recommended between BST and SW pins. The required value of C_{BS} can be calculated using the following [Equation 4-6](#).

EQUATION 4-6:

$$C_{BST} = \frac{Q_{G_HS}}{\Delta V_{BST}}$$

Where:

Q_{G_HS}	= High-side MOSFET total gate charge
ΔV_{BST}	= Drop across the CBST, generally 50 mV to 100 mV

A small resistor in series with CBST, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

4.6 Low-Side MOSFET Gate Drive (DL)

The MIC2128's low-side drive circuit is designed to switch an N-Channel external MOSFET. The internal low-side MOSFET driver is powered by PVDD. Connect a minimum of 4.7 μ F low-ESR ceramic capacitor to supply the transient gate current of the external MOSFET.

4.7 Auxiliary Bootstrap LDO (EXTVDD)

The MIC2128 features an auxiliary bootstrap LDO which improves the system efficiency by supplying the MIC2128 internal circuit bias power and gate drivers from the converter output voltage. This LDO is enabled when the voltage on the EXTVDD pin is above 4.6V (typical) and at the same time the main LDO which operates from V_{IN} is disabled to reduce power consumption.

5.0 APPLICATIONS INFORMATION

5.1 Setting the Switching Frequency

The MIC2128 is an adjustable-frequency, synchronous buck controller featuring a unique adaptive on-time control architecture. The switching frequency can be adjusted between 270 kHz and 800 kHz by changing the resistor divider network between V_{IN} and A_{GND} pins consisting of R_1 and R_2 as shown in [Figure 5-1](#).

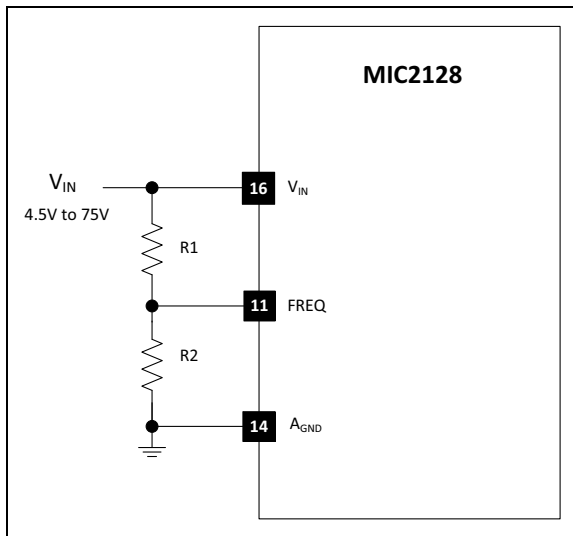


FIGURE 5-1: Switching Frequency Adjustment.

[Equation 5-1](#) shows the estimated switching frequency:

EQUATION 5-1:

$$f_{SW_ADJ} = f_O \times \frac{R_2}{R_1 + R_2}$$

f_O is the switching frequency when R_1 is 100 k Ω and R_2 being open; f_O is typically 800 kHz. For more precise setting, it is recommended to use [Figure 5-2](#):

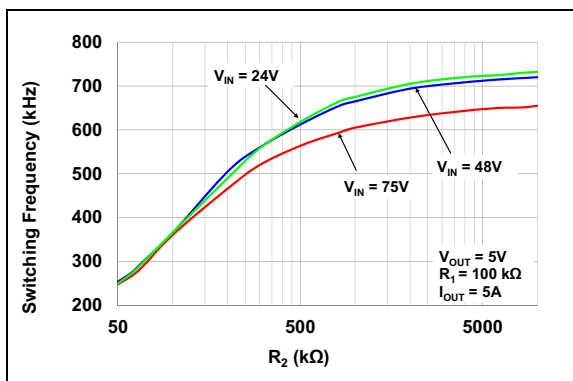


FIGURE 5-2: Switching Frequency vs. R_2 .

5.2 Output Voltage Setting

The output voltage can be adjusted using a resistor divider from output to A_{GND} whose mid-point is connected to FB pin as shown the [Figure 5-3](#).

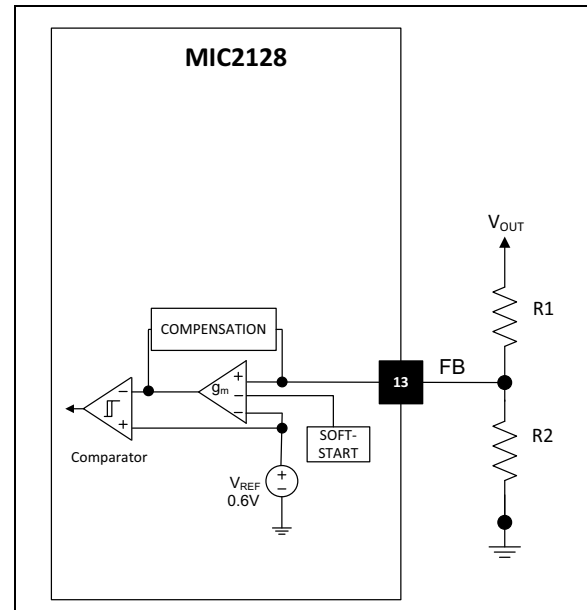


FIGURE 5-3: Output Voltage Adjustment.

The output voltage can be calculated using [Equation 5-2](#):

EQUATION 5-2:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where:
 $V_{REF} = 0.6V$

The maximum output voltage that can be programmed using the MIC2128 is limited to 30V, if not limited by the maximum duty cycle (see [Equation 4-2](#)).

A typical value of R_1 is less than 30 k Ω . If R_1 is too large, it may allow noise to be introduced into the voltage feedback loop and also increases the offset between the set output voltage and actual output voltage because of the error amplifier bias current. If R_1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_1 is selected, R_2 can be calculated using [Equation 5-3](#).

EQUATION 5-3:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{REF}} - 1}$$

MIC2128

5.3 Setting the Soft-Start Time

The output Soft-Start time can be set by connecting a capacitor from SS to A_{GND} from 2 ms to 100 ms as shown in [Figure 5-4](#).

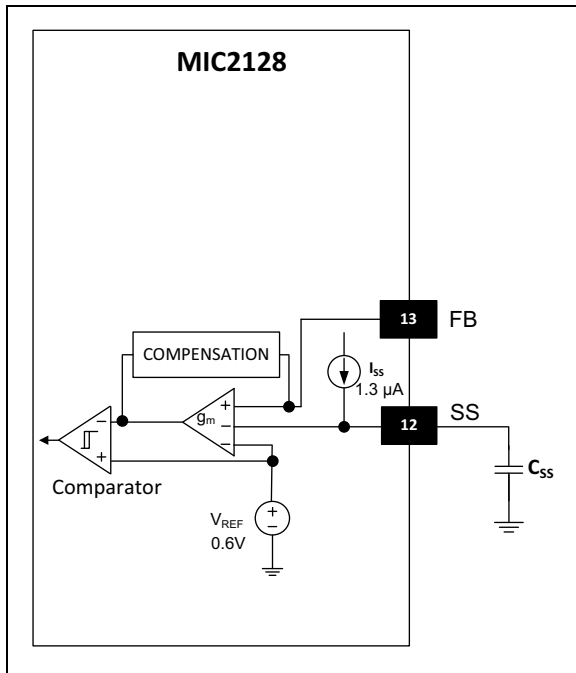


FIGURE 5-4: Setting the Soft-Start Time.

The value of the capacitor can be calculated using [Equation 5-4](#).

EQUATION 5-4:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}$$

Where:

- C_{SS} = Capacitor from SS pin to A_{GND}
- I_{SS} = Internal Soft-Start current (1.3 µA typical)
- t_{SS} = Output Soft-Start time
- V_{REF} = 0.6V

5.4 MOSFET Selection

Important parameters for MOSFET selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage rating for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{IN}. A safety factor of 30% should be added to the V_{IN(MAX)} while selecting the voltage rating of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

5.4.1 HIGH-SIDE MOSFET POWER LOSSES

The total power loss in the high-side MOSFET (P_{H_{SFET}}) is the sum of the power losses because of conduction (P_{CONDUCTION}), switching (P_{SW}), reverse recovery charge of low-side MOSFET body diode (P_{Q_{rr}}) and MOSFET's output capacitance discharge as calculated in the [Equation 5-5](#).

EQUATION 5-5:

$$P_{HSFET} = P_{CONDUCTION(HS)} + P_{SW(HS)} + P_{Qrr} + P_{COSS}$$

$$P_{CONDUCTION(HS)} = (I_{RMS(HS)})^2 \times R_{DS(ON_HS)}$$

$$P_{SW(HS)} = 0.5 \times V_{IN} \times I_{LOAD} \times (t_R + t_F) \times f_{SW}$$

$$P_{Qrr} = V_{IN} \times Q_{rr} \times f_{SW}$$

$$P_{COSS} = \frac{1}{2} \times (C_{OSS(HS)} + C_{OSS(LS)}) \times (V_{IN})^2 \times f_{SW}$$

Where:

- R_{DS(ON_HS)} = On-resistance of the high-side MOSFET
- V_{IN} = Operating input voltage
- I_{LOAD} = Load current
- f_{SW} = Operating switching frequency
- Q_{rr} = Reverse recovery charge of low-side MOSFET body diode or of external diode across low-side MOSFET
- C_{OSS(HS)} = Effective high-side MOSFET output capacitance
- C_{OSS(LS)} = Effective low-side MOSFET output capacitance
- I_{RMS(HS)} = RMS current of the high-side MOSFET which can be calculated using [Equation 5-6](#).
- t_R, t_F = The high-side MOSFET turn-on and turn-off transition times which can be approximated by [Equation 5-8](#) and [Equation 5-9](#)

EQUATION 5-6:

$$I_{RMS(HS)} = I_{LOAD} \times \sqrt{D}$$

I_{LOAD} is the load current and D is the operating duty cycle, given by [Equation 5-7](#).

EQUATION 5-7:

$$D = \frac{V_{OUT}}{V_{IN}}$$

EQUATION 5-8:

$$t_R = \frac{Q_{SW(HS)} \times [R_{DH(PULL_UP)} + R_{HS(GATE)}]}{V_{DD} - V_{TH}}$$

EQUATION 5-9:

$$t_F = \frac{Q_{SW(HS)} \times [R_{DH(PULL_DOWN)} + R_{HS(GATE)}]}{V_{TH}}$$

Where:

- $R_{DH(PULL_UP)}$ = High-side gate driver pull-up resistance
- $R_{DH(PULL_DOWN)}$ = High-side gate driver pull-down resistance
- $R_{HS(GATE)}$ = High-side MOSFET gate resistance
- V_{TH} = Gate threshold voltage of the high-side MOSFET
- $Q_{SW(HS)}$ = Switching gate charge of the high-side MOSFET which can be approximated by [Equation 5-10](#).

EQUATION 5-10:

$$Q_{SW(HS)} = \frac{Q_{GS(HS)}}{2} + Q_{GD(HS)}$$

Where:

- $Q_{GS(HS)}$ = High-side MOSFET gate to source charge
- $Q_{GD(HS)}$ = High-side MOSFET gate to drain charge

5.4.2 LOW-SIDE MOSFET POWER LOSSES

The total power loss in the low-side MOSFET (P_{LSFET}) is the sum of the power losses because of conduction ($P_{CONDUCTION(LS)}$) and body diode conduction during the dead time (P_{DT}) as calculated in [Equation 5-11](#).

EQUATION 5-11:

$$P_{LSFET} = P_{CONDUCTION(LS)} + P_{DT}$$

$$P_{CONDUCTION(LS)} = (I_{RMS(LS)})^2 \times R_{DS(ON_LS)}$$

$$P_{DT} = 2 \times V_F \times I_{LOAD} \times t_{DT} \times f_{SW}$$

Where:

- $R_{DS(ON_LS)}$ = On-resistance of the low-side MOSFET
- V_F = Low-side MOSFET body diode forward voltage drop
- t_{DT} = Dead time which is approximately 20 ns
- f_{SW} = Switching Frequency
- $I_{RMS(LS)}$ = RMS current of the low-side MOSFET which can be calculated using [Equation 5-12](#)

EQUATION 5-12:

$$I_{RMS(LS)} = I_{LOAD} \times \sqrt{1-D}$$

I_{LOAD} is the load current and D is the operating duty cycle.

5.5 Inductor Selection

Inductance value, saturation and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current.

The lower the inductance value, the higher the peak-to-peak ripple current through the inductor, which increases the core losses in the inductor. Higher inductor ripple current also requires more output capacitance to smooth out the ripple current. The greater the inductance value, the lower the peak-to-peak ripple current, which results in a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 30% of the maximum output current.

The inductance value is calculated by [Equation 5-13](#):

EQUATION 5-13:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times 0.3 \times I_{FL}}$$

Where:

- V_{IN} = Input voltage
- f_{SW} = Switching frequency
- I_{FL} = Full load current
- V_{OUT} = Output voltage

For a selected Inductor, the peak-to-peak inductor ripple current can be calculated using [Equation 5-14](#).

EQUATION 5-14:

$$\Delta I_{L_PP} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The peak inductor current is equal to the load current plus one half of the peak-to-peak inductor current ripple which is shown in [Equation 5-15](#).

EQUATION 5-15:

$$I_{L_PK} = I_{LOAD} + \frac{\Delta I_{L_PP}}{2}$$

MIC2128

The RMS and saturation current ratings of the selected inductor should be at least equal to the RMS current and saturation current calculated in the [Equation 5-16](#) and [Equation 5-17](#).

EQUATION 5-16:

$$I_{L_RMS} = \sqrt{(I_{LOAD(MAX)})^2 + \frac{(\Delta I_{L_PP})^2}{12}}$$

Where:

$I_{LOAD(MAX)}$ = Maximum load current

EQUATION 5-17:

$$I_{L_SAT} = \frac{R_{CL} \times I_{CL} + 15mV}{R_{DS(ON)}}$$

Where:

R_{CL} = Current limit resistor

I_{CL} = Current-Limit Source Current (96 μ A typical)

$R_{DS(ON)}$ = On-resistance of low-side power MOSFET

Maximizing the efficiency requires the proper selection of core material and minimizing the winding resistance. Use of ferrite materials is recommended in the higher switching frequency applications. Lower cost iron powder cores may be used but the increase in core loss reduces the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetic's vendor.

The amount of copper loss in the inductor is calculated by [Equation 5-18](#).

EQUATION 5-18:

$$P_{INDUCTOR(CU)} = (I_{L_RMS})^2 \times R_{DCR}$$

5.6 Output Capacitor Selection

The main parameters for selecting the output capacitor are capacitance value, voltage rating and RMS current rating. The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Recommended capacitor types are ceramic, tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR can be calculated using [Equation 5-19](#).

EQUATION 5-19:

$$ESR \leq \frac{\Delta V_{OUT_PP}}{\Delta I_{L_PP}}$$

Where:

ΔV_{OUT_PP} = Peak-to-peak output voltage ripple

ΔI_{L_PP} = Peak-to-peak inductor current ripple

The required output capacitance to meet steady state output ripple can be calculated using [Equation 5-20](#).

EQUATION 5-20:

$$C_{OUT} = \frac{\Delta I_{L_PP}}{8 \times f_{SW} \times \Delta V_{OUT_PP}}$$

Where:

C_{OUT} = Output capacitance value

f_{SW} = Switching frequency

As described in [Section 4.1 "Theory of Operation"](#), the MIC2128 requires at least 20 mV peak-to-peak ripple at the FB pin to ensure that the gm amplifier and the comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection circuit should be used to provide the enough feedback-voltage ripple. Refer to the [Section 5.8 "Ripple Injection"](#) for details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic, ceramic or OS-CON. The output capacitor RMS current is calculated in [Equation 5-21](#).

EQUATION 5-21:

$$I_{C_OUT(RMS)} = \frac{\Delta I_{L_PP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is shown in [Equation 5-22](#).

EQUATION 5-22:

$$P_{DIS(C_OUT)} = (I_{C_OUT(RMS)})^2 \times ESR_{C_OUT}$$

5.7 Input Capacitor Selection

The input capacitor reduces peak current drawn from the power supply and reduces noise and voltage ripple on the input. The input voltage ripple depends on the input capacitance and ESR. The input capacitance and ESR values can be calculated using [Equation 5-23](#).

EQUATION 5-23:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN_C}}$$

$$ESR_{C_IN} = \frac{\Delta V_{IN_ESR}}{I_{L_PK}}$$

Where:

I_{LOAD}	= Load Current
I_{L_PK}	= Peak Inductor Current
ΔV_{INC}	= Input ripple due to capacitance
ΔV_{INESR}	= Input ripple due to input capacitor ESR
η	= Power conversion efficiency

The input capacitor should be rated for ripple current rating and voltage rating. The RMS value of input capacitor current is determined at the maximum output current. The RMS current rating of the input capacitor should be greater than or equal to the input capacitor RMS current calculated using the [Equation 5-24](#).

EQUATION 5-24:

$$I_{C_IN(RMS)} = I_{LOAD(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is calculated using [Equation 5-25](#).

EQUATION 5-25:

$$P_{DISS(C_IN)} = (I_{C_IN(RMS)})^2 \times ESR_{C_IN}$$

5.8 Ripple Injection

The minimum recommended ripple at the FB pin for proper operation of the MIC2128 error amplifier and comparator is 20 mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For low output voltages, such as a 1V, the output voltage ripple is only 10 mV to 20 mV, and the feedback voltage ripple is less than 20 mV. If the feedback voltage ripple is so small that the gm amplifier and comparator cannot sense it, then the MIC2128 loses control and the output voltage is not regulated. In order to have sufficient V_{FB} ripple, ripple injection method should be applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback due to the large ESR of the output capacitor ([Figure 5-5](#)). The converter is stable without any additional ripple injection at the FB node. The feedback voltage ripple is given by [Equation 5-26](#).

EQUATION 5-26:

$$\Delta V_{FB(PP)} = \frac{R_2}{R_2 + R_1} \times ESR \times \Delta I_{L_PP}$$

ΔI_{L_PP} is the peak-to-peak value of the inductor current ripple.

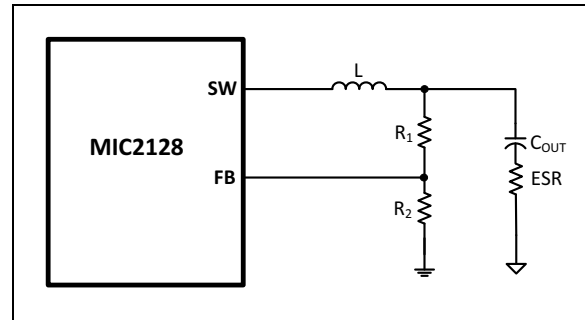


FIGURE 5-5: Enough Ripple at FB.

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitor.

The output voltage ripple can be fed into the FB pin through a feed forward capacitor, C_{FF} in this case, as shown in [Figure 5-6](#). The typical C_{FF} value is between 1 nF and 100 nF. With the feed forward capacitor, the feedback voltage ripple is very close to the output voltage ripple which is shown in [Equation 5-27](#).

EQUATION 5-27:

$$\Delta V_{FB(PP)} = ESR \times \Delta I_{L_PP}$$

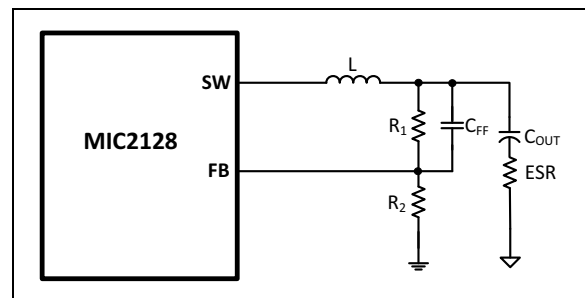


FIGURE 5-6: Inadequate Ripple at FB.

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors:

In this case, additional ripple can be injected into the FB pin from the switching node SW via a resistor R_{INJ} and a capacitor C_{INJ} , as shown in [Figure 5-7](#).

MIC2128

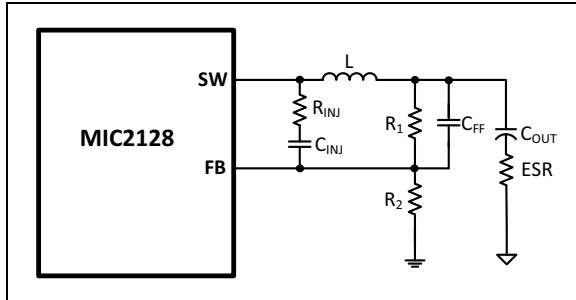


FIGURE 5-7: Invisible Ripple at FB.

The injected ripple at the FB pin in this case is given by the [Equation 5-28](#):

EQUATION 5-28:

$$\Delta V_{FB(PP)} = \frac{V_{OUT} \times (1 - D)}{C_{FF} \times R_{INJ} \times f_{SW}}$$

In the above [Equation 5-28](#), it is assumed that the time constant associated with the C_{FF} meets the criteria shown in [Equation 5-29](#).

EQUATION 5-29:

$$\tau \geq T_{SW}$$

$$\tau \geq C_{FF} \times (R_1 \parallel R_2 \parallel R_{INJ})$$

The process of sizing the ripple injection resistor and capacitors is:

1. Select C_{INJ} in the range of 47 nF to 100 nF, which can be considered as short for a wide range of the frequencies.
2. Select C_{FF} in the range of 0.47 nF to 10 nF, if R_1 and R_2 are in $k\Omega$ range.
3. Select R_{INJ} according to [Equation 5-30](#).

EQUATION 5-30:

$$R_{INJ} = \frac{V_{OUT} \times (1 - D)}{C_{FF} \times f_{SW} \times \Delta V_{FB(PP)}}$$

Where:

- V_{OUT} = Output voltage
- D = Duty cycle
- f_{SW} = Switching frequency
- $\Delta V_{FB(PP)}$ = Feedback Ripple

Once all the ripple injection component values are calculated, ensure that the criteria shown in the [Equation 5-29](#) is met.

5.9 Power Dissipation in MIC2128

The MIC2128 features two Low Dropout Regulators (LDOs) to supply power at the P_{VDD} pin from either V_{IN} or $EXTVDD$ depending on the voltage at the $EXTVDD$ pin. P_{VDD} powers MOSFET drivers and V_{DD} pin, which is recommended to connect to P_{VDD} through a low pass filter, powers the internal circuitry. In the applications where the output voltage is 5V and above (up to 14V), it is recommended to connect $EXTVDD$ to the output to reduce the power dissipation in the MIC2128, to reduce the MIC2128 junction temperature and to improve the system efficiency.

The power dissipation in the MIC2128 depends on the internal LDO being in use, gate charge of the external MOSFETs and switching frequency. The power dissipation and the junction temperature of the MIC2128 can be estimated using the [Equation 5-31](#), [Equation 5-32](#) and [Equation 5-33](#).

Power dissipation in the MIC2128 when $EXTVDD$ is not used:

EQUATION 5-31:

$$P_{IC} = V_{IN} \times (I_{SW} + I_Q)$$

Power dissipation in the MIC2128 when $EXTVDD$ is used:

EQUATION 5-32:

$$P_{IC} = V_{EXTVDD} \times (I_{SW} + I_Q)$$

$$I_{SW} = Q_G \times f_{SW}$$

$$Q_G = Q_{G_HS} + Q_{G_LS}$$

Where:

- I_{SW} = Switching current into the V_{IN} pin
- I_Q = Quiescent current (1.4 mA typ)
- Q_G = Total gate charge of the external MOSFETs which is sum of the gate charge of high-side MOSFET (Q_{G_HS}) and the low-side MOSFET (Q_{G_LS}) at 5V gate to source voltage. Gate charge information can be obtained from the MOSFETs datasheet.
- V_{EXTVDD} = Voltage at the $EXTVDD$ pin ($4.6 \leq V_{EXTVDD} \leq 14$ V typ.)

The junction temperature of the MIC2128 can be estimated using [Equation 5-33](#).

EQUATION 5-33:

$$T_J = (P_{IC} \times \theta_{JA}) + T_A$$

Where:

T_J	=	Junction temperature
P_{IC}	=	Power dissipation
θ_{JA}	=	Junction Ambient Thermal resistance (50.8°C/W)

The maximum recommended operating junction temperature for the MIC2128 is 125°C.

Using the output voltage of the same switching regulator, when it is in between 4.6V (typ.) to 14V, as the voltage at the EXTVDD pin, significantly reduces the power dissipation inside the MIC2128. This reduces the junction temperature rise as illustrated below.

For the typical case of $V_{VIN} = 48V$, $V_{OUT} = 5V$, the maximum ambient temperature = 85°C and 10 mA of I_{SW} .

The condition where EXTVDD is not used is shown in [Equation 5-34](#):

EQUATION 5-34:

$$P_{IC} = 48V \times (10mA + 1.5mA)$$

$$P_{IC} = 0.552W$$

$$T_J = (0.552W \times 50.8 \text{ } ^\circ\text{C/W}) + 85 \text{ } ^\circ\text{C}$$

$$T_J = 113 \text{ } ^\circ\text{C}$$

When the 5V output is used as the input to the EXTVDD pin, the MIC2128 junction temperature reduces from 113°C to 88°C as calculated in [Equation 5-35](#):

EQUATION 5-35:

$$P_{IC} = 5V \times (10mA + 1.5mA)$$

$$P_{IC} = 0.058W$$

$$T_J = (0.058W \times 50.8 \text{ } ^\circ\text{C/W}) + 85 \text{ } ^\circ\text{C}$$

$$T_J = 88 \text{ } ^\circ\text{C}$$

MIC2128

6.0 PCB LAYOUT GUIDELINES

PCB layout is critical to achieve reliable, stable and efficient performance. The following guidelines should be followed to ensure proper operation of the MIC2128 converter.

6.1 IC

- The ceramic bypass capacitors, which are connected to the V_{DD} and P_{VDD} pins, must be located right at the IC. Use wide traces to connect to the V_{DD} , P_{VDD} and A_{GND} , P_{GND} pins respectively.
- The signal ground pin (A_{GND}) must be connected directly to the ground planes.
- Place the IC close to the point-of-load (POL).
- Signal and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- Place the input ceramic capacitors as close as possible to the MOSFETs.
- Place several vias to the ground plane close to the input capacitor ground terminal.

6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurately sense the voltage across the low-side MOSFET.

6.4 Output Capacitor

- Use a copper plane to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

6.5 MOSFETs

- MOSFET gate drive traces must be short and wide. The ground plane should be the connection between the MOSFET source and PGND.
- Choose a low-side MOSFET with a high CGS/CGD ratio and a low internal gate resistance to minimize the effect of dV/dt inducted turn-on.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET.

7.0 PACKAGING INFORMATION

7.1 Package Marking Information

16-Pin QFN (3 x 3 mm)

Example



Legend: XX...X Customer-specific information
 WW Week code (week of January 1 is week '01')
 NNN Alphanumeric traceability code
 (e3) Pb-free JEDEC designator for Matte Tin (Sn)
 * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.
 •, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

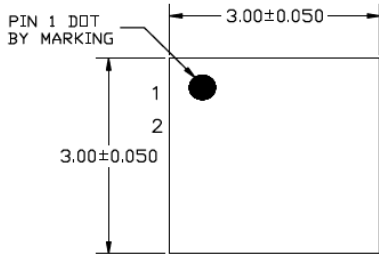
Underbar (_) symbol may not be to scale.

MIC2128

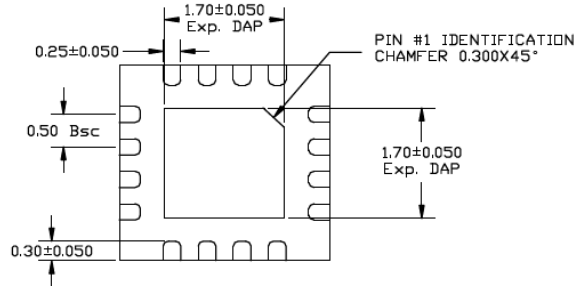
TITLE

16 LEAD QFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

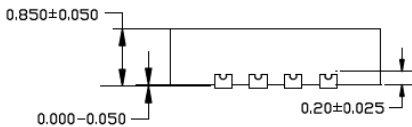
DRAWING #	QFN33-16LD-PL-3	UNIT	MM
Lead Frame	NiPdAu	Lead Finish	NiPdAu



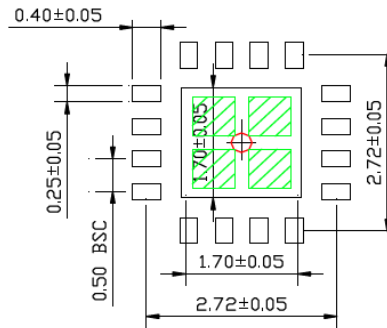
TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3



RECOMMENDED LAND PATTERN
NOTE: 4, 5

NOTE:

1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE.
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.60mm IN SIZE, 0.20mm SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision B (January 2017)

- Updated Product Identification System page.

Revision A (September 2016)

- Original release of this document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>XX</u>	<u>XX</u>
Device	Temperature	Package Code	Media Type
<p>Device: MIC2128: 75V, Synchronous Buck Controller Featuring Adaptive On-Time Control with External Soft Start</p> <p>Temperature: Y = Industrial Temperature Grade (-40°C to +125°C)</p> <p>Package: ML = 16 Lead, 3x3 mm VQFN</p> <p>Media Type: TR = 5000/reel T5 = 500/reel</p>			
<p>Examples:</p> <p>a) MIC2128YML-TR: 75V, Synchronous Buck Controller Featuring Adaptive On-Time Control with External Soft Start, -40°C to +125°C junction temperature range, 16-LD VQFN package, 5000/reel</p> <p>b) MIC2128YML-T5: 75V, Synchronous Buck Controller Featuring Adaptive On-Time Control with External Soft Start, -40°C to +125°C junction temperature range, 16-LD VQFN package, 500/reel</p>			

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

**QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
= ISO/TS 16949 =**

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELoQ, KEELoQ logo, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2017, Microchip Technology Incorporated, All Rights Reserved.
ISBN: 978-1-5224-1276-2



MICROCHIP

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://www.microchip.com/support>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-3326-8000
Fax: 86-21-3326-8021

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

France - Saint Cloud
Tel: 33-1-30-60-70-00

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anana
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7289-7561

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenberg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820