

NTB5404N, NTP5404N, NVB5404N

Power MOSFET

40 V, 167 A, Single N-Channel, D²PAK & TO-220

Features

- Low $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- AEC-Q101 Qualified and PPAP Capable – NVB5404N
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Units
Drain-to-Source Voltage			V _{DSS}	40	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current – R _{θJC}	Steady State	T _C = 25°C	I _D	167	A
		T _C = 100°C		118	
Power Dissipation – R _{θJC}	Steady State	T _C = 25°C	P _D	254	W
Continuous Drain Current – R _{θJA} (Note 1)	Steady State	T _A = 25°C	I _D	24	A
		T _A = 100°C		17	
Power Dissipation – R _{θJA} (Note 1)	Steady State	T _A = 25°C	P _D	5.4	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	670	A
Operating Junction and Storage Temperature			T _J , T _{STG}	–55 to 175	°C
Source Current (Body Diode) Pulsed			I _S	75	A
Single Pulse Drain-to Source Avalanche Energy – (V _{DD} = 50 V, V _{GS} = 10 V, I _{PK} = 45 A, L = 1 mH, R _G = 25 Ω)			EAS	1000	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	0.59	$^\circ\text{C/W}$
Junction-to-Ambient (Note 1)	$R_{\theta JA}$	50	$^\circ\text{C/W}$

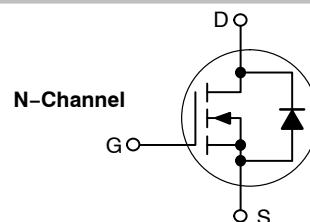
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



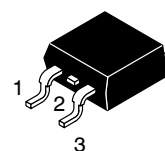
ON Semiconductor®

<http://onsemi.com>

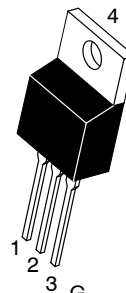
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$ (Note 1)
40 V	4.5 m Ω @ 10 V	167 A



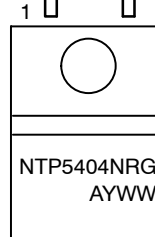
MARKING DIAGRAMS



**D²PAK
CASE 418B
STYLE 2**



**TO-220AB
CASE 221A
STYLE 5**



1 = Pb-Free Device
 A = Assembly Location
 Y = Year
 WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTB5404NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel
NTP5404NRG	TO-220 (Pb-Free)	50 Units / Rail
NVB5404NT4G	D ² PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTB5404N, NTP5404N, NVB5404N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			34		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		1.0	μA
			T _J = 100°C		10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±30 V			±100	nA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.5		3.5	V
Gate Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-8.2		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 40 A		3.5	4.5	mΩ
		V _{GS} = 5.0 V, I _D = 15 A		5.1	7.0	
Forward Transconductance	g _{FS}	V _{DS} = 10 V, I _D = 15 A		35		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 32 V		4300	7000	pF
Output Capacitance	C _{OSS}			1075	1700	
Reverse Transfer Capacitance	C _{RSS}			450	1000	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 32 V, I _D = 40 A		125		nC
Threshold Gate Charge	Q _{G(TH)}			5.5		
Gate-to-Source Charge	Q _{GS}			12.5		
Gate-to-Drain Charge	Q _{GD}			55		

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DD} = 32 V, I _D = 40 A, R _G = 2.5 Ω		10		ns
Rise Time	t _r			65		
Turn-Off Delay Time	t _{d(OFF)}			85		
Fall Time	t _f			85		

SWITCHING CHARACTERISTICS, V_{GS} = 5 V (Note 3)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 5 V, V _{DD} = 20 V, I _D = 20 A, R _G = 2.5 Ω		25		ns
Rise Time	t _r			175		
Turn-Off Delay Time	t _{d(OFF)}			46		
Fall Time	t _f			62		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 20 A	T _J = 25°C		0.8	1.1	V
			T _J = 125°C		0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/μs, I _S = 20 A		75			ns
Charge Time	t _a			38			
Discharge Time	t _b			38			
Reverse Recovery Charge	Q _{RR}			140			nC

- Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

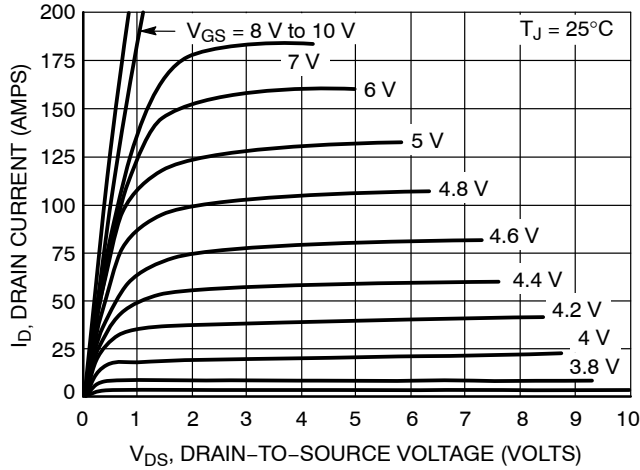


Figure 1. On-Region Characteristics

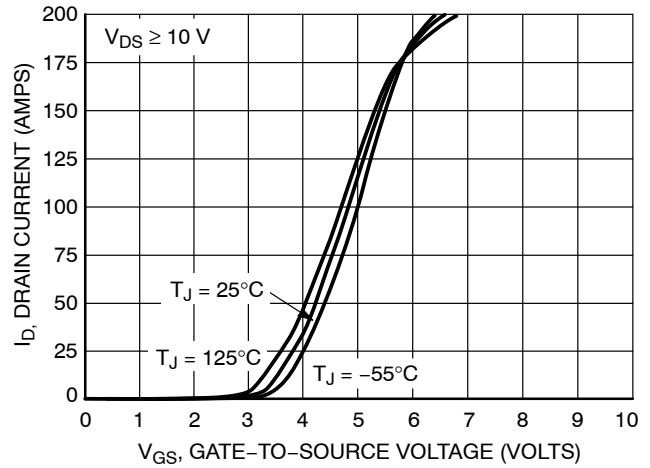


Figure 2. Transfer Characteristics

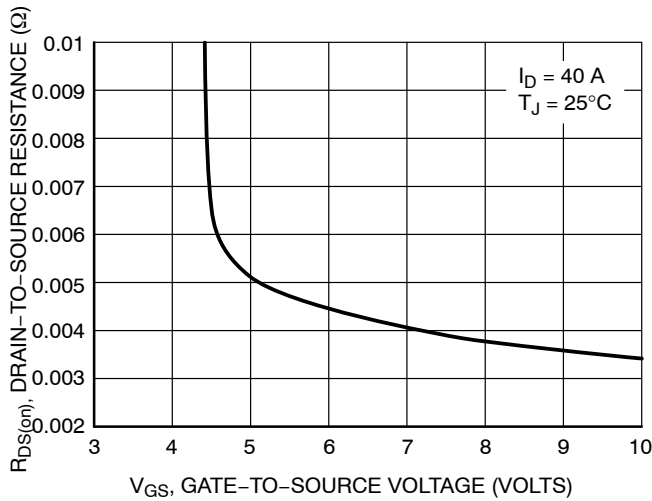


Figure 3. On-Resistance vs. Gate-to-Source Voltage

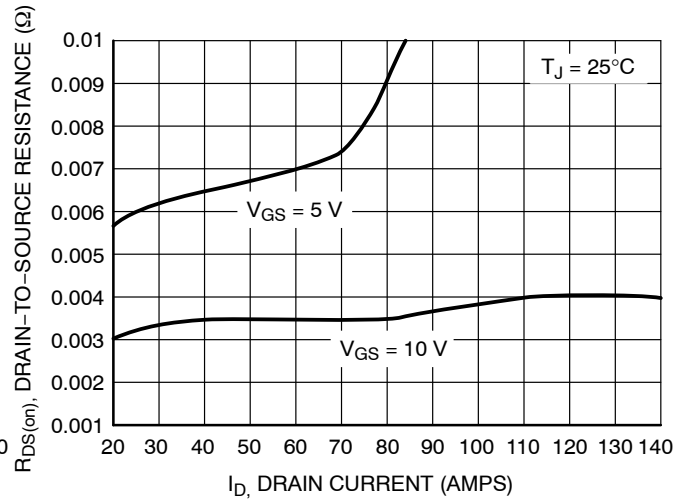


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

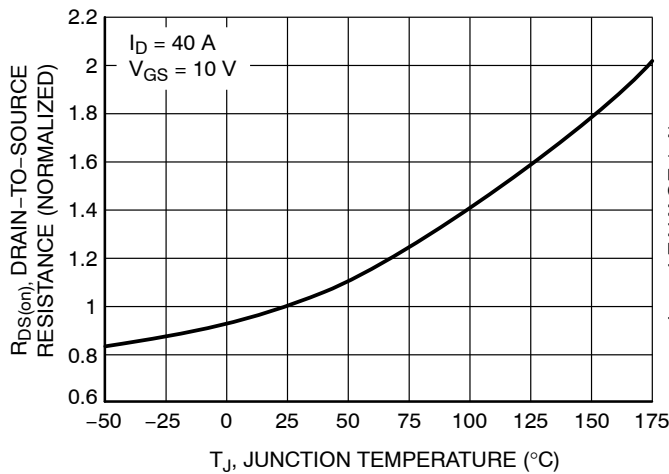


Figure 5. On-Resistance Variation with Temperature

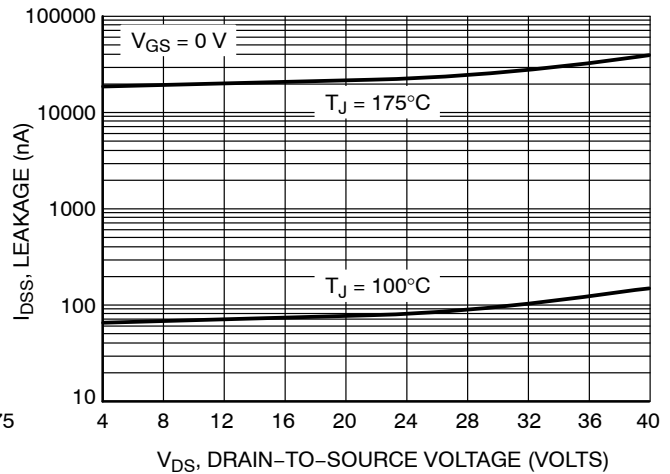
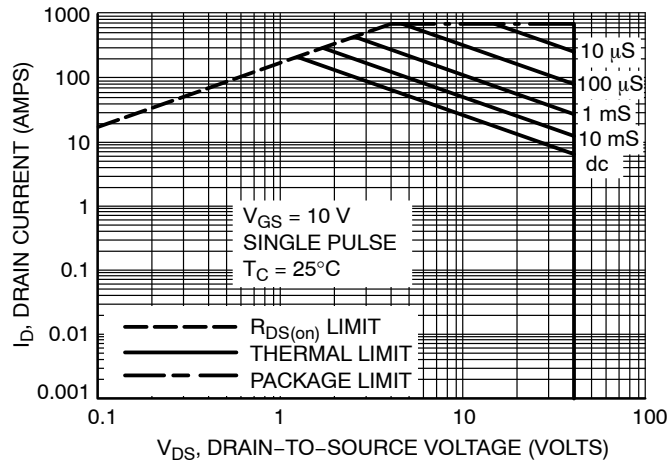
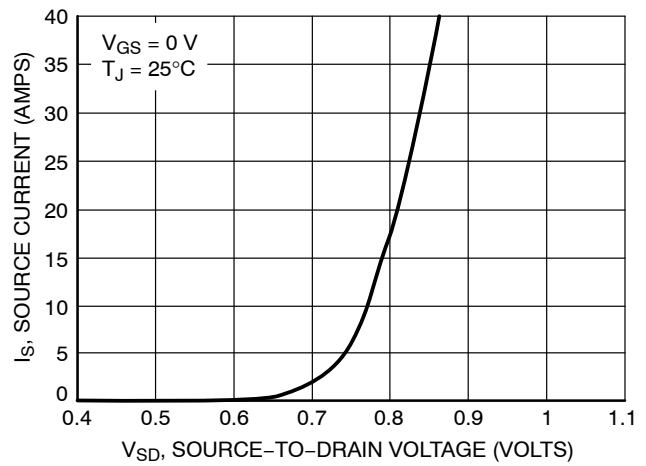
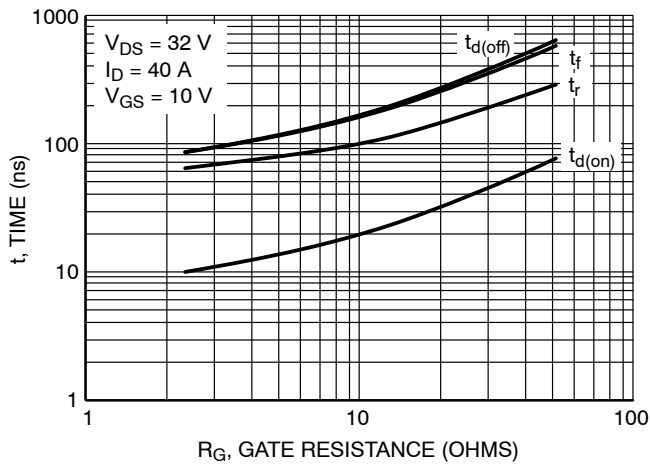
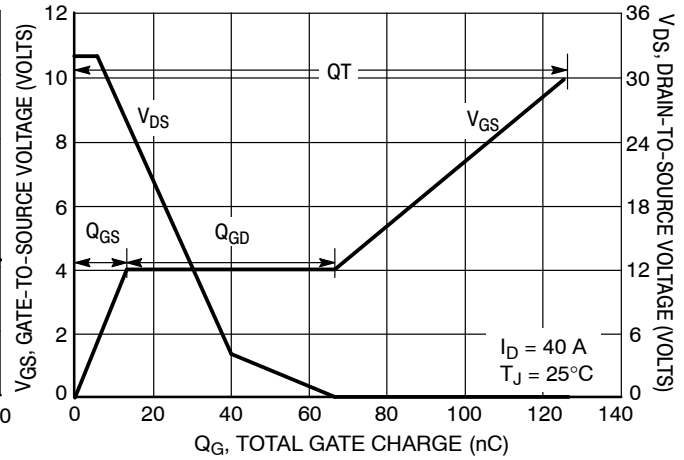
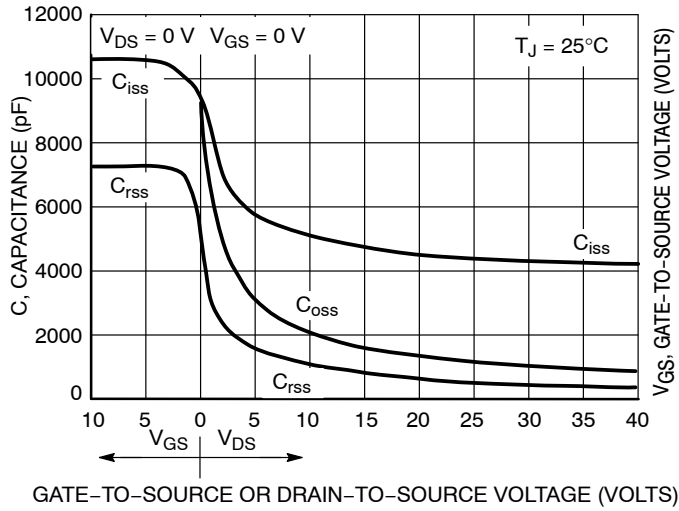


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



NTB5404N, NTP5404N, NVB5404N

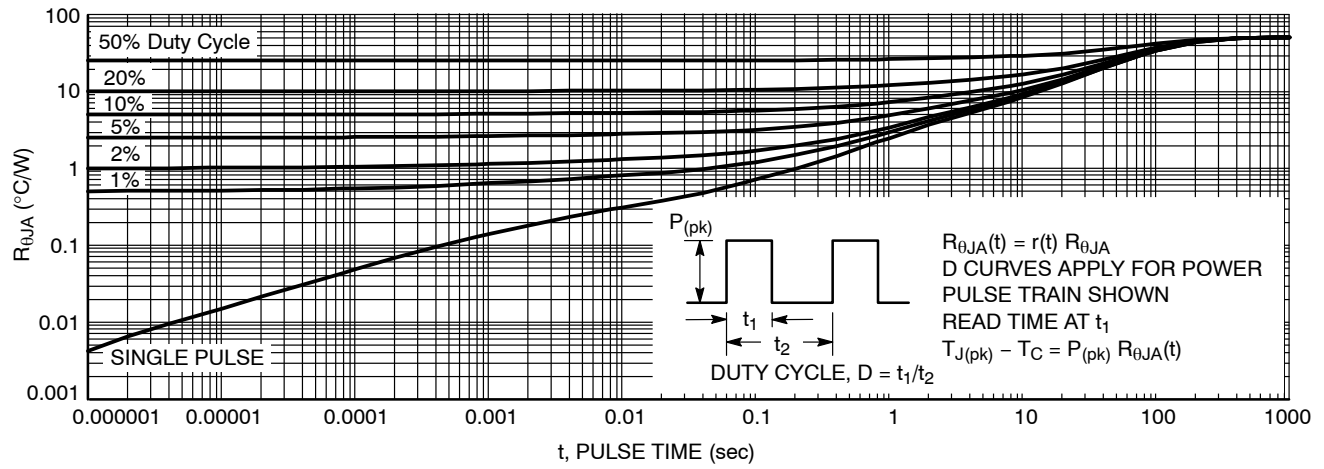
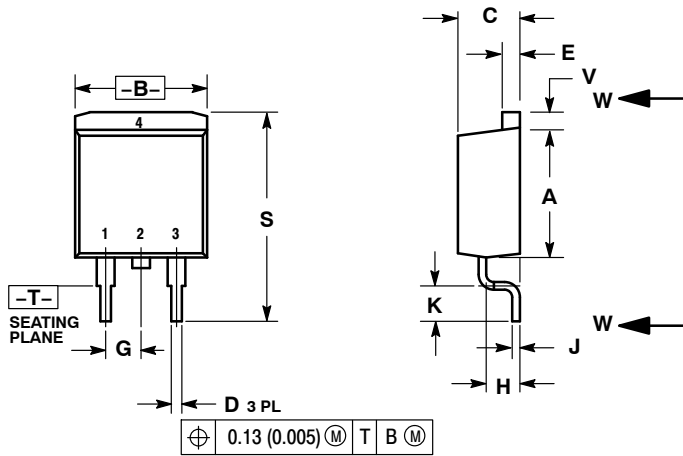


Figure 12. Thermal Response

NTB5404N, NTP5404N, NVB5404N

PACKAGE DIMENSIONS

D²PAK CASE 418B-04 ISSUE K



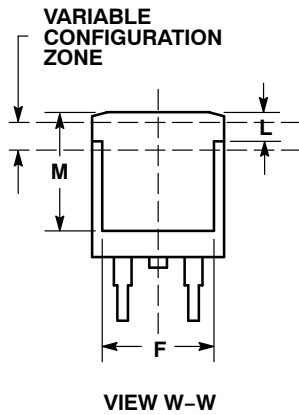
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

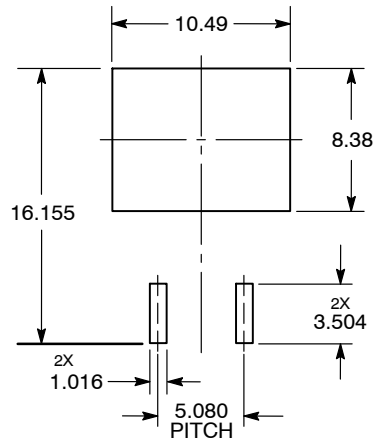
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



SOLDERING FOOTPRINT*



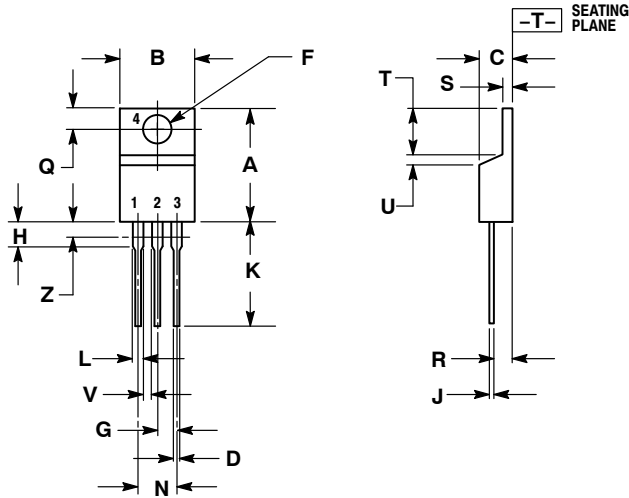
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTB5404N, NTP5404N, NVB5404N

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AG



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.036	0.64	0.91
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

NTB5404N/D