TLE5012B

GMR-Based Angle Sensor

1 Overview

Features

- Giant Magneto Resistance (GMR)-based principle
- Integrated magnetic field sensing for angle measurement
- 360° angle measurement with revolution counter and angle speed measurement
- Two separate highly accurate single bit SD-ADC
- 15 bit representation of absolute angle value on the output (resolution of 0.01°)
- 16 bit representation of sine / cosine values on the interface
- Max. 1.0° angle error over lifetime and temperature-range with activated auto-calibration
- Bi-directional SSC Interface up to 8 Mbit/s
- Supports Safety Integrity Level (SIL) with diagnostic functions and status information
- Interfaces: SSC, PWM, Incremental Interface (IIF), Hall Switch Mode (HSM), Short PWM Code (SPC, based on SENT protocol defined in SAE J2716)
- Output pins can be configured (programmed or pre-configured) as push-pull or open-drain
- Bus mode operation of multiple sensors on one line is possible with SSC or SPC interface
- 0.25 µm CMOS technology
- Automotive qualified: -40°C to 150°C (junction temperature)
- ESD > 4 kV (HBM)
- RoHS compliant (Pb-free package)
- Halogen-free

PRO-SIL™ Features

- Test vectors switchable to ADC input (activated via SSC interface)
- Inversion or combination of filter input streams (activated via SSC interface)
- Data transmission check via 8-bit Cyclic Redundancy Check (CRC) for SSC communication and 4-bit CRC nibble for SPC interface
- Built-in Self-test (BIST) routines for ISM, CORDIC, CCU, ADCs run at startup
- Two independent active interfaces possible
- Overvoltage and undervoltage detection

Potential applications

The TLE5012B GMR-based angle sensor is designed for angular position sensing in automotive applications such as:

- Electrical commutated motor (e.g. used in Electric Power Steering (EPS))
- Rotary switches
- Steering angle measurements
- General angular sensing

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE5012B is a 360° angle sensor that detects the orientation of a magnetic field. This is achieved by measuring sine and cosine angle components with monolithic integrated Giant Magneto Resistance (iGMR) elements. These raw signals (sine and cosine) are digitally processed internally to calculate the angle orientation of the magnetic field (magnet).

The TLE5012B is a pre-calibrated sensor. The calibration parameters are stored in laser fuses. At start-up the values of the fuses are written into flip-flops, where these values can be changed by the application-specific parameters. Further precision of the angle measurement over a wide temperature range and a long lifetime can be improved by enabling an optional internal autocalibration algorithm.

Data communications are accomplished with a bi-directional Synchronous Serial Communication (SSC) that is SPI-compatible. The sensor configuration is stored in registers, which are accessible by the SSC interface.

Additionally four other interfaces are available with the TLE5012B: Pulse-Width-Modulation (PWM) Protocol, Short-PWM-Code (SPC) Protocol, Hall Switch Mode (HSM) and Incremental Interface (IIF). These interfaces can be used in parallel with SSC or alone. Pre-configured sensor derivates with different interface settings are available (see Table 1 and Chapter 5).

Online diagnostic functions are provided to ensure reliable operation.

Table 1 Derivate ordering codes

Product type	Marking	Ordering code	Package
TLE5012B E1000	012B1000	SP001166960	PG-DSO-8
TLE5012B E3005	012B3005	SP001166964	PG-DSO-8
TLE5012B E5000	012B5000	SP001166968	PG-DSO-8
TLE5012B E5020	012B5020	SP001166972	PG-DSO-8
TLE5012B E9000	012B9000	SP001166998	PG-DSO-8

Note: See Chapter 5 for description of derivates.

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2 Functional description

2.1 Block diagram

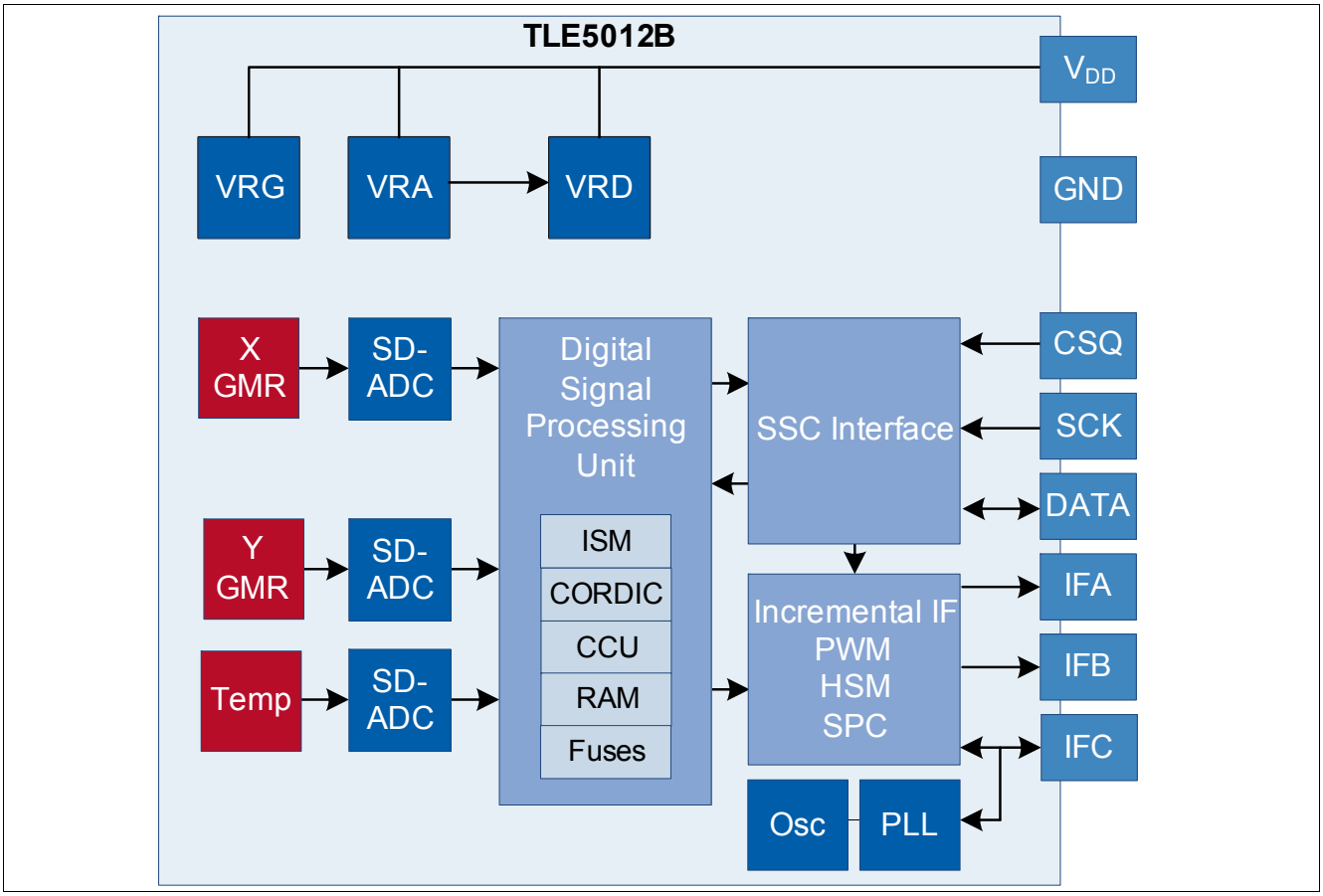

Figure 1 TLE5012B block diagram

2.2 Functional block description

2.2.1 Internal power supply

The internal stages of the TLE5012B are supplied with several voltage regulators:

- GMR Voltage Regulator, VRG
- Analog Voltage Regulator, VRA
- Digital Voltage Regulator, VRD (derived from VRA)

These regulators are directly connected to the supply voltage V_{DD}.

2.2.2 Oscillator and PLL

The digital clock of the TLE5012B is given by the Phase-Locked Loop (PLL), which is by default fed by an internal oscillator. In order to synchronize the TLE5012B with other ICs in a system, the TLE5012B can be configured via SSC interface to use an external clock signal supplied on the IFC pin as source for the PLL, instead of the internal clock. External clock mode is only available in PWM or SPC interface configuration.

2.2.3 SD-ADC

The Sigma-Delta Analog-Digital-Converters (SD-ADC) transform the analog GMR voltages and temperature voltage into the digital domain.

2.2.4 Digital Signal Processing Unit

The Digital Signal Processing Unit (DSPU) contains the:

- Intelligent State Machine (ISM), which does error compensation of offset, offset temperature drift, amplitude synchronicity and orthogonality of the raw signals from the GMR bridges, and performs additional features such as auto-calibration, prediction and angle speed calculation
- COordinate Rotation DIgital Computer (CORDIC), which contains the trigonometric function for angle calculation
- Capture Compare Unit (CCU), which is used to generate the PWM and SPC signals
- Random Access Memory (RAM), which contains the configuration registers
- Laser Fuses, which contain the calibration parameters for the error-compensation and the IC default configuration, which is loaded into the RAM at startup

2.2.5 Interfaces

Bi-directional communication with the TLE5012B is enabled by a three-wire SSC interface. In parallel to the SSC interface, one secondary interface can be selected, which is available on the IFA, IFB, IFC pins:

- PWM
- Incremental Interface
- Hall Switch Mode
- Short PWM Code

By using pre-configured derivates (see Chapter 5), the TLE5012B can also be operated with the secondary interface only, without SSC communication.

2.2.6 Safety features

The TLE5012B offers a multiplicity of safety features to support the Safety Integrity Level (SIL) and it is a PRO-SIL™ product.

Safety features are:

- Test vectors switchable to ADC input (activated via SSC interface)
- Inversion or combination of filter input streams (activated via SSC interface)
- Data transmission check via 8-bit Cyclic Redundancy Check (CRC) for SSC communication and 4-bit CRC nibble for SPC interface
- Built-in Self-test (BIST) routines for ISM, CORDIC, CCU, ADCs run at startup
- Two independent active interfaces possible
- Overvoltage and undervoltage detection

Disclaimer

PRO-SIL™ is a Registered Trademark of Infineon Technologies AG.

The PRO-SIL™ Trademark designates Infineon products which contain SIL Supporting Features.

SIL Supporting Features are intended to support the overall System Design to reach the desired SIL (according to IEC61508) or A-SIL (according to ISO26262) level for the Safety System with high efficiency.

SIL respectively A-SIL certification for such a System has to be reached on system level by the System Responsible at an accredited Certification Authority.

SIL stands for Safety Integrity Level (according to IEC 61508)

A-SIL stands for Automotive-Safety Integrity Level (according to ISO 26262)

2.3 Sensing principle

The Giant Magneto Resistance (GMR) sensor is implemented using vertical integration. This means that the GMR-sensitive areas are integrated above the logic part of the TLE5012B device. These GMR elements change their resistance depending on the direction of the magnetic field.

Four individual GMR elements are connected to one Wheatstone sensor bridge. These GMR elements sense one of two components of the applied magnetic field:

- X component, V_x (cosine) or the
- Y component, V_y (sine)

With this full-bridge structure the maximum GMR signal is available and temperature effects cancel out each other.

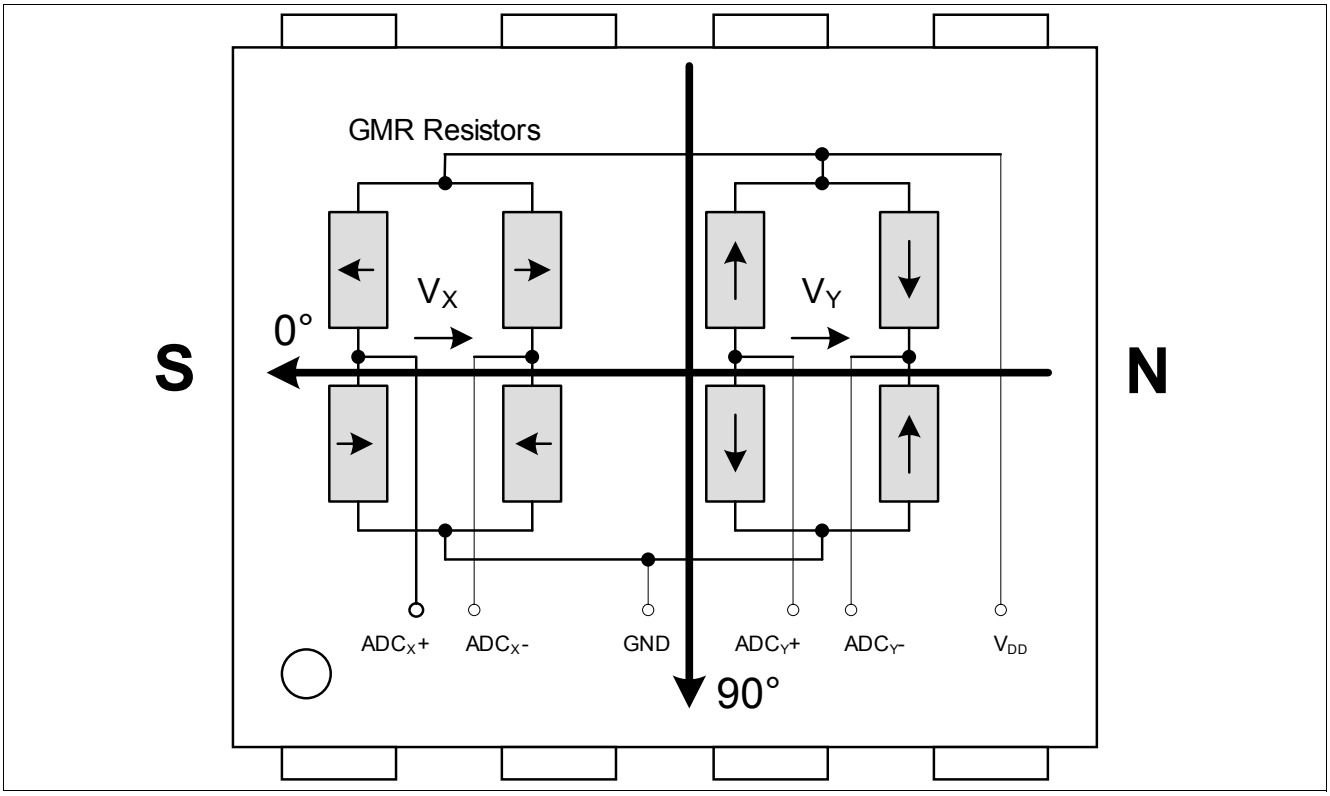

Figure 2 Sensitive bridges of the GMR sensor (not to scale)

Attention: Due to the rotational placement inaccuracy of the sensor IC in the package, the sensors 0° position may deviate by up to 3° from the package edge direction indicated in Figure 2.

In Figure 2, the arrows in the resistors represent the magnetic direction which is fixed in the reference layer. If the external magnetic field is parallel to the direction of the Reference Layer, the resistance is minimal. If they are anti-parallel, resistance is maximal.

The output signal of each bridge is only unambiguous over 180° between two maxima. Therefore two bridges are oriented orthogonally to each other to measure 360°.

With the trigonometric function ARCTAN2, the true 360° angle value is calculated out of the raw X and Y signals from the sensor bridges.

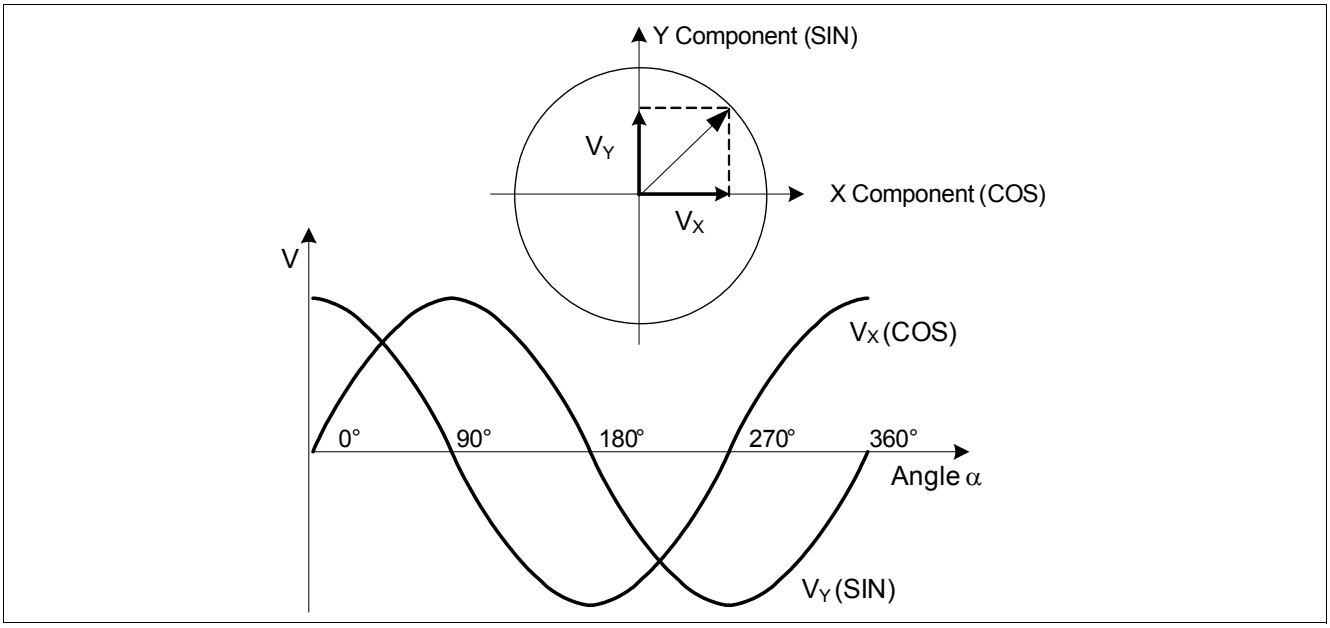

Figure 3 Ideal output of the GMR sensor bridges

2.4 Pin configuration

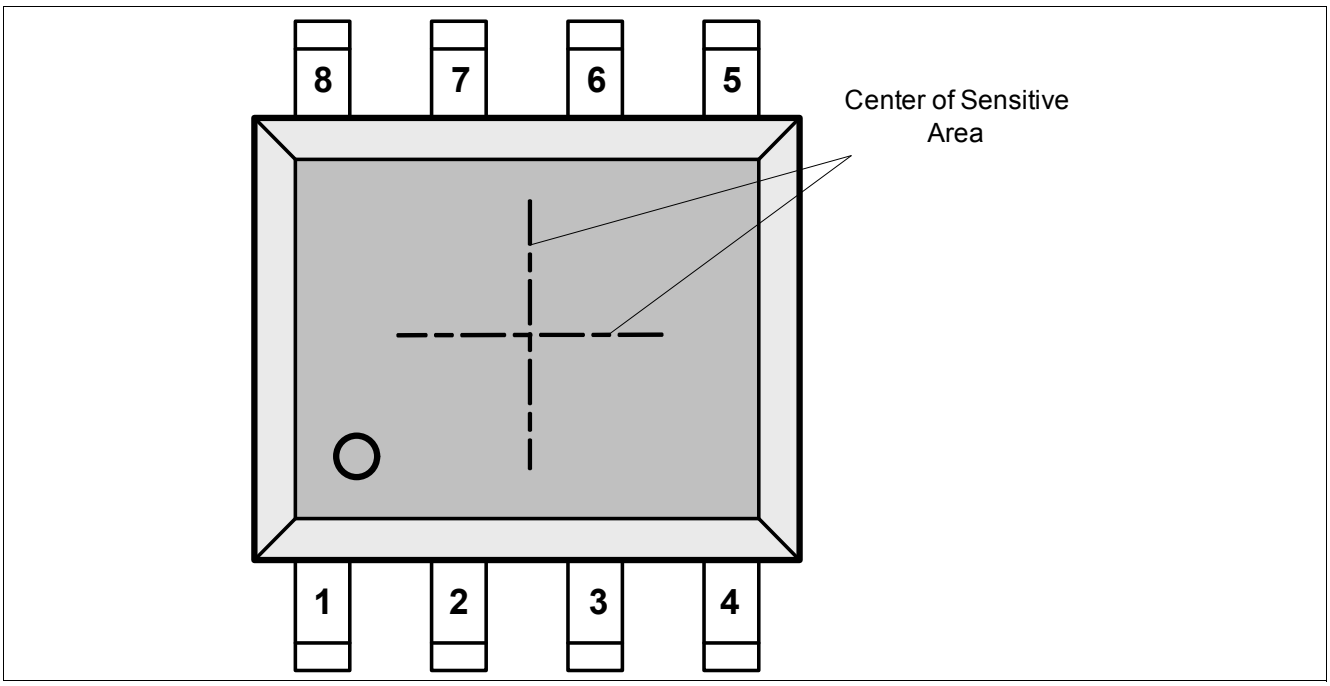

Figure 4 Pin configuration (top view)

2.5 Pin description

Table 2 Pin Description

Pin No.	Symbol	In/Out	Function
1	IFC (CLK / IIF_IDX / HS3)	I/O	Interface C: External Clock[1)] / IIF Index / Hall Switch Signal 3
2	SCK	I	SSC Clock
3	CSQ	I	SSC Chip Select
4	DATA	I/O	SSC Data
5	IFA (IIF_A / HS1 / PWM / SPC)	I/O	Interface A: IIF Phase A / Hall Switch Signal 1 / PWM / SPC output (input for SPC trigger only)
6	V_{DD}	-	Supply Voltage
7	GND	-	Ground
8	IFB (IIF_B / HS2)	O	Interface B: IIF Phase B / Hall Switch Signal 2

1) External clock feature is not available in IIF or HSM interface mode.

3 Application circuits

The application circuits in this chapter show the various communication possibilities of the TLE5012B. The pin output mode configuration is device-specific and it can be either push-pull or open-drain. The bit IFAB_OD (register IFAB, 0DH) indicates the output mode for the IFA, IFB and IFC pins. The SSC pins are by default push-pull (bit SSC_OD, register MOD_3, 09H). Every application circuits below are using otherwise specified SSC with push-pull configuration and the internal clock.

3.1 IIF interface and SSC (IIF in push-pull configuration)

Figure 5 shows a block diagram of a TLE5012B with Incremental Interface (IIF) and SSC interface. The derivate TLE5012B - E1000 is by default configured with push-pull IFA (IIF_A), IFB (IIF_ B) and IFC (IIF_IDX) pins. When the output pins are configurated as open-drain, three pull-up resistors should be added (e.g. 2K2Ω) between the data lines and VDD.

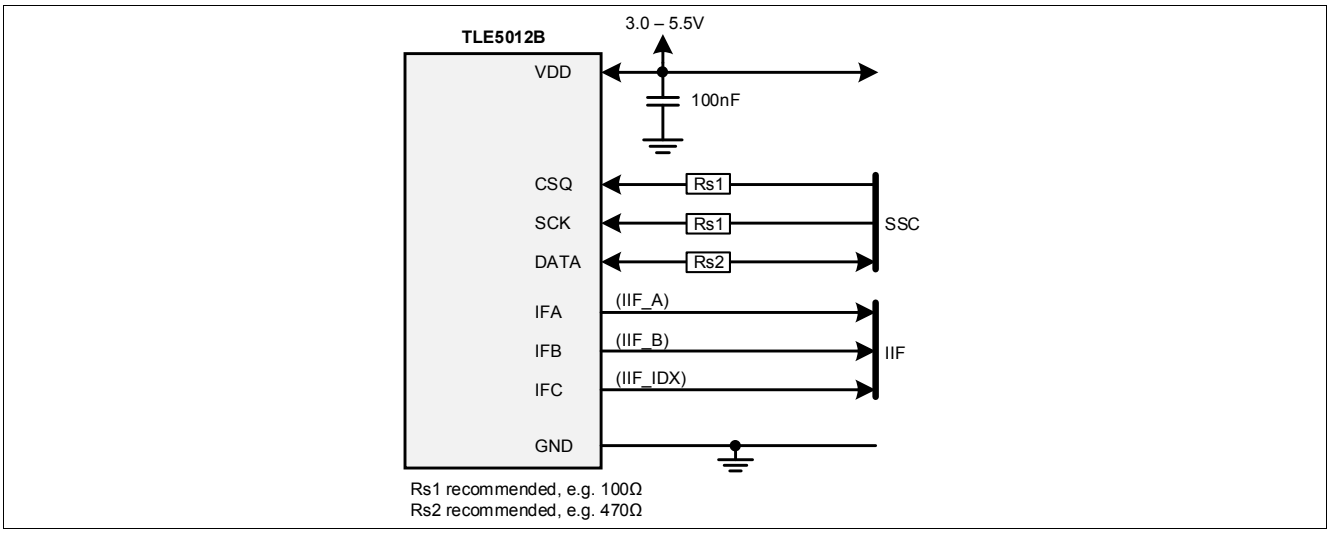

Figure 5 Application circuit for TLE5012B with IIF interface and SSC

3.2 HSM interface and SSC (HSM in push-pull configuration)

Figure 6 shows a block diagram of the TLE5012B with Hall Switch Mode (HSM) and SSC interface. The derivate TLE5012B - E3005 is by default configurated with push-pull IFA (HS1), IFB (HS2) and IFC (HS3) pins.

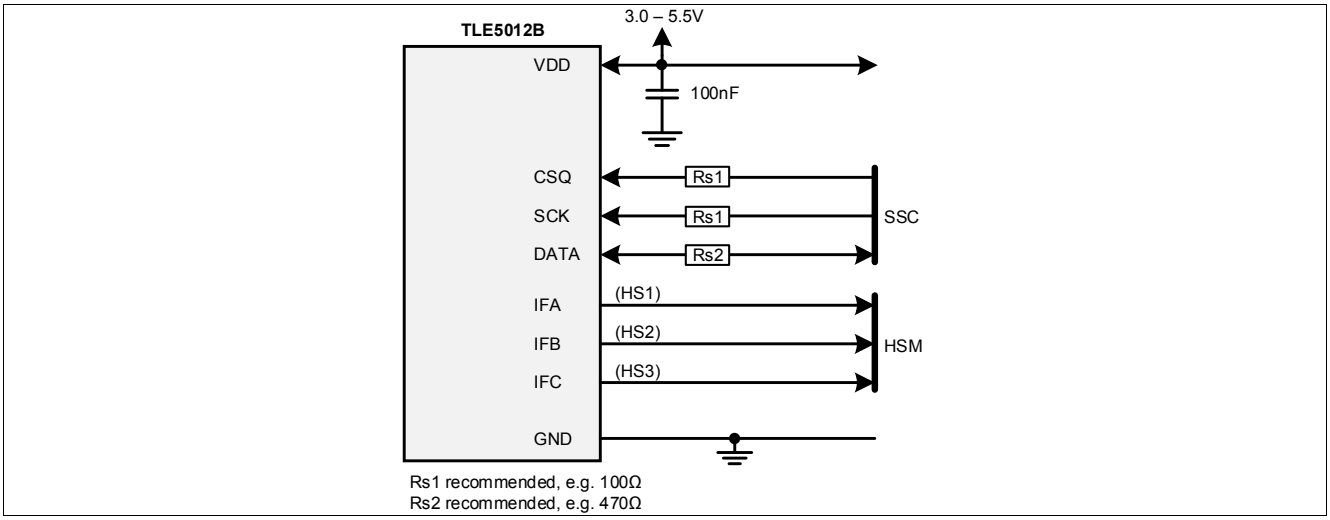

Figure 6 Application circuit for TLE5012B with HSM interface (push-pull configuration) and SSC

3.3 HSM interface and SSC (HSM in open-drain configuration)

As shown in Figure 7 when IFA, IFB and IFC are configurated via the SSC interface as open drain pins, three pull-up resistors (Rpu) should be added on the output lines.

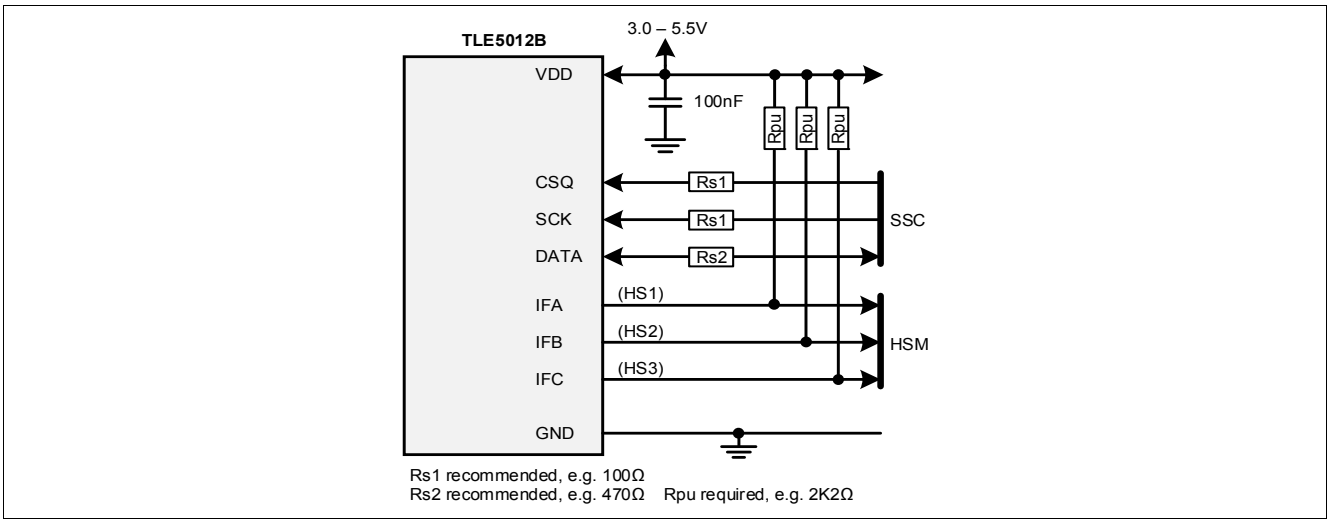

Figure 7 Application circuit for TLE5012B with HSM interface (open-drain configuration) and SSC

3.4 PWM interface (push-pull configuration)

The TLE5012B can be configured with PWM only (Figure 8). The derivate TLE5012B - E5000 is by default configurated with push-pull configuration for IFA (PWM) pin. Internal pull-up resistors are always available for DATA and CSQ pins (see Table 7). It is recommended to connect CSQ pin to VDD to provide a high level and avoid unintentional activation of the SSC interface. DATA pin should be left open. The figure below shows a typical implementation of the TLE5012B - E5000.

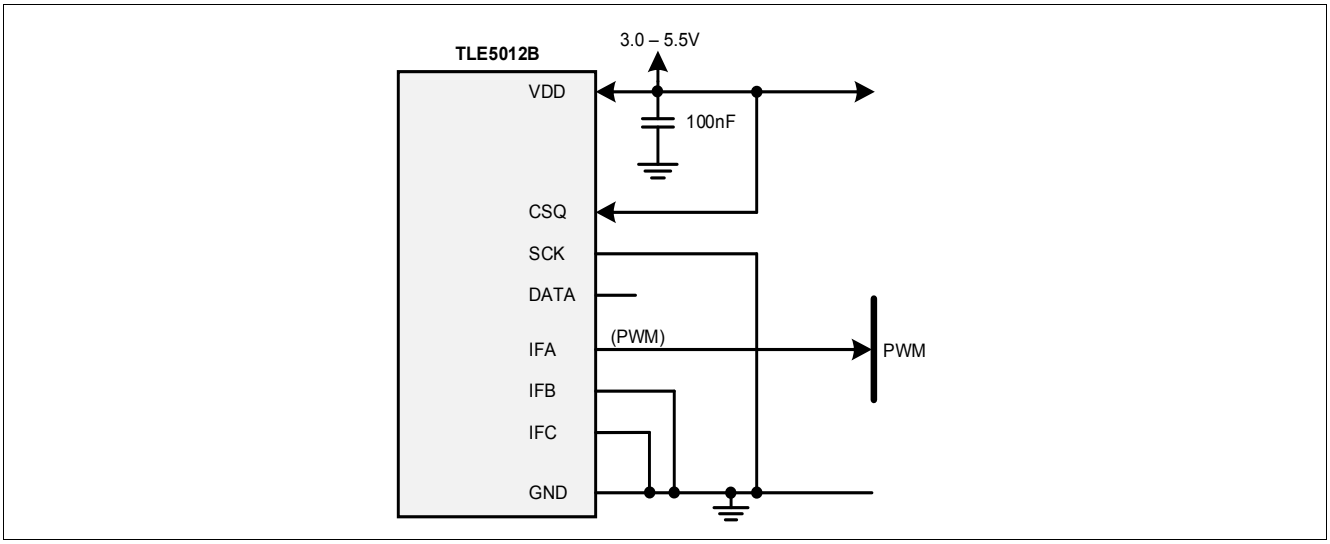

Figure 8 Application circuit for TLE5012B with PWM (push-pull configuration) interface

3.5 PWM interface (open-drain configuration)

The TLE5012B - E5020 is also a PWM derivate but with open drain for IFA (PWM) pin. A pull-up resistor (e.g. 2.2 kΩ) should be added between the IFA line and VDD, as shown in Figure 9.
Internal pull-up resistors are always available for DATA and CSQ pins (see Table 7). It is recommended to connect CSQ pin to VDD to provide a strong level and avoid unintentional activation of the SSC interface. DATA pin should be left open. The figure below shows a typical implementation of the TLE5012B - E5020.

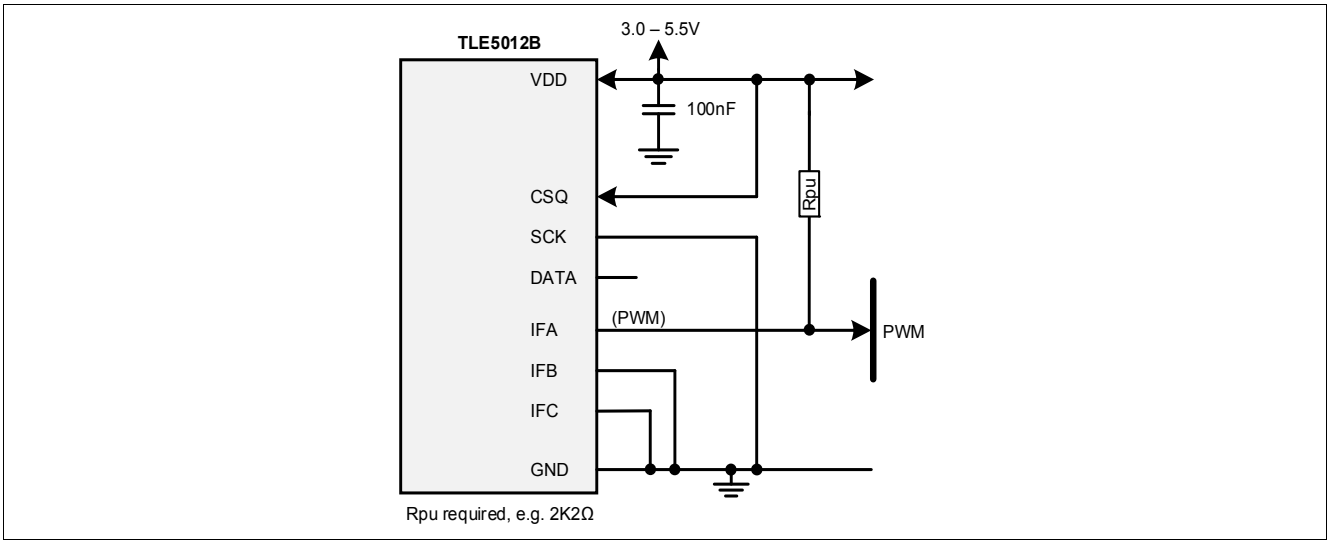

Figure 9 Application circuit for TLE5012B with PWM (open-drain configuration) interface

3.6 SPC interface

The TLE5012B can be configured with SPC only (Figure 10). This is only possible with the TLE5012B - E9000 derivate, which is by default configurated with an open-drain IFA (SPC) pin.
In Figure 10 the IFC (S_NR[1]) and SCK (S_NR[0]) pins are set to ground to generate the slave number (S_NR) 0D (or 00B). In case of SCK (S_NR[0]) needs to be set to VDD to generate another slave address, CSQ pin should be set to ground instead. Internal pull-up resistors are always available for DATA and CSQ pins (see Table 7). DATA pin should be left open. Since SCK and CSQ pins should have opposite level, it is not recommended to use the SSC interface in parallel.

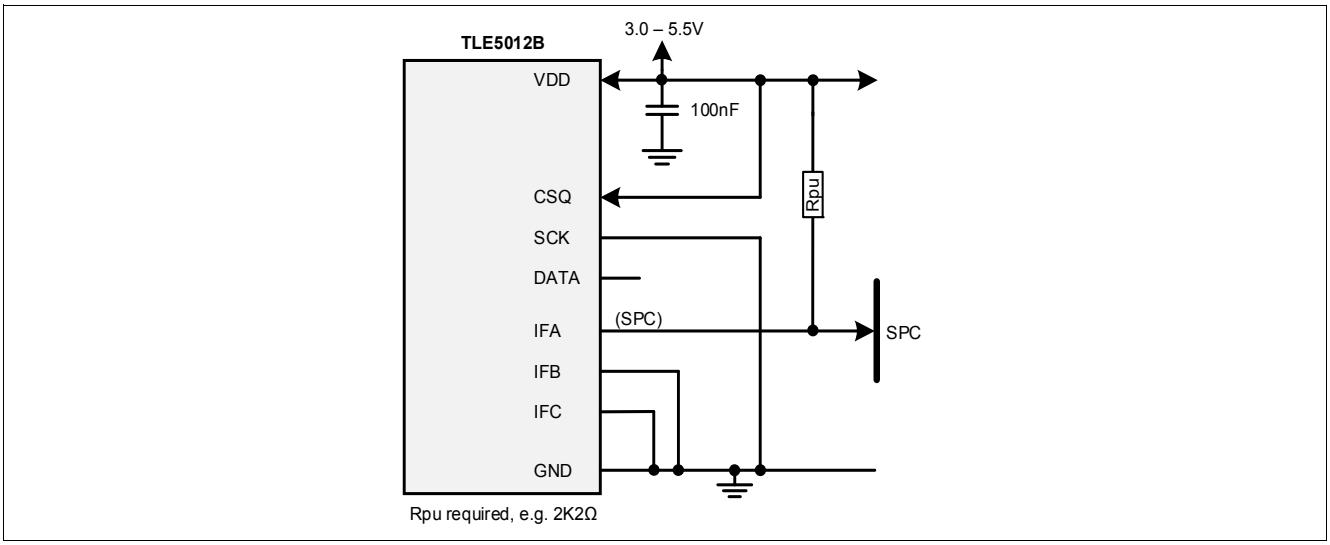

Figure 10 Application circuit for TLE5012B with SPC interface

3.7 SSC interface (push-pull configuration)

In Figure 5, Figure 6 and Figure 7 the SSC interface has the default push-pull configuration (see details in Figure 11). A series resistor on the DATA line is recommended to limit the current in erroneous cases (e.g. the sensor pushes high and the microcontroller pulls low at the same time or vice versa). Resistors on SCK and CSQ lines are recommended in case of disturbances or noise.

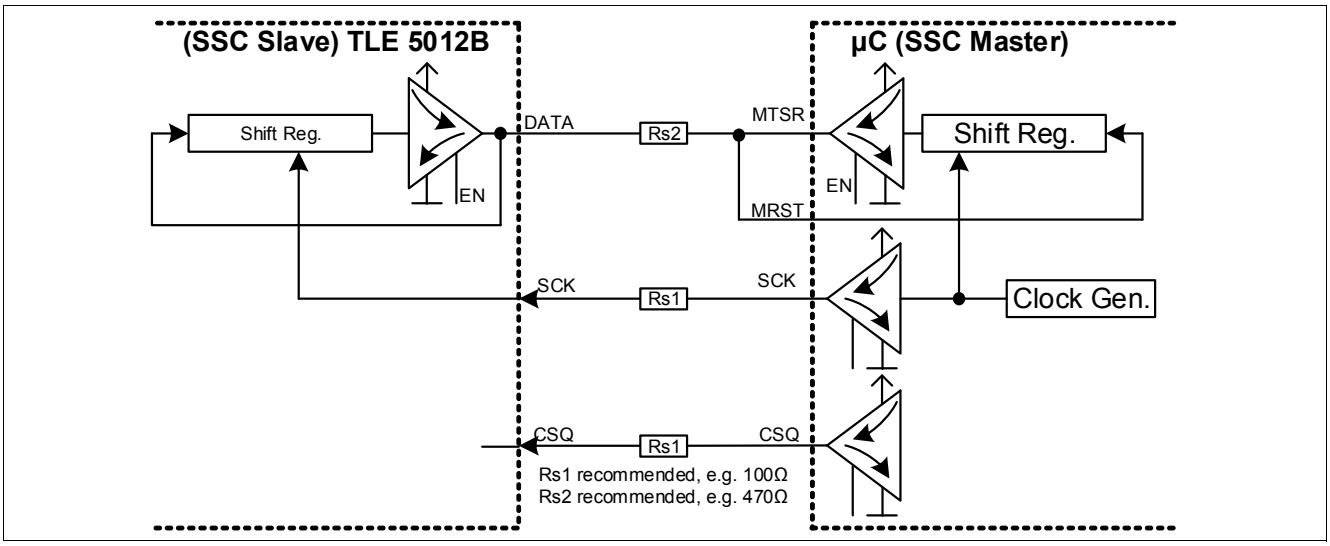

Figure 11 SSC interface with push-pull configuration (high-speed application)

3.8 SSC interface (open-drain configuration)

It is possible to use an open-drain configuration for the DATA line. This setup can be used to communicate with a microcontroller in a bus system, together with other SSC slaves (e.g. two TLE5012B devices for redundancy reasons). This mode can be activated using the bit SSC_OD.

Even though, push-pull configuration in a bus system is also possible since the addressing of the sensor is performed with CSQ pin.

The open-drain configuration can be seen in Figure 12. Series resistors on the DATA line are recommended to limit the current in erroneous cases. Resistors on SCK and CSQ lines are recommended in case of disturbances or noise A pull-up resistor of typ. 1 kΩ is required on the DATA line.

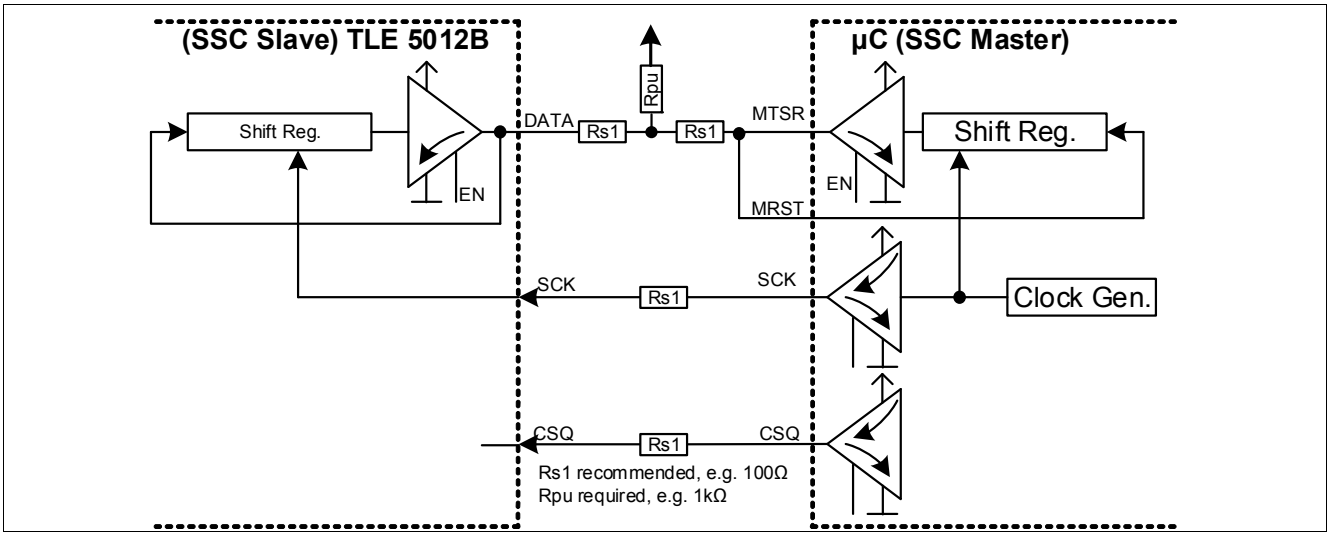

Figure 12 SSC interface with open-drain configuration (bus systems)

3.9 Sensor supply in bus mode

When using two or more devices in a bus configuration (SSC or SPC interface). It is recommended to use the same supply for every sensors connected to the bus. In case of a power loss the unpowered device is sinking current through the OUT pin. Depending on the external circuitry the additional current flow might disturb the bus behavior.

The figure below (Figure 13) shows a typical implementation of a bus mode using SPC interface. External components such as EMC filter or additional series resistors are not represented for clarity purpose. Only the pull-up resistor Rpu is shown.

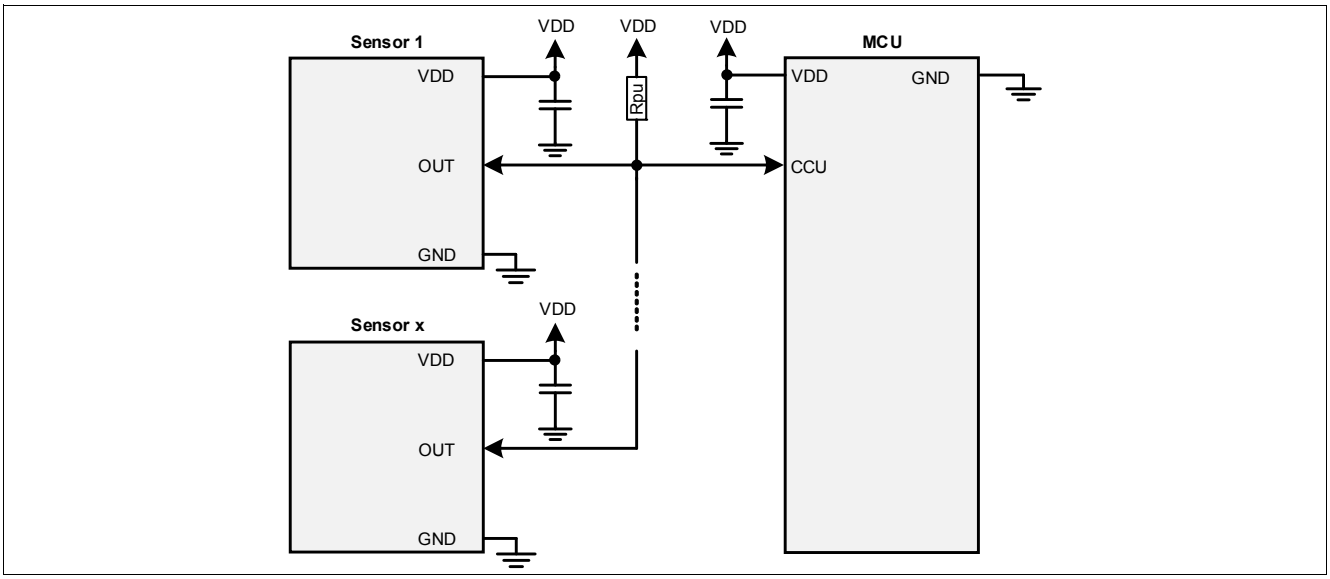

Figure 13 Sensors' supply in bus mode

4 Specification

4.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Voltage on V_{DD} pin with respect to ground (V_{SS})	V_{DD}	-0.5		6.5	V	Max 40 h/Lifetime
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5		6.5	V	
				V_{DD} + 0.5	V	
Junction temperature	T_J	-40		150	°C	
				150	°C	For 1000 h, not additive
Magnetic field induction	B			200	mT	Max. 5 min @ T_A = 25°C
				150	mT	Max. 5 h @ T_A = 25°C
Storage temperature	T_{ST}	-40		150	°C	Without magnetic field

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the device.

4.2 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE5012B. All parameters specified in the following sections refer to these operating conditions, unless otherwise noted. Table 4 is valid for -40°C < T_J < 150°C unless otherwise noted.

Table 4 Operating range and parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	5.0	5.5	V	1)
Supply current	I_{DD}		14	16	mA	
Magnetic induction at T_J = 25°C[2)3)]	B_{XY}	30		50	mT	-40°C < T_J < 150°C
		30		60	mT	-40°C < T_J < 100°C
		30		70	mT	-40°C < T_J < 85°C
Extended magnetic induction range at T_J = 25°C[2)3)]	B_{XY}	25		30	mT	Additional angle error of 0.1°
Angle range	*Ang*	0		360	°	
POR level	V_{POR}	2.0		2.9	V	Power-on reset
POR hysteresis	V_{PORhy}		30		mV	

Table 4 **Operating range and parameters** (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Power-on time[4)]	t_{Pon}		5	7	ms	$V_{DD} > V_{DDmin}$;
Fast Reset time[5)]	t_{Rfast}			0.5	ms	Fast reset is triggered by disabling startup BIST (S_BIST = 0), then enabling chip reset (AS_RST = 1)

1) Directly blocked with 100-nF ceramic capacitor.
2) Values refer to a homogeneous magnetic field (B_{XY}) without vertical magnetic induction (B_Z = 0 mT).
3) See Figure 14.
4) During "Power-on time," write access is not permitted (except for the switch to External Clock which requires a readout as a confirmation that external clock is selected).
5) Not subject to production test - verified by design/characterization.

The field strength of a magnet can be selected within the colored area of Figure 14. By limitation of the junction temperature, a higher magnetic field can be applied. In case of a maximum temperature T_J = 100°C, a magnet with up to 60 mT at T_J = 25°C is allowed.

It is also possible to widen the magnetic field range for higher temperatures. In that case, additional angle errors have to be considered.

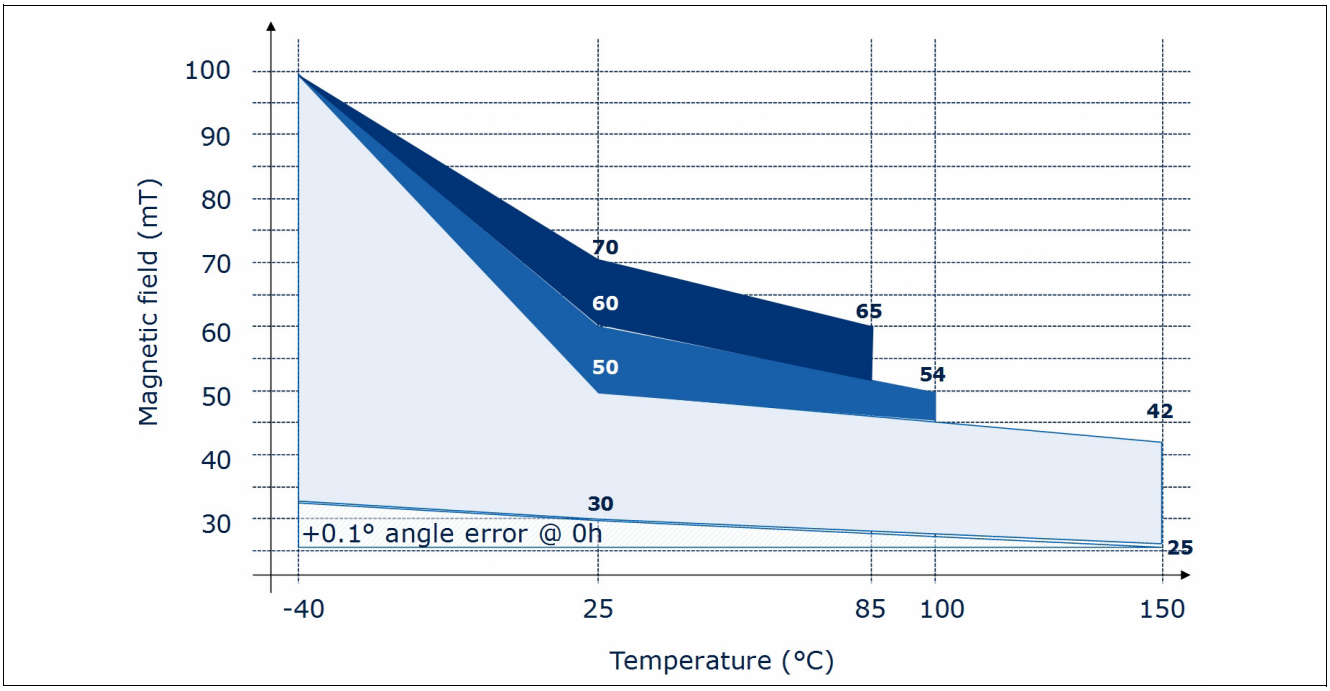

Figure 14 **Allowed magnetic field range as function of junction temperature.**

4.3 Characteristics

4.3.1 Input/Output characteristics

The indicated parameters apply to the full operating range, unless otherwise specified. The typical values correspond to a supply voltage V_{DD} = 5.0 V and 25°C, unless individually specified. All other values correspond to -40 °C < T_J < 150°C.

Within the register MOD_3, the driver strength and the slope for push-pull communication can be varied depending on the sensor output. The driver strength is specified in Table 5 and the slope fall and rise time in Table 6.

Table 5 Input voltage and output currents

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	-0.3		5.5	V	
				V_{DD}+ 0.3	V	
Output current (DATA-Pad)	I_Q			-25	mA	PAD_DRV ='0x', sink current[1)2)]
				-5	mA	PAD_DRV ='10', sink current[1)2)]
				-0.4	mA	PAD_DRV ='11', sink current[1)2)]
Output current (IFA / IFB / IFC - Pad)	I_Q			-15	mA	PAD_DRV ='0x', sink current[1)2)]
				-5	mA	PAD_DRV ='1x', sink current[1)2)]

1) Max. current to GND over open-drain output.
2) At V_{DD} = 5 V.

Table 6 Driver strength characteristic

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Output rise/fall time	t_{fall}, t_{rise}			8	ns	DATA, 50 pF, PAD_DRV='00'[1)2)]
				28	ns	DATA, 50 pF, PAD_DRV='01'[1)2)]
				45	ns	DATA, 50 pF, PAD_DRV='10'[1)2)]
				130	ns	DATA, 50 pF, PAD_DRV='11'[1)2)]
				15	ns	IFA/IFB, 20 pF, PAD_DRV='0x'[1)2)]
				30	ns	IFA/IFB, 20 pF, PAD_DRV='1x'[1)2)]

1) Valid for push-pull output
2) Not subject to production test - verified by design/characterization

Table 7 Electrical parameters for 4.5 V < V_{DD} < 5.5 V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input signal low-level	V_{L5}			0.3 V_{DD}	V	
Input signal high level	V_{H5}	0.7 V_{DD}			V	
Output signal low-level	V_{OL5}			1	V	DATA; I_Q = -25 mA (PAD_DRV='0x'), I_Q = -5 mA (PAD_DRV='10'), I_Q = -0.4 mA (PAD_DRV='11')
				1	V	IFA,B,C; I_Q = -15 mA (PAD_DRV='0x'), I_Q = -5 mA (PAD_DRV='1x')
Pull-up current[1)]	I_{PU}	-10		-225	µA	CSQ
		-10		-150	µA	DATA
Pull-down current[2)]	I_{PD}	10		225	µA	SCK
		10		150	µA	IFA, IFB, IFC

1) Internal pull-ups on CSQ and DATA pin are always enabled.
2) Internal pull-downs on IFA, IFB and IFC are enabled during startup and in open-drain mode, internal pull-down on SCK is always enabled.

Table 8 Electrical parameters for 3.0 V < V_{DD} < 3.6 V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input signal low-level	V_{L3}			0.3 V_{DD}	V	
Input signal high level	V_{H3}	0.7 V_{DD}			V	
Output signal low-level	V_{OL3}			0.9	V	DATA; I_Q = -15 mA (PAD_DRV='0x'), I_Q = -3 mA (PAD_DRV='10'), I_Q = -0.24 mA (PAD_DRV='11')
				0.9	V	IFA,IFB; I_Q = - 10 mA (PAD_DRV='0x'), I_Q = -3 mA (PAD_DRV='1x')
Pull-up current[1)]	I_{PU}	-3		-225	µA	CSQ
		-3		-150	µA	DATA
Pull-down current[2)]	I_{PD}	3		225	µA	SCK
		3		150	µA	IFA, IFB, IFC

1) Internal pull-ups on CSQ and DATA pin are always enabled.
2) Internal pull-downs on IFA, IFB and IFC are enabled during startup and in open-drain mode, internal pull-down on SCK is always enabled.

4.3.2 ESD protection

Table 9 ESD protection

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage	V_{HBM}			±4.0	kV	Human Body Model[1)]
	V_{SDM}			±0.5	kV	Socketed Device Model[2)]

1) Human Body Model (HBM) according to: AEC-Q100-002.
2) Socketed Device Model (SDM) according to: ESDA/ANSI/ESD SP5.3.2-2008.

4.3.3 GMR parameters

All parameters apply over B_{XY} = 30 mT and T_A = 25°C, unless otherwise specified.

Table 10 Basic GMR parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
X, Y output range	RG_{ADC}			±23230	digits	Operating range[1)]
X, Y amplitude[2)]	A_X, A_Y	6000	9500	15781	digits	At ambient temperature
		3922		20620	digits	Operating range
X, Y synchronicity[3)]	k	87.5	100	112.49	%	
X, Y offset[4)]	O_X, O_Y	-2048	0	+2047	digits	
X, Y orthogonality error	j	-11.25	0	+11.24	°	
X, Y amplitude without magnet	X_0, Y_0			+4096	digits	Operating range[1)]

1) Not subject to production test - verified by design/characterization.
2) See Figure 15.
3) $k = 100 * (A_X/A_Y)$
4) $O_Y = (Y_{MAX} + Y_{MIN}) / 2$; $O_X = (X_{MAX} + X_{MIN}) / 2$

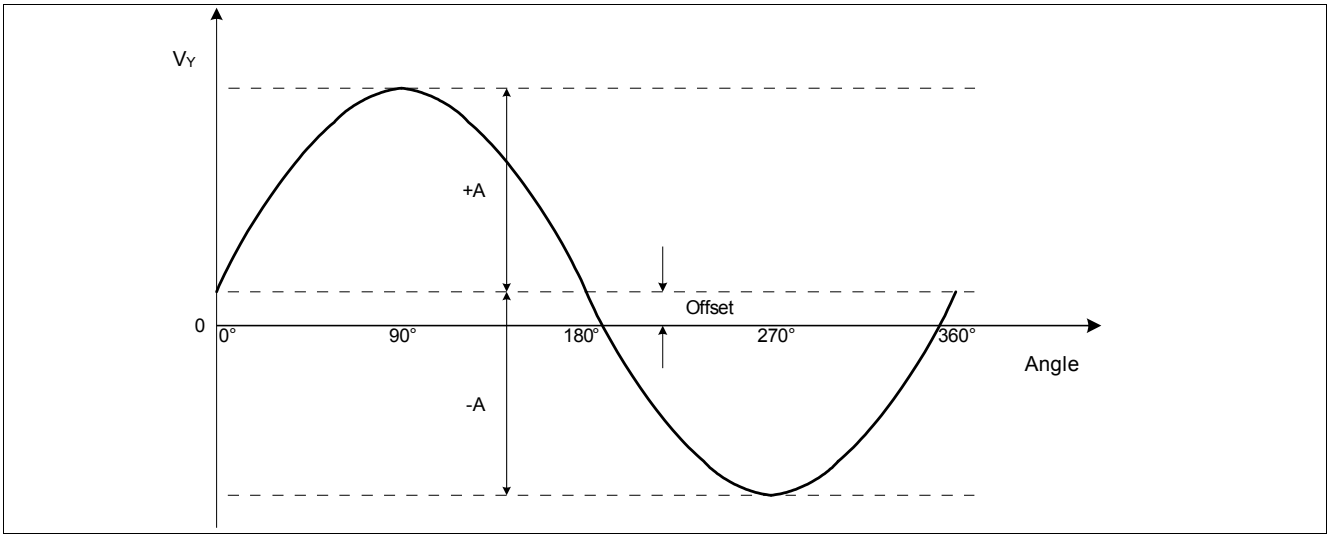

Figure 15 Offset and amplitude definition

4.3.4 Angle performance

After internal calculation, the sensor has a remaining error, as shown in Table 11. The error value refers to B_Z = 0 mT and the operating conditions given in Table 4.

The overall angle error represents the relative angle error. This error describes the deviation from the reference line after zero-angle definition. It is valid for a static magnetic field.

If the magnetic field is rotating during the measurement, an additional propagation error is caused by the angle delay time (see Table 12), which the sensor needs to calculate the angle from the raw sine and cosine values from the MR bridges. In fast-turning applications, prediction can be enabled to reduce this propagation error.

Table 11 Angle performance

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overall angle error (with auto-calibration)	α_{Err}		0.6[1)]	1.0	°	Including lifetime and temperature drift[2)3)4)]. Note: in case of temperature changes above 5 Kelvin within 1.5 revolutions refer to Figure 16 for additional angle error.
Overall angle error (without auto- calibration)	α_{Err}		0.6[1)]	1.3	°	Including temperature drift[2)3)5)]
				1.9	°	Including lifetime and temperature drift[2)3)4)]

1) At 25°C, B = 30 mT.
2) Including hysteresis error, caused by revolution direction change.
3) Relative error after zero angle definition.
4) Not subject to production test - verified by design/characterization.
5) 0 h.

If autocalibration (see Chapter 4.3.5) is enabled and the temperature changes by more than 5 Kelvin during 1.5 revolutions an additional error has to be added to the specified angle error in Table 11. This error depends on the temperature change (Delta Temperature) as well as from the initial temperature (Tstart) as shown in Figure 16. Once the temperature stabilizes and the application completes 1.5 revolutions, then the angle error is as specified in Table 11.

For negative Delta Temperature changes (from higher to lower temperatures) the additional angle error will be smaller than the corresponding positive Delta Temperature changes (from lower to higher temperatures) shown in Figure 16. The Figure 16 applies to the worst case.

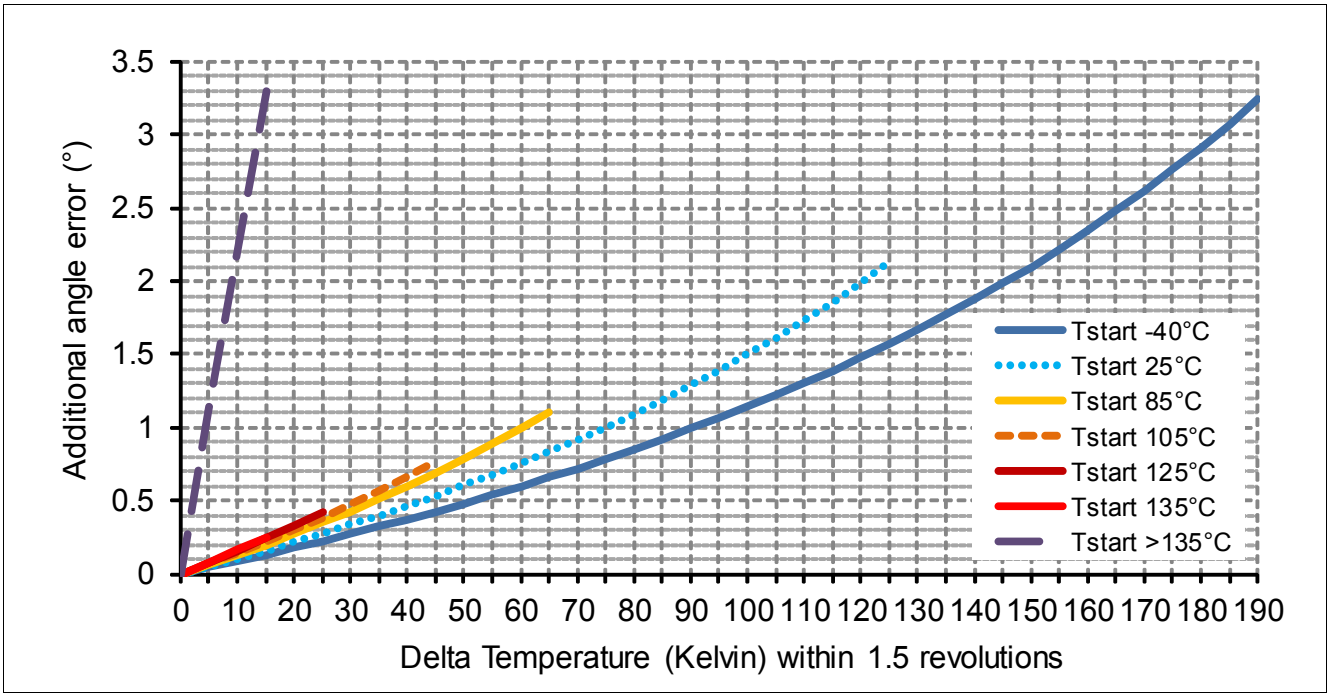

Figure 16 Additional angle error for temperature changes above 5 Kelvin within 1.5 revolutions

4.3.5 Autocalibration

The autocalibration enables online parameter calculation and therefore reduces the angle error due to temperature and lifetime drifts.

The TLE5012B is a pre-calibrated sensor, so autocalibration is only enabled in some devices by default. The update mode can be chosen with the AUTOCAL setting in the MOD_2 register. The TLE5012B needs 1.5 revolutions to generate new autocalibration parameters. These parameters are continuously updated. The parameters are updated in a smooth way (one Least-Significant Bit within the chosen range or time) to avoid an angle jump on the output.

AUTOCAL Modes:

- 00: No autocalibration.
- 01: Autocalibration Mode 1. One LSB to final values within the update time t_{upd} (depending on FIR_MD setting).
- 10: Autocalibration Mode 2. Only one LSB update over one full parameter generation (1.5 revolutions). After update of one LSB, the autocalibration will calculate the parameters again.
- 11: Autocalibration Mode 3. One LSB to final values within an angle range of 11.25°.

4.3.6 Signal processing

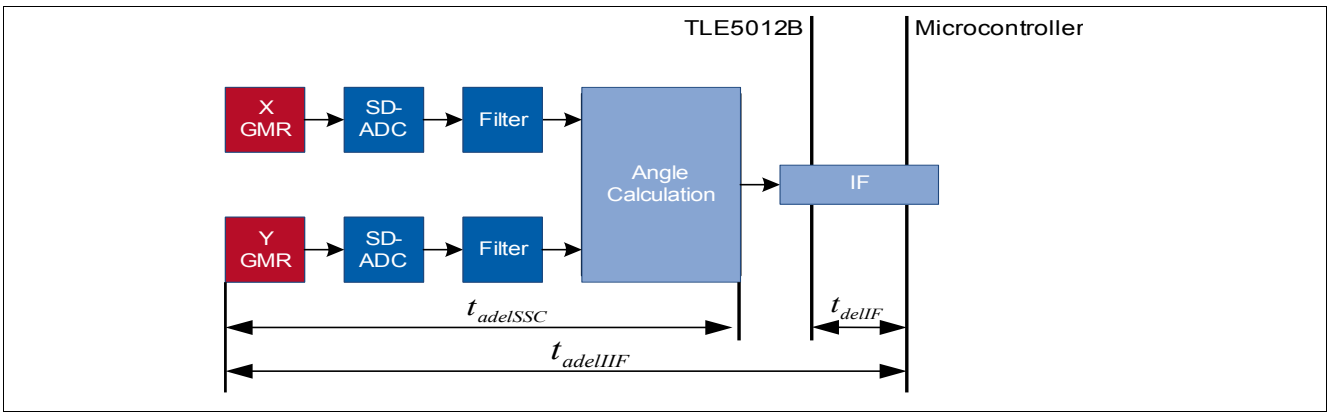

Figure 17 Signal path

The signal path of the TLE5012B is depicted in Figure 17. It consists of the GMR-bridge, ADC, filter and angle calculation. The delay time between a physical change in the GMR elements and a signal on the output depends on the filter and interface configurations. In fast turning applications, this delay causes an additional rotation speed dependent angle error.

The TLE5012B has an optional prediction feature, which serves to reduce the speed dependent angle error in applications where the rotation speed does not change abruptly. Prediction uses the difference between current and last two angle values to approximate the angle value which will be present after the delay time (see Figure 18). The output value is calculated by adding this difference to the measured value, according to Equation (4.1).

$$\alpha(t+1) = \alpha(t) + \alpha(t-1) - \alpha(t-2) \tag{4.1}$$

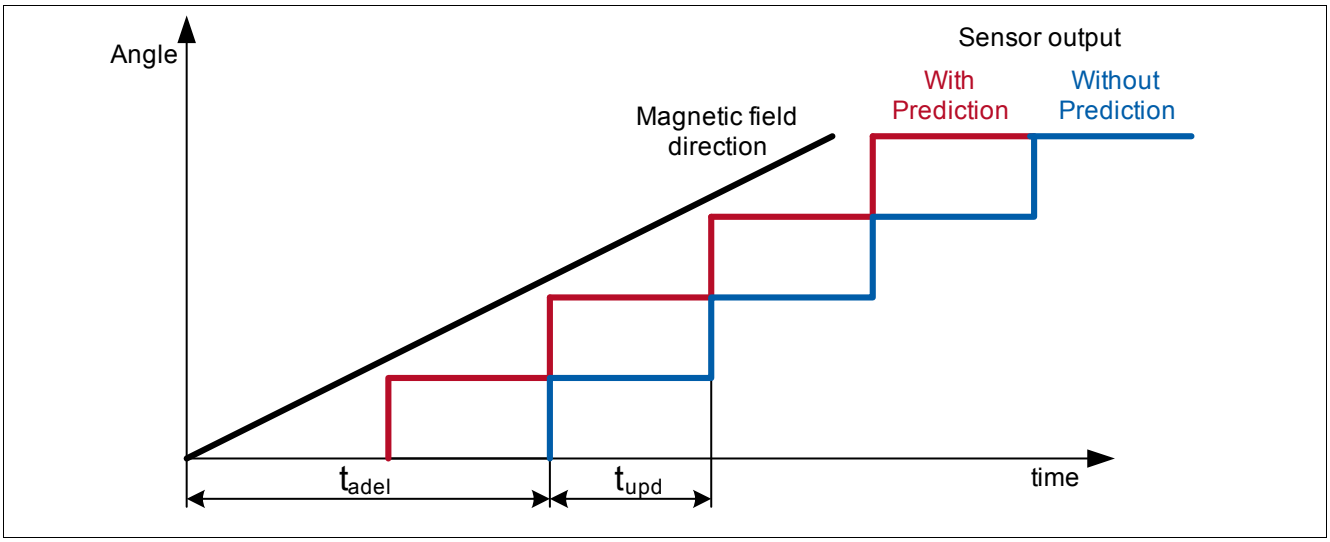

Figure 18 Delay of sensor output

Table 12 Signal processing

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Filter update period	t_{upd}		42.7		µs	FIR_MD = 1[1)]
			85.3		µs	FIR_MD = 2[1)]
			170.6		µs	FIR_MD = 3[1)]
Angle delay time without prediction[2)]	$t_{adelSSC}$		85	95	µs	FIR_MD = 1[1)]
			150	165	µs	FIR_MD = 2[1)]
			275	300	µs	FIR_MD = 3[1)]
	$t_{adelIIF}$		120	135	µs	FIR_MD = 1[1)]
			180	200	µs	FIR_MD = 2[1)]
			305	330	µs	FIR_MD = 3[1)]
Angle delay time with prediction[2)]	$t_{adelSSC}$		45	50	µs	FIR_MD = 1; PREDICT = 1[1)]
			65	70	µs	FIR_MD = 2; PREDICT = 1[1)]
			105	115	µs	FIR_MD = 3; PREDICT = 1 [1)]
	$t_{adelIIF}$		75	90	µs	FIR_MD = 1; PREDICT = 1[1)]
			95	110	µs	FIR_MD = 2; PREDICT = 1[1)]
			135	150	µs	FIR_MD = 3; PREDICT = 1 [1)]
Angle noise (RMS)	N_{Angle}		0.08		°	FIR_MD = 1[1)]
			0.05		°	FIR_MD = 2[1)](default)
			0.04		°	FIR_MD = 3[1)]

1) Not subject to production test - verified by design/characterization.
2) Valid at constant rotation speed.

All delay times specified in Table 12 are valid for an ideal internal oscillator frequency of 24 MHz. For the exact timing, the variation of the internal oscillator frequency has to be taken into account (see Chapter 4.3.7).

4.3.7 Clock supply (CLK timing definition)

The internal clock supply of the TLE5012B is subject to production-specific variations, which have to be considered for all timing specifications.

Table 13 Internal clock timing specification

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Digital clock	f_{DIG}	22.8	24	25.8	MHz	
Internal oscillator frequency	f_{CLK}	3.8	4.0	4.3	MHz	

In order to fix the IC timing and synchronize the TLE5012B with other ICs in a system, it can be switched to operate with an external clock signal supplied to the IFC pin. The clock input signal must fulfill certain requirements:

- The high or low pulse width must not exceed the specified values, because the PLL needs a minimum pulse width and must be spike-filtered.
- The duty cycle factor should typically be 50%, but it can vary between 30% and 70%.
- The PLL is triggered at the positive edge of the clock. If more than 2 edges are missing, a chip reset is generated automatically and the sensor restarts with the internal clock. This is indicated by the S_RST, and CLK_SEL bits, and additionally by the Safety Word (see Chapter 4.4.1.2).

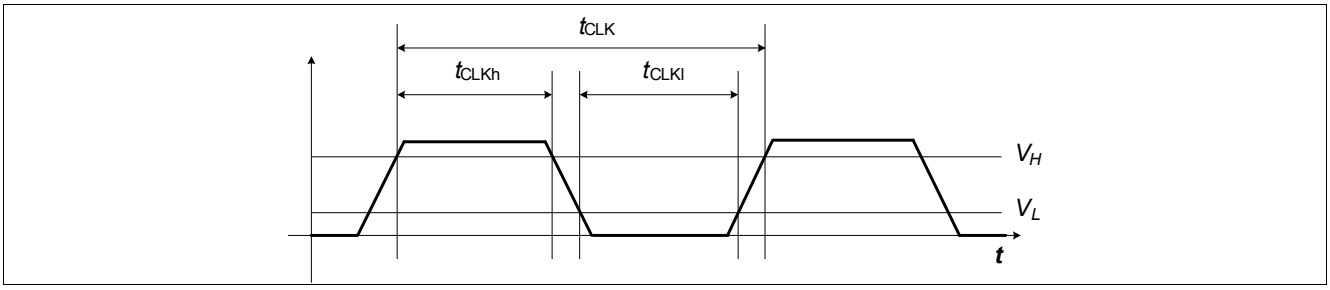

Figure 19 External CLK timing definition

Table 14 External clock specification

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{CLK}	3.8	4.0	4.3	MHz	
CLK duty cycle[1)2)]	CLK_{DUTY}	30	50	70	%	
CLK rise time	t_{CLKr}			30	ns	From V_L to V_H
CLK fall time	t_{CLKf}			30	ns	From V_H to V_L

1) Minimum duty cycle factor: $t_{CLKh(min)}$ / t_{CLK} with t_{CLK}= 1 / f_{CLK}
2) Maximum duty cycle factor: $t_{CLKh(max)}$ / t_{CLK} with t_{CLK}= 1 / f_{CLK}

4.4 Interfaces

4.4.1 Synchronous Serial Communication (SSC)

The 3-pin SSC interface consists of a bi-directional push-pull (tri-state on receive) or open-drain data pin (configurable with SSC_OD bit) and the serial clock and chip-select input pins. The SSC Interface is designed to communicate with a microcontroller peer-to-peer for fast applications.

4.4.1.1 SSC timing definition

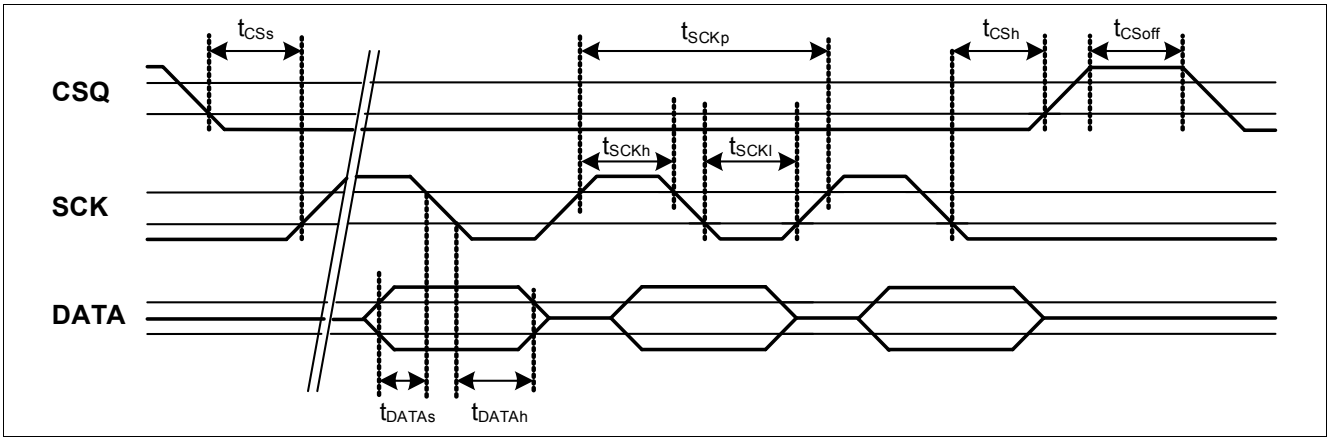

Figure 20 SSC timing

SSC inactive time (CS_{off})

The SSC inactive time defines the delay time after a transfer before the TLE5012B can be selected again.

Table 15 SSC push-pull timing specification

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}		8.0		Mbit/s	1)
CSQ setup time	t_{CSs}	105			ns	1)
CSQ hold time	t_{CSh}	105			ns	1)
CSQ off	t_{CSoff}	600			ns	SSC inactive time[1)]
SCK period	t_{SCKp}	120	125		ns	1)
SCK high	t_{SCKh}	40			ns	1)
SCK low	t_{SCKl}	30			ns	1)
DATA setup time	t_{DATAs}	25			ns	1)
DATA hold time	t_{DATAh}	40			ns	1)
Write read delay	t_{wr_delay}	130			ns	1)
Update time	$t_{CSupdate}$	1			µs	See Figure 24[1)]
SCK off	t_{SCKoff}	170			ns	1)

1) Not subject to production test - verified by design/characterization.

Table 16 SSC open-drain timing specification

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
SSC baud rate	f_{SSC}		2.0		Mbit/s	Pull-up Resistor = 1 kΩ[1)]
CSQ setup time	t_{CSs}	300			ns	[1)]
CSQ hold time	t_{CSh}	400			ns	[1)]
CSQ off	t_{CSoff}	600			ns	SSC inactive time[1)]
SCK period	t_{SCKp}	500			ns	[1)]
SCK high	t_{SCKh}		190		ns	[1)]
SCK low	t_{SCKl}		190		ns	[1)]
DATA setup time	t_{DATAs}	25			ns	[1)]
DATA hold time	t_{DATAh}	40			ns	[1)]
Write read delay	t_{wr_delay}	130			ns	[1)]
Update time	$t_{CSupdate}$	1			µs	See Figure 24[1)]
SCK off	t_{SCKoff}	170			ns	[1)]

1) Not subject to production test - verified by design/characterization.

4.4.1.2 SSC data transfer

The SSC data transfer is word-aligned. The following transfer words are possible:

- Command Word (to access and change operating modes of the TLE5012B)
- Data words (any data transferred in any direction)
- Safety Word (confirms the data transfer and provides status information)

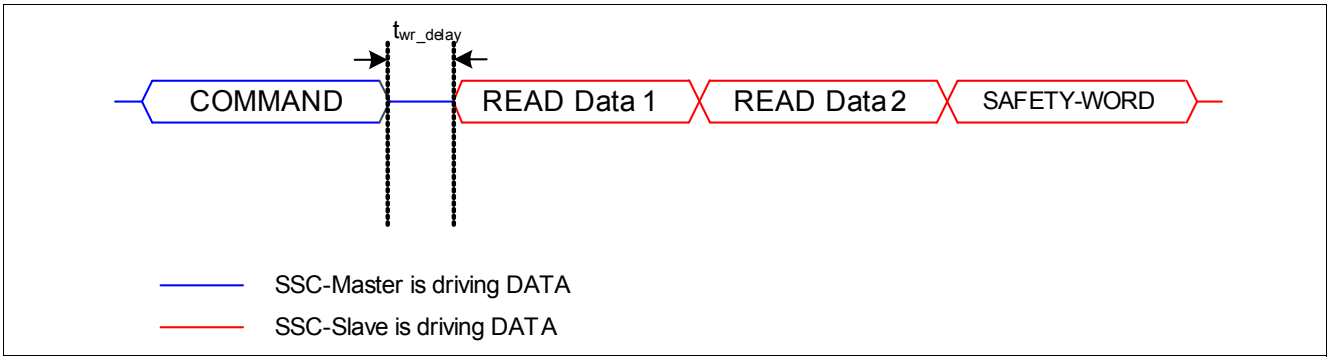

Figure 21 SSC data transfer (data-read example)

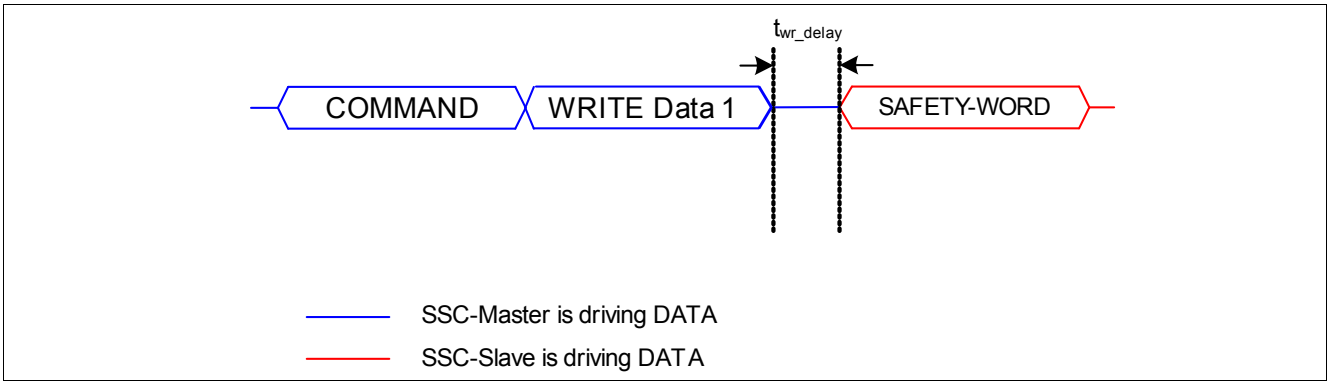

Figure 22 SSC data transfer (data-write example)

Command Word

SSC Communication between the TLE5012B and a microcontroller is generally initiated by a command word. The structure of the command word is shown in Table 17. If an update is triggered by shortly pulling low CSQ without a clock on SCK a snapshot of all system values is stored in the update registers simultaneously. A read command with the UPD bit set then allows to readout this consistent set of values instead of the current values. Bits with an update buffer are marked by an “u” in the Type column in register descriptions. The initialization of such an update is described on page 30.

Table 17 Structure of the Command Word

Name	Bits	Description
RW	[15]	Read - Write 0: Write 1: Read
Lock	[14..11]	4-bit Lock Value 0000_B: Default operating access for addresses 0x00:0x04 1010_B: Configuration access for addresses 0x05:0x11

Table 17 Structure of the Command Word (cont'd)

Name	Bits	Description
UPD	[10]	Update-Register Access 0: Access to current values 1: Access to values in update buffer
ADDR	[9..4]	6-bit Address
ND	[3..0]	4-bit Number of Data Words

Safety Word

The safety word consists of the following bits:

Table 18 Structure of the Safety Word

Name	Bits	Description
STAT[1)]	Chip and Interface Status	
	[15]	Indication of chip reset or watchdog overflow (resets after readout) via SSC 0: Reset occurred 1: No reset
	[14]	System error (e.g. overvoltage; undervoltage; V_{DD}-, GND- off; ROM;...) 0: Error occurred (S_VR; S_DSPU; S_OV; S_XYOL: S_MAGOL; S_FUSE; S_ROM; S_ADCT) 1: No error
	[13]	Interface access error (access to wrong address; wrong lock) 0: Error occurred 1: No error
	[12]	Valid angle value (NO_GMR_A = 0; NO_GMR_XY = 0) 0: Angle value invalid 1: Angle value valid
RESP	[11..8]	Sensor number response indicator The sensor number bit is pulled low and the other bits are high
CRC	[7..0]	Cyclic Redundancy Check (CRC)

1) When an error occurs, the corresponding status bit in the safety word remains "low" until the STAT register (address 00_H) is read via SSC interface.

Bit Types

The types of bits used in the registers are listed here:

Table 19 Bit Types

Abbreviation	Function	Description
r	Read	Read-only registers
w	Write	Read and write registers
u	Update	Update buffer for this bit is present. If an update is issued and the Update-Register Access bit (UPD in Command Word) is set, the immediate values are stored in this update buffer simultaneously. This allows a snapshot of all necessary system parameters at the same time.

Data communication via SSC

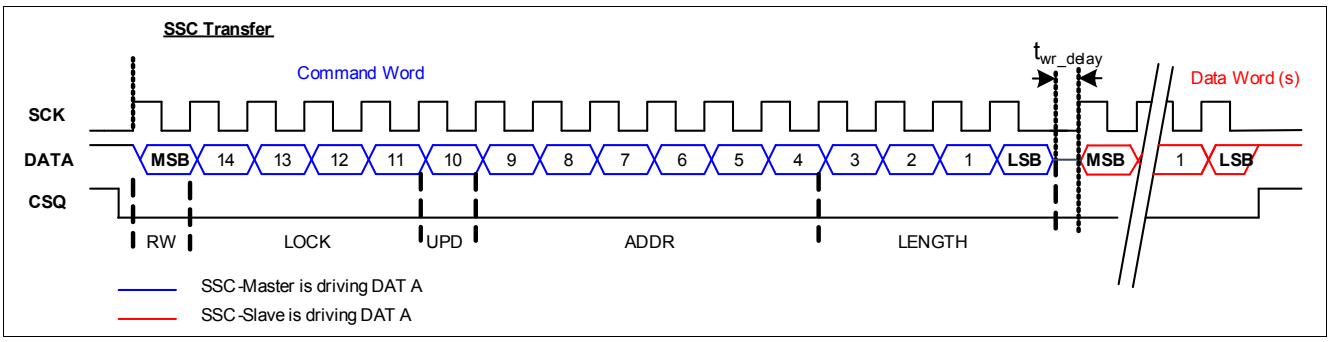

Figure 23 SSC bit ordering (read example)

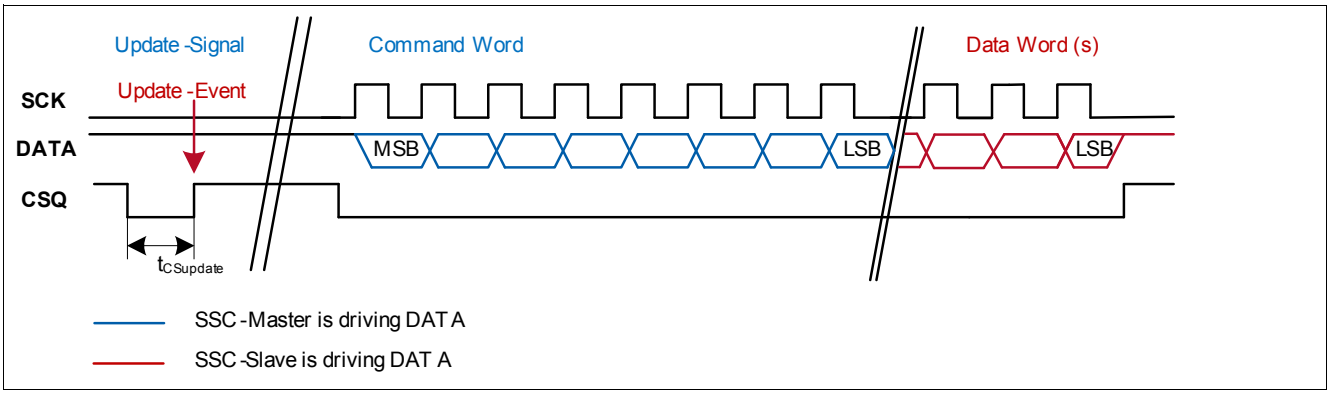

Figure 24 Update of update registers

The data communication via SSC interface has the following characteristics:

- The data transmission order is Most-Significant Bit (MSB) first, Last-Significant Bit (LSB) last.
- Data is put on the data line with the rising edge on SCK and read with the falling edge on SCK.
- The SSC Interface is word-aligned. All functions are activated after each transmitted word.
- After every data transfer with ND ≥ 1, the 16-bit Safety Word is appended by the TLE5012B.
- A “high” condition on the Chip Select pin (CSQ) of the selected TLE5012B interrupts the transfer immediately. The CRC calculator is automatically reset.
- After changing the data direction, a delay t_{wr_delay} (see Table 16) has to be implemented before continuing the data transfer. This is necessary for internal register access.

- If in the Command Word the number of data is greater than 1 (ND > 1), then a corresponding number of consecutive registers is read, starting at the address given by ADDR.
- In case an overflow occurs at address $3F_H$, the transfer continues at address 00_H.
- If in the Command Word the number of data is zero (ND = 0), the register at the address given by ADDR is read, but no Safety Word is sent by the TLE5012B. This allows a fast readout of one register.
- At a rising edge of CSQ without a preceding data transfer (no SCK pulse, see Figure 24), the content of all registers which have an update buffer is saved into the buffer. This procedure serves to take a snapshot of all relevant sensor parameters at a given time. The content of the update buffer can then be read by sending a read command for the desired register and setting the UPD bit of the Command Word to “1”.
- After sending the Safety Word, the transfer ends. To start another data transfer, the CSQ has to be deselected once for at least t_{CSoff}.
- By default, the SSC interface is set to push-pull. The push-pull driver is active only if the TLE5012B has to send data, otherwise the DATA pin is set to high-impedance.

Cyclic Redundancy Check (CRC)

- This CRC is according to the J1850 Bus Specification.
- Every new transfer restarts the CRC generation.
- Every Byte of a transfer will be taken into account to generate the CRC (also the sent command(s)).
- Generator polynomial: X8+X4+X3+X2+1, but for the CRC generation the fast-CRC generation circuit is used (see Figure 25).
- The seed value of the fast CRC circuit is ‘11111111_B’.
- The remainder is inverted before transmission.

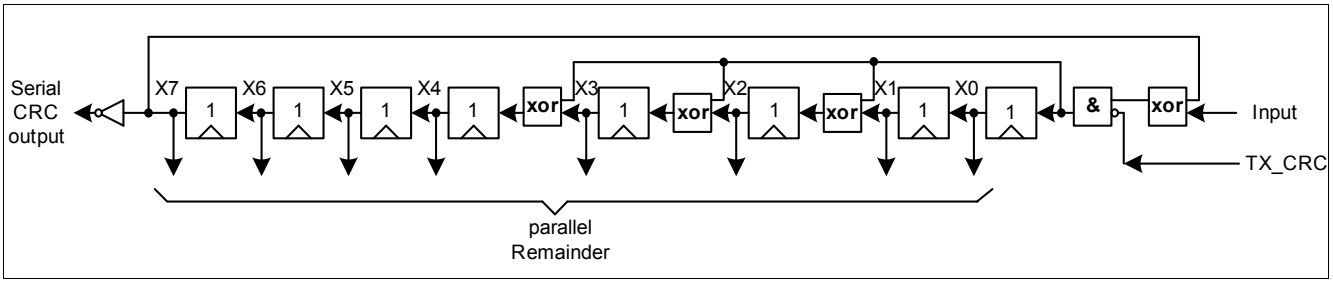

Figure 25 Fast CRC polynomial division circuit

4.4.2 Pulse Width Modulation (PWM) interface

The Pulse Width Modulation (PWM) interface can be selected via SSC (IF_MD = '01').

The PWM update rate can be programmed within the register $0E_H$ (IFAB_RES) in the following steps:

- ~0.25 kHz with 12-bit resolution
- ~0.5 kHz with 12-bit resolution
- ~1.0 kHz with 12-bit resolution
- ~2.0 kHz with 12-bit resolution

PWM uses a square wave with constant frequency whose duty cycle is modulated according to the last measured angle value (AVAL register).

Figure 26 shows the principal behavior of a PWM with various duty cycles and the definition of timing values. The duty cycle of a PWM is defined by the following general formulas:

$$Duty\ Cycle = \frac{t_{on}}{t_{PWM}}$$

$$t_{PWM} = t_{on} + t_{off}$$

$$f_{PWM} = \frac{1}{t_{PWM}} \tag{4.2}$$

The duty cycle range between 0 - 6.25% and 93.75 - 100% is used only for diagnostic purposes. In case the sensor detects an error, the corresponding error bit in the Status register is set and the PWM duty cycle goes to the lower (0 - 6.25%) or upper (93.75 - 100%) diagnostic range, depending on the kind of error (see "Output duty cycle range" in Table 20). Except for an S_ADCT error, an error is only indicated by the corresponding diagnostic duty-cycle as long as it persists, but at least once. However the value in the status register will remain until a read-out via the SSC interface or a chip reset is performed. An S_ADCT error on the other side will be transmitted until the next chip reset. This fail-safe diagnostic function can be disabled via the MOD_4 register.

Sensors with preset PWM are available as TLE5012B E50x0.

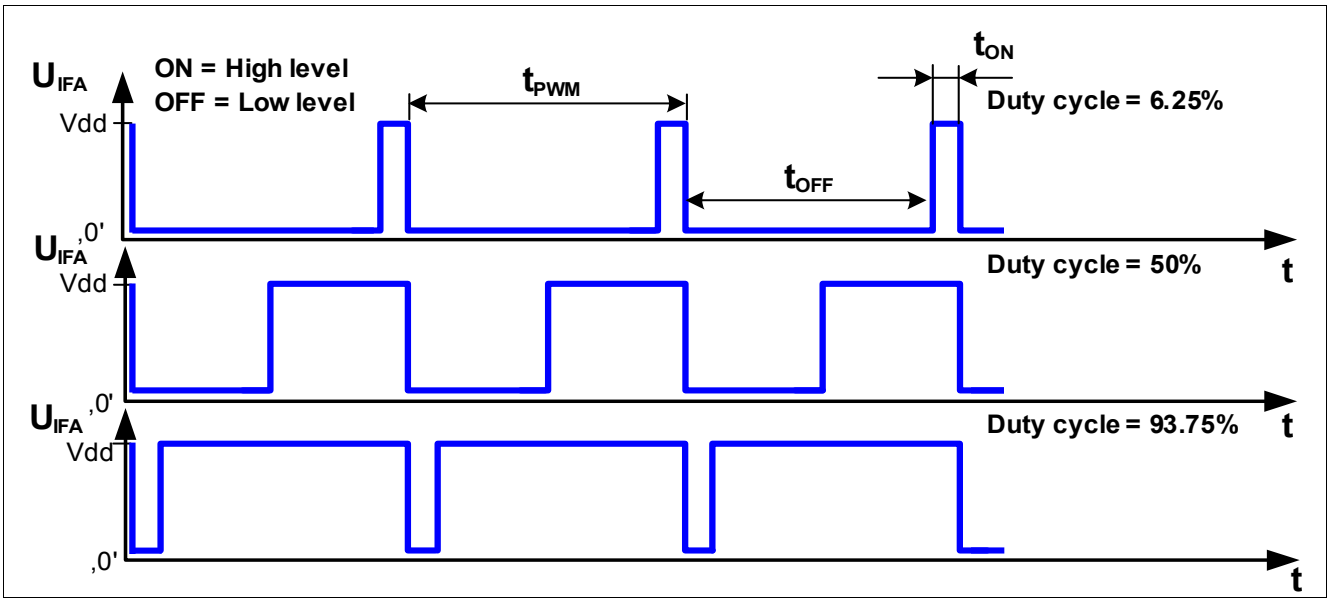

Figure 26 Typical example of a PWM signal

Table 20 PWM interface

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
PWM output frequencies (Selectable by IFAB_RES)	f_{PWM1}	232	244	262	Hz	1)
	f_{PWM2}	464	488	525	Hz	1)
	f_{PWM3}	929	977	1050	Hz	1)
	f_{PWM4}	1855	1953	2099	Hz	1)
Output duty cycle range	DY_{PWM}	6.25		93.75	%	Absolute angle[1)]
			2		%	Electrical Error (S_RST; S_VR)[1)]
			98		%	System error (S_FUSE; S_OV; S_XYOL; S_MAGOL; S_ADCT)[1)]
		0		1	%	Short to GND[1)]
		99		100	%	Short to V_{DD}, power loss[1)]

1) Not subject to production test - verified by design/characterization.

The PWM frequency is derived from the digital clock via:

$$f_{PWM} = \frac{f_{DIG} * 2^{IFAB_RES}}{24 * 4096} \tag{4.3}$$

The min/max values given in Table 20 take into account the internal digital clock variation specified in Chapter 4.3.7. If external clock is used, the variation of the PWM frequency can be derived from the variation of the external clock using Equation (4.3).

4.4.3 Short PWM Code (SPC)

The Short PWM Code (SPC) is a synchronized data transmission based on the SENT protocol (Single Edge Nibble Transmission) defined by SAE J2716. As opposed to SENT, which implies a continuous transmission of data, the SPC protocol transmits data only after receiving a specific trigger pulse from the microcontroller. The required length of the trigger pulse depends on the sensor number, which is configurable. Thereby, SPC allows the operation of up to four sensors on one bus line.

SPC enables the use of enhanced protocol functionality due to the ability to select between various sensor slaves (ID selection). The slave number (S_NR) can be given by the external circuit of SCK and IFC pin. In case of V_{DD} on SCK, the S_NR[0] can be set to 1 and in the case of GND on SCK the S_NR[0] is equal to 0. S_NR[1] can be adjusted in the same way by the IFC pin.

As in SENT, the time between two consecutive falling edges defines the value of a 4-bit nibble, thus representing numbers between 0 and 15. The transmission time therefore depends on the transmitted data values. The single edge is defined by a 3 Unit Time (UT, see Chapter 4.4.3.1) low pulse on the output, followed by the high time defined in the protocol (nominal values, may vary depending on the tolerance of the internal oscillator and the influence of external circuitry). All values are multiples of a unit time frame concept. A transfer consists of the following parts (Figure 27):

- A trigger pulse by the master, which initiates the data transmission
- A synchronization period of 56 UT (in parallel, a new sample is calculated)
- A status nibble of 12-27 UT
- Between 3 and 6 data nibbles of 12-27 UT
- A CRC nibble of 12-27 UT
- An end pulse to terminate the SPC transmission

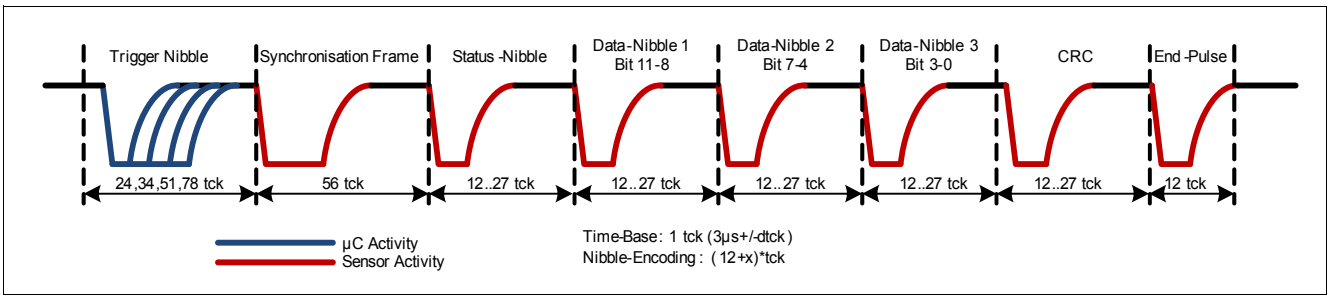

Figure 27 SPC frame example

The CRC checksum includes the status nibble and the data nibbles, and can be used to check the validity of the decoded data. The sensor is available for the next trigger pulse 90 µs after the falling edge of the end pulse (see Figure 28).

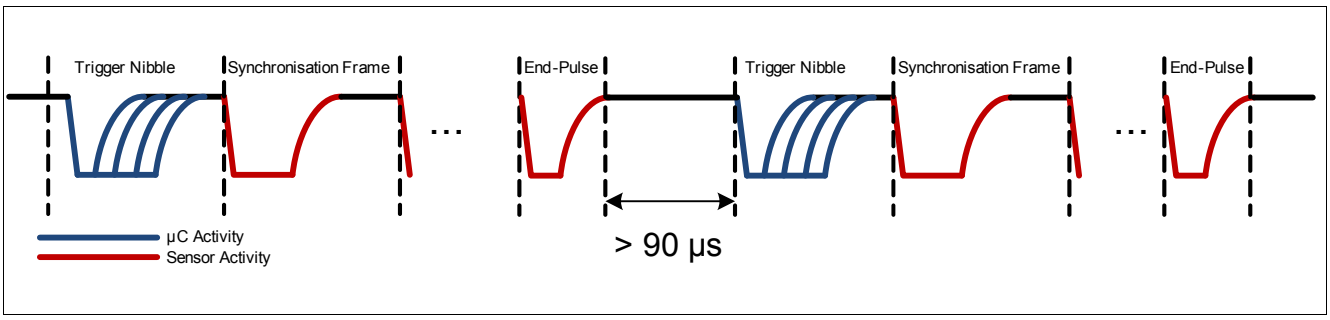

Figure 28 SPC pause timing diagram

In SPC mode, the sensor does not continuously calculate an angle from the raw data. Instead, the angle calculation is started by the trigger nibble from the master. In this mode, the AVAL register, which stores the angle value and can be read via SSC, contains the angle which was calculated after the last SPC trigger nibble.

In parallel to SPC, the SSC interface can be used for individual configuration. The number of transmitted SPC nibbles can be changed to customize the amount of information sent by the sensor. The frame contains a 16-bit angle value and an 8-bit temperature value in the full configuration (Table 21).

Sensors with preset SPC are available as TLE5012B E9000.

Table 21 Frame configuration

Frame type	IFAB_RES	Data nibbles
12-bit angle	00	3 nibbles
16-bit angle	01	4 nibbles
12-bit angle, 8-bit temperature	10	5 nibbles
16-bit angle, 8-bit temperature	11	6 nibbles

The status nibble, which is sent with each SPC data frame, provides an error indication similar to the Safety Word of the SSC protocol. In case the sensor detects an error, the corresponding error bit in the Status register is set and either the bit SYS_ERR or the bit ELEC_ERR of the status nibble will be “high”, depending on the kind of error (see Table 22). Except for an S_ADCT error, an error is only indicated by the corresponding error bit in the status nibble as long as it persists, but at least once. However the value in the status register will remain until a read-out via the SSC interface or a chip reset is performed. An S_ADCT error on the other side will be transmitted until the next chip reset. The fail-safe diagnostic function can be disabled via the MOD_4 register.

Table 22 Structure of status nibble

Name	Bits	Description
SYS_ERR	[3]	Indication of system error (S_FUSE, S_OV, S_XYOL, S_MAGOL, S_ADCT) 0: No system error 1: System error occurred
ELEC_ERR	[2]	Indication of electrical error (S_RST, S_VR) 0: No electrical error 1: Electrical error occurred
S_NR	[1]	Slave number bit 1 (level on IFC)
	[0]	Slave number bit 0 (level on SCK)

4.4.3.1 Unit time setup

The basic SPC protocol unit time granularity is defined as 3 µs. Every timing is a multiple of this basic time unit.To achieve more flexibility, trimming of the unit time can be done within IFAB_HYST. This enables a setup of different unit times.

Table 23 Predivider setting

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Unit time	t_{Unit}		3.0		µs	IFAB_HYST = 00[1)]
			2.5			IFAB_HYST = 01[1)]
			2.0			IFAB_HYST = 10[1)]
			1.5			IFAB_HYST = 11[1)]

1) Not subject to production test - verified by design/characterization.

4.4.3.2 Master trigger pulse requirements

An SPC transmission is initiated by a master trigger pulse on the IFA pin. To detect a low-level on the IFA pin, the voltage must be below a threshold V_{th}. The sensor detects that the IFA line has been released as soon as V_{th} is crossed. Figure 29 shows the timing definitions for the master pulse. The master low time t_{mlow} as well as the total trigger time t_{mtr} are given in Table 24.

If the master low time exceeds the maximum low time, the sensor does not respond and is available for a next triggering 30 µs after the master pulse crosses V_{thr}. $t_{md,tot}$ is the delay between internal triggering of the falling edge in the sensor and the triggering of the ECU.

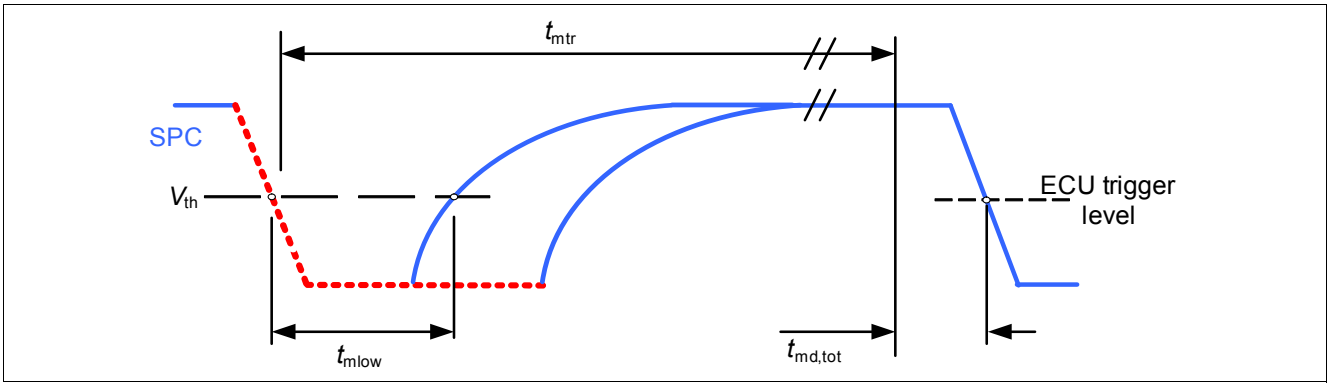

Figure 29 SPC master pulse timing

Table 24 Master pulse parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Threshold	V_{th}		50		% of V_{DD}	1)
Threshold hysteresis	V_{thhyst}		8		% of V_{DD}	V_{DD} = 5 V 1)
			3			V_{DD} = 3 V 1)
Total trigger time	t_{mtr}		90		UT	SPC_Trigger = 0; 1)2)
			t_{mlow} +12		UT	SP_Trigger = 1 1)
Master low time	t_{mlow}	8	12	14	UT	S_NR =00 1)
		16	22	27		S_NR =01 1)
		29	39	48		S_NR =10 1)
		50	66	81		S_NR =11 1)
Master delay time	$t_{md,tot}$		5.8		µs	1)

1) Not subject to production test - verified by design/characterization.
2) Trigger time in the sensor is fixed to the number of units specified in the “Typ.” column, but the effective trigger time varies due to the sensor’s clock variation.

4.4.3.3 Checksum nibble details

The checksum nibble is a 4-bit CRC of the data nibbles including the status nibble. The CRC is calculated using a polynomial $x^4+x^3+x^2+1$ with a seed value of 0101_B. The remainder after the last data nibble is transmitted as CRC.

4.4.4 Hall Switch Mode (HSM)

The Hall Switch Mode (HSM) within the TLE5012B makes it possible to emulate the output of 3 Hall switches. Hall switches are often used in electrical commutated motors to determine the rotor position. With these 3 output signals, the motor will be commutated in the right way. Depending on which pole pairs of the rotor are used, various electrical periods have to be controlled. This is selectable within $0E_H$ (HSM_PLP). Figure 30 depicts the three output signals with the relationship between electrical angle and mechanical angle. The mechanical 0° point is always used as reference.

The HSM is generally used with push-pull output, but it can be changed to open-drain within the register IFAB_OD.

Sensors with preset HSM are available as TLE5012B E3005.

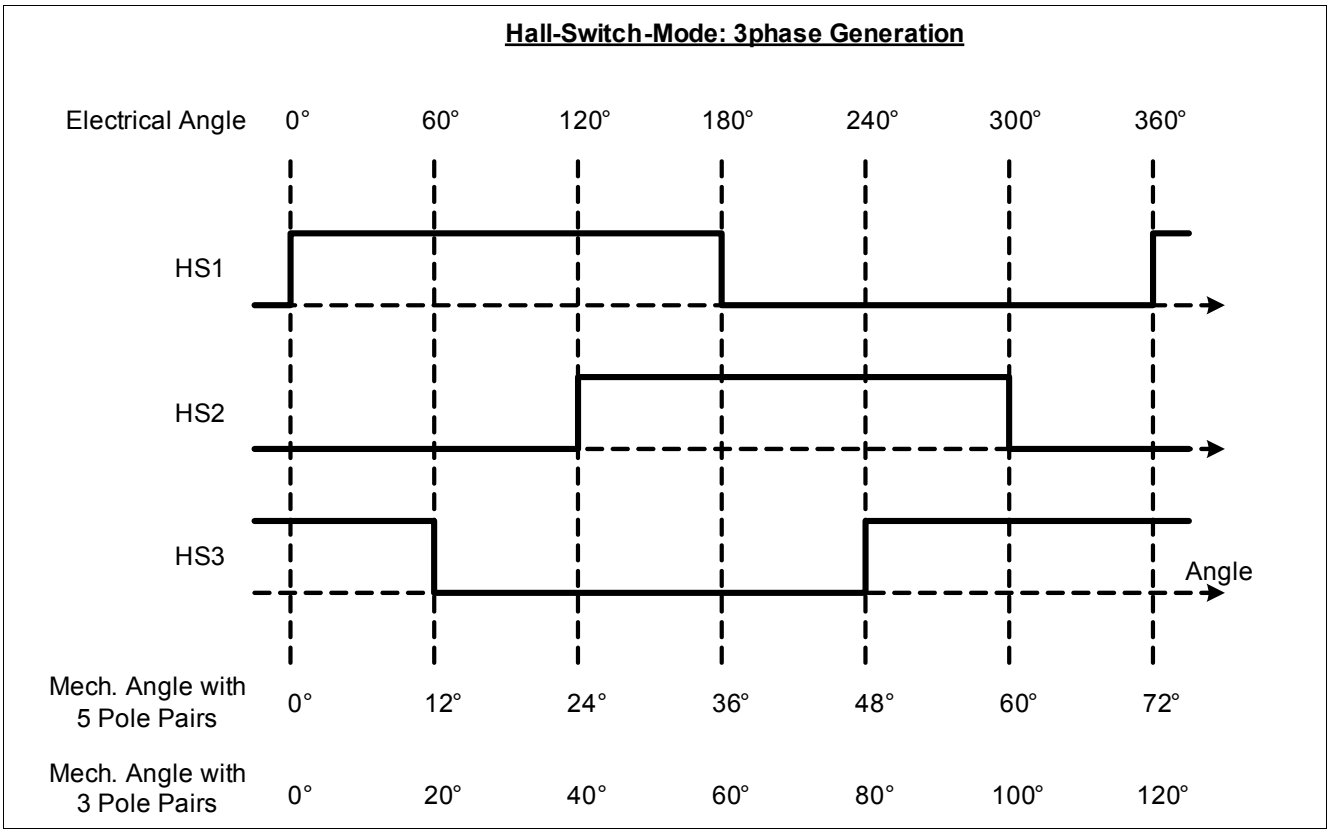

Figure 30 Hall Switch Mode

The HSM Interface can be selected via SSC (IF_MD = 010).

Table 25 Hall Switch Mode

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Rotation speed	*n*			10000	rpm	Mechanical[2)]
Electrical angle accuracy	α_{elect}		0.6	1	°	1 pole pair with autocalibration[1)2)]
			1.2	2	°	2 pole pairs with autocal.[1)2)]
			1.8	3	°	3 pole pairs with autocal.[1)2)]
			2.4	4	°	4 pole pairs with autocal.[1)2)]
			3.0	5	°	5 pole pairs with autocal.[1)2)]
			3.6	6	°	6 pole pairs with autocal.[1)2)]
			4.2	7	°	7 pole pairs with autocal.[1)2)]
			4.8	8	°	8 pole pairs with autocal.[1)2)]
			5.4	9	°	9 pole pairs with autocal.[1)2)]
			6.0	10	°	10 pole pairs with autocal.[1)2)]
			6.6	11	°	11 pole pairs with autocal.[1)2)]
			7.2	12	°	12 pole pairs with autocal.[1)2)]
			7.8	13	°	13 pole pairs with autocal.[1)2)]
			8.4	14	°	14 pole pairs with autocal.[1)2)]
			9.0	15	°	15 pole pairs with autocal.[1)2)]
			9.6	16	°	16 pole pairs with autocal.[1)2)]
Mechanical angle switching hysteresis	$\alpha_{HShystm}$	0		0.703	°	Selectable by IFAB_HYST[2)3)4)]
Electrical angle switching hysteresis[5)]	$\alpha_{HShystel}$		0.70		°	1 pole pair; IFAB_HYST=11[1)2)]
			1.41		°	2 pole pairs; IFAB_HYST=11[1)2)]
			2.11		°	3 pole pairs; IFAB_HYST=11[1)2)]
			2.81		°	4 pole pairs; IFAB_HYST=11[1)2)]
			3.52		°	5 pole pairs; IFAB_HYST=11[1)2)]
			4.22		°	6 pole pairs; IFAB_HYST=11[1)2)]
			4.92		°	7 pole pairs; IFAB_HYST=11[1)2)]
			5.62		°	8 pole pairs; IFAB_HYST=11[1)2)]
			6.33		°	9 pole pairs; IFAB_HYST=11[1)2)]
			7.03		°	10 pole pairs; IFAB_HYST=11[1)2)]
			7.73		°	11 pole pairs; IFAB_HYST=11[1)2)]
			8.44		°	12 pole pairs; IFAB_HYST=11[1)2)]
			9.14		°	13 pole pairs; IFAB_HYST=11[1)2)]
			9.84		°	14 pole pairs; IFAB_HYST=11[1)2)]
			10.55		°	15 pole pairs; IFAB_HYST=11[1)2)]
			11.25		°	16 pole pairs; IFAB_HYST=11[1)2)]

Table 25 Hall Switch Mode (cont'd)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Fall time	t_{HSfall}		0.02	1	µs	R_L = 2.2 kΩ; C_L < 50 pF[2)]
Rise time	t_{HSrise}		0.4	1	µs	R_L = 2.2 kΩ; C_L < 50 pF[2)]

1) Depends on internal oscillator frequency variation (Section 4.3.7).
2) Not subject to production test - verified by design/characterization.
3) GMR hysteresis not considered.
4) Minimum hysteresis without switching.
5) The hysteresis has to be considered only at change of rotation direction.

To avoid switching due to mechanical vibrations of the rotor, an artificial hysteresis is recommended (Figure 31).

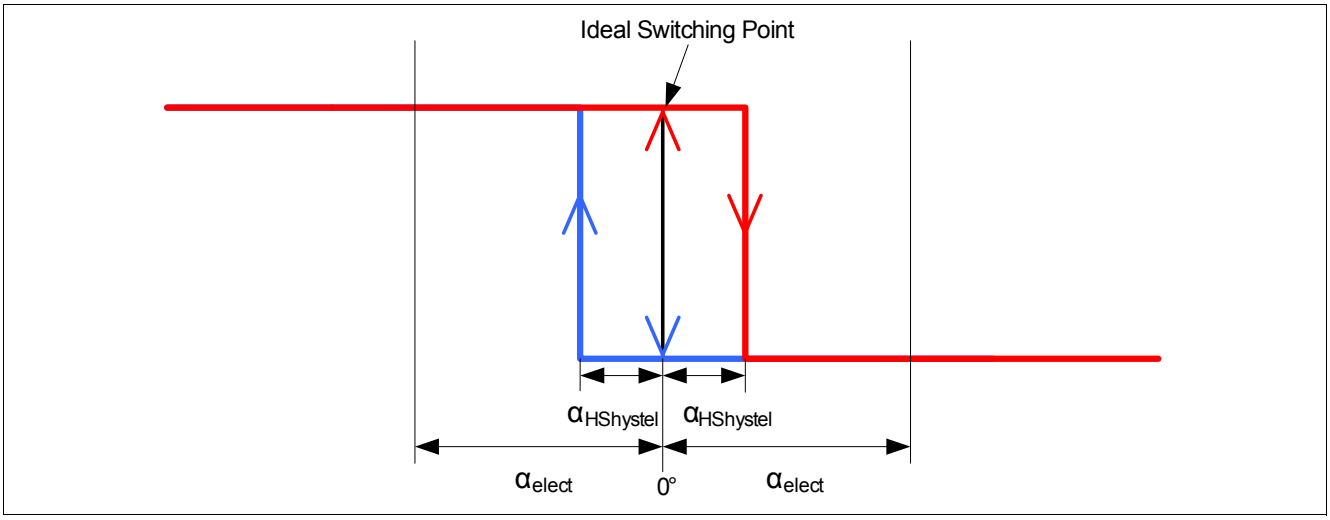

Figure 31 HS hysteresis

4.4.5 Incremental Interface (IIF)

The Incremental Interface (IIF) emulates the operation of an optical quadrature encoder with a 50% duty cycle. It transmits a square pulse per angle step, where the width of the steps can be configured from 9 bit (512 steps per full rotation) to 12 bit (4096 steps per full rotation) within the register MOD_4 (IFAB_RES)[1)]. The rotation direction is given either by the phase shift between the two channels IFA and IFB (A/B mode) or by the level of the IFB channel (Step/Direction mode), as shown in Figure 32 and Figure 33. The incremental interface can be configured for A/B mode or Step/Direction mode in register MOD_1 (IIF_MOD).

Using the Incremental Interface requires an up/down counter on the microcontroller, which counts the pulses and thus keeps track of the absolute position. The counter can be synchronized periodically by using the SSC interface in parallel. The angle value (AVAL register) read out by the SSC interface can be compared to the stored counter value. In case of a non-synchronization, the microcontroller adds the difference to the actual counter value to synchronize the TLE5012B with the microcontroller.

After startup, the IIF transmits a number of pulses which correspond to the actual absolute angle value. Thus, the microcontroller gets the information about the absolute position. The Index Signal that indicates the zero crossing is available on the IFC pin.

Sensors with preset IIF are available as TLE5012B E1000.

1) Decreasing the number of bits does not increase the maximum rotation speed.

A/B Mode

The phase shift between phases A and B indicates either a clockwise (A follows B) or a counterclockwise (B follows A) rotation of the magnet.

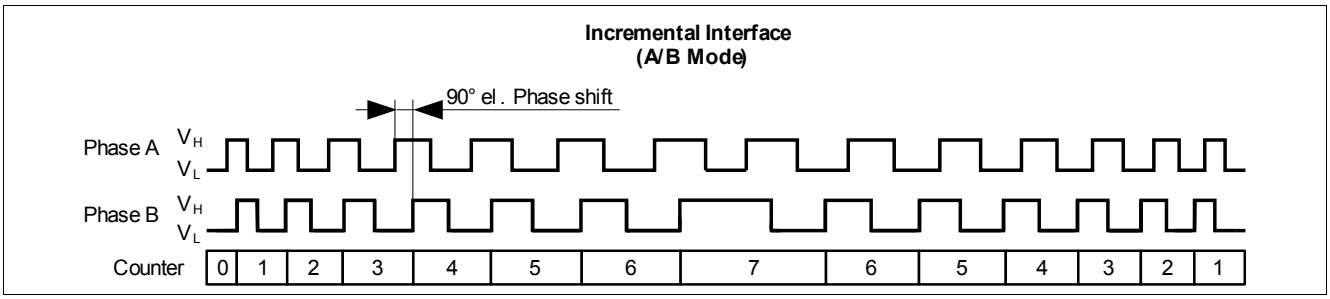

Figure 32 Incremental interface with A/B mode

Step/Direction Mode

Phase A pulses out the increments and phase B indicates the direction.

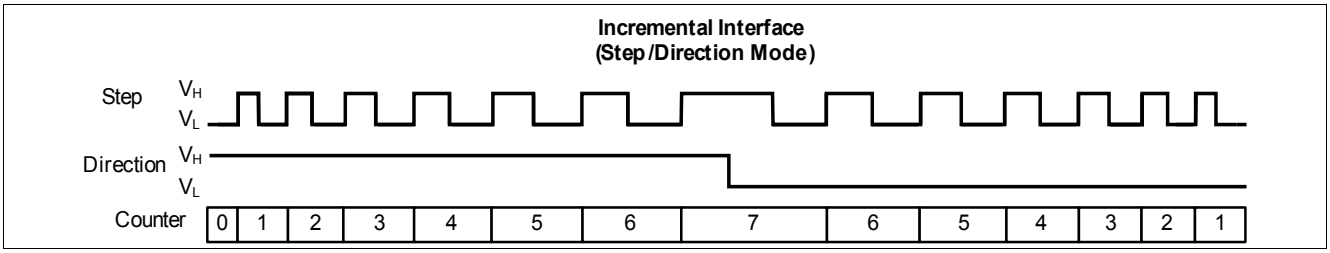

Figure 33 Incremental interface with Step/Direction mode

Table 26 Incremental interface

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Incremental output frequency	f_{Inc}			1.0	MHz	Frequency of phase A and phase B[1)]
Index pulse width	$t_{0°}$		5		µs	0°[1)]

1) Not subject to production test - verified by design/characterization.

4.5 Test mechanisms

4.5.1 ADC test vectors

In order to test the correct functionality of the ADCs, the ADC inputs can be switched from the GMR bridge outputs to a chain of fixed resistors which act as a voltage divider. The ADCs are then fed with test vectors of fixed voltages to simulate a set of magnet positions. The functionality of the ADCs is verified by checking the angle value (AVAL register) for each test vector. This test is activated via SSC command within the SIL register (ADCTV_EN). Registers ADCTV_Y and ADCTV_X are used to select the test vector, as shown in Figure 34.

The following X/Y ADC values can be programmed:

- 4 points, circle amplitude = 70% (0°,90°, 180°, 270°)
- 8 points, circle amplitude = 100% (0°, 45°, 90°, 135°, 180°, 225°, 270°, 315°)
- 8 points, circle amplitude = 122.1% (35.3°, 54.7°, 125.3°, 144.7°, 215.3°, 234.7°, 305.3°, 324.7°)
- 4 points, circle amplitude = 141.4% (45°, 135°, 225°, 315°)

Note: The 100% values typically correspond to 21700 digits and the 70% values to 15500 digits.

Table 27 ADC test vectors

Register bits	X/Y values (decimal)		
	Min.	Typ.	Max.
000		0	
001		15500	
010		21700	
011		32767	
100[1)]		0	
101		-15500	
110		-21700	
111		-32768	

1) Not allowed to use.

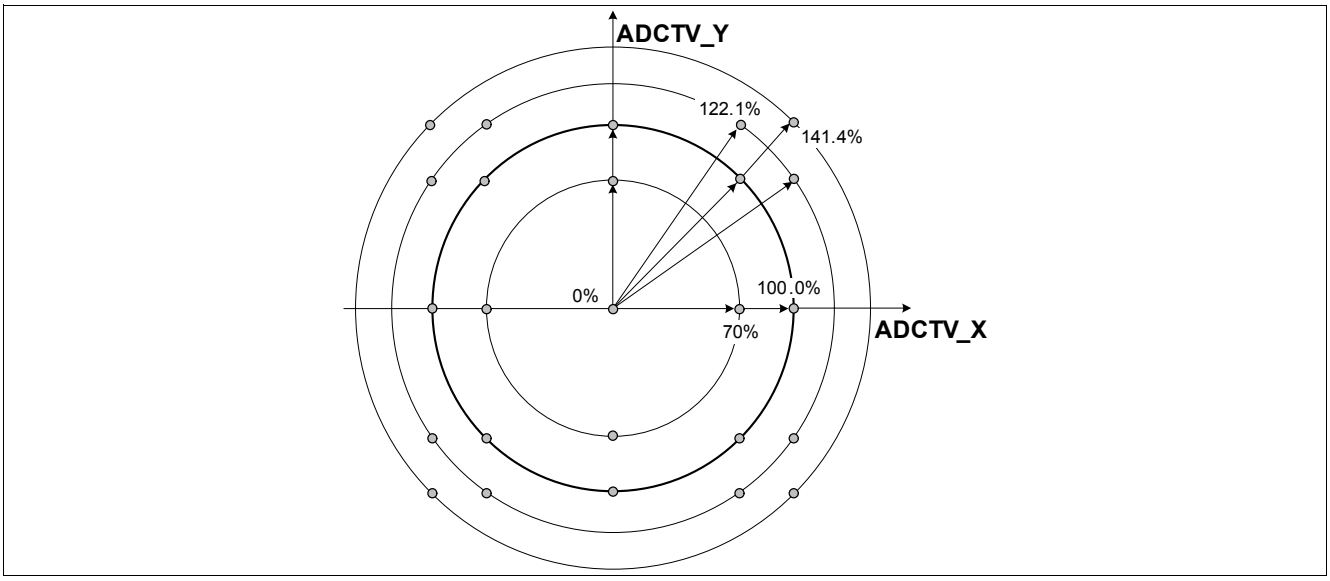

Figure 34 ADC test vectors

4.6 Supply monitoring

The internal voltage nodes of the TLE5012B are monitored by a set of comparators in order to ensure error-free operation. An over- or undervoltage condition must be active at least 256 periods of the digital clock to set the corresponding error bits in the Status register. This works as digital spike suppression.

Over- or undervoltage errors trigger the S_VR bit of Status register. This error condition is signaled via the in the Safety Word of the SSC protocol, the status nibble of the SPC interface or the lower diagnostic range of the PWM interface.

Table 28 Test comparator threshold voltages

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Overvoltage detection	V_{OVG}		2.80		V	1)
	V_{OVA}		2.80		V	1)
	V_{OVD}		2.80		V	1)
V_{DD} overvoltage	V_{DDOV}		6.05		V	1)
V_{DD} undervoltage	V_{DDUV}		2.70		V	1)
GND - off voltage	V_{GNDoff}		-0.55		V	1)
V_{DD} - off voltage	V_{VDDoff}		0.55		V	1)
Spike filter delay	t_{DEL}		10		µs	1)

1) Not subject to production test - verified by design/characterization

4.6.1 Internal supply voltage comparators

Every voltage regulator has an overvoltage (OV) comparator to detect malfunctions. If the nominal output voltage of 2.5 V is larger than V_{OVG}, V_{OVA} and V_{OVD}, then this overvoltage comparator is activated.

4.6.2 V_{DD} overvoltage detection

The overvoltage detection comparator monitors the external supply voltage at the VDD pin.

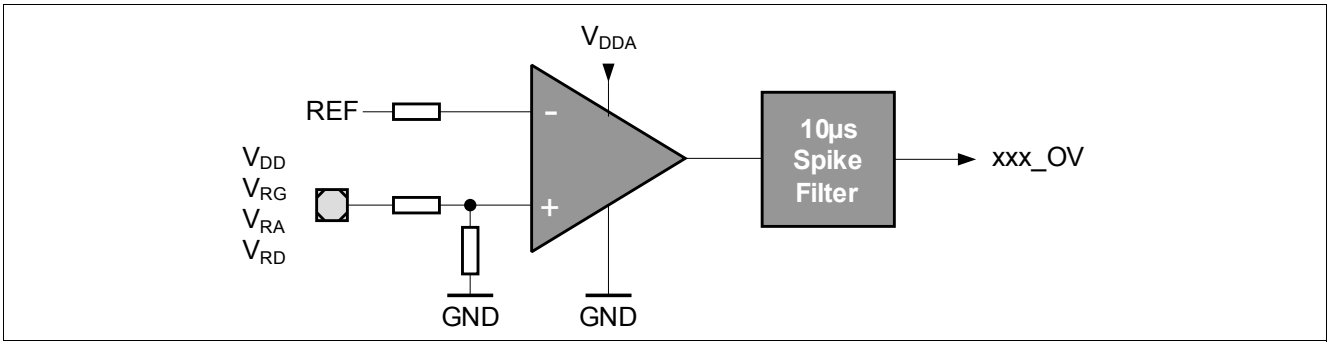

Figure 35 Overvoltage comparator

4.6.3 GND - Off comparator

The GND - Off comparator is used to detect a voltage difference between the GND pin and SCK. This circuit can detect a disconnection of the supply GND pin.

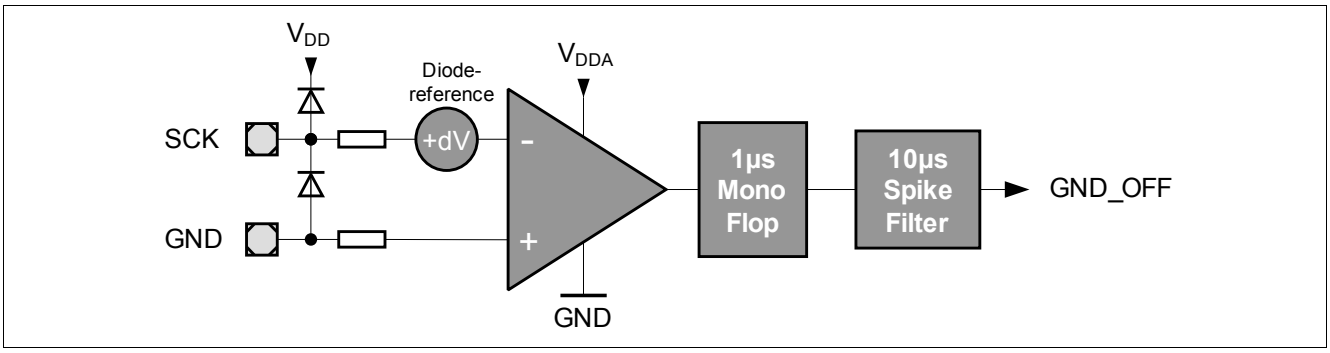

Figure 36 GND - Off comparator

4.6.4 V_{DD} - Off comparator

The V_{DD} - Off comparator detects a disconnection of the VDD pin supply voltage. In this case, the TLE5012B is supplied by the SCK and CSQ input pins via the ESD structures.

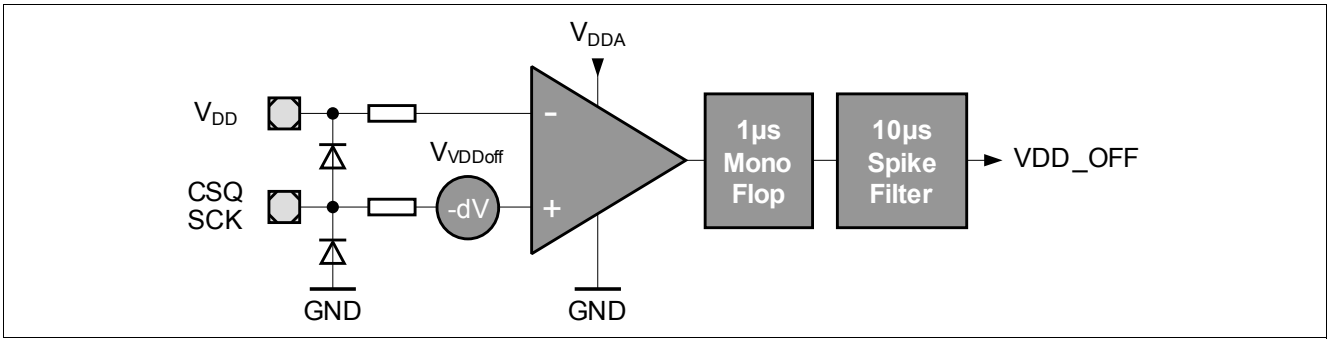

Figure 37 V_{DD} - Off comparator

5 Pre-configured derivates

Derivates of the TLE5012B are available with different pre-configured register settings for specific applications. The configuration of all derivates can be changed via SSC interface.

5.1 IIF-type: E1000

The TLE5012B-E1000 is preconfigured for Incremental Interface and fast angle update period (42.7 µs). It is most suitable for BLDC motor commutation.

- Autocalibration mode 1 enabled.
- Prediction enabled.
- Hysteresis is set to 0.703°.
- 12bit mode, one count per 0.088° angle step.
- Incremental Interface A/B mode.

5.2 HSM-type: E3005

The TLE5012B-E3005 is preconfigured for Hall-Switch-Mode and fast angle update period (42.7 µs). It is most suitable as a replacement for three Hall switches for BLDC motor commutation.

- Number of pole pairs is set to 5.
- Autocalibration mode 1 enabled.
- Prediction enabled.
- Hysteresis is set to 0.703°.

5.3 PWM-type: E5000

The TLE5012B-E5000 is preconfigured for Pulse-Width-Modulation interface. It is most suitable for steering angle and actuator position sensing.

- Filter update period is 85.4 µs.
- PWM frequency is 244 Hz.
- Autocalibration, Prediction, and Hysteresis are disabled.

5.4 PWM-type: E5020

The TLE5012B-E5020 is preconfigured for Pulse-Width-Modulation interface with high frequency. It is most suitable for steering angle and actuator position sensing.

- Filter update period is 42.7 µs.
- PWM frequency is 1953 Hz.
- Autocalibration mode 2 enabled.
- Prediction and Hysteresis are disabled.
- PWM interface is set to open-drain output.

5.5 SPC-type: E9000

The TLE5012B-E9000 is preconfigured for Short-PWM-Code interface. It is most suitable for steering angle and actuator position sensing.

- Filter update period is 85.4 µs.
- Autocalibration, Prediction, and Hysteresis are disabled.
- SPC unit time is 3 µs.
- SPC interface is set to open-drain output.

6 Package information

6.1 Package parameters

Table 29 Package parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Thermal resistance	R_{thJA}		150	200	K/W	Junction to air[1)]
	R_{thJC}			75	K/W	Junction to case
	R_{thJL}			85	K/W	Junction to lead
Soldering moisture level	MSL 3					260°C
Lead Frame	Cu					
Plating	Sn 100%					> 7 µm

1) according to Jedec JESD51-7

6.2 Package outline

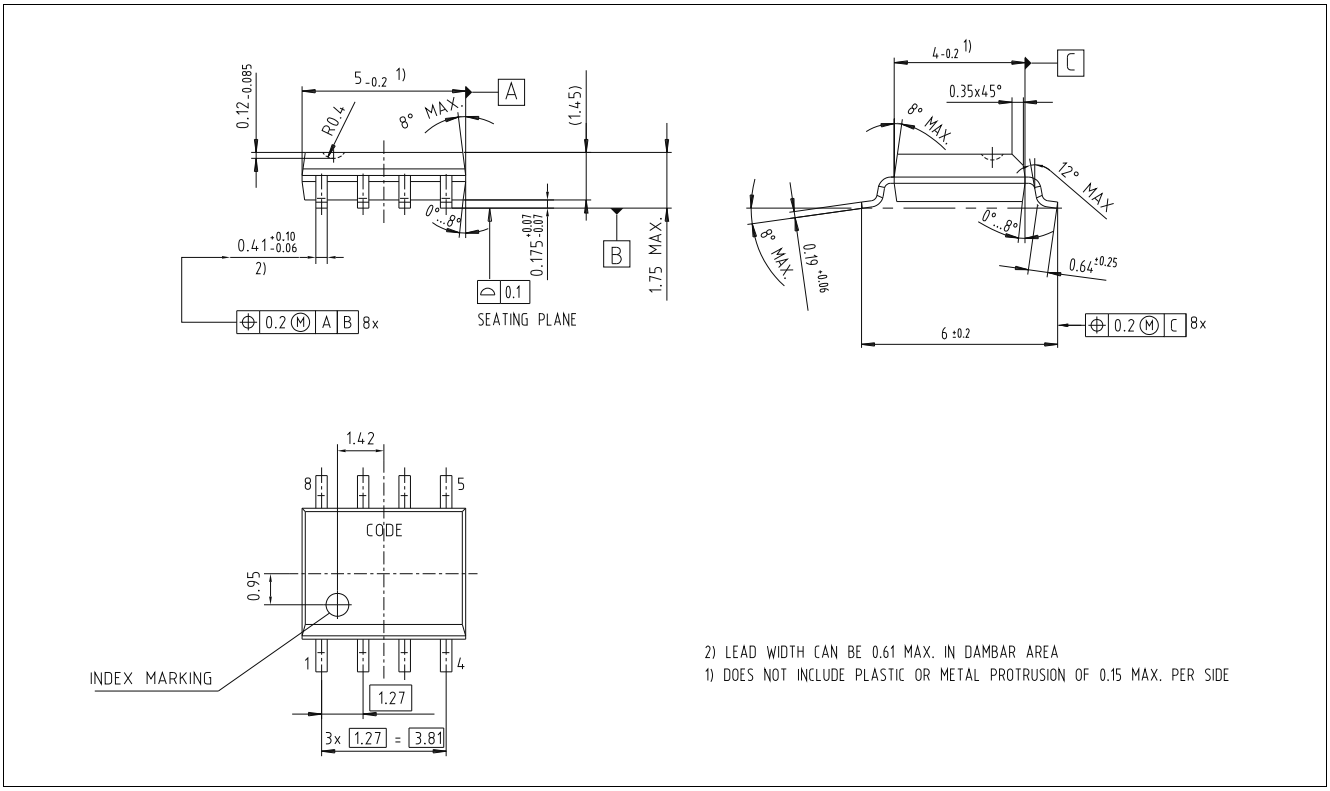

Figure 38 PG-DSO-8 package dimension

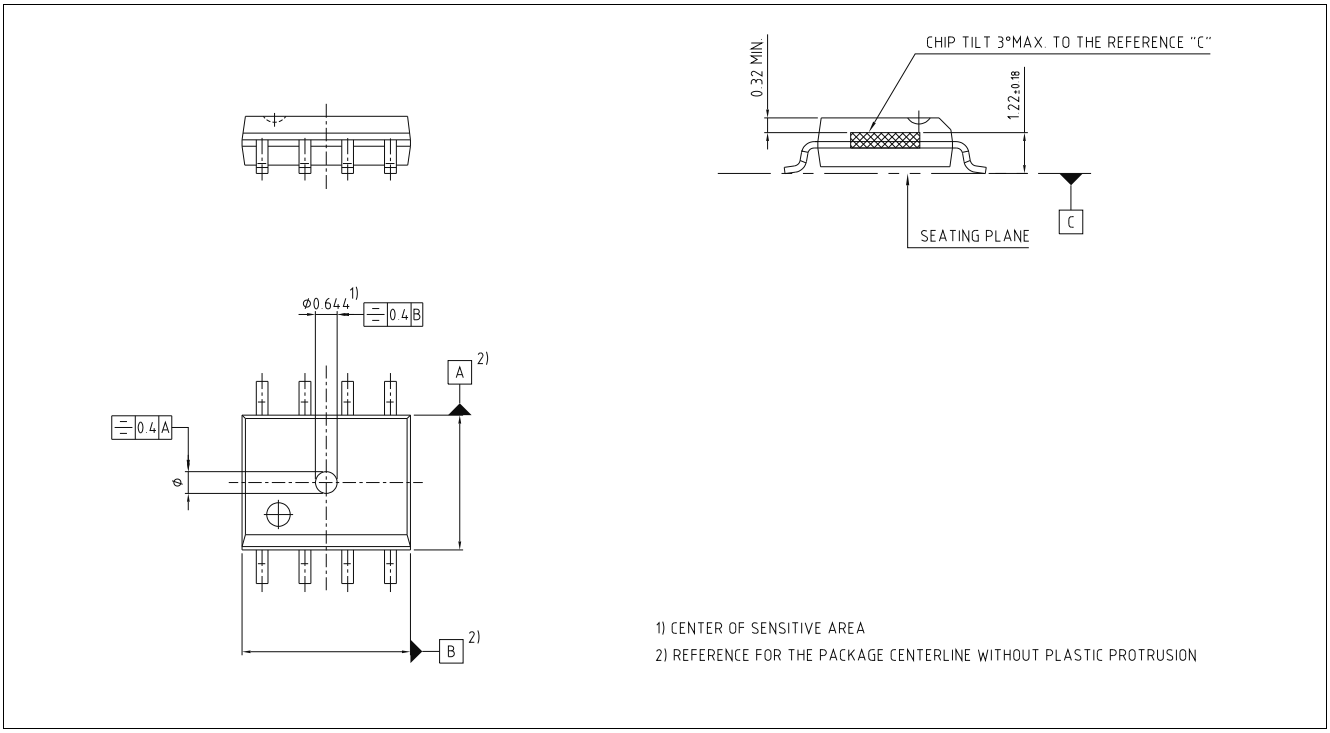

Figure 39 Position of sensing element

Table 30 Sensor IC placement tolerances in package

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Position eccentricity		-200		200	µm	In X- and Y-direction
Rotation		-3		3	°	Affects zero position offset of sensor
Tilt		-3		3	°	

6.3 Footprint

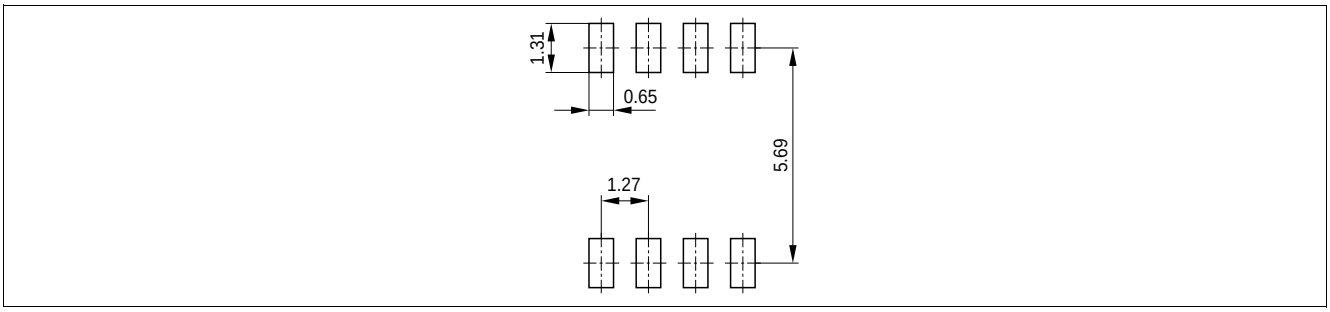

Figure 40 Footprint of PG-DSO-8

6.4 Packing

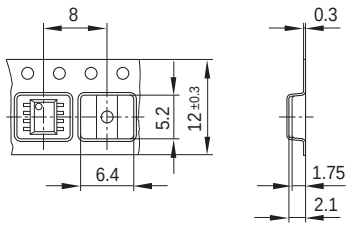

Figure 41 Tape and Reel

6.5 Marking

Position	Marking	Description
1st Line	012Bxxxx	See Table 1 “Derivate ordering codes” on Page 2
2nd Line	xxx	Lot code
3rd Line	Gxxxx	G..green, 4-digit..date code

Processing

Note: For processing recommendations, please refer to Infineon’s Notes on processing

7 Revision history

Revision	Date	Changes
Rev. 2.1	2018-06-20	New Template/New Logo Chapter 4.4.5: Add footnote regarding maximum rotation speed Chapter 3: Update Chapter 3

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