# DRAM MODULE

MT8D432(X)
MT16D832(X)

## FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single in-line memory module (SIMM)
- 16MB (4 Meg x 32) and 32MB (8 Meg x 32)
- High-performance CMOS silicon-gate process
- Single 5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) operating mode or Extended Data-Out (EDO) PAGE MODE operating mode

## OPTIONS — MARKING

- Timing
  - 50ns access — -5*
  - 60ns access — -6
- Packages
  - 72-pin SIMM — M
  - 72-pin SIMM (gold) — G
- Operating Modes
  - FAST PAGE MODE — Blank
  - EDO PAGE MODE — X

*EDO version only

## PART NUMBERS

EDO Operating Mode

| PART NUMBER | CONFIGURATION | PLATING |
|---|---|---|
| MT8D432G- xx X | 4 Meg x 32 | Gold |
| MT8D432M- xx X | 4 Meg x 32 | Tin/Lead |
| MT16D832G-xx X | 8 Meg x 32 | Gold |
| MT16D832M-xx X | 8 Meg x 32 | Tin/Lead |

xx = speed

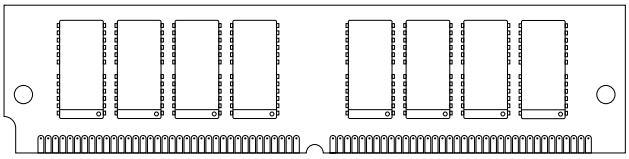
FPM Operating Mode

| PART NUMBER | CONFIGURATION | PLATING |
|---|---|---|
| MT8D432G-xx | 4 Meg x 32 | Gold |
| MT8D432M-xx | 4 Meg x 32 | Tin/Lead |
| MT16D832G-xx | 8 Meg x 32 | Gold |
| MT16D832M-xx | 8 Meg x 32 | Tin/Lead |

xx = speed

## PIN ASSIGNMENT (Front View)

**72-Pin SIMM**
(DD-3) 4 Meg x 32
(DD-4) 8 Meg x 32



| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|---|---|---|---|---|---|---|---|
| 1 | Vss | 19 | A10 | 37 | NC | 55 | DQ12 |
| 2 | DQ1 | 20 | DQ5 | 38 | NC | 56 | DQ28 |
| 3 | DQ17 | 21 | DQ21 | 39 | Vss | 57 | DQ13 |
| 4 | DQ2 | 22 | DQ6 | 40 | CAS0# | 58 | DQ29 |
| 5 | DQ18 | 23 | DQ22 | 41 | CAS2# | 59 | Vcc |
| 6 | DQ3 | 24 | DQ7 | 42 | CAS3# | 60 | DQ30 |
| 7 | DQ19 | 25 | DQ23 | 43 | CAS1 | 61 | DQ14 |
| 8 | DQ4 | 26 | DQ8 | 44 | RAS0# | 62 | DQ31 |
| 9 | DQ20 | 27 | DQ24 | 45 | NC/RAS1#* | 63 | DQ15 |
| 10 | Vcc | 28 | A7 | 46 | NC | 64 | DQ32 |
| 11 | NC | 29 | NC (A11) | 47 | WE# | 65 | DQ16 |
| 12 | A0 | 30 | Vcc | 48 | NC | 66 | NC |
| 13 | A1 | 31 | A8 | 49 | DQ9 | 67 | PRD1 |
| 14 | A2 | 32 | A9 | 50 | DQ25 | 68 | PRD2 |
| 15 | A3 | 33 | NC/RAS3#* | 51 | DQ10 | 69 | PRD3 |
| 16 | A4 | 34 | RAS2# | 52 | DQ26 | 70 | PRD4 |
| 17 | A5 | 35 | NC | 53 | DQ11 | 71 | NC |
| 18 | A6 | 36 | NC | 54 | DQ27 | 72 | Vss |

*32MB version only

**NOTE:** Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

## KEY TIMING PARAMETERS

EDO Operating Mode

| SPEED | $^tRC$ | $^tRAC$ | $^tPC$ | $^tAA$ | $^tCAC$ | $^tCAS$ |
|---|---|---|---|---|---|---|
| -5 | 84ns | 50ns | 20ns | 25ns | 13ns | 8ns |
| -6 | 104ns | 60ns | 25ns | 30ns | 15ns | 10ns |

FPM Operating Mode

| SPEED | $^tRC$ | $^tRAC$ | $^tPC$ | $^tAA$ | $^tCAC$ | $^tRP$ |
|---|---|---|---|---|---|---|
| -6 | 110ns | 60ns | 35ns | 30ns | 15ns | 40ns |

## GENERAL DESCRIPTION

The MT8D432(X) and MT16D832(X) are randomly accessed 16MB and 32MB solid-state memories organized in a x32 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS# is used to latch the first 11 bits and CAS# the latter 11 bits. READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS#. Since WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

## FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

## EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time ($^{t}$CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates like FAST-PAGE-MODE READs, except data will be held valid or become valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW. (Reference MT4C4M4E8 DRAM data sheet for additional information on EDO functionality.)

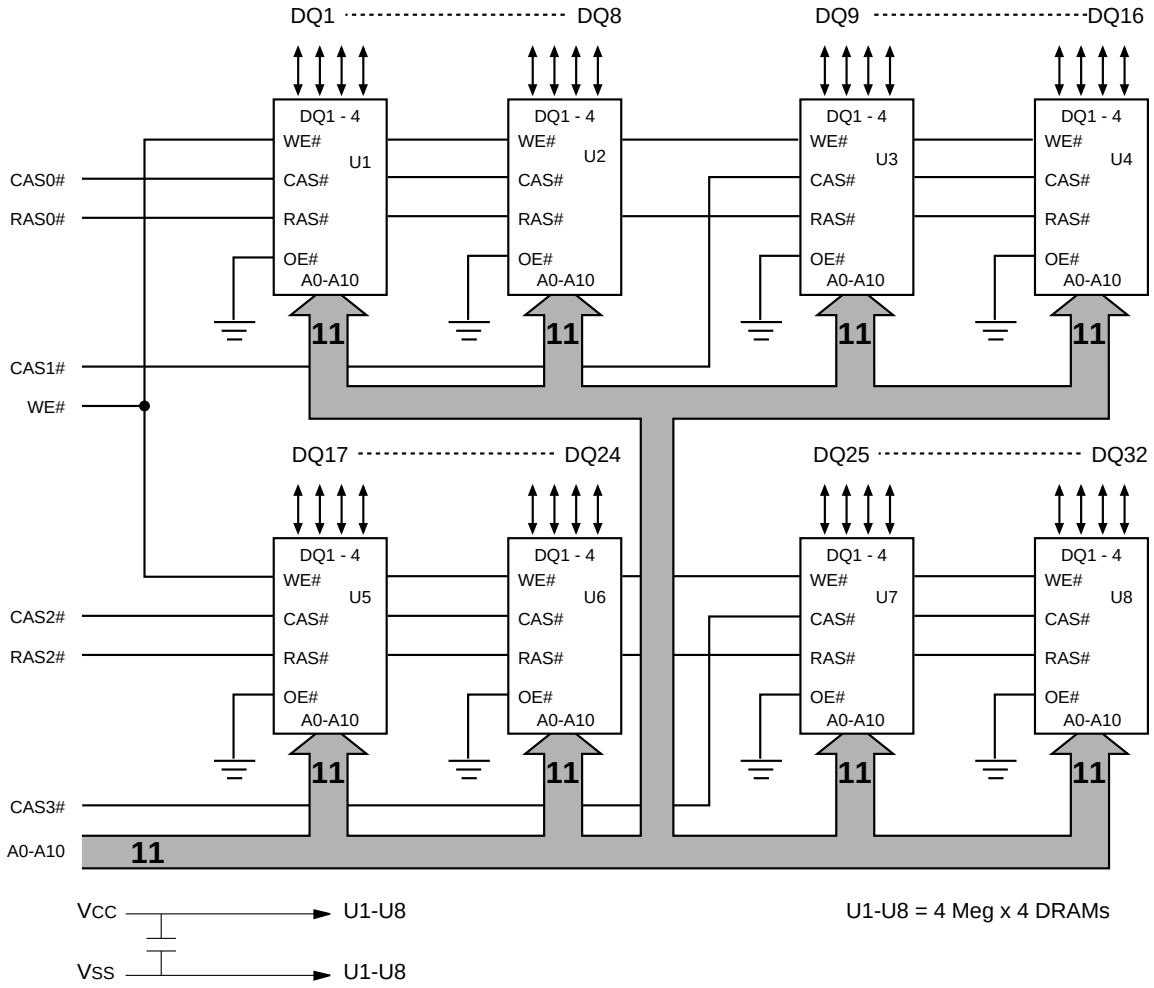
## REFRESH

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS# addressing.

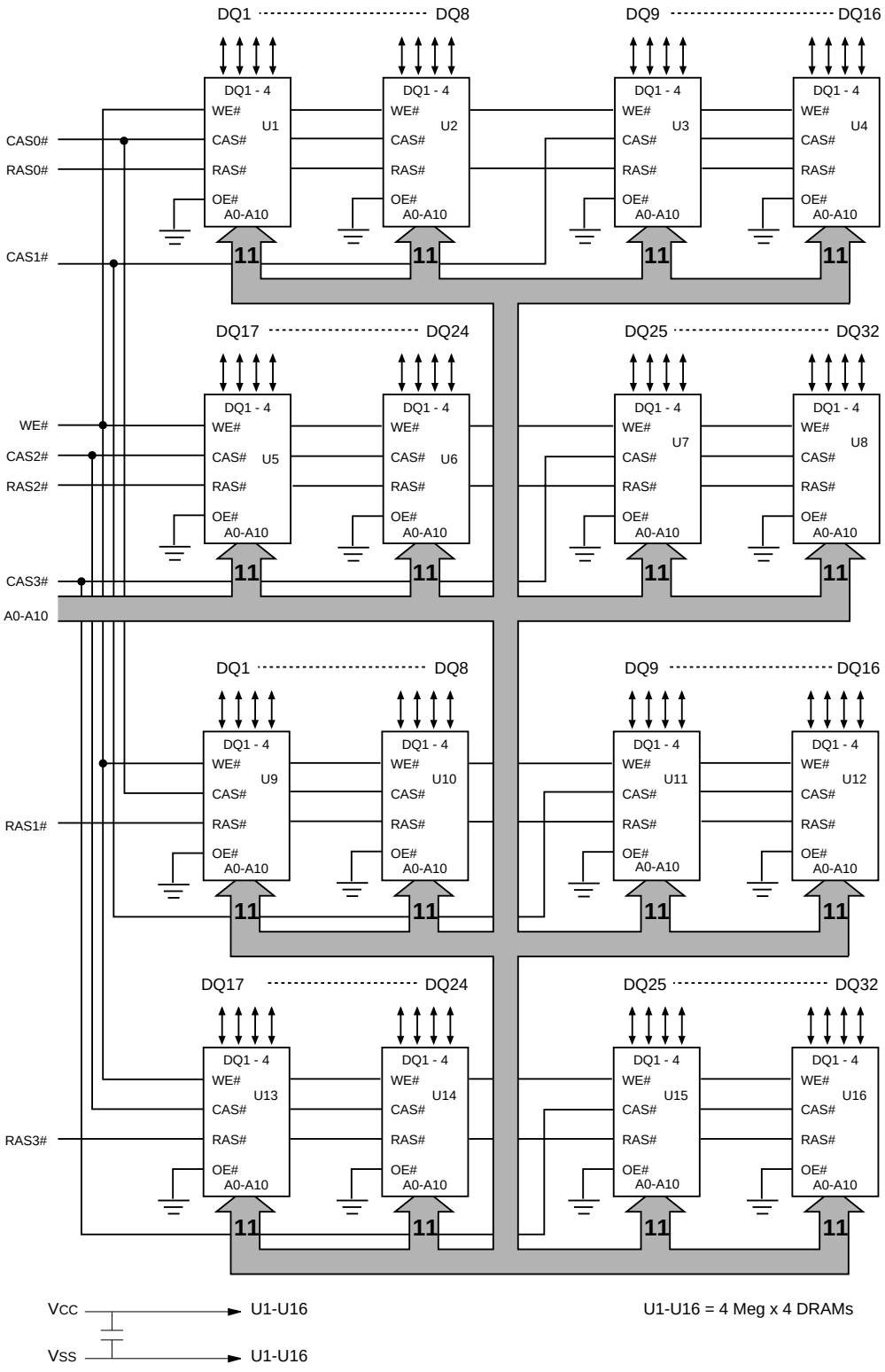
## x16 CONFIGURATION

For x16 applications, the corresponding DQ and CAS# pins must be connected together (DQ1 to DQ17, DQ2 to DQ18 and so forth, and CAS0# to CAS2# and CAS1# to CAS3#). Each RAS# is then a bank select for the x16 memory organization.

## FUNCTIONAL BLOCK DIAGRAM
## MT8D432(X) (16MB)



## FUNCTIONAL BLOCK DIAGRAM
## MT16D832(X) (32MB)



## TRUTH TABLE

| FUNCTION | | RAS# | CAS# | WE# | ADDRESSES | | DATA-IN/OUT |
|---|---|---|---|---|---|---|---|
| | | | | | $^tR$ | $^tC$ | DQ1-DQ32 |
| Standby | | H | H→X | X | X | X | High-Z |
| READ | | L | L | H | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | ROW | COL | Data-In |
| EDO/FAST-PAGE- | 1st Cycle | L | H→L | H | ROW | COL | Data-Out |
| MODE READ | 2nd Cycle | L | H→L | H | n/a | COL | Data-Out |
| EDO/FAST-PAGE- | 1st Cycle | L | H→L | L | ROW | COL | Data-In |
| MODE EARLY-WRITE | 2nd Cycle | L | H→L | L | n/a | COL | Data-In |
| | Any Cycle (X version) | L | L→H | H | n/a | n/a | Data-Out |
| RAS#-ONLY REFRESH | | L | H | X | ROW | n/a | High-Z |
| HIDDEN | READ | L→H→L | L | H | ROW | COL | Data-Out |
| REFRESH | WRITE | L→H→L | L | L | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | High-Z |

## JEDEC-DEFINED PRESENCE-DETECT – MT8D432(X) (16MB)

| SYMBOL | PIN | -5* | -6 |
|---|---|---|---|
| PRD1 | 67 | Vss | Vss |
| PRD2 | 68 | NC | NC |
| PRD3 | 69 | Vss | NC |
| PRD4 | 70 | Vss | NC |

## JEDEC-DEFINED PRESENCE-DETECT – MT16D832(X) (32MB)

| SYMBOL | PIN | -5* | -6 |
|---|---|---|---|
| PRD1 | 67 | NC | NC |
| PRD2 | 68 | Vss | Vss |
| PRD3 | 69 | Vss | NC |
| PRD4 | 70 | Vss | NC |

*EDO version only

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to $V_{SS}$ ..... -1V to +7V
Operating Temperature, $T_A$ (ambient) ..... 0°C to +70°C
Storage Temperature (plastic)..... -55°C to +125°C
Power Dissipation ..... 8W
Short Circuit Output Current ..... 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) ($V_{CC}$ = +5V ±10%)

| PARAMETER/CONDITION | | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | 4.5 | 5.5 | V | |
| Input High (Logic 1) Voltage, all inputs | | $V_{IH}$ | 2.0 | 5.5 | V | |
| Input Low (Logic 0) Voltage, all inputs | | $V_{IL}$ | -1.0 | 0.8 | V | |
| INPUT LEAKAGE CURRENT | RAS0#-RAS3# | $I_{I1}$ | -8 | 8 | µA | |
| Any input 0V ≤ $V_{IN}$ ≤ 5.5V | A0-A10, WE# | $I_{I2}$ | -32 | 32 | µA | 23 |
| (All other pins not under test = 0V) | CAS0#-CAS3# | $I_{I3}$ | -8 | 8 | µA | 23 |
| OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ $V_{OUT}$ ≤ 5.5V) | DQ1-DQ32 | $I_{OZ}$ | -10 | 10 | µA | 23 |
| OUTPUT LEVELS | | $V_{OH}$ | 2.4 | | V | |
| Output High Voltage ($I_{OUT}$ = -5mA) | | | | | | |
| Output Low Voltage ($I_{OUT}$ = 4.2mA) | | $V_{OL}$ | | 0.4 | V | |

## $I_{CC}$ OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 5, 6) ($V_{CC}$ = +5V ±10%)

| | | | MAX | | | |
|---|---|---|---|---|---|---|
| **PARAMETER/CONDITION** | **SYMBOL** | **SIZE** | **-5*** | **-6** | **UNITS** | **NOTES** |
| STANDBY CURRENT: (TTL)<br>(RAS# = CAS# = $V_{IH}$) | $I_{CC1}$ | 16MB<br>32MB | 18<br>36 | 18<br>36 | mA | |
| STANDBY CURRENT: (CMOS)<br>(RAS# = CAS# = other inputs = $V_{CC}$ -0.2V) | $I_{CC2}$ | 16MB<br>32MB | 14<br>28 | 14<br>28 | mA | |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC3}$ | 16MB<br>32MB | 880<br>898 | 800<br>818 | mA | 3, 22 |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>(RAS# = $V_{IL}$, CAS#, address cycling: $^tPC$ = $^tPC$ [MIN] | $I_{CC4}$ | 16MB<br>32MB | -<br>- | 640<br>666 | mA | 3, 22 |
| OPERATING CURRENT: EDO PAGE MODE<br>Average power supply current<br>(RAS# = $V_{IL}$, CAS#, address cycling: $^tPC$ = $^tPC$ [MIN]) | $I_{CC5}$<br>(X only) | 16MB<br>32MB | 880<br>898 | 800<br>818 | mA | 3, 22 |
| REFRESH CURRENT: RAS#-ONLY<br>Average power supply current<br>(RAS# cycling, CAS# = $V_{IH}$: $^tRC$ = $^tRC$ [MIN]) | $I_{CC6}$ | 16MB<br>32MB | 880<br>898 | 800<br>818 | mA | 3, 22 |
| REFRESH CURRENT: CBR<br>Average power supply current<br>(RAS#, CAS#, address cycling: $^tRC$ = $^tRC$ [MIN]) | $I_{CC7}$ | 16MB<br>32MB | 880<br>898 | 800<br>818 | mA | 3, 4 |

*EDO version only

## CAPACITANCE

| | | MAX | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **16MB** | **32MB** | **UNITS** | **NOTES** |
| Input Capacitance: A0-A10 | $C_{I1}$ | 48 | 95 | pF | 2 |
| Input Capacitance: WE# | $C_{I2}$ | 64 | 127 | pF | 2 |
| Input Capacitance: RAS0# - RAS3# | $C_{I3}$ | 32 | 32 | pF | 2 |
| Input Capacitance: CAS0# - CAS3# | $C_{I4}$ | 16 | 32 | pF | 2 |
| Input/Output Capacitance: DQ1-DQ32 | $C_{IO}$ | 10 | 16 | pF | 2 |

## FAST PAGE MODE
## AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC}$ = +5V ±10%)

| AC CHARACTERISTICS - FAST PAGE MODE OPTION | | -6 | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Access time from column address | $^tAA$ | | 30 | ns | |
| Column-address hold time (referenced to RAS#) | $^tAR$ | 45 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | ns | |
| Row-address setup time | $^tASR$ | 0 | | ns | |
| Access time from CAS# | $^tCAC$ | | 15 | ns | |
| Column-address hold time | $^tCAH$ | 10 | | ns | |
| CAS# pulse width | $^tCAS$ | 15 | 10,000 | ns | |
| CAS# hold time (CBR REFRESH) | $^tCHR$ | 10 | | ns | 4 |
| CAS# to output in Low-Z | $^tCLZ$ | 3 | | ns | 21 |
| CAS# precharge time | $^tCP$ | 10 | | ns | 13 |
| Access time from CAS# precharge | $^tCPA$ | | 35 | ns | |
| CAS# to RAS# precharge time | $^tCRP$ | 5 | | ns | |
| CAS# hold time | $^tCSH$ | 60 | | ns | |
| CAS# setup time (CBR REFRESH) | $^tCSR$ | 5 | | ns | 4 |
| Write command to CAS# lead time | $^tCWL$ | 15 | | ns | |
| Data-in hold time | $^tDH$ | 10 | | ns | 18 |
| Data-in setup time | $^tDS$ | 0 | | ns | 18 |
| Output buffer turn-off delay | $^tOFF$ | 3 | 15 | ns | 17, 21 |
| FAST-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 35 | | ns | |
| Access time from RAS# | $^tRAC$ | | 60 | ns | |
| RAS# to column-address delay time | $^tRAD$ | 15 | | ns | 15 |
| Row-address hold time | $^tRAH$ | 10 | | ns | |
| RAS# pulse width | $^tRAS$ | 60 | 10,000 | ns | |
| RAS# pulse width (FAST PAGE MODE) | $^tRASP$ | 60 | 125,000 | ns | |
| Random READ or WRITE cycle time | $^tRC$ | 110 | | ns | |
| RAS# to CAS# delay time | $^tRCD$ | 20 | | ns | 14 |
| Read command hold time (referenced to CAS#) | $^tRCH$ | 0 | | ns | 16 |
| Read command setup time | $^tRCS$ | 0 | | ns | |
| Refresh period (2,048 cycles) | $^tREF$ | | 32 | ms | |
| RAS# precharge time | $^tRP$ | 40 | | ns | |
| RAS# to CAS# precharge time | $^tRPC$ | 0 | | ns | |
| Read command hold time (referenced to RAS#) | $^tRRH$ | 0 | | ns | 16 |
| RAS# hold time | $^tRSH$ | 15 | | ns | |
| Write command to RAS# lead time | $^tRWL$ | 15 | | ns | |
| Transition time (rise or fall) | $^tT$ | 2 | 50 | ns | |
| Write command hold time | $^tWCH$ | 10 | | ns | |
| Write command hold time (referenced to RAS#) | $^tWCR$ | 45 | | ns | |
| WE# command setup time | $^tWCS$ | 0 | | ns | |
| Write command pulse width | $^tWP$ | 10 | | ns | |
| WE# hold time (CBR REFRESH) | $^tWRH$ | 10 | | ns | |
| WE# setup time (CBR REFRESH) | $^tWRP$ | 10 | | ns | |

## EDO PAGE MODE
## AC ELECTRICAL CHARACTERISTICS

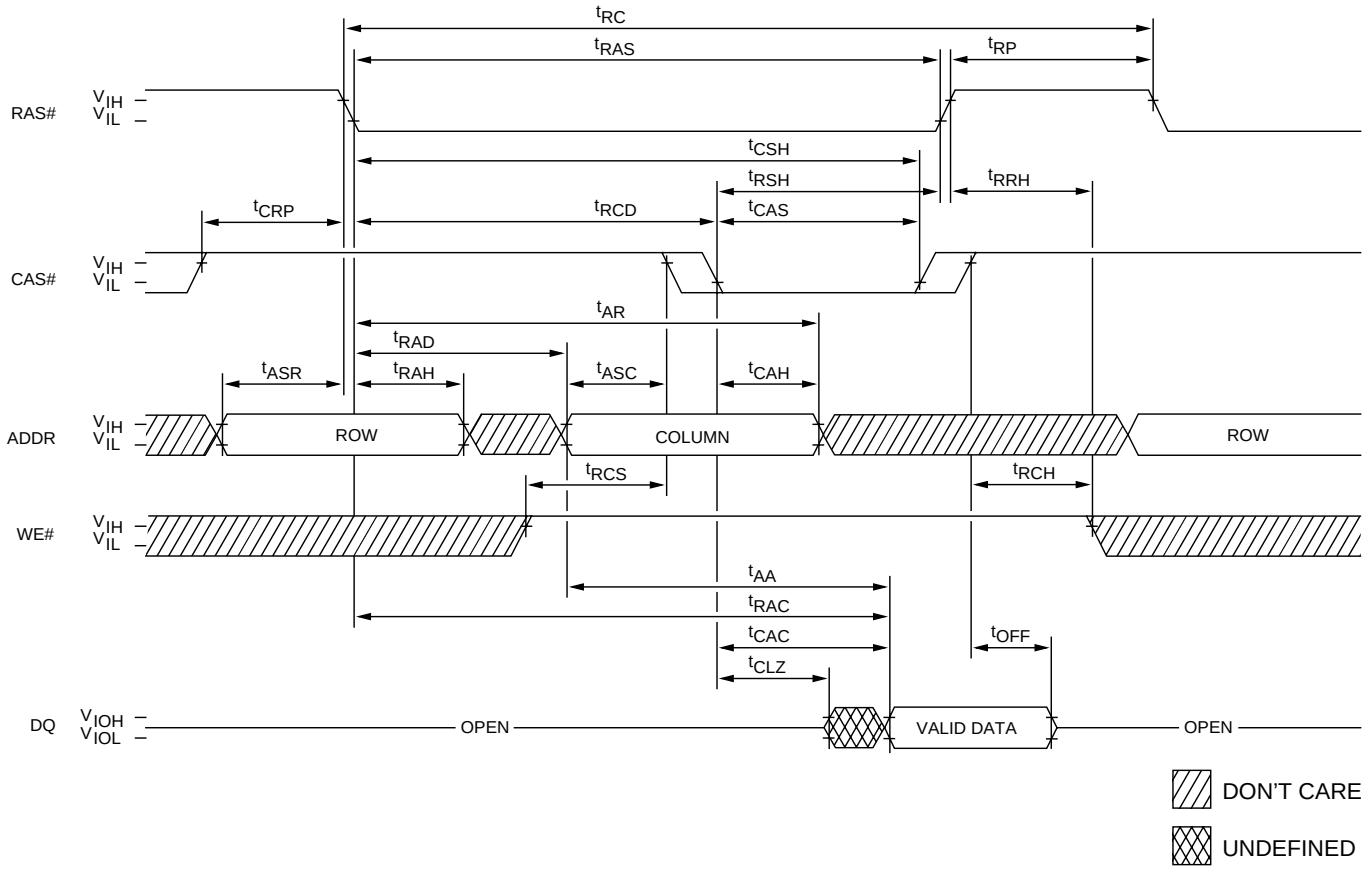
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC}$ = +5V ±10%)

| AC CHARACTERISTICS - EDO PAGE MODE OPTION | | -5 | | -6 | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| Access time from column address | $^tAA$ | | 25 | | 30 | ns | |
| Column-address set-up to CAS# precharge | $^tACH$ | 12 | | 15 | | ns | |
| Column-address hold time (referenced to RAS#) | $^tAR$ | 38 | | 45 | | ns | |
| Column-address setup time | $^tASC$ | 0 | | 0 | | ns | |
| Row-address setup time | $^tASR$ | 0 | | 0 | | ns | |
| Access time from CAS# | $^tCAC$ | | 13 | | 15 | ns | |
| Column-address hold time | $^tCAH$ | 8 | | 10 | | ns | |
| CAS# pulse width | $^tCAS$ | 8 | 10,000 | 10 | 10,000 | ns | |
| CAS# hold time (CBR REFRESH) | $^tCHR$ | 8 | | 10 | | ns | 4 |
| CAS# to output in Low-Z | $^tCLZ$ | 0 | | 0 | | ns | |
| Data output hold after next CAS# LOW | $^tCOH$ | 3 | | 3 | | ns | |
| CAS# precharge time | $^tCP$ | 8 | | 10 | | ns | 13 |
| Access time from CAS# precharge | $^tCPA$ | | 28 | | 35 | ns | |
| CAS# to RAS# precharge time | $^tCRP$ | 5 | | 5 | | ns | |
| CAS# hold time | $^tCSH$ | 38 | | 45 | | ns | |
| CAS# setup time (CBR REFRESH) | $^tCSR$ | 5 | | 5 | | ns | 4 |
| Write command to CAS# lead time | $^tCWL$ | 8 | | 10 | | ns | |
| Data-in hold time | $^tDH$ | 8 | | 10 | | ns | 18 |
| Data-in setup time | $^tDS$ | 0 | | 0 | | ns | 18 |
| Output buffer turn-off delay | $^tOFF$ | 0 | 12 | 0 | 15 | ns | 17, 21 |
| EDO-PAGE-MODE READ or WRITE cycle time | $^tPC$ | 20 | | 25 | | ns | |
| Access time from RAS# | $^tRAC$ | | 50 | | 60 | ns | |
| RAS# to column-address delay time | $^tRAD$ | 9 | | 12 | | ns | 15 |
| Row-address hold time | $^tRAH$ | 9 | | 10 | | ns | |
| RAS# pulse width | $^tRAS$ | 50 | 10,000 | 60 | 10,000 | ns | |
| RAS# pulse width (EDO PAGE MODE) | $^tRASP$ | 50 | 125,000 | 60 | 125,000 | ns | |
| Random READ or WRITE cycle time | $^tRC$ | 84 | | 104 | | ns | |
| RAS# to CAS# delay time | $^tRCD$ | 11 | | 14 | | ns | 14 |
| Read command hold time (referenced to CAS#) | $^tRCH$ | 0 | | 0 | | ns | 16 |
| Read command setup time | $^tRCS$ | 0 | | 0 | | ns | |
| Refresh period (2,048 cycles) | $^tREF$ | | 32 | | 32 | ms | |
| RAS# precharge time | $^tRP$ | 30 | | 40 | | ns | |
| RAS# to CAS# precharge time | $^tRPC$ | 5 | | 5 | | ns | |
| Read command hold time (referenced to RAS#) | $^tRRH$ | 0 | | 0 | | ns | 16 |
| RAS# hold time | $^tRSH$ | 13 | | 15 | | ns | |
| Write command to RAS# lead time | $^tRWL$ | 13 | | 15 | | ns | |
| Transition time (rise or fall) | $^tT$ | 2 | 50 | 2 | 50 | ns | |
| Write command hold time | $^tWCH$ | 8 | | 10 | | ns | |
| Write command hold time (referenced to RAS#) | $^tWCR$ | 38 | | 45 | | ns | |
| WE# command setup time | $^tWCS$ | 0 | | 0 | | ns | |
| Output disable delay from WE# | $^tWHZ$ | 0 | 12 | 0 | 15 | ns | |
| Write command pulse width | $^tWP$ | 5 | | 5 | | ns | |
| WE# pulse to disable at CAS# HIGH | $^tWPZ$ | 10 | | 10 | | ns | |
| WE# hold time (CBR REFRESH) | $^tWRH$ | 8 | | 10 | | ns | |
| WE# setup time (CBR REFRESH) | $^tWRP$ | 8 | | 10 | | ns | |

## NOTES

1. All voltages referenced to $V_{SS}$.
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, $V_{CC}$ = 4.5V, DC bias = 2.4V at 15mV RMS).
3. $I_{CC}$ is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the $^{t}$REF refresh requirement is exceeded.
7. AC characteristics assume $^{t}$T = 5ns for FAST PAGE MODE and $^{t}$T = 2.5ns for EDO PAGE MODE.
8. $V_{IH}$ (MIN) and $V_{IL}$ (MAX) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
9. In addition to meeting the transition rate specification, all input signals must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
10. If CAS# = $V_{IH}$, data output is High-Z.
11. If CAS# = $V_{IL}$, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, $V_{OL}$ = 0.8V and $V_{OH}$ = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for $^{t}$CP.
14. The $^{t}$RCD (MAX) limit is no longer specified. $^{t}$RCD (MAX) was specified as a reference point only. If $^{t}$RCD was greater than the specified $^{t}$RCD (MAX) limit, then access time was controlled exclusively by $^{t}$CAC ($^{t}$RAC [MIN] no longer applied). With or without the $^{t}$RCD (MAX) limit, $^{t}$AA and $^{t}$CAC must always be met.
15. The $^{t}$RAD (MAX) limit is no longer specified. $^{t}$RAD (MAX) was specified as a reference point only. If $^{t}$RAD was greater than the specified $^{t}$RAD (MAX) limit, then access time was controlled exclusively by $^{t}$AA ($^{t}$RAC and $^{t}$CAC no longer applied). With or without the $^{t}$RAD (MAX) limit, $^{t}$AA, $^{t}$RAC and $^{t}$CAC must always be met.
16. Either $^{t}$RCH or $^{t}$RRH must be satisfied for a READ cycle.
17. $^{t}$OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to $V_{OH}$ or $V_{OL}$.
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 16MB module values will be half of those shown.
24. For FAST PAGE MODE option, $^{t}$OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, $^{t}$OFF on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
25. Applies to both EDO and FAST PAGE MODE modules.

## READ CYCLE
(FAST PAGE MODE Module)

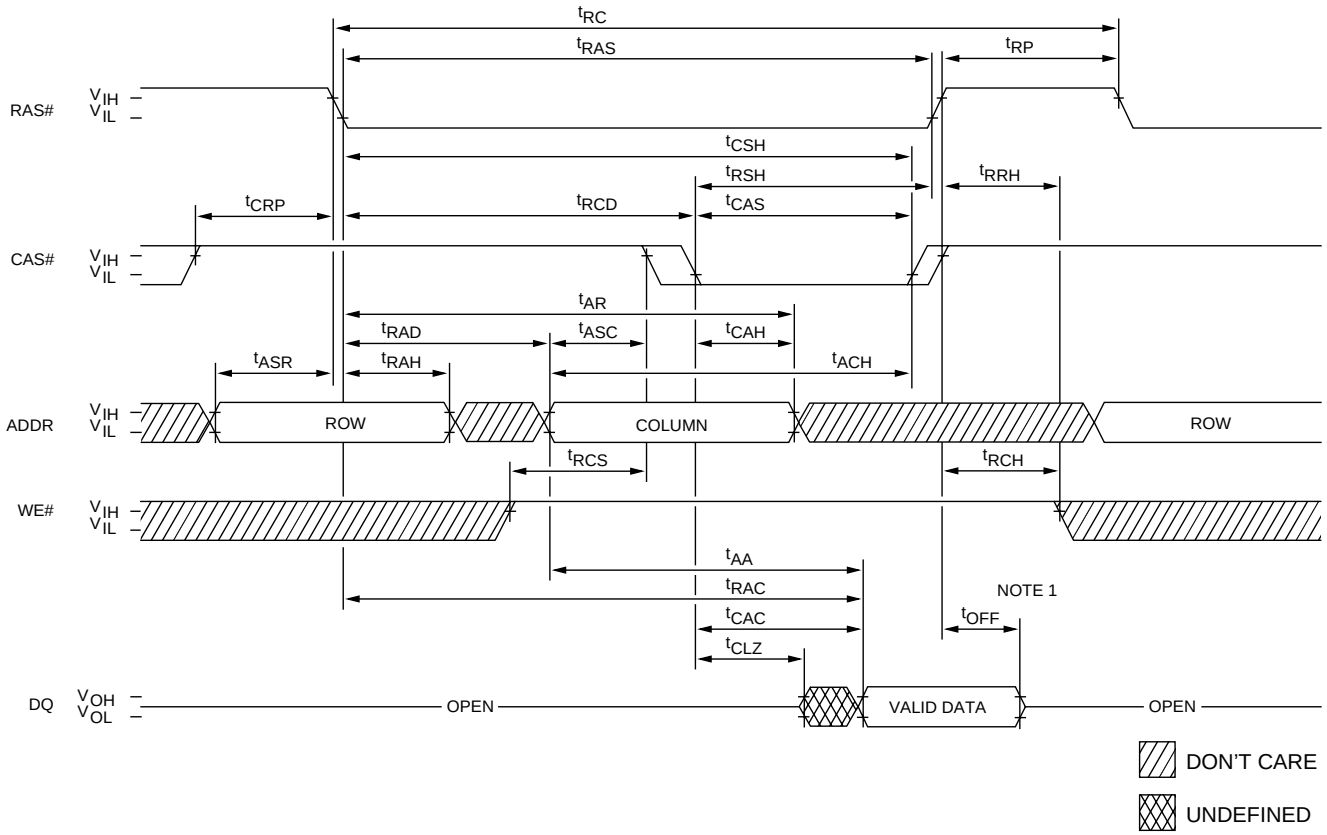



### FAST PAGE MODE
### TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tAA | | 30 | ns |
| tAR | 45 | | ns |
| tASC | 0 | | ns |
| tASR | 0 | | ns |
| tCAC | | 15 | ns |
| tCAH | 10 | | ns |
| tCAS | 15 | 10,000 | ns |
| tCLZ | 3 | | ns |
| tCRP | 5 | | ns |
| tCSH | 60 | | ns |
| tOFF | 3 | 15 | ns |

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tRAC | | 60 | ns |
| tRAD | 15 | | ns |
| tRAH | 10 | | ns |
| tRAS | 60 | 10,000 | ns |
| tRC | 110 | | ns |
| tRCD | 20 | | ns |
| tRCH | 0 | | ns |
| tRCS | 0 | | ns |
| tRP | 40 | | ns |
| tRRH | 0 | | ns |
| tRSH | 15 | | ns |

## READ CYCLE
(EDO PAGE MODE Module)



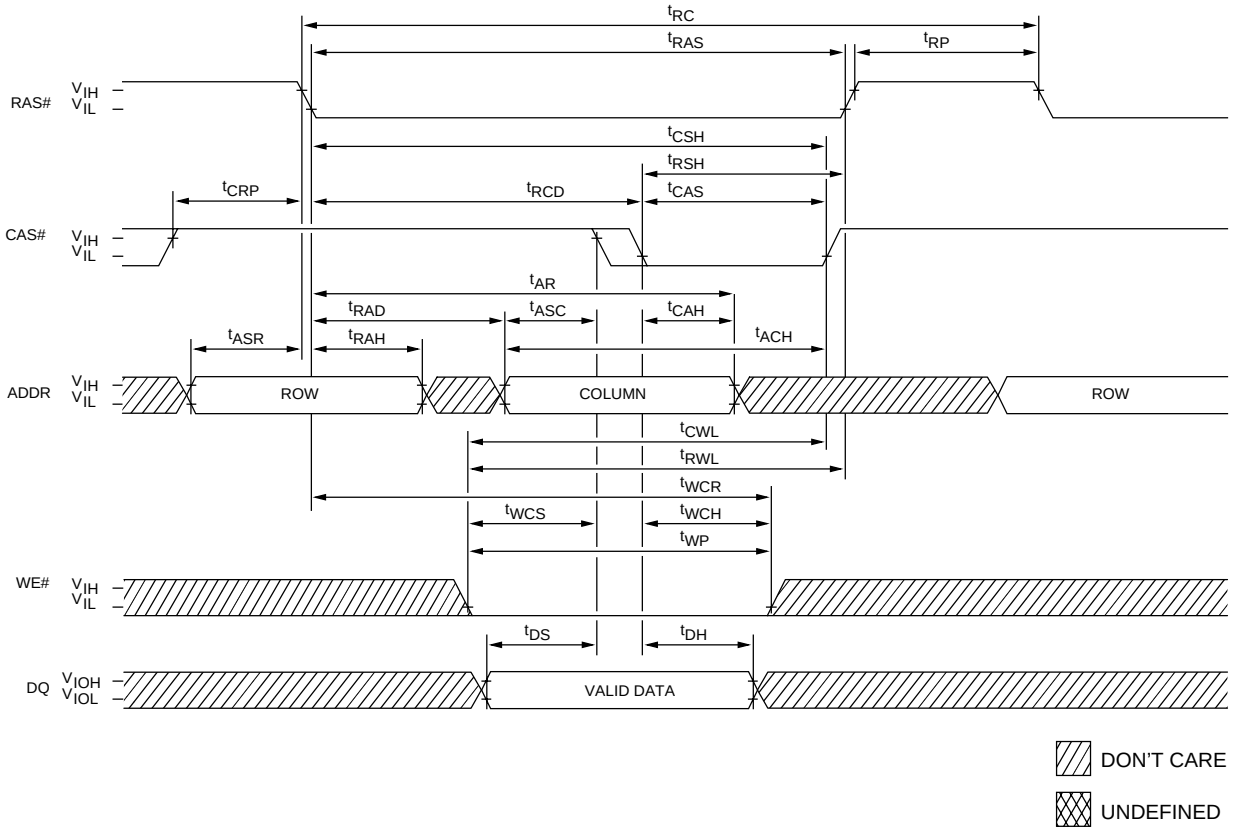

### EDO PAGE MODE
### TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tOFF | 0 | 12 | 0 | 15 | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC | 84 | | 104 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |

**NOTE:** 1. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

## EARLY WRITE CYCLE [25]



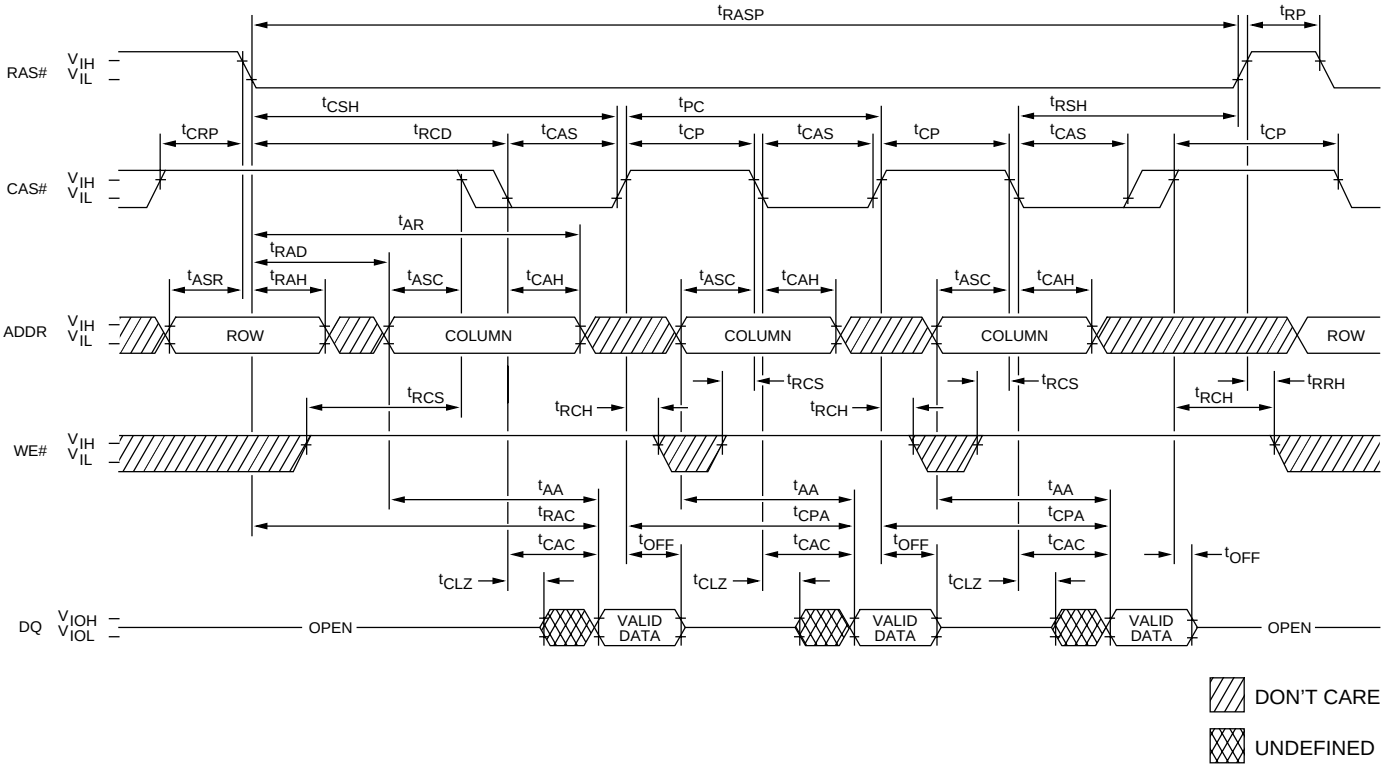

### FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| | -5* | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tACH (EDO) | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS (FPM) | — | — | 15 | 10,000 | ns |
| tCAS (EDO) | 8 | 10,000 | 10 | 10,000 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH (FPM) | — | | 60 | | ns |
| tCSH (EDO) | 38 | | 45 | | ns |
| tCWL (FPM) | — | | 15 | | ns |
| tCWL (EDO) | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |
| tRAD (FPM) | — | | 15 | | ns |

| | -5* | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tRAD (EDO) | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRC (FPM) | — | | 110 | | ns |
| tRC (EDO) | 84 | | 104 | | ns |
| tRCD (FPM) | — | | 20 | | ns |
| tRCD (EDO) | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCR | 38 | | 45 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP (FPM) | — | | 10 | | ns |
| tWP (EDO) | 5 | | 5 | | ns |

*EDO version only

## FAST-PAGE-MODE READ CYCLE

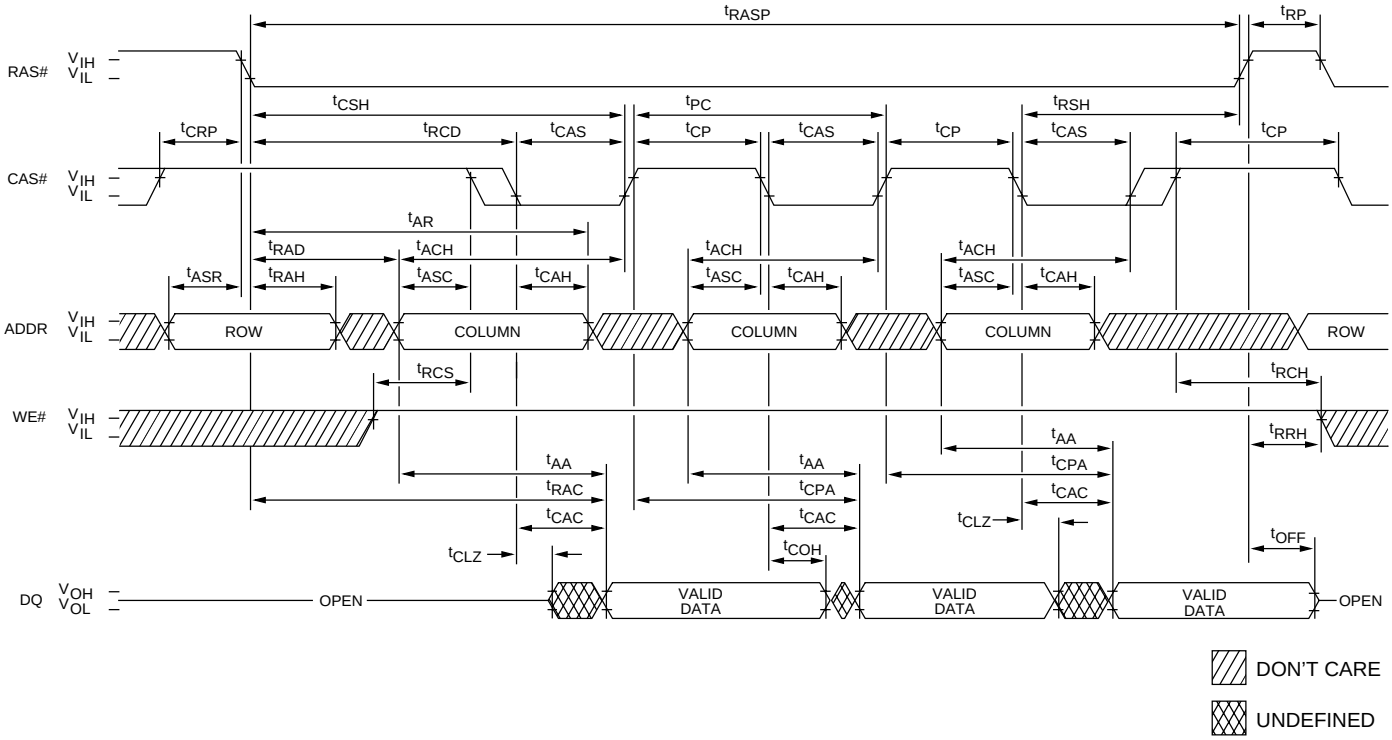



### FAST PAGE MODE TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tAA | | 30 | ns |
| tAR | 45 | | ns |
| tASC | 0 | | ns |
| tASR | 0 | | ns |
| tCAC | | 15 | ns |
| tCAH | 10 | | ns |
| tCAS | 15 | 10,000 | ns |
| tCLZ | 3 | | ns |
| tCP | 10 | | ns |
| tCPA | | 35 | ns |
| tCRP | 5 | | ns |
| tCSH | 60 | | ns |

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tOFF | 3 | 15 | ns |
| tPC | 35 | | ns |
| tRAC | | 60 | ns |
| tRAD | 15 | | ns |
| tRAH | 10 | | ns |
| tRASP | 60 | 125,000 | ns |
| tRCD | 20 | | ns |
| tRCH | 0 | | ns |
| tRCS | 0 | | ns |
| tRP | 40 | | ns |
| tRRH | 0 | | ns |
| tRSH | 15 | | ns |

## EDO-PAGE-MODE READ CYCLE

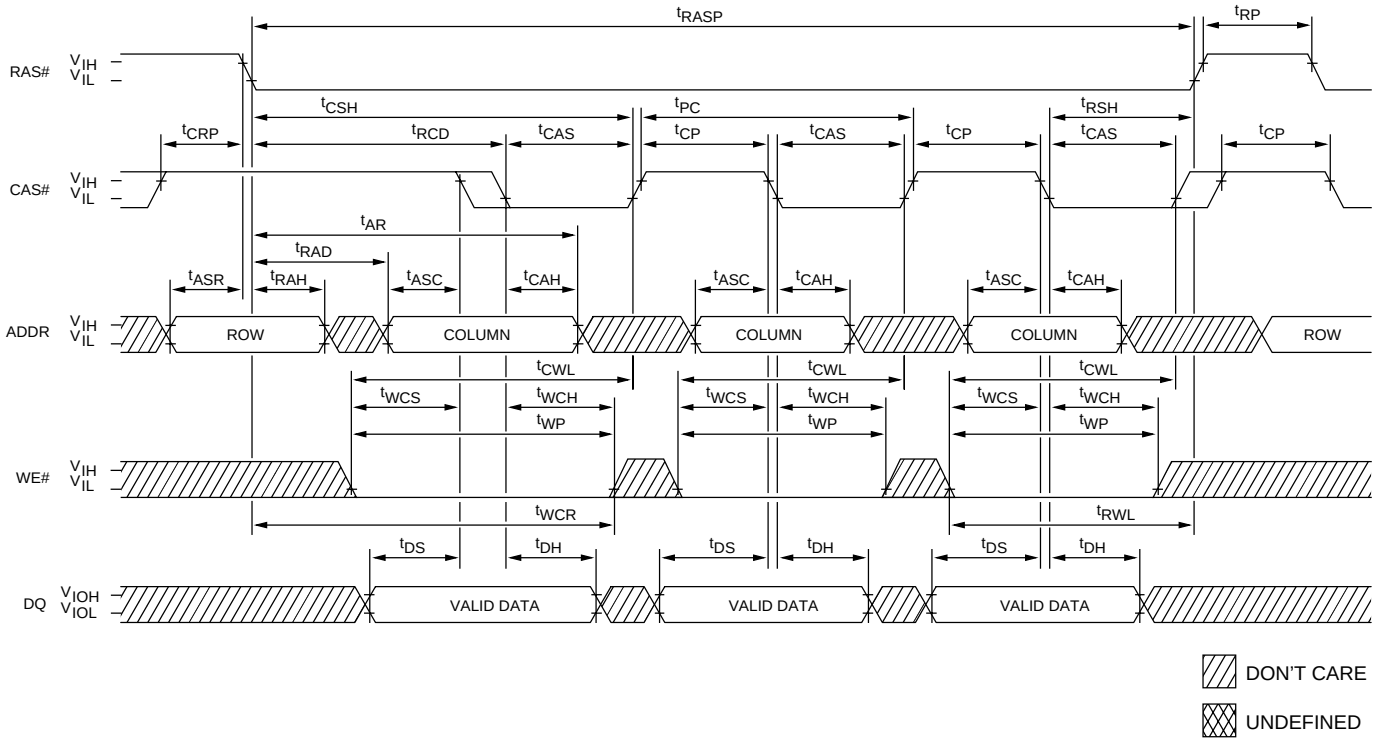



### EDO PAGE MODE TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tCSH | 38 | | 45 | | ns |
| tOFF | 0 | 12 | 0 | 15 | ns |
| tPC | 20 | | 25 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRRH | 0 | | 0 | | ns |
| tRSH | 13 | | 15 | | ns |

## FAST-PAGE-MODE EARLY-WRITE CYCLE

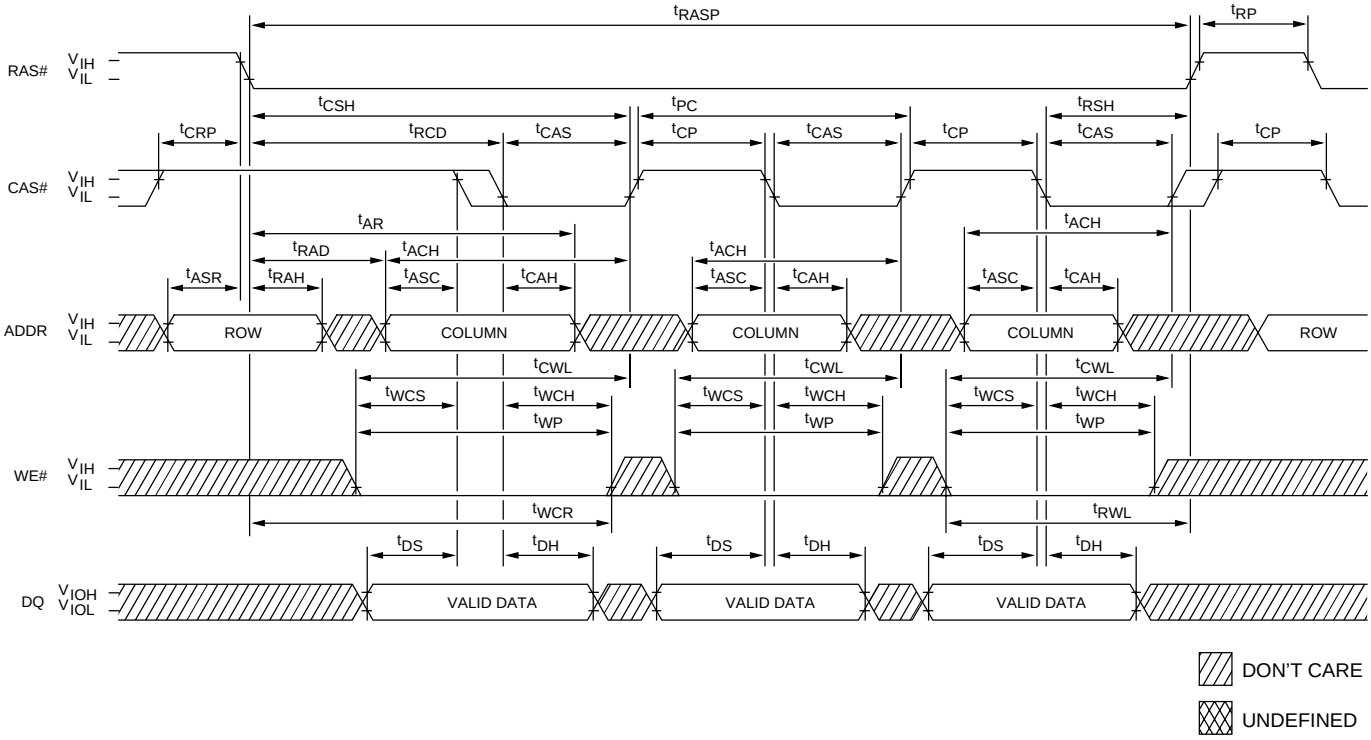



### FAST PAGE MODE TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tAR | 45 | | ns |
| tASC | 0 | | ns |
| tASR | 0 | | ns |
| tCAH | 10 | | ns |
| tCAS | 15 | 10,000 | ns |
| tCP | 10 | | ns |
| tCRP | 5 | | ns |
| tCSH | 60 | | ns |
| tCWL | 15 | | ns |
| tDH | 10 | | ns |
| tDS | 0 | | ns |
| tPC | 35 | | ns |

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tRAD | 15 | | ns |
| tRAH | 10 | | ns |
| tRASP | 60 | 125,000 | ns |
| tRCD | 20 | | ns |
| tRP | 40 | | ns |
| tRSH | 15 | | ns |
| tRWL | 15 | | ns |
| tWCH | 10 | | ns |
| tWCR | 45 | | ns |
| tWCS | 0 | | ns |
| tWP | 10 | | ns |

## EDO-PAGE-MODE EARLY-WRITE CYCLE

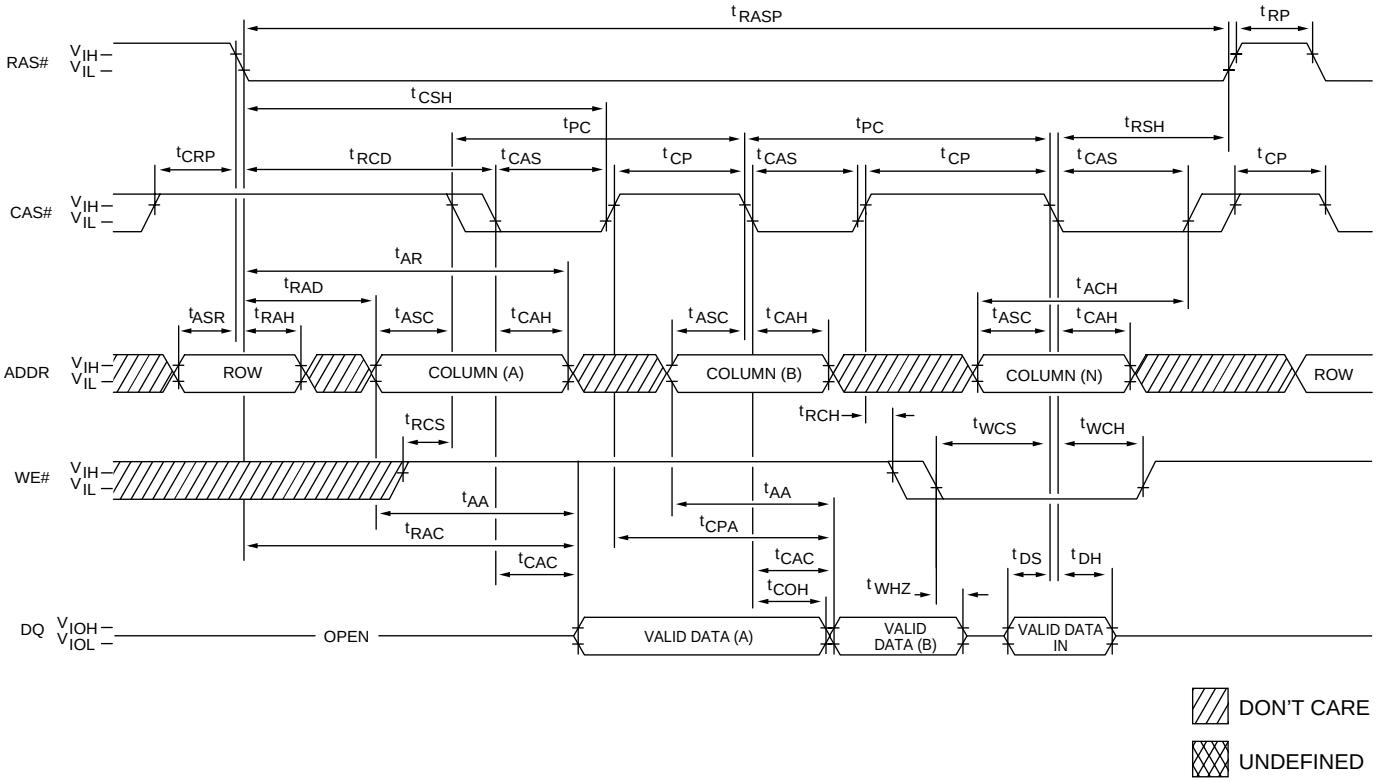



### EDO PAGE MODE TIMING PARAMETERS

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tCWL | 8 | | 10 | | ns |
| tDH | 8 | | 10 | | ns |
| tDS | 0 | | 0 | | ns |

| | -5 | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tPC | 20 | | 25 | | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tRWL | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCR | 38 | | 45 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWP | 5 | | 5 | | ns |

## EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)

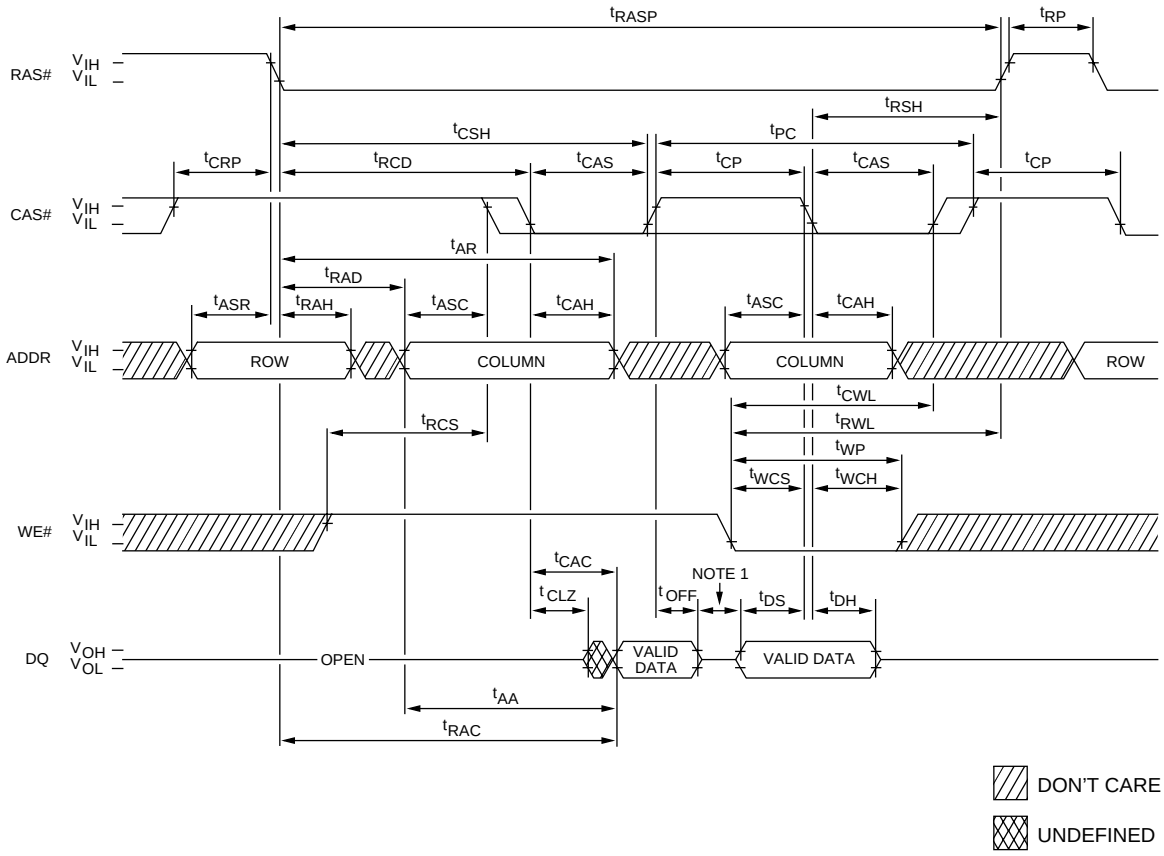



### EDO PAGE MODE TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tACH | 12 | | 15 | | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCOH | 3 | | 3 | | ns |
| tCP | 8 | | 10 | | ns |
| tCPA | | 28 | | 35 | ns |
| tCRP | 5 | | 5 | | ns |
| tCSH | 38 | | 45 | | ns |
| tDH | 8 | | 10 | | ns |

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tDS | 0 | | 0 | | ns |
| tPC | 20 | | 25 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRASP | 50 | 125,000 | 60 | 125,000 | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |
| tWCH | 8 | | 10 | | ns |
| tWCS | 0 | | 0 | | ns |
| tWHZ | 0 | 12 | 0 | 15 | ns |

## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



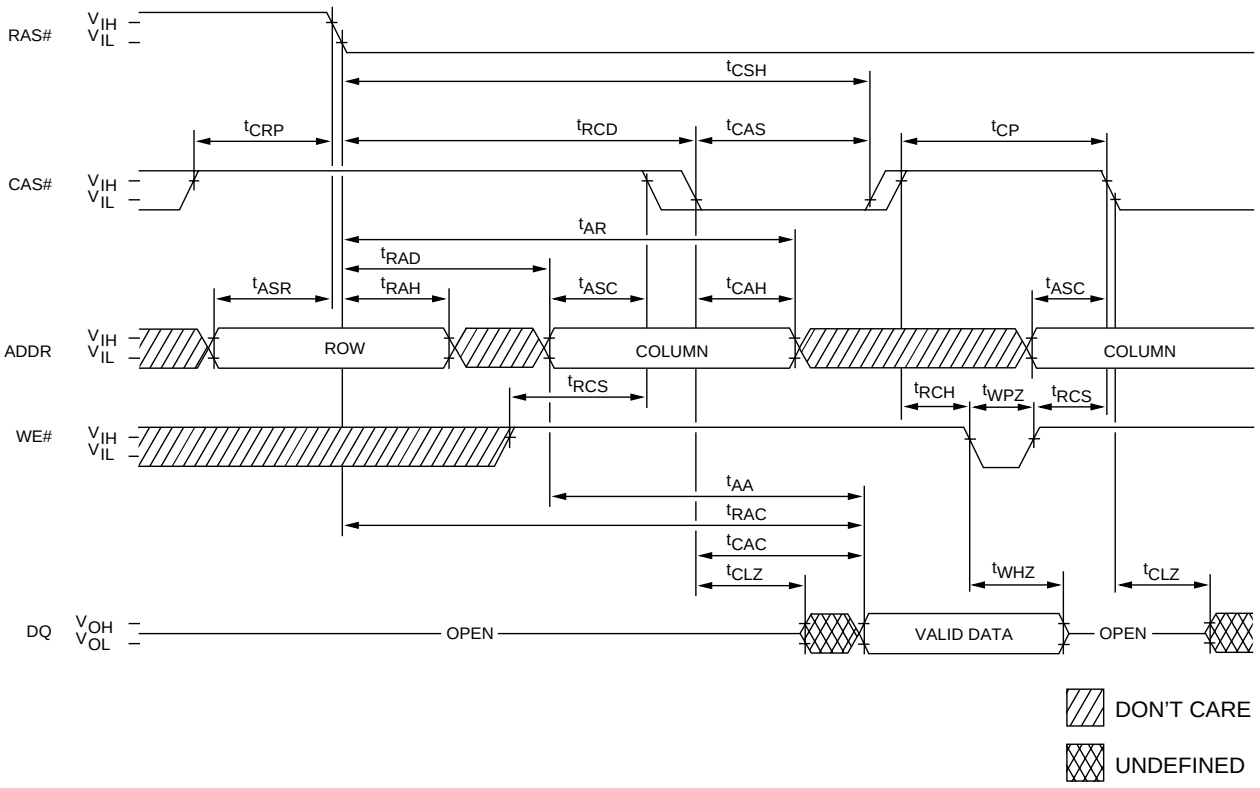

### FAST PAGE MODE TIMING PARAMETERS

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tAA | | 30 | ns |
| tAR | 45 | | ns |
| tASC | 0 | | ns |
| tASR | 0 | | ns |
| tCAC | | 15 | ns |
| tCAH | 10 | | ns |
| tCAS | 15 | 10,000 | ns |
| tCLZ | 3 | | ns |
| tCP | 10 | | ns |
| tCRP | 5 | | ns |
| tCSH | 60 | | ns |
| tCWL | 15 | | ns |
| tDH | 10 | | ns |
| tDS | 0 | | ns |

| SYMBOL | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|
| tOFF | 3 | 15 | ns |
| tPC | 35 | | ns |
| tRAC | | 60 | ns |
| tRAD | 15 | | ns |
| tRAH | 10 | | ns |
| tRASP | 60 | 125,000 | ns |
| tRCD | 20 | | ns |
| tRCS | 0 | | ns |
| tRP | 40 | | ns |
| tRSH | 15 | | ns |
| tRWL | 15 | | ns |
| tWCH | 10 | | ns |
| tWCS | 0 | | ns |
| tWP | 10 | | ns |

**NOTE:** 1. Do not drive data prior to tristate.

## EDO READ CYCLE
(with WE#-controlled disable)

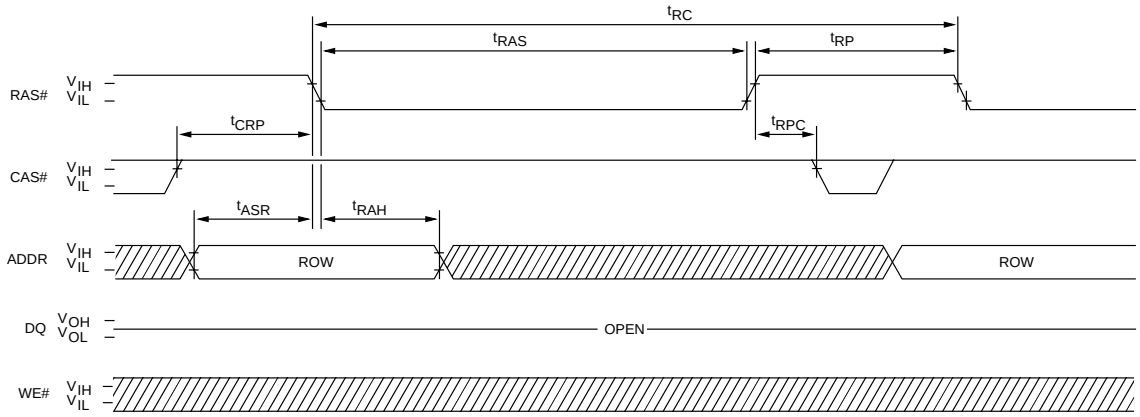



### EDO PAGE MODE TIMING PARAMETERS

| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCAS | 8 | 10,000 | 10 | 10,000 | ns |
| tCLZ | 0 | | 0 | | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |

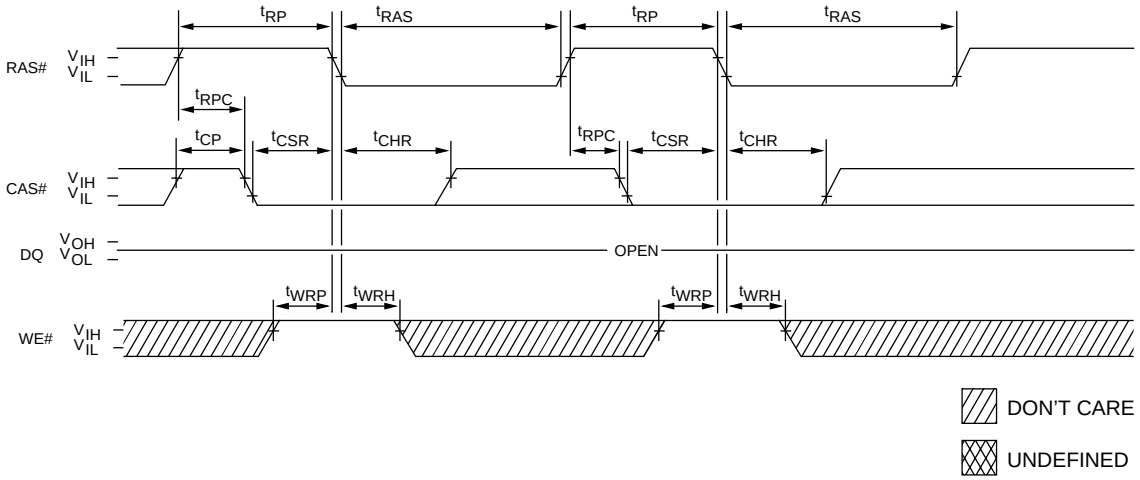
| SYMBOL | -5 MIN | -5 MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tCSH | 38 | | 45 | | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRCD | 11 | | 14 | | ns |
| tRCH | 0 | | 0 | | ns |
| tRCS | 0 | | 0 | | ns |
| tWHZ | 0 | 12 | 0 | 15 | ns |
| tWPZ | 10 | | 10 | | ns |

## RAS#-ONLY REFRESH CYCLE [25]




## CBR REFRESH CYCLE [25]

(Addresses = DON'T CARE)



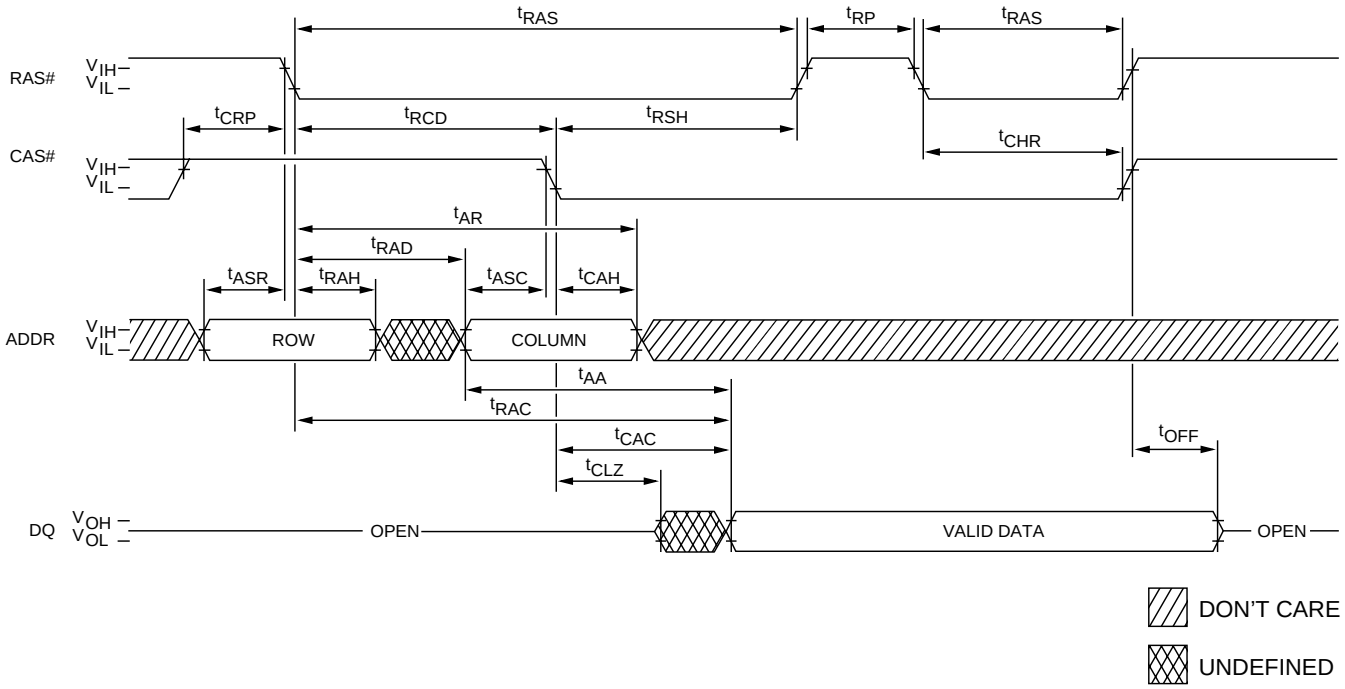

### FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

| SYMBOL | -5* MIN | -5* MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tASR | 0 | | 0 | | ns |
| tCHR (FPM) | — | | 10 | | ns |
| tCHR (EDO) | 8 | | 10 | | ns |
| tCP | 8 | | 10 | | ns |
| tCRP | 5 | | 5 | | ns |
| tCSR | 5 | | 5 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |

| SYMBOL | -5* MIN | -5* MAX | -6 MIN | -6 MAX | UNITS |
|---|---|---|---|---|---|
| tRC (FPM) | — | | 110 | | ns |
| tRC (EDO) | 84 | | 104 | | ns |
| tRP | 30 | | 40 | | ns |
| tRPC (FPM) | — | | 0 | | ns |
| tRPC (EDO) | 5 | | 5 | | ns |
| tWRH | 8 | | 10 | | ns |
| tWRP | 8 | | 10 | | ns |

*EDO version only

## HIDDEN REFRESH CYCLE [20, 25]
(WE# = HIGH)




### FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

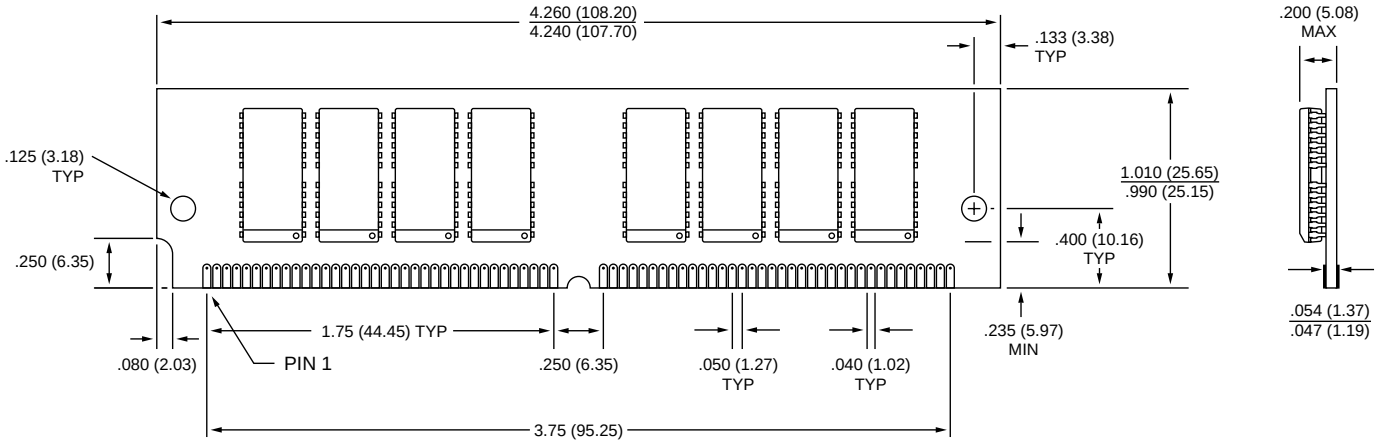
| | -5* | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tAA | | 25 | | 30 | ns |
| tAR | 38 | | 45 | | ns |
| tASC | 0 | | 0 | | ns |
| tASR | 0 | | 0 | | ns |
| tCAC | | 13 | | 15 | ns |
| tCAH | 8 | | 10 | | ns |
| tCHR | 8 | | 10 | | ns |
| tCLZ (FPM) | — | | 3 | | ns |
| tCLZ (EDO) | 0 | | 0 | | ns |
| tCRP | 5 | | 5 | | ns |
| tOFF (FPM) | — | — | 3 | 15 | ns |

| | -5* | | -6 | | |
|---|---|---|---|---|---|
| SYMBOL | MIN | MAX | MIN | MAX | UNITS |
| tOFF (EDO) | 0 | 12 | 0 | 15 | ns |
| tRAC | | 50 | | 60 | ns |
| tRAD (FPM) | — | | 15 | | ns |
| tRAD (EDO) | 9 | | 12 | | ns |
| tRAH | 9 | | 10 | | ns |
| tRAS | 50 | 10,000 | 60 | 10,000 | ns |
| tRCD (FPM) | — | | 20 | | ns |
| tRCD (EDO) | 11 | | 14 | | ns |
| tRP | 30 | | 40 | | ns |
| tRSH | 13 | | 15 | | ns |

*EDO version only

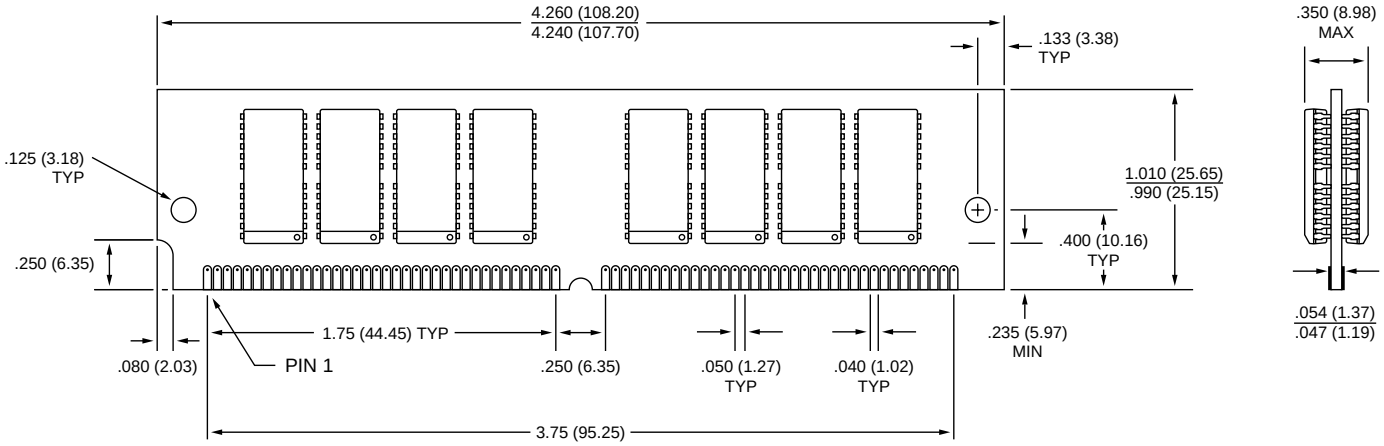
## 72-PIN SIMM

DD-3




## 72-PIN SIMM

DD-4




**NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

MICRON
*Technology that works for you.*

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900, Micron DataFax: 208-368-5800
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992